

# MC74HC365A

## Hex 3-State Noninverting Buffer with Common Enables

### High-Performance Silicon-Gate CMOS

The MC74HC365A is identical in pinout to the LS365. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device is a high-speed hex buffer with 3-state outputs and two common active-low Output Enables. When either of the enables is high, the buffer outputs are placed into high-impedance states. The HC365A has noninverting outputs.

#### Features

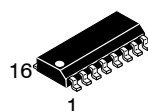
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 90 FETs or 22.5 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



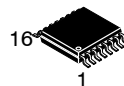
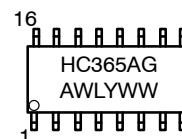
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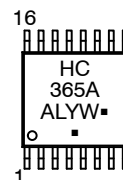
#### MARKING DIAGRAMS



SOIC-16  
D SUFFIX  
CASE 751B



TSSOP-16  
DT SUFFIX  
CASE 948F



A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G or ■ = Pb-Free Package  
(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MC74HC365A

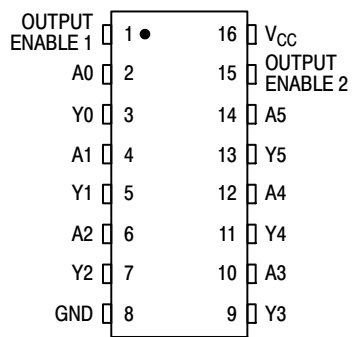


Figure 1. Pin Assignment

| FUNCTION TABLE |          |   |        |
|----------------|----------|---|--------|
| Inputs         |          |   | Output |
| Enable 1       | Enable 2 | A | Y      |
| L              | L        | L | L      |
| L              | L        | H | H      |
| H              | X        | X | Z      |
| X              | H        | X | Z      |

X = don't care  
Z = high impedance

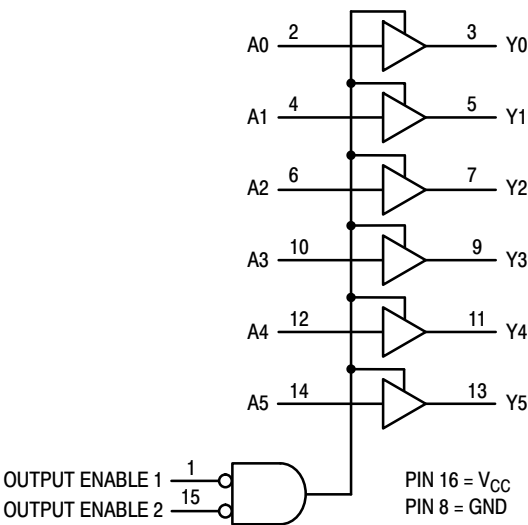


Figure 2. Logic Diagram

ORDERING INFORMATION

| Device            | Package               | Shipping†                |
|-------------------|-----------------------|--------------------------|
| MC74HC365ADG      | SOIC-16<br>(Pb-Free)  | 48 Units / Rail          |
| MC74HC365ADR2G    | SOIC-16<br>(Pb-Free)  | 2500 Units / Tape & Reel |
| MC74HC365ADTR2G   | TSSOP-16<br>(Pb-Free) | 2500 Units / Tape & Reel |
| NLV74HC365ADTR2G* | TSSOP-16<br>(Pb-Free) | 2500 Units / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

# MC74HC365A

## MAXIMUM RATINGS\*

| Symbol    | Parameter                                                                | Value                   | Unit |
|-----------|--------------------------------------------------------------------------|-------------------------|------|
| $V_{CC}$  | DC Supply Voltage (Referenced to GND)                                    | – 0.5 to + 7.0          | V    |
| $V_{in}$  | DC Input Voltage (Referenced to GND)                                     | – 0.5 to $V_{CC} + 0.5$ | V    |
| $V_{out}$ | DC Output Voltage (Referenced to GND)                                    | – 0.5 to $V_{CC} + 0.5$ | V    |
| $I_{in}$  | DC Input Current, per Pin                                                | $\pm 20$                | mA   |
| $I_{out}$ | DC Output Current, per Pin                                               | $\pm 25$                | mA   |
| $I_{CC}$  | DC Supply Current, $V_{CC}$ and GND Pins                                 | $\pm 50$                | mA   |
| $P_D$     | Power Dissipation in Still Air,<br>SOIC Package†<br>TSSOP Package†       | 500<br>450              | mW   |
| $T_{stg}$ | Storage Temperature                                                      | – 65 to + 150           | °C   |
| $T_L$     | Lead Temperature, 1 mm from Case for 10 Seconds<br>SOIC or TSSOP Package | 260                     | °C   |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating — SOIC Package: – 7 mW/°C from 65° to 125°C  
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

| Symbol            | Parameter                                            | Min                                                                                                                              | Max                       | Unit |
|-------------------|------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------|---------------------------|------|
| $V_{CC}$          | DC Supply Voltage (Referenced to GND)                | 2.0                                                                                                                              | 6.0                       | V    |
| $V_{in}, V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | 0                                                                                                                                | $V_{CC}$                  | V    |
| $T_A$             | Operating Temperature, All Package Types             | – 55                                                                                                                             | + 125                     | °C   |
| $t_r, t_f$        | Input Rise and Fall Time<br>(Figure 1)               | $V_{CC} = 2.0 \text{ V}$<br>0<br>$V_{CC} = 3.0 \text{ V}$<br>0<br>$V_{CC} = 4.5 \text{ V}$<br>0<br>$V_{CC} = 6.0 \text{ V}$<br>0 | 1000<br>600<br>500<br>400 | ns   |

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol   | Parameter                         | Test Conditions                                                       | $V_{CC}$<br>V            | Guaranteed Limit             |                              |                              | Unit |
|----------|-----------------------------------|-----------------------------------------------------------------------|--------------------------|------------------------------|------------------------------|------------------------------|------|
|          |                                   |                                                                       |                          | – 55 to<br>25°C              | ≤ 85°C                       | ≤ 125°C                      |      |
| $V_{IH}$ | Minimum High-Level Input Voltage  | $V_{out} = V_{CC} - 0.1 \text{ V}$<br>$ I_{out}  \leq 20 \mu\text{A}$ | 2.0<br>3.0<br>4.5<br>6.0 | 1.5<br>2.1<br>3.15<br>4.2    | 1.5<br>2.1<br>3.15<br>4.2    | 1.5<br>2.1<br>3.15<br>4.2    | V    |
| $V_{IL}$ | Maximum Low-Level Input Voltage   | $V_{out} = 0.1 \text{ V}$<br>$ I_{out}  \leq 20 \mu\text{A}$          | 2.0<br>3.0<br>4.5<br>6.0 | 0.50<br>0.90<br>1.35<br>1.80 | 0.50<br>0.90<br>1.35<br>1.80 | 0.50<br>0.90<br>1.35<br>1.80 | V    |
| $V_{OH}$ | Minimum High-Level Output Voltage | $V_{in} = V_{IH}$<br>$ I_{out}  \leq 20 \mu\text{A}$                  | 2.0<br>4.5<br>6.0        | 1.9<br>4.4<br>5.9            | 1.9<br>4.4<br>5.9            | 1.9<br>4.4<br>5.9            | V    |
|          |                                   | $V_{in} = V_{IH}$ $ I_{out}  \leq 3.6 \text{ mA}$                     | 3.0                      | 2.48                         | 2.34                         | 2.20                         |      |
|          |                                   | $ I_{out}  \leq 6.0 \text{ mA}$                                       | 4.5                      | 3.98                         | 3.84                         | 3.70                         |      |
|          |                                   | $ I_{out}  \leq 7.8 \text{ mA}$                                       | 6.0                      | 5.48                         | 5.34                         | 5.20                         |      |
| $V_{OL}$ | Maximum Low-Level Output Voltage  | $V_{in} = V_{IL}$<br>$ I_{out}  \leq 20 \mu\text{A}$                  | 2.0<br>4.5<br>6.0        | 0.1<br>0.1<br>0.1            | 0.1<br>0.1<br>0.1            | 0.1<br>0.1<br>0.1            | V    |
|          |                                   | $V_{in} = V_{IL}$ $ I_{out}  \leq 3.6 \text{ mA}$                     | 3.0                      | 0.26                         | 0.33                         | 0.40                         |      |
|          |                                   | $ I_{out}  \leq 6.0 \text{ mA}$                                       | 4.5                      | 0.26                         | 0.33                         | 0.40                         |      |
|          |                                   | $ I_{out}  \leq 7.8 \text{ mA}$                                       | 6.0                      | 0.26                         | 0.33                         | 0.40                         |      |

# MC74HC365A

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol          | Parameter                                      | Test Conditions                                                                                                                     | V <sub>CC</sub><br>V | Guaranteed Limit |        |         | Unit |
|-----------------|------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|----------------------|------------------|--------|---------|------|
|                 |                                                |                                                                                                                                     |                      | – 55 to 25°C     | ≤ 85°C | ≤ 125°C |      |
| I <sub>in</sub> | Maximum Input Leakage Current                  | V <sub>in</sub> = V <sub>CC</sub> or GND                                                                                            | 6.0                  | ± 0.1            | ± 1.0  | ± 1.0   | μA   |
| I <sub>OZ</sub> | Maximum Three-State Leakage Current            | Output in High-Impedance State<br>V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>V <sub>out</sub> = V <sub>CC</sub> or GND | 6.0                  | ± 0.5            | ± 5.0  | ± 10    | μA   |
| I <sub>CC</sub> | Maximum Quiescent Supply Current (per Package) | V <sub>in</sub> = V <sub>CC</sub> or GND<br>I <sub>out</sub> = 0 μA                                                                 | 6.0                  | 4                | 40     | 160     | μA   |

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

| Symbol                                 | Parameter                                                                  | V <sub>CC</sub><br>V                    | Guaranteed Limit |        |         | Unit |
|----------------------------------------|----------------------------------------------------------------------------|-----------------------------------------|------------------|--------|---------|------|
|                                        |                                                                            |                                         | – 55 to 25°C     | ≤ 85°C | ≤ 125°C |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Input A to Output Y<br>(Figures 1 and 3)        | 2.0                                     | 120              | 150    | 180     | ns   |
|                                        |                                                                            | 3.0                                     | 60               | 75     | 90      |      |
|                                        |                                                                            | 4.5                                     | 24               | 30     | 36      |      |
|                                        |                                                                            | 6.0                                     | 20               | 26     | 31      |      |
| t <sub>PLZ</sub> ,<br>t <sub>PHZ</sub> | Maximum Propagation Delay, Output Enable to Output Y<br>(Figures 2 and 4)  | 2.0                                     | 220              | 275    | 330     | ns   |
|                                        |                                                                            | 3.0                                     | 110              | 140    | 170     |      |
|                                        |                                                                            | 4.5                                     | 44               | 55     | 66      |      |
|                                        |                                                                            | 6.0                                     | 37               | 47     | 56      |      |
| t <sub>PZL</sub> ,<br>t <sub>PZH</sub> | Maximum Propagation Delay, Output Enable to Output Y<br>(Figures 2 and 4)  | 2.0                                     | 220              | 275    | 330     | ns   |
|                                        |                                                                            | 3.0                                     | 110              | 140    | 170     |      |
|                                        |                                                                            | 4.5                                     | 44               | 55     | 66      |      |
|                                        |                                                                            | 6.0                                     | 37               | 47     | 56      |      |
| t <sub>TLH</sub> ,<br>t <sub>THL</sub> | Maximum Output Transition Time, Any Output<br>(Figures 1 and 3)            | 2.0                                     | 60               | 75     | 90      | ns   |
|                                        |                                                                            | 3.0                                     | 22               | 28     | 34      |      |
|                                        |                                                                            | 4.5                                     | 12               | 15     | 18      |      |
|                                        |                                                                            | 6.0                                     | 10               | 13     | 15      |      |
| C <sub>in</sub>                        | Maximum Input Capacitance                                                  | —                                       | 10               | 10     | 10      | pF   |
| C <sub>out</sub>                       | Maximum Three-State Output Capacitance<br>(Output in High-Impedance State) | —                                       | 15               | 15     | 15      | pF   |
| C <sub>PD</sub>                        | Power Dissipation Capacitance (Per Buffer)*                                | Typical @ 25°C, V <sub>CC</sub> = 5.0 V |                  |        |         | pF   |
|                                        |                                                                            | 60                                      |                  |        |         |      |

\* Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

## SWITCHING WAVEFORMS

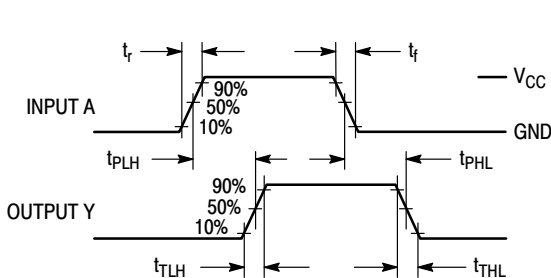


Figure 1.

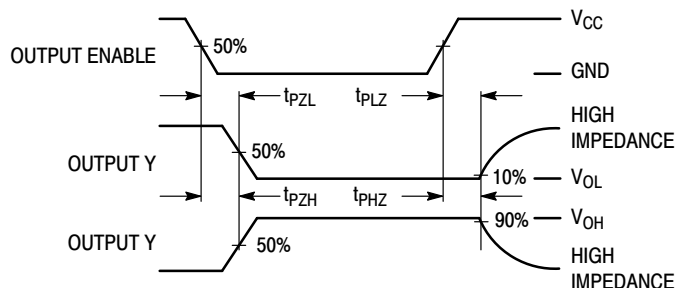
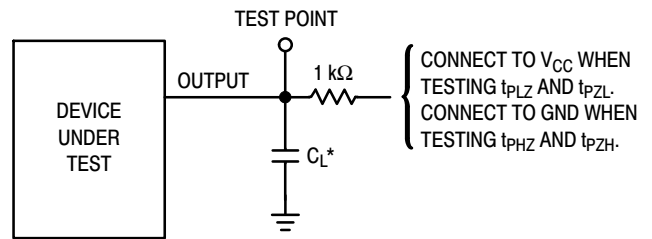


Figure 2.

## TEST CIRCUITS



\*Includes all probe and jig capacitance

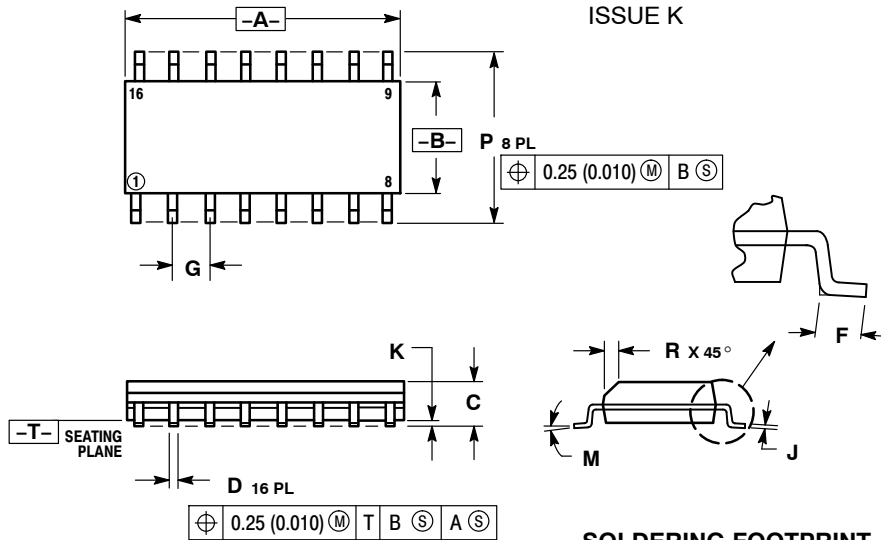
**Figure 4.**

The diagram illustrates a 6-to-1 multiplexer circuit using CMOS technology. The circuit is enclosed in a dashed box. It features an input A, two output enable inputs (OUTPUT ENABLE 1 and OUTPUT ENABLE 2), and a select input. The circuit uses two 3-input AND gates, two 3-input OR gates, and a CMOS output stage. The output Y is connected to  $V_{CC}$  and ground through PMOS and NMOS transistors. The circuit is labeled "TO OTHER FIVE BUFFERS" and "ONE OF 6 BUFFERS".

# MC74HC365A

## PACKAGE DIMENSIONS

SOIC-16  
D SUFFIX  
CASE 751B-05  
ISSUE K

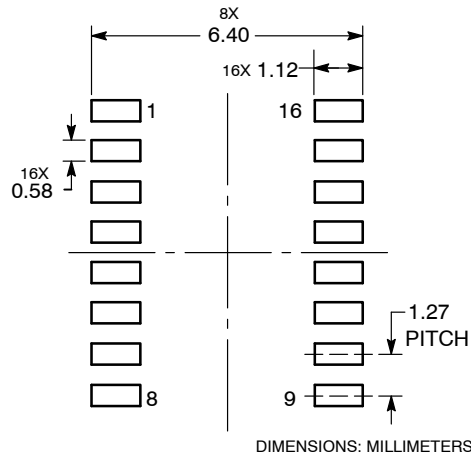


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 9.80        | 10.00 | 0.386     | 0.393 |
| B   | 3.80        | 4.00  | 0.150     | 0.157 |
| C   | 1.35        | 1.75  | 0.054     | 0.068 |
| D   | 0.35        | 0.49  | 0.014     | 0.019 |
| F   | 0.40        | 1.25  | 0.016     | 0.049 |
| G   | 1.27 BSC    |       | 0.050 BSC |       |
| J   | 0.19        | 0.25  | 0.008     | 0.009 |
| K   | 0.10        | 0.25  | 0.004     | 0.009 |
| M   | 0°          | 7°    | 0°        | 7°    |
| P   | 5.80        | 6.20  | 0.229     | 0.244 |
| R   | 0.25        | 0.50  | 0.010     | 0.019 |

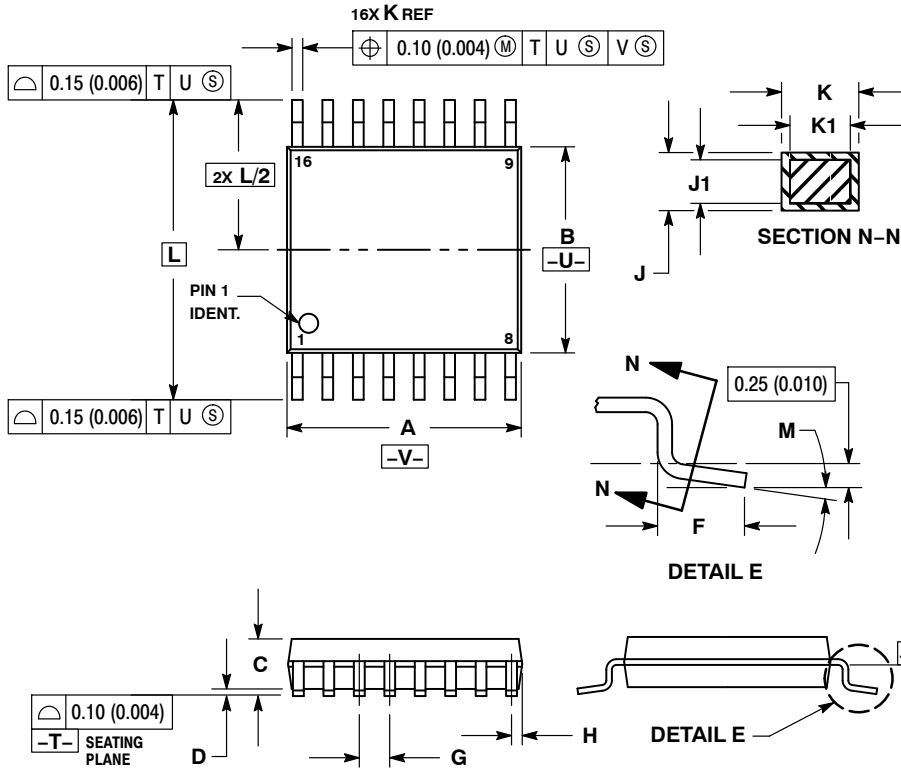
### SOLDERING FOOTPRINT



# MC74HC365A

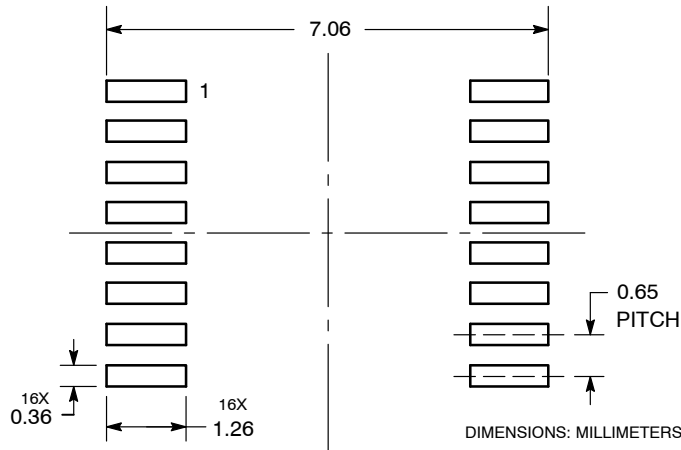
## PACKAGE DIMENSIONS

**TSSOP-16**  
**DT SUFFIX**  
**CASE 948F**  
**ISSUE B**



- NOTES:**
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.18        | 0.28 | 0.007     | 0.011 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |



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