

## USB-Serial Single-Channel (UART/I<sup>2</sup>C/SPI) Bridge with CapSense<sup>®</sup> and BCD

### Features

- USB 2.0-certified, Full-Speed (12 Mbps)
  - Supports communication driver class (CDC), personal health care device class (PHDC), and vendor-specific drivers
  - Battery charger detection (BCD) compliant with USB Battery Charging Specification, Rev. 1.2 (Peripheral Detect only)
  - Integrated USB termination resistors
- Single-channel configurable UART interface
  - Data rates up to 3 Mbps
  - 256 bytes for each transmit and receive buffer
  - Data format:
    - 7 to 8 data bits
    - 1 to 2 stop bits
    - No parity, even, odd, mark, or space parity
  - Supports parity, overrun, and framing errors
  - Supports flow control using CTS, RTS, DTR, DSR
- Single-channel configurable SPI interface
  - Master/slave up to 3 MHz
  - Data width: 4 bits to 16 bits
  - 256 bytes for each transmit and receive buffer
  - Supports Motorola, TI, and National SPI modes
- Single-channel configurable I<sup>2</sup>C interface
  - Master/slave up to 400 kHz
  - 256 bytes each transmit and receive buffer
  - Supports multi-master I<sup>2</sup>C
- CapSense<sup>®</sup>
  - SmartSense<sup>™</sup> Auto-Tuning is supported through a Cypress-supplied configuration utility
  - Max CapSense buttons: 5
  - GPIOs linked to CapSense buttons
- General-purpose input/output (GPIO) pins: 10
- 512-byte flash for storing configuration parameters
- Configuration utility (Windows) to configure the following:
  - Vendor ID (VID), Product ID (PID), and Product and Manufacturer descriptors
  - UART/I<sup>2</sup>C/SPI
  - CapSense
  - Charger detection
  - GPIO
- Driver support for VCOM and DLL
  - Windows 8: 32- and 64-bit versions
  - Windows 7: 32- and 64-bit versions
  - Windows Vista: 32- and 64-bit versions
  - Windows XP: 32- and 64-bit versions
  - Windows CE
  - Mac OS-X: 10.6, 10.7
  - Linux: Kernel version 2.6.35 onwards.
  - Android: Gingerbread and later versions
- Clocking: Integrated 48-MHz clock oscillator
- Supports bus-/self-powered configurations
- USB Suspend mode for low power
- Operating voltage: 1.71 to 5.5 V
- Operating temperature: -40 °C to 85 °C
- ESD protection: 2.2-kV HBM
- RoHS-compliant package
  - 24-pin QFN (4.0 mm × 4.0 mm, 0.55 mm, 0.5 mm pitch)
- Ordering part number
  - CY7C65211-24LTXI

### Applications

- Medical/healthcare devices
- Point-of-Sale (POS) terminals
- Test and measurement system
- Gaming systems
- Set-top box PC-USB interface
- Industrial
- Networking
- Enabling USB connectivity in legacy peripherals

### USB-Compliant

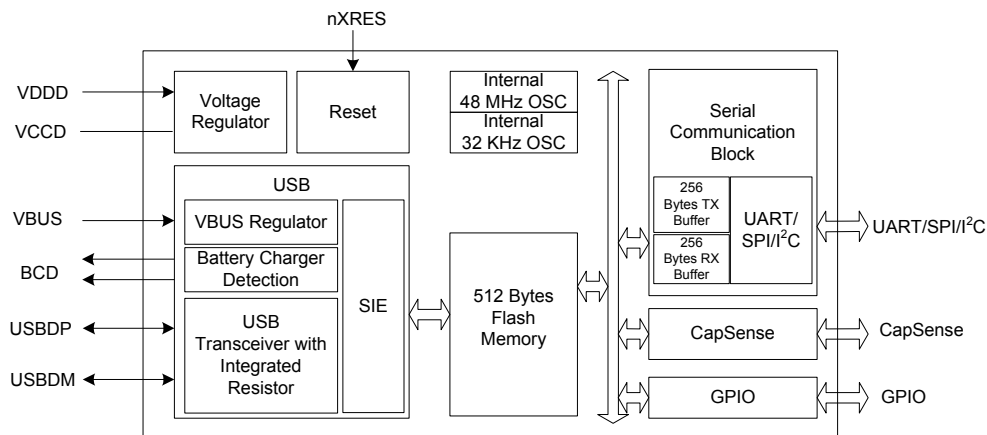
The USB-Serial Single-Channel Bridge with CapSense and BCD (CY7C65211) is fully compliant with the USB 2.0 specification and Battery Charging Specification v1.2, USB-IF Test-ID (TID) 40001521.



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## Block Diagram



## Functional Overview

The CY7C65211 is a Full-Speed USB controller that enables seamless PC connectivity for peripherals with serial interfaces, such as UART, SPI, and I<sup>2</sup>C. CY7C65211 also integrates CapSense and BCD compliant with the USB Battery Charging Specification, Rev. 1.2. It integrates a voltage regulator, an oscillator, and flash memory for storing configuration parameters, offering a cost-effective solution. CY7C65211 supports bus-powered and self-powered modes and enables efficient system power management with suspend and remote wake-up signals. It is available in a 24-pin QFN package.

## USB and Charger Detect

### USB

CY7C65211 has a built-in USB 2.0 Full-Speed transceiver. The transceiver incorporates the internal USB series termination resistors on the USB data lines and a 1.5-k $\Omega$  pull-up resistor on USBDP.

### Charger Detection

CY7C65211 supports BCD for Peripheral Detect only and complies with the USB Battery Charging Specification, Rev. 1.2. It supports the following charging ports:

- Standard Downstream Port (SDP): Allows the system to draw up to 500 mA current from the host
- Charging Downstream Port (CDP): Allows the system to draw up to 1.5 A current from the host
- Dedicated Charging Port (DCP): Allows the system to draw up to 1.5 A of current from the wall charger

## Serial Communication

CY7C65211 has a serial communication block (SCB). Each SCB can implement UART, SPI, or I<sup>2</sup>C interface. A 256-byte buffer is available in both the TX and RX lines.

### UART Interface

The UART interface provides asynchronous serial communication with other UART devices operating at speeds of up to 3 Mbps. It supports 7 to 8 data bits, 1 to 2 stop bits, odd, even, mark, space, and no parity. The UART interface supports

full-duplex communication with a signaling format that is compatible with the standard UART protocol. The UART pins may be interfaced to industry-standard RS-232 transceivers to manage different voltage levels.

Common UART functions, such as parity error and frame error, are supported. CY7C65211 supports baud rates ranging from 300 baud to 3 Mbaud. The UART baud rates can be set using the configuration utility.

### UART Flow Control

The CY7C65211 device supports UART hardware flow control using control signal pairs, such as RTS# (Request to Send) / CTS# (Clear to Send) and DTR# (Data Terminal Ready) / DSR# (Data Set Ready). Data flow control is enabled by default. Flow control can be disabled using the configuration utility.

The following section describes the flow control signals:

#### ■ CTS# (Input) / RTS# (Output)

CTS# can pause or resume data transmission over the UART interface. Data transmission can be paused by de-asserting the CTS signal and resumed with CTS# assertion. The pause and resume operation does not affect data integrity. The receive buffer has a watermark level of 80%. After the data in the receive buffer reaches that level, the RTS# signal is de-asserted, instructing the transmitting device to stop data transmission. The start of data consumption by application reduces the device data backlog; when it reaches the 50% watermark level, the RTS# signal is asserted to resume data reception.

#### ■ DSR# (Input) / DTR# (Output)

The DSR#/DTR# signals are used to establish a communication link with the UART. These signals complement each other in their functionality, similar to CTS# and RTS#.

### SPI Interface

The SPI interface supports an SPI Master and SPI Slave. This interface supports the Motorola, TI, and National Microwire protocols. The maximum frequency of operation is 3 MHz in Master and Slave modes. It can support transaction sizes ranging from 4 bits to 16 bits in length (refer to [USB-to-SPI Bridge on page 23](#) for more details).

### *I<sup>2</sup>C Interface*

The I<sup>2</sup>C interface implements full multi-master/slave modes and supports up to 400 kHz. The configuration utility tool is used to set the I<sup>2</sup>C address in the slave mode. The tool enables only even slave addresses. For further details on the protocol, refer to the NXP I<sup>2</sup>C specification, Rev. 5.

#### **Notes**

- I<sup>2</sup>C ports are not tolerant of higher voltages. Therefore, they cannot be hot-swapped or powered up independently.
- The minimum fall time is not met, as required by the NXP I<sup>2</sup>C specification Rev. 5, except when V<sub>DD</sub> = 1.71 V to 3.0 V. The minimum fall time can be met by adding a 50-pF capacitor for the V<sub>DD</sub> = 3.0 V–3.6 V range.

### **CapSense**

CapSense functionality is supported on all the GPIO pins. Any GPIO pin can be configured as a sense pin (CS0–CS7) using the configuration utility. When implementing CapSense functionality, the GPIO\_0 pin (configured as a modulator capacitor - Cmod) should be connected to ground through a 2.2-nF capacitor (see [Figure 10 on page 21](#)).

CY7C65211 supports SmartSense Auto-Tuning of the CapSense parameters and does not require manual tuning. SmartSense Auto-tuning compensates for printed circuit board (PCB) variations and device process variations.

Optionally, any GPIO pin can be configured as a Cshield and connected to the shield of the CapSense button, as shown in [Figure 10 on page 21](#). Shield prevents false triggering of buttons due to water droplets and guarantees CapSense operation (sensors respond to finger touch).

GPIOs can be linked to the CapSense buttons to indicate the presence of a finger. CapSense functionality can be configured using the configuration utility.

CY7C65211 supports up to five CapSense buttons. For more information on CapSense, refer to [Getting Started with CapSense](#).

### **GPIO Interface**

CY7C65211 has 10 GPIOs. The maximum available GPIOs for configuration is 10 if one two-pin (I<sup>2</sup>C/2-pin UART) serial interface is implemented. The configuration utility allows configuration of the GPIO pins. The configurable options are as follows:

- TRISTATE: GPIO tristated
  - DRIVE 1: Output static 1
  - DRIVE 0: Output static 0
  - POWER#: Power control for bus power designs
  - TXLED#: Drives LED during USB transmit
  - RXLED#: Drives LED during USB receive
  - TX or RX LED#: Drives LED during USB transmit or receive
- GPIO can be configured to drive LED at 8-mA drive strength.
- BCD0/BCD1: Two-pin output to indicate the type of USB charger
  - BUSDETECT: Connects the VBUS pin for USB host detection
  - CS0–CS4: CapSense button input (Sense pin)

- CSout0–CSout2: Indicates which CapSense button is pressed
- Cmod: External modulator capacitor; connects a 2.2-nF capacitor (±10%) to ground (GPIO\_0 only)
- Cshield: Shield for waterproofing

### **Memory**

CY7C65211 has a 512-byte flash. Flash is used to store USB parameters, such as VID/PID, serial number, product and manufacturer descriptors, which can be programmed by the configuration utility.

### **System Resources**

#### *Power System*

CY7C65211 supports the USB Suspend mode to control power usage. CY7C65211 operates in bus-powered or self-powered modes over a range of 3.15 to 5.25 V.

#### *Clock System*

CY7C65211 has a fully integrated clock with no external components required. The clock system is responsible for providing clocks to all subsystems.

#### *Internal 48-MHz Oscillator*

The internal 48-MHz oscillator is the primary source of internal clocking in CY7C65211.

#### *Internal 32-kHz Oscillator*

The internal 32-kHz oscillator is low power and relatively inaccurate. It is primarily used to generate clocks for peripheral operation in the USB Suspend mode.

#### *Reset*

The reset block ensures reliable power-on reset or reconfiguration to a known state. The nXRES (active low) pin can be used by the external devices to reset the CY7C65211.

### **Suspend and Resume**

The CY7C65211 device asserts the SUSPEND pin when the USB bus enters the suspend state. This helps in meeting the stringent suspend current requirement of the USB 2.0 specification, while using the device in bus-powered mode. The device resumes from the suspend state under either of the two following conditions:

1. Any activity is detected on the USB bus
2. The WAKEUP pin is asserted to generate remote wakeup to the host

### **WAKEUP**

The WAKEUP pin is used to generate the remote wakeup signal on the USB bus. The remote wakeup signal is sent only if the host enables this feature through the SET\_FEATURE request. The device communicates support for the remote wakeup to the host through the configuration descriptor during the USB enumeration process. The CY7C65211 device allows enabling/disabling and polarity of the remote wakeup feature through the configuration utility.

## Software

Cypress delivers a complete set of software drivers and a configuration utility to enable configuration of the product during system development.

### *Drivers for Linux Operating Systems*

Cypress provides a User Mode USB driver library (*libcyusb-serial.so*) that abstracts vendor commands for the UART interface and provides a simplified API interface for user applications. This library uses the standard open-source libUSB library to enable USB communication. The Cypress serial library supports the USB plug-and-play feature using the Linux 'udev' mechanism.

CY7C65211 supports the standard USB CDC UART class driver, which is bundled with the Linux kernel.

### *Android Support*

The CY7C65211 solution includes an Android Java class—*CyUsbSerial.java*—which exposes a set of interface functions to communicate with the device.

### *Drivers for Mac OSx*

Cypress delivers a dynamically linked shared library (*CyUSB-Serial.dylib*) based on libUSB, which enables communication to the CY7C65211 device.

In addition, the device also supports the native Mac OSx CDC UART-class driver.

### *Drivers for Windows Operating Systems*

For Windows operating systems (XP, Vista, Win7, and Win8), Cypress delivers a user-mode dynamically linked library—*CyUSBSerial.dll*—that abstracts a vendor-specific interface of the CY7C65211 devices and provides convenient APIs to the user. It provides interface APIs for vendor-specific UART and class-specific APIs for PHDC.

A virtual COM port driver—*CyUSBSerial.sys*—is also delivered, which implements the USB CDC class driver. The Cypress Windows drivers are:

- Windows Driver Foundation (WDF)-compliant
- Compatible with any USB 2.0-compliant device
- Compatible with Cypress USB 3.0-compliant devices

They also support Windows plug-and-play and power management and USB Remote Wake-up.

■

CY7C65211 also works with the Windows-standard USB CDC UART class driver

### *Windows-CE support*

The CY7C65211 solution also includes a dynamically linked library (DLL) and CDC UART driver library for Windows-CE platforms.

### **Device Configuration Utility (Windows only)**

A Windows-based configuration utility is available to configure device initialization parameters. This graphical user application provides an interactive interface to define the boot parameters stored in the device flash.

This utility allows the user to save a user-selected configuration to text or xml formats. It also allows users to load a selected configuration from text or xml formats. The configuration utility allows the following operations:

- View current device configuration
- Select and configure UART/I2C/SPI, CapSense, battery charging, and GPIOs
- Configure USB VID, PID, and string descriptors
- Save or Load configuration

You can download the free configuration utility and drivers at [www.cypress.com](http://www.cypress.com).

## Internal Flash Configuration

The internal flash memory can be used to store the configuration parameters shown in the following table. A free configuration utility is provided to configure the parameters listed in the table to meet application-specific requirements over the USB interface. The configuration utility can be downloaded at [www.cypress.com](http://www.cypress.com).

**Table 1. Internal Flash Configuration**

| Parameter              | Default Value               | Description   |
|------------------------|-----------------------------|---|
| USB Configuration      |                             |   |
| USB Vendor ID (VID)    | 0x04B4                      | Default Cypress VID. Can be configured to customer VID  |
| USB Product ID (PID)   | 0x0002                      | Default Cypress PID. Can be configured to customer PID  |
| Manufacturer string    | Cypress                     | Can be configured with any string up-to 64 characters   |
| Product string         | USB-Serial (Single Channel) | Can be configured with any string up-to 64 characters   |
| Serial string          |                             | Can be configured with any string up-to 64 characters   |
| Power mode             | Bus powered                 | Can be configured to bus-powered or self-powered mode   |
| Max current draw       | 100 mA                      | Can be configured to any value from 0 to 500 mA. The configuration descriptor will be updated based on this,. |
| Remote wakeup          | Enabled                     | Can be disabled. Remote wakeup is initiated by asserting the WAKEUP pin                                       |
| USB interface protocol | CDC                         | Can be configured to function in CDC, PHDC, or Cypress vendor class   |
| BCD                    | Disabled                    | Charger detect is disabled by default. When BCD is enabled, three of the GPIOs must be configured for BCD     |
| GPIO Configuration     |                             |   |
| GPIO_0                 | TXLED#                      | GPIO can be configured as shown in <a href="#">Table 14 on page 14</a> .                                      |
| GPIO_1                 | RXLED#                      |   |
| GPIO_2                 | DSR#                        |   |
| GPIO_3                 | RTS#                        |   |
| GPIO_4                 | CTS#                        |   |
| GPIO_5                 | TxD                         |   |
| GPIO_6                 | RxD                         |   |
| GPIO_7                 | DTR#                        |   |
| GPIO_8                 | TRISTATE                    |   |
| GPIO_9                 | TRISTATE                    |   |
| GPIO_10                | TRISTATE                    |   |
| GPIO_11                | POWER#                      |   |



## Electrical Specifications

### Absolute Maximum Ratings

Exceeding maximum ratings<sup>[1]</sup> may shorten the useful life of the device.

|  |                        |
|--|------------------------|
| Storage temperature .....                                  | –55 °C to +100 °C      |
| Ambient temperature with power supplied (Industrial) ..... | –40 °C to +85 °C       |
| Supply voltage to ground potential                         |                        |
| V <sub>DDD</sub> .....                                     | 6.0 V                  |
| V <sub>BUS</sub> .....                                     | 6.0 V                  |
| V <sub>CCD</sub> .....                                     | 1.95 V                 |
| V <sub>GPIO</sub> .....                                    | V <sub>DDD</sub> + 0.5 |

Static discharge voltage ESD protection levels:

■ 2.2-KV HBM per JESD22-A114

Latch-up current ..... 140 mA

Current per GPIO ..... 25 mA

### Operating Conditions

T<sub>A</sub> (ambient temperature under bias)

Industrial ..... –40 °C to +85 °C

V<sub>BUS</sub> supply voltage ..... 3.15 V to 5.25 V

V<sub>DDD</sub> supply voltage ..... 1.71 V to 5.50 V

V<sub>CCD</sub> supply voltage ..... 1.71 V to 1.89 V

### Device-Level Specifications

All specifications are valid for –40 °C ≤ T<sub>A</sub> ≤ 85 °C, T<sub>J</sub> ≤ 100 °C, and 1.71 V to 5.50 V, except where noted.

**Table 2. DC Specifications**

| Parameter        | Description                       | Min  | Typ  | Max  | Units | Details/Conditions  |
|------------------|-----------------------------------|------|------|------|-------|---|
| V <sub>BUS</sub> | V <sub>BUS</sub> supply voltage   | 3.15 | 3.30 | 3.45 | V     | Set and configure the correct voltage range using a configuration utility for V <sub>BUS</sub> . Default 5 V.   |
|                  |                                   | 4.35 | 5.00 | 5.25 | V     |   |
| V <sub>DDD</sub> | V <sub>DDD</sub> supply voltage   | 1.71 | 1.80 | 1.89 | V     | Used to set I/O and core voltage. Set and configure the correct voltage range using a configuration utility for V <sub>DDD</sub> . Default 3.3 V.   |
|                  |                                   | 2.0  | 3.3  | 5.5  | V     |   |
| V <sub>CCD</sub> | Output voltage (for core logic)   | –    | 1.80 | –    | V     | Do not use this supply to drive the external device.<br><ul style="list-style-type: none"> <li>• 1.71 V ≤ V<sub>DDD</sub> ≤ 1.89 V: Short the V<sub>CCD</sub> pin with the V<sub>DDD</sub> pin</li> <li>• V<sub>DDD</sub> &gt; 2 V – connect a 1-μF capacitor (C<sub>efc</sub>) between the V<sub>CCD</sub> pin and ground</li> </ul> |
| C <sub>efc</sub> | External regulator voltage bypass | 1.00 | 1.30 | 1.60 | μF    | X5R ceramic or better   |
| I <sub>DD1</sub> | Operating supply current          | –    | 20   | –    | mA    | USB 2.0 FS, UART at 1-Mbps single channel, no GPIO switching  |
| I <sub>DD2</sub> | USB Suspend supply current        | –    | 5    | –    | μA    | Does not include current through a pull-up resistor on USB DP   |

**Table 3. AC Specifications**

| Parameter           | Description                  | Min   | Typ | Max   | Units | Details/Conditions |
|---------------------|------------------------------|-------|-----|-------|-------|--------------------|
| F1                  | Frequency                    | 47.04 | 48  | 48.96 | Mhz   | Non-USB mode       |
| F2                  |                              | 47.88 | 48  | 48.12 |       | USB mode           |
| Z <sub>out</sub>    | USB driver output impedance  | 28    | –   | 44    | Ω     |                    |
| T <sub>wakeup</sub> | Wakeup from USB Suspend mode | –     | 25  | –     | μs    |                    |

#### Note

1. Usage above the Absolute Maximum conditions may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.

**GPIO**
**Table 4. GPIO DC Specification**

| Parameter      | Description                              | Min                  | Typ | Max                 | Units      | Details/Conditions                           |
|----------------|--|----------------------|-----|---------------------|------------|--|
| $V_{IH}^{[2]}$ | Input voltage high threshold             | $0.7 \times V_{DD}$  | –   | –                   | V          | CMOS Input                                   |
| $V_{IL}$       | Input voltage low threshold              | –                    | –   | $0.3 \times V_{DD}$ | V          | CMOS Input                                   |
| $V_{IH}^{[2]}$ | LVTTL input, $V_{DD} < 2.7$ V            | $0.7 \times V_{DD}$  | –   | –                   | V          |  |
| $V_{IL}$       | LVTTL input, $V_{DD} < 2.7$ V            | –                    | –   | $0.3 \times V_{DD}$ | V          |  |
| $V_{IH}^{[2]}$ | LVTTL input, $V_{DD} \geq 2.7$ V         | 2                    | –   | –                   | V          |  |
| $V_{IL}$       | LVTTL input, $V_{DD} \geq 2.7$ V         | –                    | –   | 0.8                 | V          |  |
| $V_{OH}$       | Output voltage high level                | $V_{DD} - 0.4$       | –   | –                   | V          | $I_{OH} = 4$ mA,<br>$V_{DD} = 5$ V +/- 10%   |
| $V_{OH}$       | Output voltage high level                | $V_{DD} - 0.6$       | –   | –                   | V          | $I_{OH} = 4$ mA,<br>$V_{DD} = 3.3$ V +/- 10% |
| $V_{OH}$       | Output voltage high level                | $V_{DD} - 0.5$       | –   | –                   | V          | $I_{OH} = 1$ mA,<br>$V_{DD} = 1.8$ V +/- 5%  |
| $V_{OL}$       | Output voltage low level                 | –                    | –   | 0.4                 | V          | $I_{OL} = 8$ mA,<br>$V_{DD} = 5$ V +/- 10%   |
| $V_{OL}$       | Output voltage low level                 | –                    | –   | 0.6                 | V          | $I_{OL} = 8$ mA,<br>$V_{DD} = 3.3$ V +/- 10% |
| $V_{OL}$       | Output voltage low level                 | –                    | –   | 0.6                 | V          | $I_{OL} = 4$ mA,<br>$V_{DD} = 1.8$ V +/- 5%  |
| Rpullup        | Pull-up resistor                         | 3.5                  | 5.6 | 8.5                 | k $\Omega$ |  |
| Rpulldown      | Pull-down resistor                       | 3.5                  | 5.6 | 8.5                 | k $\Omega$ |  |
| $I_{IL}$       | Input leakage current (absolute value)   | –                    | –   | 2                   | nA         | 25 °C, $V_{DD} = 3.0$ V                      |
| $C_{IN}$       | Input capacitance                        | –                    | –   | 7                   | pF         |  |
| Vhysttl        | Input hysteresis LVTTL; $V_{DD} > 2.7$ V | 25                   | 40  | C                   | mV         |  |
| Vhyscmos       | Input hysteresis CMOS                    | $0.05 \times V_{DD}$ | –   | –                   | mV         |  |

**Table 5. GPIO AC Specification**

| Parameter       | Description            | Min | Typ | Max | Units | Details/Conditions                         |
|-----------------|------------------------|-----|-----|-----|-------|--|
| $T_{RiseFast1}$ | Rise Time in Fast mode | 2   | –   | 12  | ns    | $V_{DD} = 3.3$ V/ 5.5 V,<br>Clload = 25 pF |
| $T_{FallFast1}$ | Fall Time in Fast mode | 2   | –   | 12  | ns    | $V_{DD} = 3.3$ V/ 5.5 V,<br>Clload = 25 pF |
| $T_{RiseSlow1}$ | Rise Time in Slow mode | 10  | –   | 60  | ns    | $V_{DD} = 3.3$ V/ 5.5 V,<br>Clload = 25 pF |
| $T_{FallSlow1}$ | Fall Time in Slow mode | 10  | –   | 60  | ns    | $V_{DD} = 3.3$ V/ 5.5 V,<br>Clload = 25 pF |
| $T_{RiseFast2}$ | Rise Time in Fast mode | 2   | –   | 20  | ns    | $V_{DD} = 1.8$ V, Clload = 25 pF           |
| $T_{FallFast2}$ | Fall Time in Fast mode | 20  | –   | 100 | ns    | $V_{DD} = 1.8$ V, Clload = 25 pF           |
| $T_{RiseSlow2}$ | Rise Time in Slow mode | 2   | –   | 20  | ns    | $V_{DD} = 1.8$ V, Clload = 25 pF           |
| $T_{FallSlow2}$ | Fall Time in Slow mode | 20  | –   | 100 | ns    | $V_{DD} = 1.8$ V, Clload = 25 pF           |

**Note**

 2.  $V_{IH}$  must not exceed  $V_{DD} + 0.2$  V.



**nXRES**
**Table 6. nXRES DC Specifications**

| Parameter     | Description                  | Min                  | Typ | Max                  | Units      | Details/Conditions |
|---------------|------------------------------|----------------------|-----|----------------------|------------|--------------------|
| $V_{IH}$      | Input voltage high threshold | $0.7 \times V_{DDD}$ | –   | –                    | V          |                    |
| $V_{IL}$      | Input voltage low threshold  | –                    | –   | $0.3 \times V_{DDD}$ | V          |                    |
| $R_{pullup}$  | Pull-up resistor             | 3.5                  | 5.6 | 8.5                  | k $\Omega$ |                    |
| $C_{IN}$      | Input capacitance            | –                    | 5   | –                    | pF         |                    |
| $V_{hysxres}$ | Input voltage hysteresis     | –                    | 100 | –                    | mV         |                    |

**Table 7. nXRES AC Specifications**

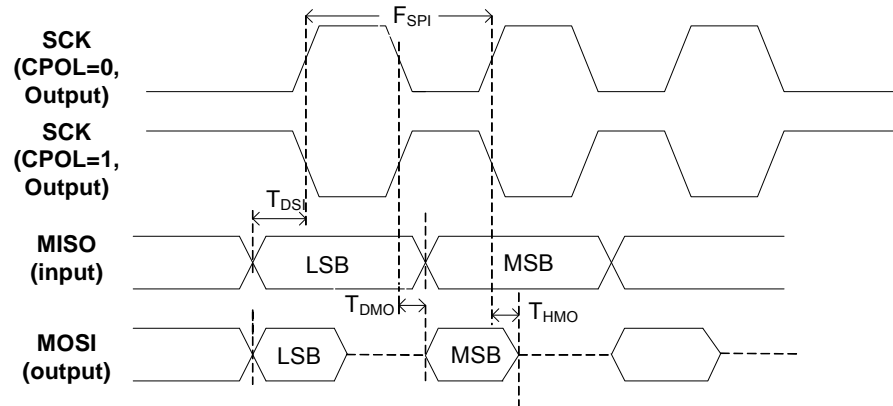
| Parameter   | Description       | Min | Typ | Max | Units   | Details/Conditions |
|-------------|-------------------|-----|-----|-----|---------|--------------------|
| Tresetwidth | Reset pulse width | 1   | –   | –   | $\mu$ s |                    |

**Table 8. UART AC Specifications**

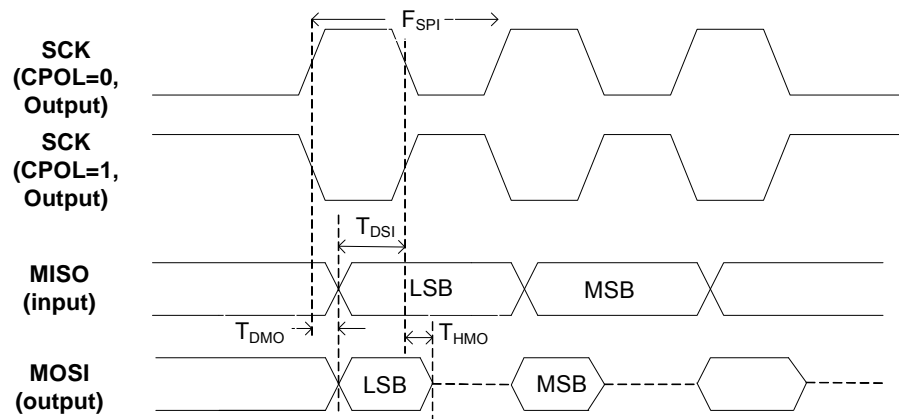
| Parameter  | Description   | Min | Typ | Max  | Units | Details/Conditions |
|------------|---------------|-----|-----|------|-------|--------------------|
| $F_{UART}$ | UART bit rate | 0.3 | –   | 3000 | kbps  |                    |

## SPI Specifications

**Figure 1. SPI Master Timing**

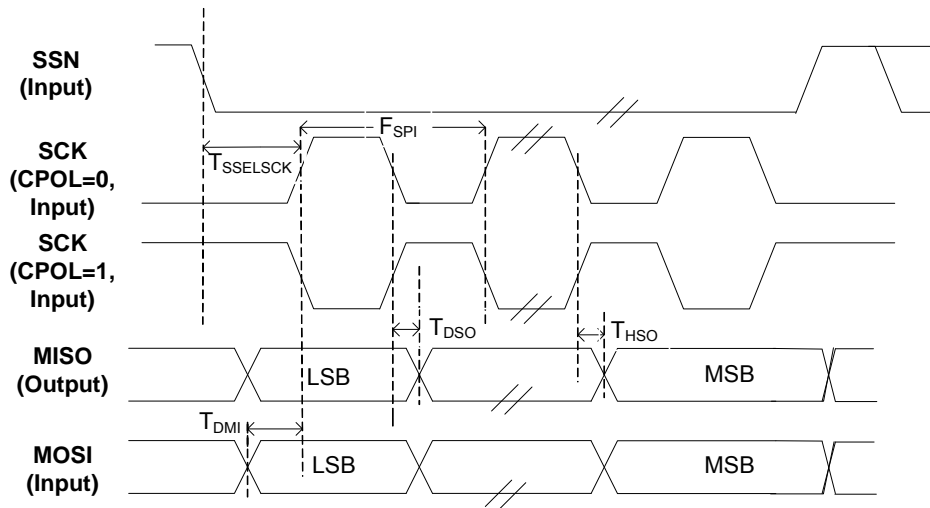


**SPI Master Timing for CPHA = 0 (Refer to Table 15)**

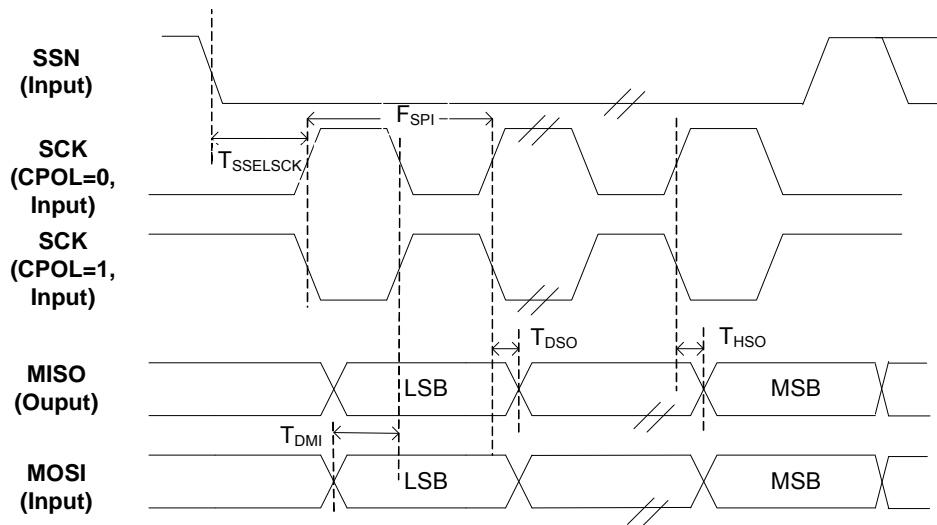


**SPI Master Timing for CPHA = 1 (Refer to Table 15)**

**Figure 2. SPI Slave Timing**



**SPI Slave Timing for CPHA = 0 (Refer to Table 15)**



**SPI Slave Timing for CPHA = 1 (Refer to Table 15)**

Table 9. SPI AC Specifications

| Parameter              | Description  | Min | Typ | Max   | Units | Details/Conditions |
|------------------------|--|-----|-----|-------|-------|--------------------|
| F <sub>SPI</sub>       | SPI operating frequency (Master/Slave)                               | –   | –   | 3     | MHz   |                    |
| WL <sub>SPI</sub>      | SPI word length  | 4   | –   | 16    | bits  |                    |
| <b>SPI Master Mode</b> |  |     |     |       |       |                    |
| T <sub>DMO</sub>       | MOSI valid after SClock driving edge                                 | –   | –   | 15    | ns    |                    |
| T <sub>DSI</sub>       | MISO valid before SClock capturing edge                              | 20  | –   | –     | ns    |                    |
| T <sub>HMO</sub>       | Previous MOSI data hold time with respect to capturing edge at slave | 0   | –   | –     | ns    |                    |
| <b>SPI Slave Mode</b>  |  |     |     |       |       |                    |
| T <sub>DMI</sub>       | MOSI valid before Sclock Capturing edge                              | 40  | –   | –     | ns    |                    |
| T <sub>DSO</sub>       | MISO valid after Sclock driving edge                                 | –   | –   | 104.4 | ns    |                    |
| T <sub>HSO</sub>       | Previous MISO data hold time   | 0   | –   | –     | ns    |                    |
| T <sub>SSELSCK</sub>   | SSEL valid to first SCK Valid edge                                   | 100 | –   | –     | ns    |                    |

## I<sup>2</sup>C Specifications

Table 10. I<sup>2</sup>C AC Specifications

| Parameter        | Description                | Min | Typ | Max | Units | Details/Conditions |
|------------------|----------------------------|-----|-----|-----|-------|--------------------|
| F <sub>I2C</sub> | I <sup>2</sup> C frequency | 1   | –   | 400 | kHz   |                    |

## CapSense Specifications

Table 11. CapSense AC Specifications

| Parameter        | Description                        | Min  | Typ | Max  | Units | Details/Conditions  |
|------------------|------------------------------------|------|-----|------|-------|---|
| V <sub>CSD</sub> | Voltage range of operation         | 1.71 | –   | 5.50 | V     |   |
| SNR              | Ratio of counts of finger to noise | 5    | –   | –    | Ratio | Sensor capacitance range of 9 to 35 pF; finger capacitance ≥ 0.1 pF sensitivity |

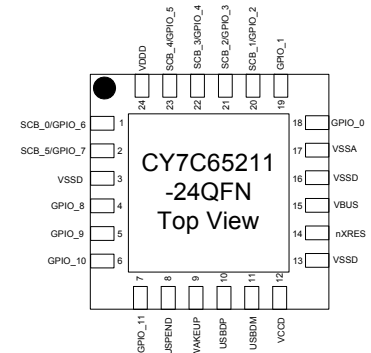
## Flash Memory Specifications

Table 12. Flash Memory Specifications

| Parameter        | Description  | Min  | Typ | Max | Units  | Details/Conditions |
|------------------|--|------|-----|-----|--------|--------------------|
| F <sub>end</sub> | Flash endurance  | 100K | –   | –   | cycles |                    |
| F <sub>ret</sub> | Flash retention. T <sub>A</sub> ≤ 85 °C, 10 K program/erase cycles | 10   | –   | –   | years  |                    |

## Pin Description

| Pin <sup>[3]</sup> | Type     | Name    | Default  | Description  |   |
|--------------------|----------|---------|----------|--|---|
| 1                  | SCB/GPIO | SCB_0   | GPIO_6   | RxD  | SCB/GPIO. See Table 13 and Table 14 on page 14. |
| 2                  | SCB/GPIO | SCB_5   | GPIO_7   | DTR#   | SCB/GPIO. See Table 13 and Table 14 on page 14. |
| 3                  | Power    | VSSD    | —        | Digital Ground   |   |
| 4                  | GPIO     | GPIO_8  | TRISTATE | GPIO. See Table 14   |   |
| 5                  | GPIO     | GPIO_9  | TRISTATE | GPIO. See Table 14   |   |
| 6                  | GPIO     | GPIO_10 | TRISTATE | GPIO. See Table 14   |   |
| 7                  | GPIO     | GPIO_11 | POWER#   | GPIO. See Table 14   |   |
| 8                  | Output   | SUSPEND | —        | Indicates device in suspend mode. Can be configured as active low/high using the configuration utility |   |
| 9                  | Input    | WAKEUP  | —        | Wakeup device from suspend mode. Can be configured as active low/high using the configuration utility  |   |
| 10                 | USBIO    | USBDP   | —        | USB Data Signal Plus, integrates termination resistor and a 1.5-k $\Omega$ pull-up resistor            |   |
| 11                 | USBIO    | USBDM   | —        | USB Data Signal Minus, integrates termination resistor   |   |
| 12                 | Power    | VCCD    | —        | This pin should be decoupled to ground using a 1- $\mu$ F capacitor or by connecting a 1.8-V supply    |   |
| 13                 | Power    | VSSD    | —        | Digital Ground   |   |
| 14                 | nXRES    | nXRES   | —        | Chip reset, active low. Can be left unconnected or have a pull-up resistor connected if not used       |   |
| 15                 | Power    | VBUS    | —        | VBUS Supply, 3.15 V to 5.25 V  |   |
| 16                 | Power    | VSSD    | —        | Digital Ground   |   |
| 17                 | Power    | VSSA    | —        | Analog Ground  |   |
| 18                 | GPIO     | GPIO_0  | TXLED#   | GPIO. See Table 14   |   |
| 19                 | GPIO     | GPIO_1  | RXLED#   | GPIO. See Table 14   |   |
| 20                 | SCB/GPIO | SCB_1   | GPIO_2   | DSR#   | SCB/GPIO. See Table 13 and Table 14 on page 14. |
| 21                 | SCB/GPIO | SCB_2   | GPIO_3   | RTS#   | SCB/GPIO. See Table 13 and Table 14 on page 14. |
| 22                 | SCB/GPIO | SCB_3   | GPIO_4   | CTS#   | SCB/GPIO. See Table 13 and Table 14 on page 14. |
| 23                 | SCB/GPIO | SCB_4   | GPIO_5   | TxD  | SCB/GPIO. See Table 13 and Table 14 on page 14. |
| 24                 | Power    | VDDD    | —        | Supply to the device core and Interface, 1.71 to 5.5 V   |   |



### Note

3. Any pin acting as an Input pin should not be left unconnected.

**Table 13. Serial Communication Block Configuration**

| Pin | Serial Port | Mode 0*           | Mode 1            | Mode 2            | Mode 3            | Mode 4           | Mode 5            | Mode 6           |
|-----|-------------|-------------------|-------------------|-------------------|-------------------|------------------|-------------------|------------------|
|     |             | <b>6-pin UART</b> | <b>4-pin UART</b> | <b>2-pin UART</b> | <b>SPI Master</b> | <b>SPI Slave</b> | <b>I2C Master</b> | <b>I2C Slave</b> |
| 1   | SCB_0       | RxD               | RxD               | RxD               | GPIO_6            | GPIO_6           | GPIO_6            | GPIO_6           |
| 20  | SCB_1       | DSR#              | GPIO_2            | GPIO_2            | SSEL_OUT          | SSEL_IN          | GPIO_2            | GPIO_2           |
| 21  | SCB_2       | RTS#              | RTS#              | GPIO_3            | MISO_IN           | MISO_OUT         | SCL_OUT           | SCL_IN           |
| 22  | SCB_3       | CTS#              | CTS#              | GPIO_4            | MOSI_OUT          | MOSI_IN          | SDA               | SDA              |
| 23  | SCB_4       | TxD               | TxD               | TxD               | SCLK_OUT          | SCLK_IN          | GPIO_5            | GPIO_5           |
| 2   | SCB_5       | DTR#              | GPIO_7            | GPIO_7            | GPIO_7            | GPIO_7           | GPIO_7            | GPIO_7           |

\*Note: The device is configured in Mode 0 as the default. Other modes can be configured using the configuration utility provided by Cypress.

|  |      |
|--|------|
|  | GPIO |
|  | SCB  |

**Table 14. GPIO Configuration**

| GPIO Configuration Option          | Description  |
|------------------------------------|--|
| TRISTATE                           | I/O tristated  |
| DRIVE 1                            | Output static 1  |
| DRIVE 0                            | Output static 0  |
| POWER#                             | This output is used to control power to an external logic through a switch to cut power off during an unconfigured USB device and USB suspend.<br>0 - USB device in Configured state<br>1 - USB device in Unconfigured state or during USB suspend mode  |
| TXLED#                             | Drives LED during USB transmit   |
| RXLED#                             | Drives LED during USB receive  |
| TX or RX LED#                      | Drives LED during USB transmit or receive  |
| BCD0<br>BCD1                       | Configurable battery charger detect pins to indicate the type of USB charger (SDP, CDP, or DCP)<br>Configuration example:<br>00 - Draw up to 100 mA (unconfigured state)<br>01 - SDP (up to 500 mA)<br>10 - CDP/DCP (up to 1.5 A)<br>11 - Suspend (up to 2.5 mA)<br>This truth table can be configured using a configuration utility |
| BUSDETECT                          | VBUS detection. Connect the VBUS to this pin through a resistor network for VBUS detection when using the BCD feature (refer to page 19).  |
| CS0, CS1, CS2, CS3, CS4            | CapSense button input (max up to 5)  |
| CSout0, CSout1, CSout2             | Indicates which CapSense button is pressed   |
| CMOD<br>(Available on GPIO_0 only) | External modulator capacitor, connect a 2.2-nF capacitor ( $\pm 10\%$ ) to ground  |
| Cshield (optional)                 | Shield for waterproofing   |

Note: These signal options can be configured on any of the available GPIO pins using the configuration utility provided by Cypress.



## USB Power Configurations

The following section describes possible USB power configurations for the CY7C65211. Refer to the [Pin Description on page 13](#) for signal details.

### USB Bus-Powered Configuration

Figure 3 shows an example of the CY7C65211 in a bus-powered design. The VBUS is connected directly to the CY7C65211 because it has an internal regulator.

The USB bus-powered system must comply with the following requirements:

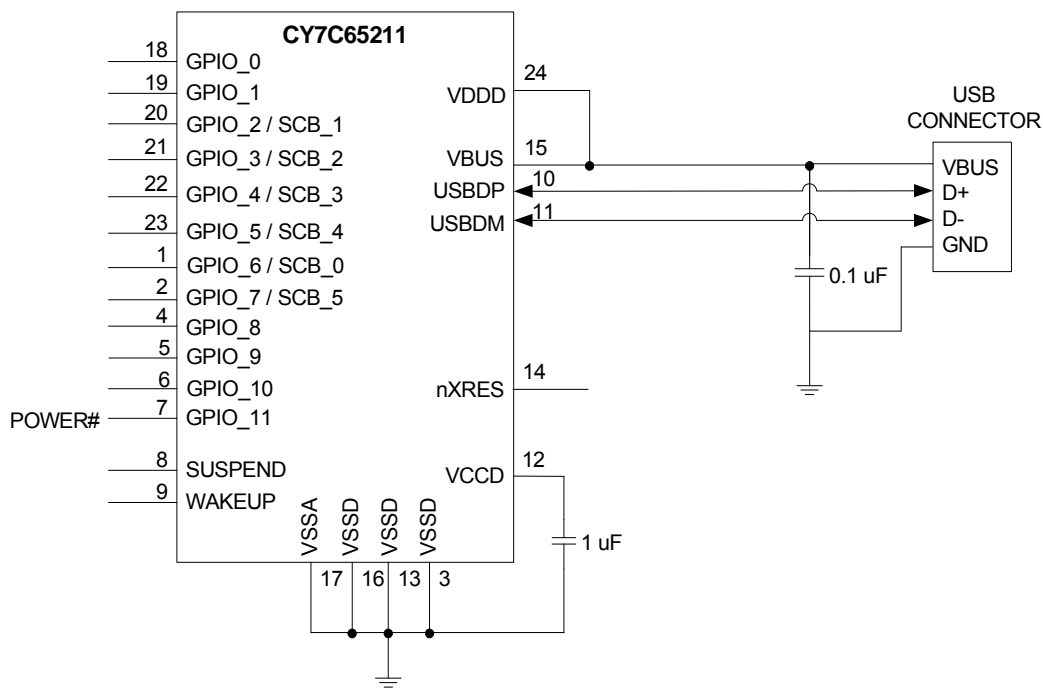
1. The system should not draw more than 100 mA prior to USB enumeration (Unconfigured state).
2. The system should not draw more than 2.5 mA during the USB Suspend mode.

3. A high-power bus-powered system (can draw more than 100 mA when operational) must use POWER# (configured over GPIO) to keep the current consumption below 100 mA prior to USB enumeration, and 2.5 mA during USB Suspend state.

4. The system should not draw more than 500 mA from the USB host.

The configuration descriptor in the CY7C65211 flash should be updated to indicate bus power and the maximum current required by the system using the configuration utility.

**Figure 3. Bus-Powered Configuration**



## Self-Powered Configuration

Figure 4 shows an example of CY7C65211 in a self-powered design. A self-powered system does not use the VBUS from the host to power the system, but it has its own power supply. A self-powered system has no restriction on current consumption because it does not draw any current from the VBUS.

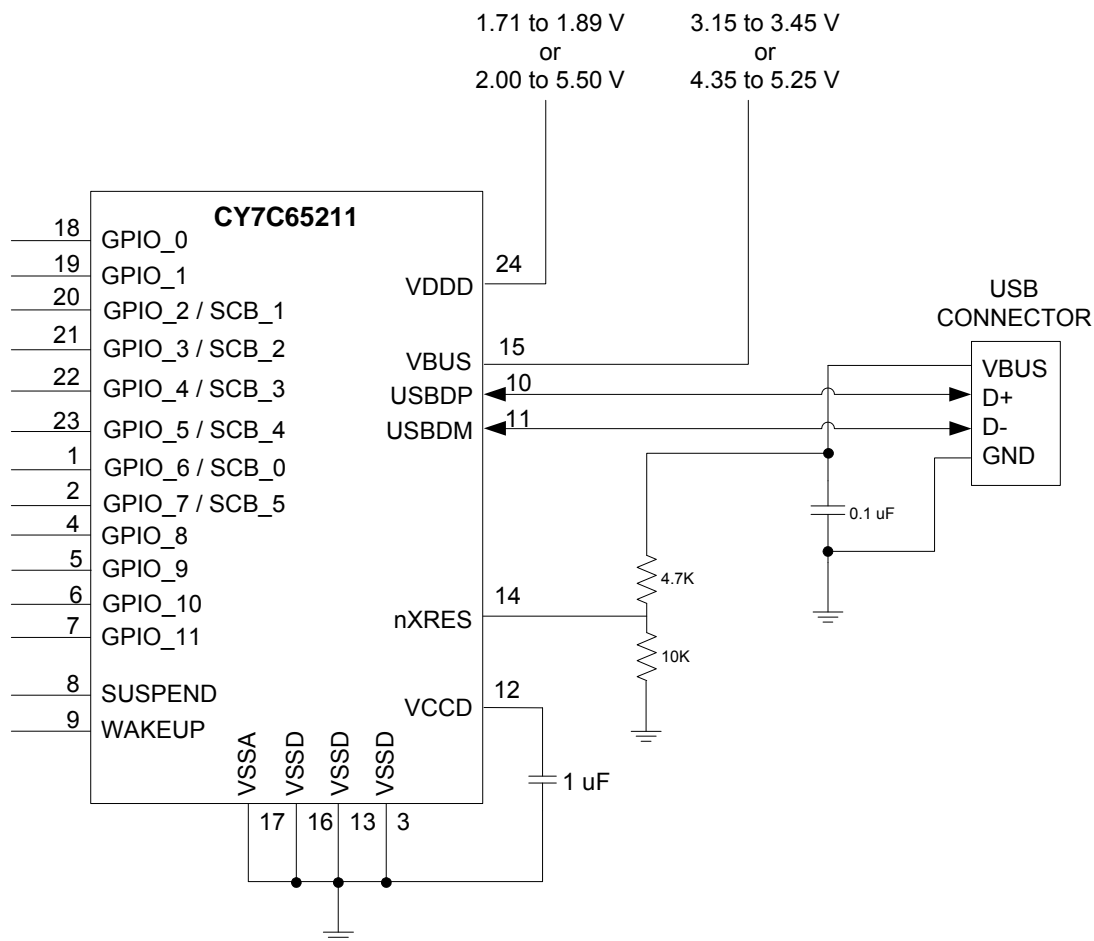
When the VBUS is present, CY7C65211 enables an internal, 1.5-k $\Omega$  pull-up resistor on USBDP. When the VBUS is absent (USB host is powered down), CY7C65211 removes the 1.5-k $\Omega$  pull-up resistor on USBDP. This ensures that no current flows

from the USBDP to the USB host through a 1.5-k $\Omega$  pull-up resistor, to comply with the USB 2.0 specification.

When reset is asserted to CY7C65211, all the I/O pins are tristated.

The configuration descriptor in the CY7C65211 flash should be updated to indicate self-power using the configuration utility.

**Figure 4. Self-Powered Configuration**



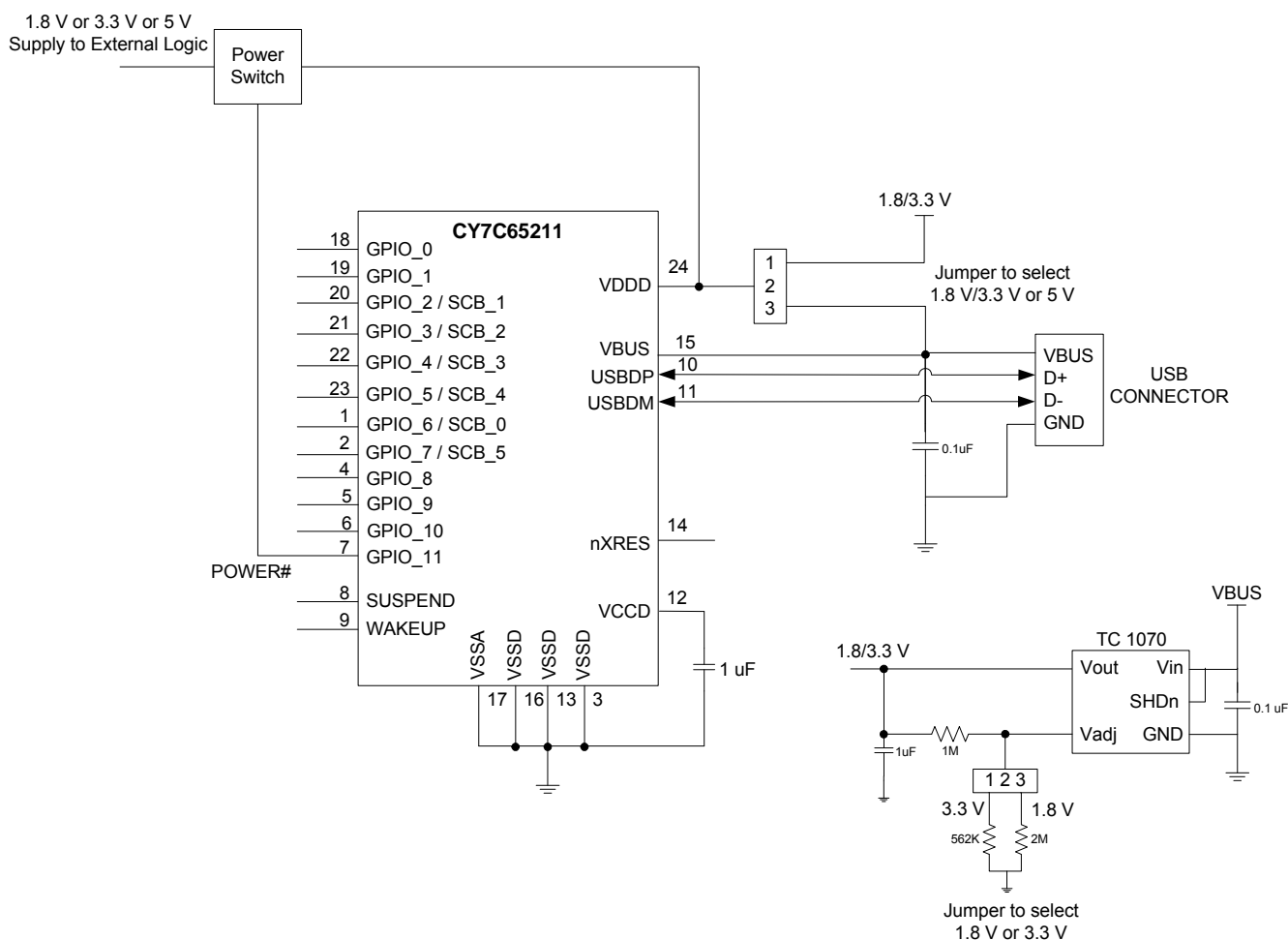
## USB Bus Powered with Variable I/O Voltage

Figure 5 shows CY7C65211 in a bus-powered system with variable I/O voltage. A low dropout (LDO) regulator is used to supply 1.8 V or 3.3 V, using a jumper switch the input of which is 5 V from the VBUS. Another jumper switch is used to select 1.8/3.3 V or 5 V from the VBUS for the VDDD pin of CY7C65211. This allows I/O voltage and supply to external logic to be selected among 1.8 V, 3.3 V, or 5 V.

The USB bus-powered system must comply with the following conditions:

- The system should not draw more than 100 mA prior to USB enumeration (unconfigured state)
- The system should not draw more than 2.5 mA during USB Suspend mode
- A high-power bus-powered system (can draw more than 100 mA when operational) must use POWER# (configured over GPIO) to keep the current consumption below 100 mA prior to USB enumeration and 2.5 mA during the USB Suspend state

**Figure 5. USB bus powered with 1.8-V, 3.3-V, or 5-V Variable I/O Voltage** <sup>[4]</sup>



### Note

4.  $1.71 \text{ V} \leq \text{VDDD} \leq 1.89 \text{ V}$  - Short VCCD pin with VDDD pin;  $\text{VDDD} > 2 \text{ V}$  - connect a 1-μF decoupling capacitor to the VCCD pin.

## Application Examples

The following section provides CY7C65211 application examples.

### USB-to-RS232 Bridge

CY7C65211 can connect any embedded system, with a serial port, to a host PC through USB. CY7C65211 enumerates as a COM port on the host PC.

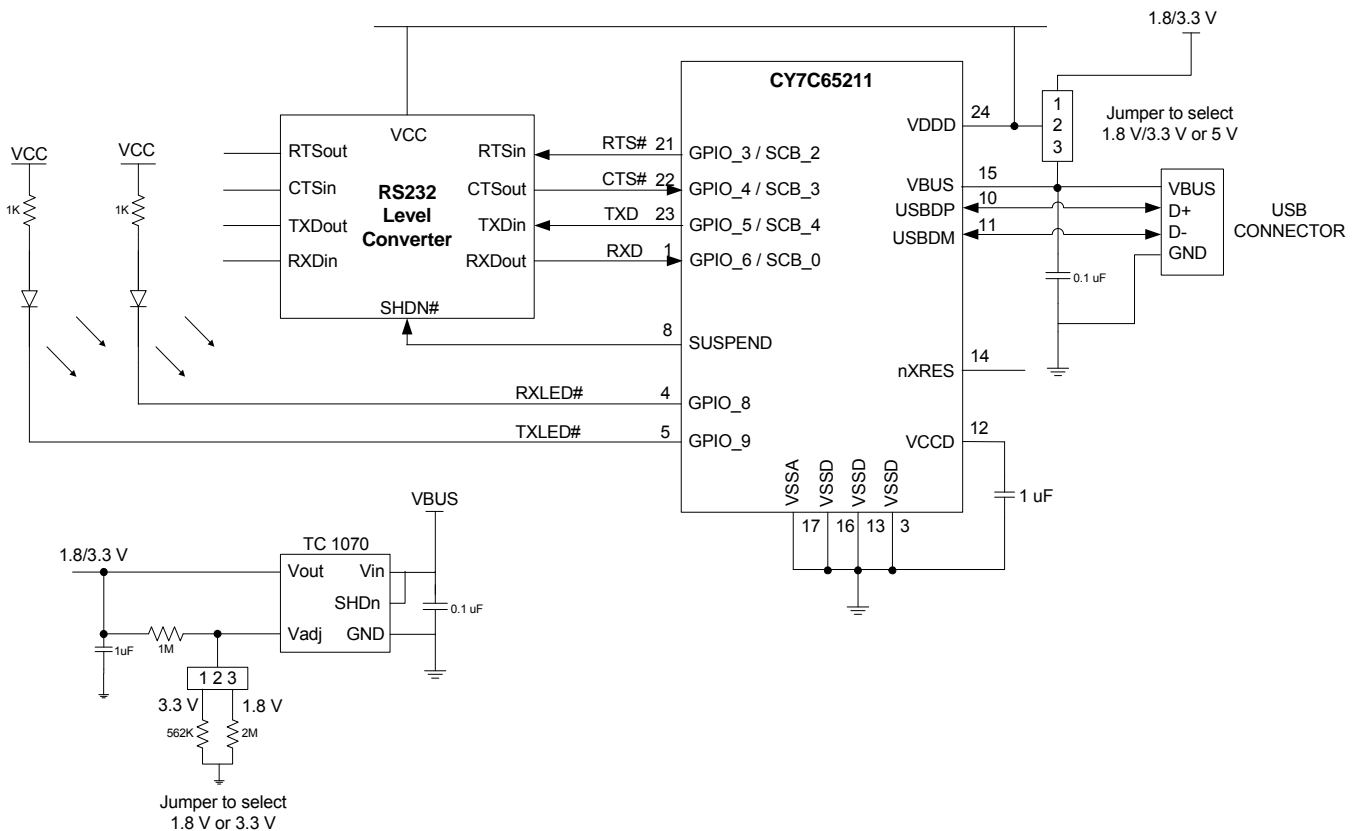
The RS232 protocol follows bipolar signaling – that is, the output signal toggles between negative and positive polarity. The valid RS232 signal is either in the  $-3\text{V}$  to  $-15\text{V}$  range or in the  $+3\text{V}$  to  $+15\text{V}$  range, and the range between  $-3\text{V}$  to  $+3\text{V}$  is invalid. In the RS232, Logic 1 is called "Mark" and it corresponds to a negative voltage range. Logic 0 is called "Space" and it corresponds to a positive voltage range. The RS232 level converter

facilitates this polarity inversion and the voltage-level translation between the CY7C65211's UART interface and RS232 signaling.

In this application, as shown in Figure 6, SUSPEND is connected to the SHDN# pin of the RS232-level converter to indicate USB suspend or USB not enumerated.

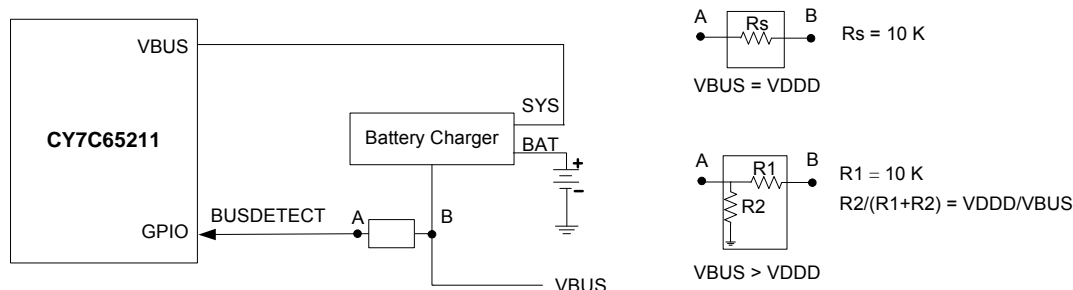
GPIO8 and GPIO9 are configured as RXLED# and TXLED# to drive two LEDs, indicating data transmit and receive.

Figure 6. USB to RS232 Bridge



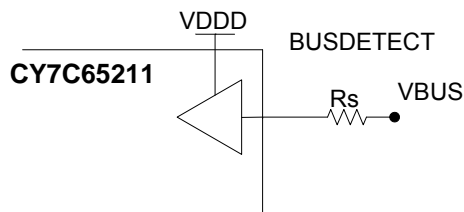


In a battery charger system, a 9-V spike on the VBUS is possible. The CY7C65211 VBUS pin is intolerant to voltage above 6 V. In the absence of over-voltage protection (OVP) on the VBUS line, the VBUS should be connected to BUSDETECT (GPIO configured) using the resistive network and the output of the battery charger to the VBUS pin of CY7C65211, as shown in the following figure.



When the VBUS and VDDD are at the same voltage potential, the VBUS can be connected to the GPIO using a series resistor ( $R_s$ ). This is shown in the following figure. If there is a charger failure and the VBUS becomes 9 V, then the 10-k $\Omega$  resistor plays two roles. It reduces the amount of current flowing into the forward-biased diodes in the GPIO, and it reduces the voltage seen on the pad.

**Figure 8. GPIO VBUS Detection, VBUS = VDDD**



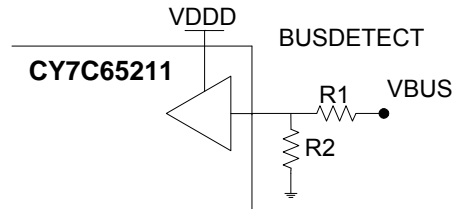
When the VBUS > VDDD, a resistor voltage divider is required to reduce the voltage from the VBUS down to VDDD for the GPIO sensing the VBUS voltage. This is shown in the following figure. The resistors should be sized as follows:

$$R_1 \geq 10 \text{ k}$$

$$R_2 / (R_1 + R_2) = V_{DDD} / V_{BUS}$$

The first condition limits the voltage and current for the charger failure situation, as described in the previous paragraph, while the second condition allows for normal-operation VBUS detection.

**Figure 9. GPIO VBUS detection, VBUS > VDDD**





## CapSense

In Figure 10, CY7C65211 is configured to support four CapSense buttons. Three GPIOs are configured to indicate which CapSense button is pressed by the finger (as shown in the table next to the schematic). If two CapSense buttons are implemented, then two GPIOs (CSout0 and CSout1) are configured to indicate which CapSense button is pressed.

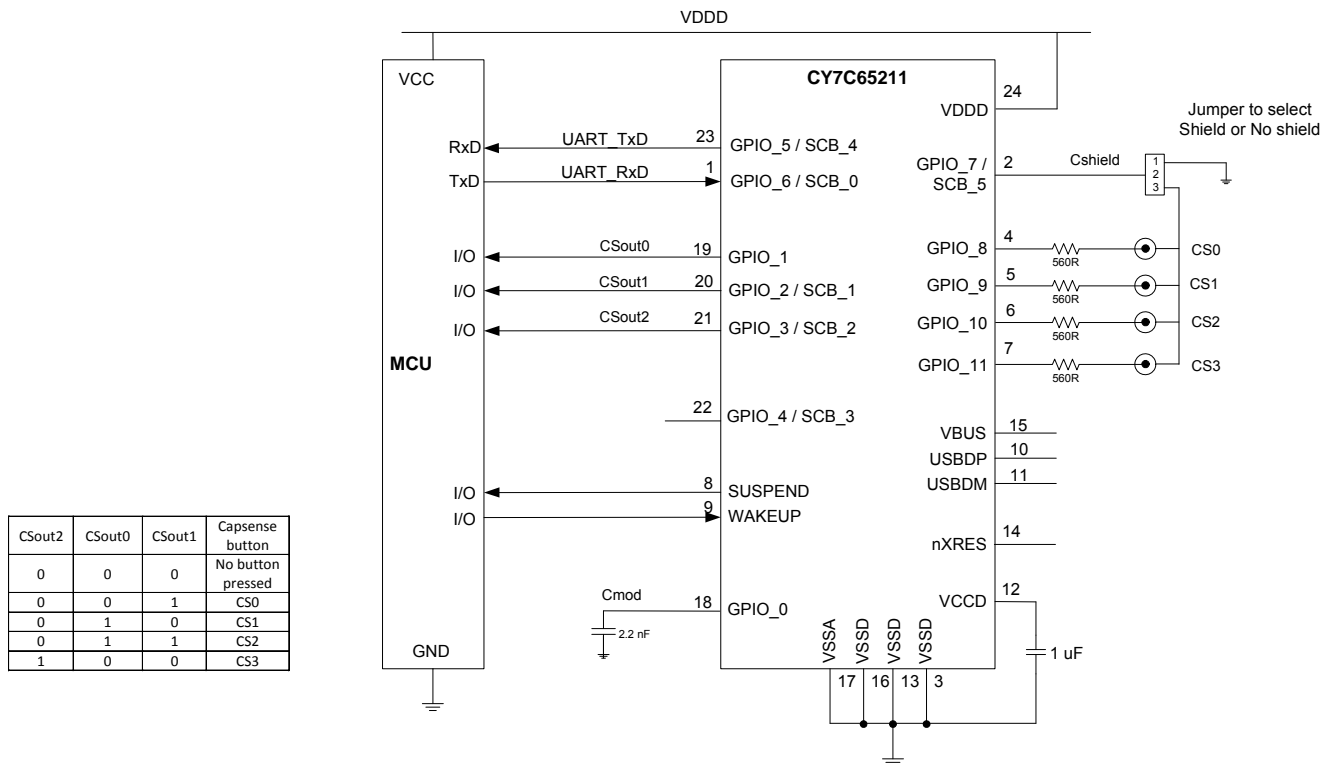
A 2.2-nF (10%) capacitor (Cmod) must be connected on the GPIO\_0 pin for proper CapSense operation.

Optionally, the GPIO\_7 pin is configured as Cshield and connected to the shield of the CapSense button, as shown in Figure 10.

Shield prevents false triggering of buttons due to water droplets, and guarantees CapSense operation (the sensors respond to finger touch).

For further information on CapSense, refer to [Getting Started with CapSense](#).

Figure 10. CapSense Schematic



## USB-to-I<sup>2</sup>C Bridge

In Figure 11, CY7C65211 is configured as a USB-to-I<sup>2</sup>C Bridge. The CY7C65211 I<sup>2</sup>C can be configured as a master or a slave using the configuration utility. CY7C65211 supports I<sup>2</sup>C data rates up to 100 kbps in the standard mode (SM) and 400 kbps in the fast mode (FM).

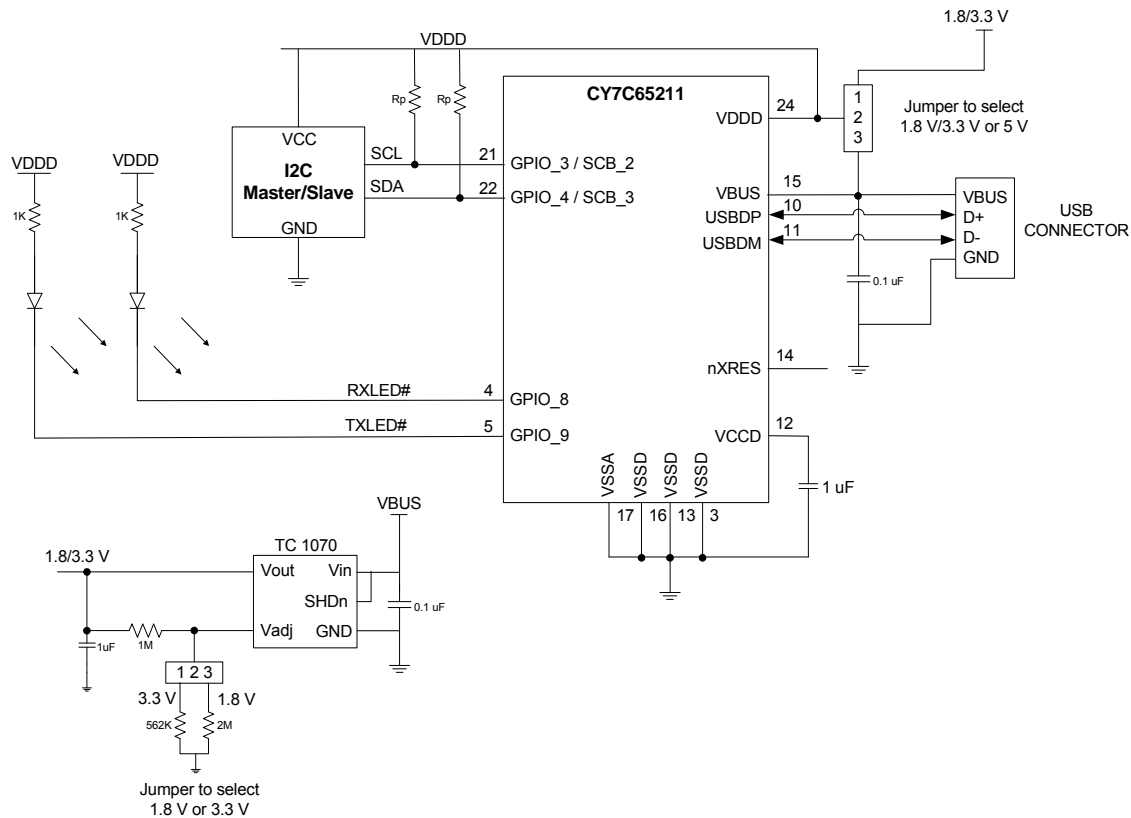
In the master mode, SCL is output from CY7C65211. In the slave mode, SCL is input to CY7C65211. The I<sup>2</sup>C slave address for CY7C65211 can be configured using the configuration utility. The

SDA data line is bi-directional in the master/slave modes. The drive modes of the SCL and SDA port pins are always open drain.

GPIO8 and GPIO9 are configured as RXLED# and TXLED# to drive two LEDs to indicate USB receive and transmit.

Refer to the NXP I<sup>2</sup>C specification for further details on the protocol.

**Figure 11. USB-to-I<sup>2</sup>C Bridge**



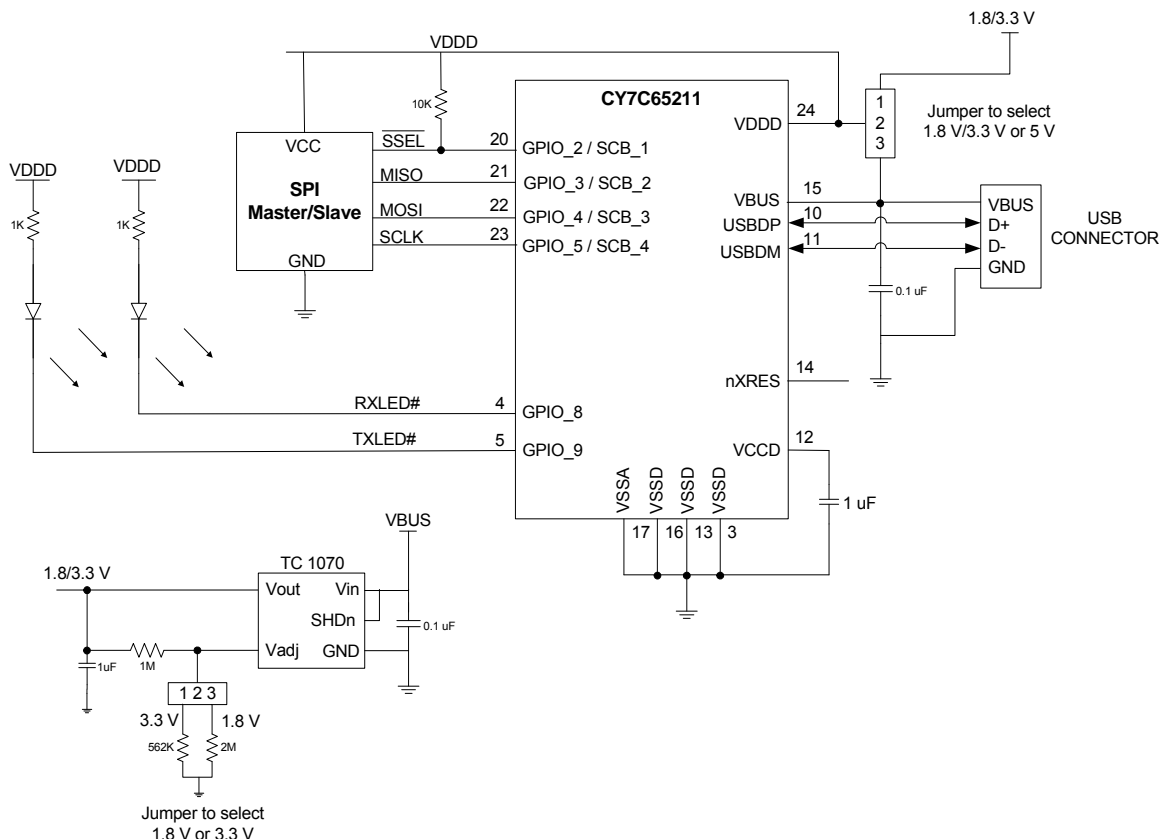
## USB-to-SPI Bridge

In [Figure 12](#), CY7C65211 is configured as a USB-to-SPI Bridge. The CY7C65211 SPI can be configured as a master or a slave using the configuration utility. CY7C65211 supports SPI frequency up to 3 MHz. It can support transaction sizes ranging from 4 bits to 16 bits, which can be configured using the configuration utility.

In the master mode, the SCLK, MOSI, and SSEL lines act as outputs and MISO acts as an input. In the slave mode, the SCLK, MOSI, and SSEL lines act as inputs and MISO acts as an output.

GPIO8 and GPIO9 are configured as RXLED# and TXLED# to drive two LEDs to indicate USB receive and transmit.

### Figure 12. USB-to-SPI Bridge



CY7C65211 supports three versions of the SPI protocol:

- **Motorola** - This is the original SPI protocol.
- **Texas Instruments** - A variation of the original SPI protocol in which the data frames are identified by a pulse on the SSEL line.
- **National Semiconductors** - A half-duplex variation of the original SPI protocol.

## Motorola

The original SPI protocol is defined by Motorola. It is a full-duplex protocol: transmission and reception occur at the same time.

A single (full-duplex) data transfer follows these steps: The master selects a slave by driving its SSEL line to '0'. Next, it drives the data on its MOSI line and it drives a clock on its SCLK line. The slave uses the edges of the transmitted clock to capture the data on the MOSI line. The slave drives data on its MISO line. The master captures the data on the MISO line. Repeat the process for all bits in the data transfer.

Multiple data transfers may happen without the SSEL line changing from '0' to '1' and back from '1' to '0' in between the individual transfers. As a result, slaves must keep track of the progress of data transfers to separate individual transfers.

When not transmitting data, the SSEL line is '1' and the SCLK is typically off.

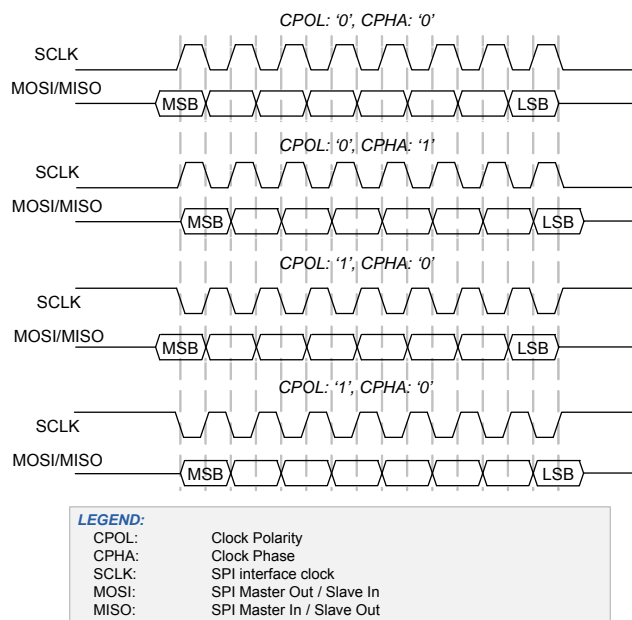
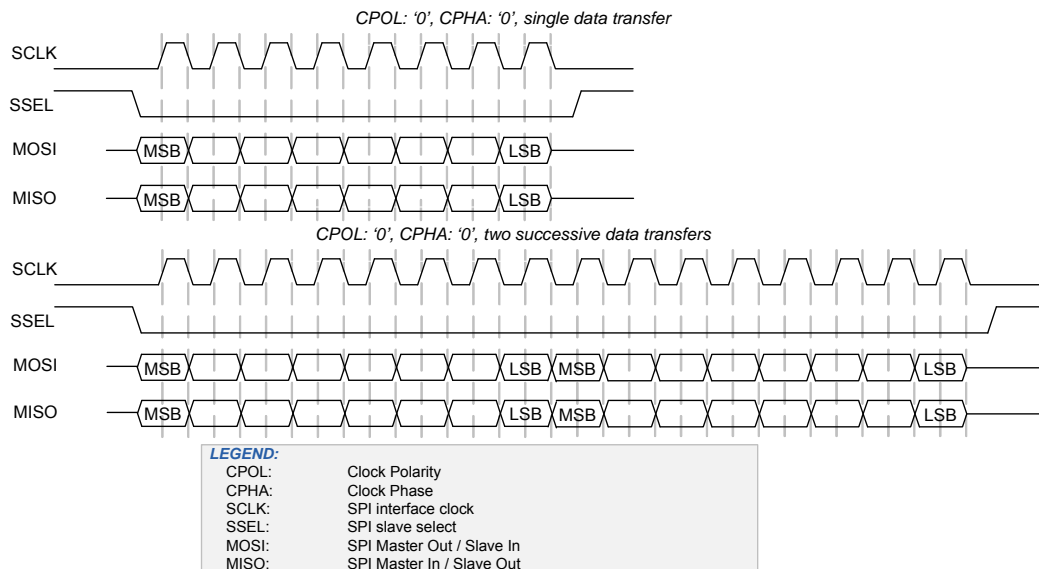
The Motorola SPI protocol has four modes that determine how data is driven and captured on the MOSI and MISO lines. These modes are determined by clock polarity (CPOL) and clock phase (CPHA). Clock polarity determines the value of the SCLK line when not transmitting data:

- CPOL is '0': SCLK is '0' when not transmitting data.
- CPOL is '1': SCLK is '1' when not transmitting data.

The clock phase determines when data is driven and captured. It is dependent on the value of CPOL:

**Table 15. SPI Protocol Modes**

| Mode | CPOL | CPHA | Description   |
|------|------|------|---|
| 0    | 0    | 0    | Data is driven on a falling edge of SCLK. Data is captured on a rising edge of SCLK |
| 1    | 0    | 1    | Data is driven on a rising edge of SCLK. Data is captured on a falling edge of SCLK |
| 2    | 1    | 0    | Data is driven on a rising edge of SCLK. Data is captured on a falling edge of SCLK |
| 3    | 1    | 1    | Data is driven on a falling edge of SCLK. Data is captured on a rising edge of SCLK |

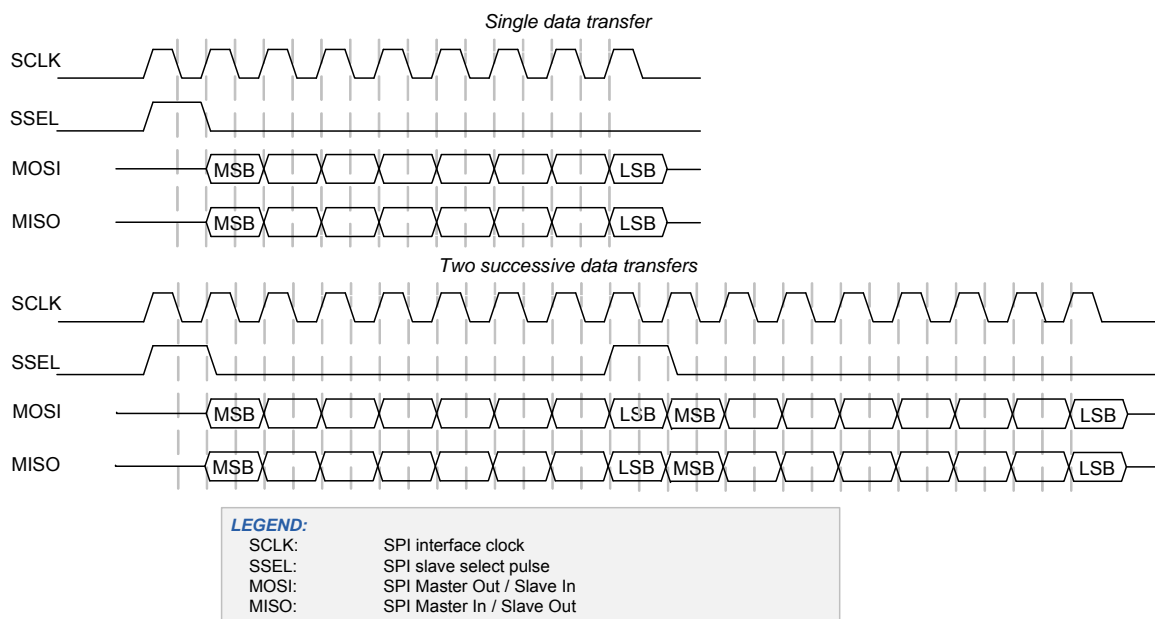
**Figure 13. Driving and Capturing MOSI/MISO Data As A Function of CPOL and CPHA**

**Figure 14. Single 8-bit Data Transfer and Two Successive 8-bit Data Transfers in Mode 0 (CPOL is '0', CPHA is '0')**


### Texas Instruments

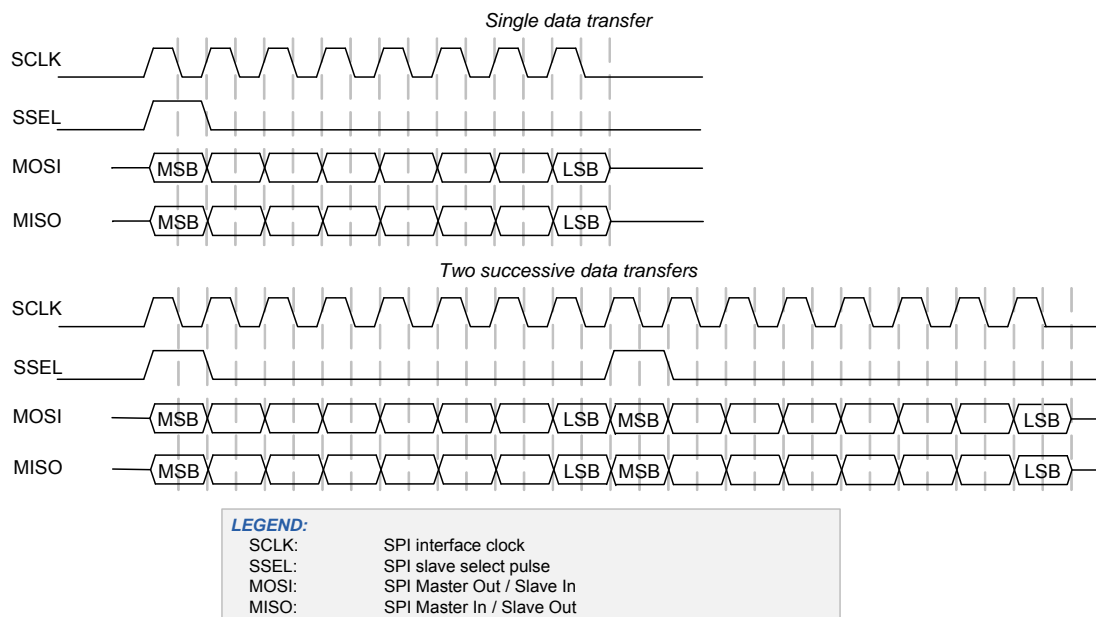
Texas Instruments' SPI protocol redefines the use of the SSEL signal. It uses the signal to indicate the start of a data transfer, rather than a low, active slave-select signal. The start of a transfer is indicated by a high, active pulse of a single-bit transfer period. This pulse may occur one cycle before the transmission of the first data bit, or it may coincide with the transmission of the first data bit. The transmitted clock SCLK is a free-running clock.

The TI SPI protocol only supports mode 1 (CPOL is '0' and CPHA is '1'): Data is driven on a rising edge of SCLK and data is captured on a falling edge of SCLK.

The following figure illustrates a single 8-bit data transfer and two successive 8-bit data transfers. The SSEL pulse precedes the first data bit. Note how the SSEL pulse of the second data transfer coincides with the last data bit of the first data transfer.



The following figure illustrates a single 8-bit data transfer and two successive 8-bit data transfers. The SSEL pulse coincides with the first data bit.



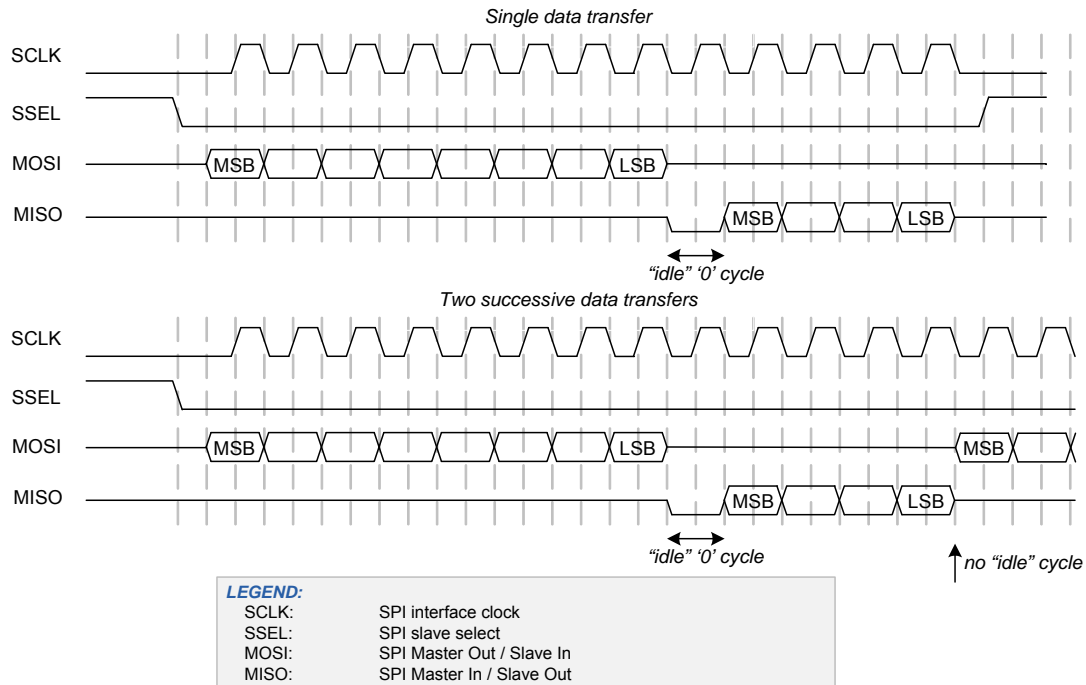
### National Semiconductor

National Semiconductor's SPI protocol is a half-duplex protocol. Rather than transmission and reception occurring at the same time, they take turns (transmission happens before reception). A single "idle" bit transfer period separates transmission from reception.

**Note** Successive data transfers are NOT separated by an "idle" bit transfer period.

The transmission data transfer size and reception data transfer size may differ. National Semiconductor's SPI protocol supports only mode 0: Data is driven on a falling edge of SCLK, and data is captured on a rising edge of SCLK.

The following figure illustrates a single data transfer and two successive data transfers. In both cases, the transmission transfer size is 8 bits and the reception transfer size is 4 bits.



**Note** The above figure defines MISO and MOSI as undefined when the lines are considered idle (not carrying valid information). It will drive the outgoing line values to '0' during idle time (to satisfy the requirements of specific master devices (NXP LPC17xx) and specific slave devices (MicroChip EEPROM)).



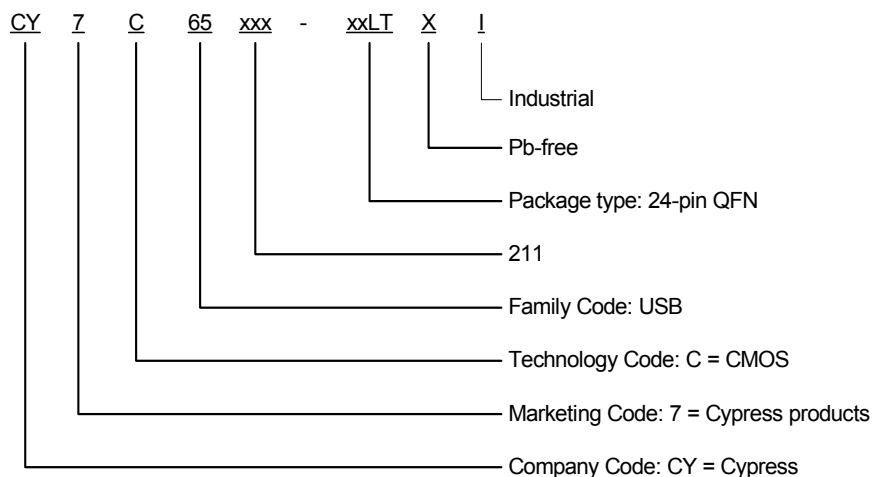
## Ordering Information

Table 16 lists the key package features and ordering codes of the CY7C65211. For more information, contact your local sales representative.

**Table 16. Key Features and Ordering Information**

| Package  | Ordering Code    | Operating Range |
|--|------------------|-----------------|
| 24-pin QFN (4.00 × 4.00 × 0.55 mm, 0.5 mm pitch) (Pb-free) | CY7C65211-24LTXI | Industrial      |

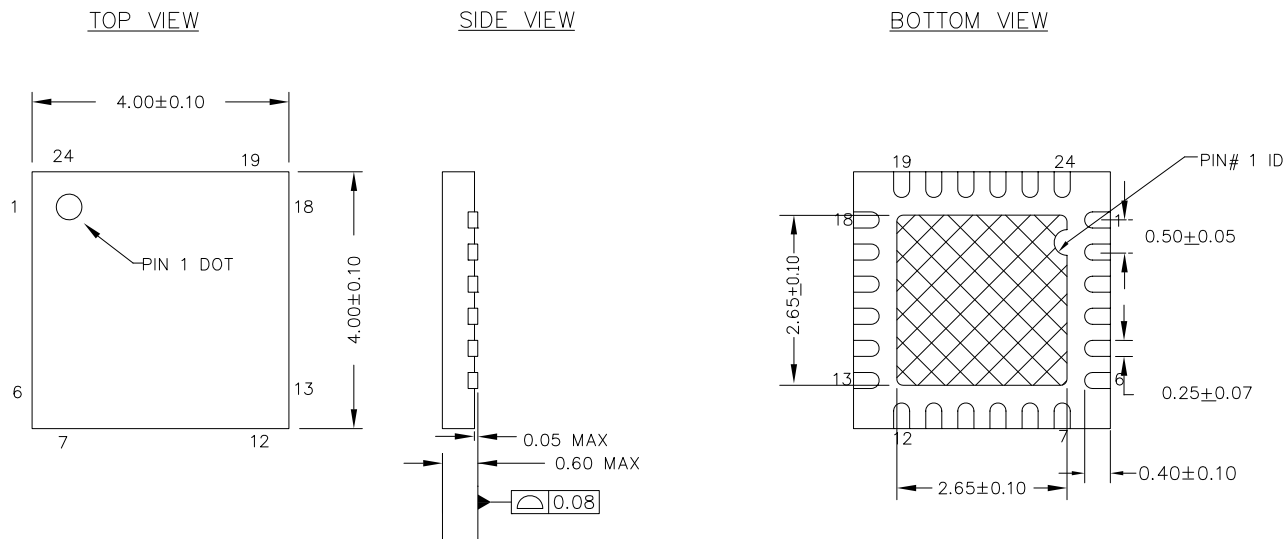
### Ordering Code Definitions




## Package Information

Support currently is planned for the 24-pin QFN package.

**Figure 15. 24-pin QFN 4 mm × 4 mm × 0.55 mm LQ24A 2.65 × 2.65 EPAD (Sawn)**



### NOTES :

1.  HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT : 29 ± 3 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13937 \*E

**Table 17. Package Characteristics**

| Parameter      | Description                   | Min | Typ  | Max | Units |
|----------------|-------------------------------|-----|------|-----|-------|
| T <sub>A</sub> | Operating ambient temperature | -40 | 25   | 85  | °C    |
| THJ            | Package θ <sub>JA</sub>       | —   | 18.4 | —   | °C/W  |

**Table 18. Solder Reflow Peak Temperature**

| Package    | Maximum Peak Temperature | Maximum Time at Peak Temperature |
|------------|--------------------------|----------------------------------|
| 24-pin QFN | 260 °C                   | 30 seconds                       |

**Table 19. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2**

| Package    | MSL   |
|------------|-------|
| 24-pin QFN | MSL 3 |

## Acronyms

**Table 20. Acronyms Used in this Document**

| Acronym          | Description                                 |
|------------------|---|
| BCD              | battery charger detection                   |
| CDC              | communication driver class                  |
| CDP              | charging downstream port                    |
| DCP              | dedicated charging port                     |
| DLL              | dynamic link library                        |
| ESD              | electrostatic discharge                     |
| GPIO             | general purpose input/output                |
| HBM              | human-body model                            |
| I <sup>2</sup> C | inter-integrated circuit                    |
| MCU              | microcontroller unit                        |
| OSC              | oscillator                                  |
| PHDC             | personal health care device class           |
| PID              | product identification                      |
| SCB              | serial communication block                  |
| SCL              | I <sup>2</sup> C serial clock               |
| SDA              | I <sup>2</sup> C serial data                |
| SDP              | standard downstream port                    |
| SIE              | serial interface engine                     |
| SPI              | serial peripheral interface                 |
| VCOM             | virtual communication port                  |
| USB              | Universal Serial Bus                        |
| UART             | universal asynchronous receiver transmitter |
| VID              | vendor identification                       |

## Document Conventions

### Units of Measure

**Table 21. Units of Measure**

| Symbol | Unit of Measure                           |
|--------|---|
| °C     | degree Celsius                            |
| DMIPS  | Dhrystone million instructions per second |
| kΩ     | kilo-ohm                                  |
| KB     | kilobyte                                  |
| kHz    | kilohertz                                 |
| kV     | kilovolt                                  |
| Mbps   | megabits per second                       |
| MHz    | megahertz                                 |
| mm     | millimeter                                |
| V      | volt                                      |

## Document History Page

| Document Title: CY7C65211 USB-Serial Single-Channel (UART/I <sup>2</sup> C/SPI) Bridge with CapSense® and BCD<br>Document Number: 001-82042 |         |                 |                 |   |
|---|---------|-----------------|-----------------|---|
| Revision  | ECN     | Orig. of Change | Submission Date | Description of Change   |
| **  | 3714911 | ZKR             | 08/24/2012      | New datasheet.  |
| *A  | 3814090 | ZKR             | 12/19/2012      | Removed reference to HID.<br>Changed number of GPIO pins from 14 to 12.<br>Updated description for Vhysttl parameter.<br>Updated Pin Description.   |
| *B  | 3947144 | ZKR             | 03/28/2013      | Removed "4-KB SRAM" from <a href="#">Features</a> and <a href="#">Contents</a> .<br>Updated <a href="#">Block Diagram</a> and <a href="#">System Resources</a> .<br>Removed CPU, Flash, and SRAM sections.<br>Updated USB PID in <a href="#">Internal Flash Configuration Table 1</a> .<br>Removed VCC2 and VCCIO2 parameter descriptions in <a href="#">DC Specifications</a> .<br>Changed CPU Frequency parameter to Frequency parameter in <a href="#">AC Specifications</a> .<br>Updated <a href="#">GPIO AC Specification</a><br>Updated <a href="#">Pin Description</a> and <a href="#">Battery-Operated, Bus-Powered USB to MCU with Battery Charge Detection</a> sections.<br>Added <a href="#">USB Power Configurations</a> and <a href="#">Application Examples</a> sections.<br>Removed Flash/SRAM feature from <a href="#">Ordering Information</a> |
| *C  | 4002280 | ZKR             | 05/16/2013      | Changed XRES to nXRES throughout the document.<br>Changed flash size to 512 bytes.<br>Added note in I2C Interface section.<br>Added note for Absolute Maximum Ratings.<br>Changed maximum current per GPIO from 100 mA to 25 mA.<br>Added note for V <sub>IH</sub> parameter in GPIO DC Specification<br>Removed C <sub>sout_int</sub> from GPIO Configuration section.<br>Updated schematic USB to MCU Interface with Battery Charge Detection.<br>Updated CapSense schematic.   |
| *D  | 4019327 | ZKR             | 06/13/2013      | Changed status from Preliminary to Final.<br>Updated <a href="#">Features</a> .<br>Updated <a href="#">Block Diagram</a> .<br>Updated <a href="#">Functional Overview</a> .<br>Updated <a href="#">Electrical Specifications</a> .<br>Updated <a href="#">Pin Description</a> .<br>Updated <a href="#">USB Power Configurations</a> .<br>Updated <a href="#">Application Examples</a> .   |

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