

FEATURES

- **Guaranteed Offset Voltage:** 150 μ V Max
 -55°C to 125°C: 500 μ V Max
- **Guaranteed Drift:** 4 μ V/°C Max
- **Guaranteed Bias Current**
 70°C: 150pA Max
 125°C: 2.5nA Max
- **Guaranteed Slew Rate:** 12V/ μ s Min
- Available in 8-Pin PDIP and SO Packages

APPLICATIONS

- Precision, High Speed Instrumentation
- Logarithmic Amplifiers
- D/A Output Amplifiers
- Photodiode Amplifiers
- Voltage-to-Frequency Converters
- Frequency-to-Voltage Converters
- Fast, Precision Sample-and-Hold

DESCRIPTION

The **LT[®]1055/LT1056** JFET input operational amplifiers combine precision specifications with high speed performance.

For the first time, 16V/ μ s slew rate and 6.5MHz gain bandwidth product are simultaneously achieved with offset voltage of typically 50 μ V, 1.2 μ V/°C drift, bias currents of 40pA at 70°C and 500pA at 125°C.

The 150 μ V maximum offset voltage specification is the best available on any JFET input operational amplifier.

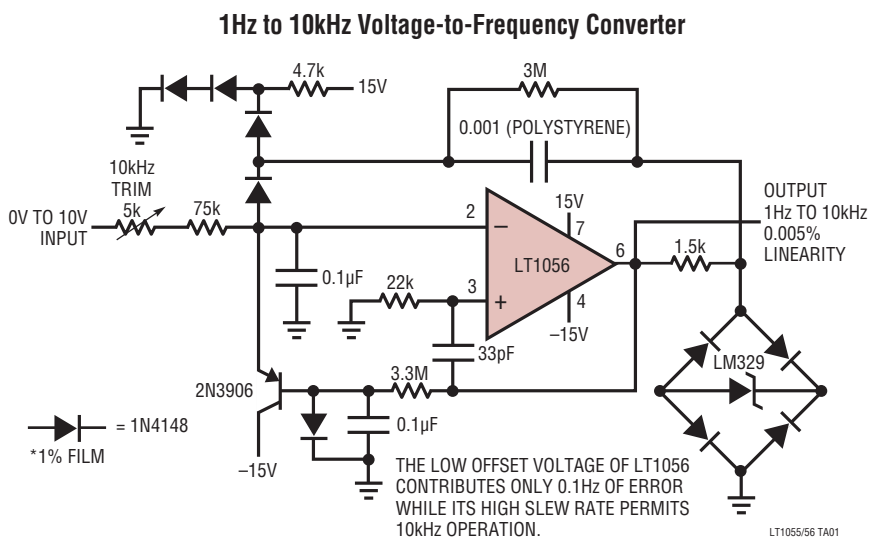
The LT1055 and LT1056 are differentiated by their operating currents. The lower power dissipation LT1055 achieves lower bias and offset currents and offset voltage. The additional power dissipation of the LT1056 permits higher slew rate, bandwidth and faster settling time with a slight sacrifice in DC performance.

The voltage-to-frequency converter shown below is one of the many applications which utilize both the precision and high speed of the LT1055/LT1056.

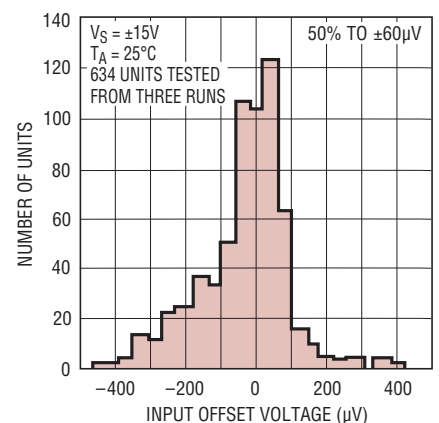
For a JFET input op amp with 23V/ μ s guaranteed slew rate, refer to the LT1022 data sheet.

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TYPICAL APPLICATION



**Distribution of Input Offset Voltage
(H Package)**



LT1055/56 TA02

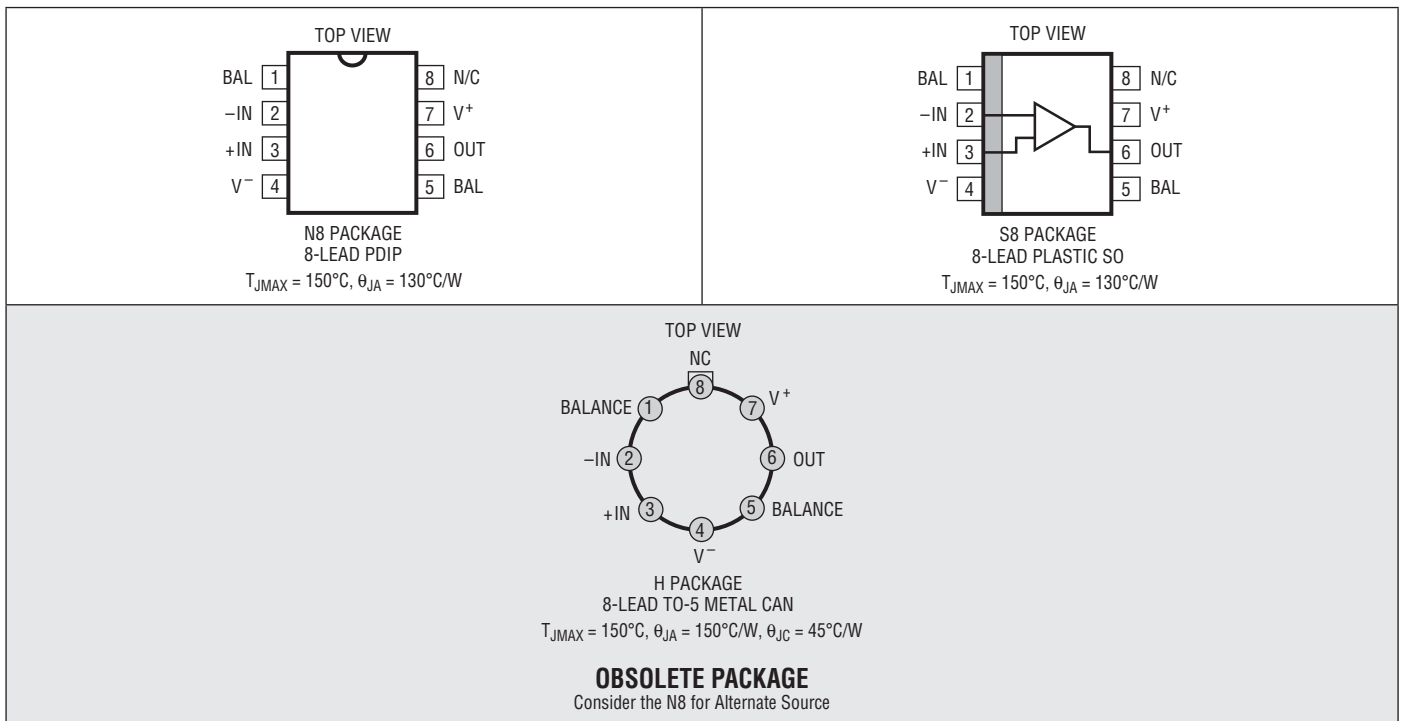
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LT1055/LT1056

ABSOLUTE MAXIMUM RATINGS (Note 1)

| | | | |
|--|----------------|---|-------------------|
| Supply Voltage | ±20V | LT1055AC/LT1055C/LT1056AC/ LT1056C | 0°C to 70°C |
| Differential Input Voltage | ±40V | Storage Temperature Range | All Devices |
| Input Voltage | ±20V | Lead Temperature (Soldering, 10 sec)..... | 300°C |
| Output Short-Circuit Duration | Indefinite | | |
| Operating Temperature Range | | | |
| LT1055AM/LT1055M/LT1056AM/ LT1056M (OBSOLETE) | -55°C to 125°C | | |

PIN CONFIGURATION



ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|------------------|-----------------|--------------|-----------------------|-------------------|
| LT1055CN8#PBF | LT1055CN8#TRPBF | LT1055CN8 | 8-Lead PDIP | 0°C to 70°C |
| LT1056CN8#PBF | LT1056CN8#TRPBF | LT1056CN8 | 8-Lead PDIP | 0°C to 70°C |
| LT1055S8#PBF | LT1055S8#TRPBF | 1055 | 8-Lead Plastic SO | 0°C to 70°C |
| LT1056S8#PBF | LT1056S8#TRPBF | 1056 | 8-Lead Plastic SO | 0°C to 70°C |
| OBSOLETE PACKAGE | | | | |
| LT1055ACH#PBF | LT1055ACH#TRPBF | LT1055ACH | 8-Lead TO-5 Metal Can | 0°C to 70°C |
| LT1055CH#PBF | LT1055CH#TRPBF | LT1055CH | 8-Lead TO-5 Metal Can | 0°C to 70°C |
| LT1055AMH#PBF | LT1055AMH#TRPBF | LT1055AMH | 8-Lead TO-5 Metal Can | -55°C to 125°C |
| LT1055MH#PBF | LT1055MH#TRPBF | LT1055MH | 8-Lead TO-5 Metal Can | -55°C to 125°C |
| LT1056ACH#PBF | LT1056ACH#TRPBF | LT1056ACH | 8-Lead TO-5 Metal Can | 0°C to 70°C |
| LT1056CH#PBF | LT1056CH#TRPBF | LT1056CH | 8-Lead TO-5 Metal Can | 0°C to 70°C |
| LT1056AMH#PBF | LT1056AMH#TRPBF | LT1056AMH | 8-Lead TO-5 Metal Can | -55°C to 125°C |
| LT1056MH#PBF | LT1056MH#TRPBF | LT1056MH | 8-Lead TO-5 Metal Can | -55°C to 125°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part markings, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$. $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$ unless otherwise noted.

| SYMBOL | PARAMETER | CONDITIONS | LT1055AM/LT1056AM LT1055AC/LT1056AC | | | LT1055M/LT1056M LT1055CH/LT1056CH LT1055CN8/LT1056CN8 | | | UNITS |
|-----------|-------------------------------|---|--|----------------|-----------------|---|----------------|-----------------|--|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V_{OS} | Input Offset Voltage (Note 2) | LT1055 H Package LT1056 H Package LT1055 N8 Package LT1056 N8 Package | | 50 50 | 150 180 | | 70 70 | 400 450 | μV μV μV μV |
| I_{OS} | Input Offset Current | Fully Warmed Up | | 2 | 10 | | 2 | 20 | pA |
| I_B | Input Bias Current | Fully Warmed Up $V_{CM} = 10\text{V}$ | | ± 10 30 | ± 50 130 | | ± 10 30 | ± 50 150 | pA pA |
| | Input Resistance:Differential | Common Mode $V_{CM} = -11\text{V to } 8\text{V}$ $V_{CM} = 8\text{V to } 11\text{V}$ | | 10^{12} | | | 10^{12} | | Ω |
| | | | | 10^{12} | | | 10^{12} | | Ω |
| | Input Capacitance | | | 10^{11} | | | 10^{11} | | Ω |
| | | | | 4 | | | 4 | | pF |
| e_n | Input Noise Voltage | 0.1Hz to 10Hz LT1055 LT1056 | | 1.8 2.5 | | | 2.0 2.8 | | μV_{P-P} μV_{P-P} |
| | Input Noise Voltage Density | $f_0 = 10\text{Hz}$ (Note 3) $f_0 = 1\text{kHz}$ (Note 4) | | 28 14 | 50 20 | | 30 15 | 60 22 | $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ |
| I_n | Input Noise Current Density | $f_0 = 10\text{Hz}, 1\text{kHz}$ (Note 5) | | 1.8 | 4 | | 1.8 | 4 | $\text{fA}/\sqrt{\text{Hz}}$ |
| A_{VOL} | Large-Signal Voltage Gain | $V_0 = \pm 10\text{V}$ $R_L = 2\text{k}$ $R_L = 1\text{k}$ | | 150 130 | 400 300 | | 120 100 | 400 300 | V/mV V/mV |
| | Input Voltage Range | | | ± 11 | ± 12 | | ± 11 | ± 12 | V |
| CMRR | Common Mode Rejection Ratio | $V_{CM} = \pm 11\text{V}$ | | 86 | 100 | | 83 | 98 | dB |
| PSRR | Power Supply Rejection Ratio | $V_S = \pm 10\text{V to } \pm 18\text{V}$ | | 90 | 106 | | 88 | 104 | dB |
| V_{OUT} | Output Voltage Swing | $R_L = 2\text{k}$ | | ± 12 | ± 13.2 | | ± 12 | ± 13.2 | V |

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LT1055/LT1056

ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$. $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$ unless otherwise noted.†

| SYMBOL | PARAMETER | CONDITIONS | LT1055AM/LT1056AM LT1055AC/LT1056AC | | | LT1055M/LT1056M LT1055CH/LT1056CH LT1055CN8/LT1056CN8 | | | UNITS |
|----------------|---------------------------------|-------------------------|--|-----|-----|---|-----|-----|------------------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| SR | Slew Rate | LT1055 | 10 | 13 | | 7.5 | 12 | | V/ μs |
| | | LT1056 | 12 | 16 | | 9.0 | 14 | | V/ μs |
| GBW | Gain Bandwidth Product | f = 1MHz LT1055 | | 5.0 | | | 4.5 | | MHz |
| | | LT1056 | | 6.5 | | | 5.5 | | MHz |
| I _S | Supply Current | LT1055 | | 2.8 | 4.0 | | 2.8 | 4.0 | mA |
| | | LT1056 | | 5.0 | 6.5 | | 5.0 | 7.0 | mA |
| | Offset Voltage Adjustment Range | R _{POT} = 100k | | ±5 | | | ±5 | | mV |

The ● denotes the specifications which apply over the temperature range $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$. $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$ unless otherwise noted.

| SYMBOL | PARAMETER | CONDITIONS | | LT1055AC LT1056AC | | | LT1055CH/LT1056CH LT1055CN8/LT1056CN8 | | | UNITS |
|------------------|---|--|---|----------------------|-------|------|--|-------|------|------------------------------|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V _{OS} | Input Offset Voltage (Note 2) | LT1055 H Package | ● | | 100 | 330 | | 140 | 750 | μV |
| | | LT1056 H Package | ● | | 100 | 360 | | 140 | 800 | μV |
| | | LT1055 N8 Package | ● | | | | | 250 | 1250 | μV |
| | | LT1056 N8 Package | ● | | | | | 280 | 1350 | μV |
| | Average Temperature Coefficient of Input Offset Voltage | H Package (Note 6) | ● | | 1.2 | 4.0 | | 1.6 | 8.0 | $\mu\text{V}/^\circ\text{C}$ |
| | | N8 Package (Note 6) | ● | | | | | 3.0 | 12.0 | $\mu\text{V}/^\circ\text{C}$ |
| I _{OS} | Input Offset Current | Warmed Up T _A = 70°C LT1055 | ● | | 10 | 50 | | 16 | 80 | pA |
| | | LT1056 | ● | | 14 | 70 | | 18 | 100 | pA |
| I _B | Input Bias Current | Warmed Up T _A = 70°C LT1055 | ● | | ±30 | ±150 | | ±40 | ±200 | pA |
| | | LT1056 | ● | | ±40 | ±80 | | ±50 | ±240 | pA |
| A _{VOL} | Large-Signal Voltage Gain | V _O = ±10V, R _L = 2k | ● | 80 | 250 | | 60 | 250 | V/mV | |
| CMRR | Common Mode Rejection Ratio | V _{CM} = ±10.5V | ● | 85 | 100 | | 82 | 98 | dB | |
| PSRR | Power Supply Rejection Ratio | V _S = ±10V to ±18V | ● | 89 | 105 | | 87 | 103 | dB | |
| V _{OUT} | Output Voltage Swing | R _L = 2k | ● | ±12 | ±13.1 | | ±12 | ±13.1 | V | |

The ● denotes the specifications which apply over the temperature range $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$. $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$, unless otherwise noted.

| SYMBOL | PARAMETER | CONDITIONS | | LT1055AM LT1056AM | | | LT1055M LT1056M | | | UNITS |
|------------------|---|---|---|----------------------|-------|------|--------------------|-------|------|------------------------------|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V _{OS} | Input Offset Voltage (Note 2) | LT1055 | ● | | 180 | 500 | | 250 | 1200 | μV |
| | | LT1056 | ● | | 180 | 550 | | 250 | 1250 | μV |
| | Average Temperature Coefficient of Input Offset Voltage | (Note 6) | ● | | 1.3 | 4.0 | | 1.8 | 8.0 | $\mu\text{V}/^\circ\text{C}$ |
| I _{OS} | Input Offset Current | Warmed Up T _A = 125°C LT1055 | ● | | 0.20 | 1.2 | | 0.25 | 1.8 | nA |
| | | LT1056 | ● | | 0.25 | 1.5 | | 0.30 | 2.4 | nA |
| I _B | Input Bias Current | Warmed Up T _A = 125°C LT1055 | ● | | ±0.4 | ±2.5 | | ±0.5 | ±4.0 | nA |
| | | LT1056 | ● | | ±0.5 | ±3.0 | | ±0.6 | ±5.0 | nA |
| A _{VOL} | Large-Signal Voltage Gain | V _O = ±10V, R _L = 2k | ● | 40 | 120 | | 35 | 120 | V/mV | |
| CMRR | Common Mode Rejection Ratio | V _{CM} = ±10.5V | ● | 85 | 100 | | 82 | 98 | dB | |
| PSRR | Power Supply Rejection Ratio | V _S = ±10V to ±17V | ● | 88 | 104 | | 86 | 102 | dB | |
| V _{OUT} | Output Voltage Swing | R _L = 2k | ● | ±12 | ±12.9 | | ±12 | ±12.9 | V | |

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ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$. $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$ unless otherwise noted.

| SYMBOL | PARAMETER | CONDITIONS | LT1055CS8/LT1056CS8 | | | UNITS |
|-----------|-------------------------------|--|-------------------------|--------------------|------------------|--|
| | | | MIN | TYP | MAX | |
| V_{OS} | Input Offset Voltage (Note 2) | | | 500 | 1500 | μV |
| I_{OS} | Input Offset Current | Fully Warm Up | | 5 | 30 | pA |
| I_B | Input Bias Current | Fully Warm Up $V_{CM} = 10\text{V}$ | | ± 30 30 | ± 100 150 | pA pA |
| | Input Resistance | Differential Common Mode $V_{CM} = -11\text{V}$ to 8V $V_{CM} = 8\text{V}$ to 11V | | 0.4 0.4 0.05 | | $\text{T}\Omega$ $\text{T}\Omega$ $\text{T}\Omega$ |
| | Input Capacitance | | | 4 | | pF |
| e_n | Input Noise Voltage | 0.1Hz to 10Hz | LT1055 LT1056 | 2.5 3.5 | | μV_{P-P} μV_{P-P} |
| | Input Noise Voltage Density | $f_0 = 10\text{Hz}$ (Note 4) $f_0 = 1\text{kHz}$ (Note 4) | | 35 15 | 70 22 | $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ |
| i_n | Input Noise Current Density | $f_0 = 10\text{Hz}$, 1kHz (Note 5) | | 2.5 | 10 | $\text{fA}/\sqrt{\text{Hz}}$ |
| A_{VOL} | Large-Signal Voltage Gain | $V_0 = \pm 10\text{V}$ $R_L = 2\text{k}$ $R_L = 1\text{k}$ | | 120 100 | 400 300 | V/mV V/mV |
| | Input Voltage Range | | | ± 11 | ± 12 | V |
| CMRR | Common Mode Rejection Ratio | $V_{CM} = \pm 11\text{V}$ | | 83 | 98 | dB |
| PSRR | Power Supply Rejection Ratio | $V_S = \pm 10\text{V}$ to $\pm 18\text{V}$ | | 88 | 104 | dB |
| V_{OUT} | Output Voltage Swing | $R_L = 2\text{K}$ | | ± 12 | ± 13.2 | V |
| SR | Slew Rate | | LT1055 LT1056 | 7.5 9.0 | 12 14 | $\text{V}/\mu\text{s}$ $\text{V}/\mu\text{s}$ |
| | | | | | 4.5 5.5 | MHz MHz |
| GBW | Gain Bandwidth Product | $f = 1\text{MHz}$ | LT1055 LT1056 | | | |
| I_S | Supply Current | | LT1055 LT1056 | 2.8 5.0 | 4.0 7.0 | mA mA |
| | | Offset Voltage Adjustment Range | $R_{POT} = 100\text{k}$ | | ± 5 | |

The ● denotes the specifications which apply over the temperature range $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$. $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$ unless otherwise noted.

| SYMBOL | PARAMETER | CONDITIONS | | LT1055CS8/LT1056CS8 | | | UNITS |
|-----------|---|--|---|---------------------|------------|-----------|------------------------------|
| | | | | MIN | TYP | MAX | |
| V_{OS} | Input Offset Voltage (Note 2) | | ● | | 800 | 2200 | μV |
| | Average Temperature Coefficient of Input Offset Voltage | | ● | | 4 | 15 | $\mu\text{V}/^\circ\text{C}$ |
| I_{OS} | Input Offset Current | Warm Up, $T_A = 70^\circ\text{C}$ | ● | | 18 | 150 | pA |
| I_B | Input Bias Current | Warm Up, $T_A = 70^\circ\text{C}$ | ● | | ± 60 | ± 400 | pA |
| A_{VOL} | Large-Signal Voltage Gain | $V_0 = \pm 10\text{V}$, $R_L = 2\text{k}$ | ● | 60 | 250 | | V/mV |
| CMRR | Common Mode Rejection Ratio | $V_{CM} = \pm 10.5\text{V}$ | ● | 82 | 98 | | dB |
| PSRR | Power Supply Rejection Ratio | $V_S = \pm 10\text{V}$ to $\pm 18\text{V}$ | ● | 87 | 103 | | dB |
| V_{OUT} | Output Voltage Swing | $R_L = 2\text{K}$ | ● | ± 12 | ± 13.1 | | V |

LT1055/LT1056

ELECTRICAL CHARACTERISTICS

For MIL-STD components, please refer to LTC883 data sheet for test listing and parameters.

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Offset voltage is measured under two different conditions: (a) approximately 0.5 seconds after application of power; (b) at $T_A = 25^\circ\text{C}$ only, with the chip heated to approximately 38°C for the LT1055 and to 45°C for the LT1056, to account for chip temperature rise when the device is fully warmed up.

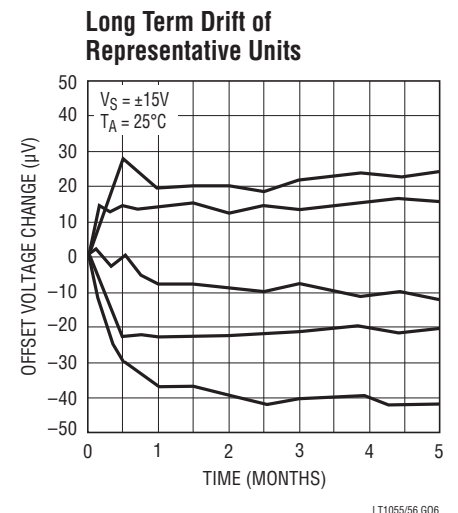
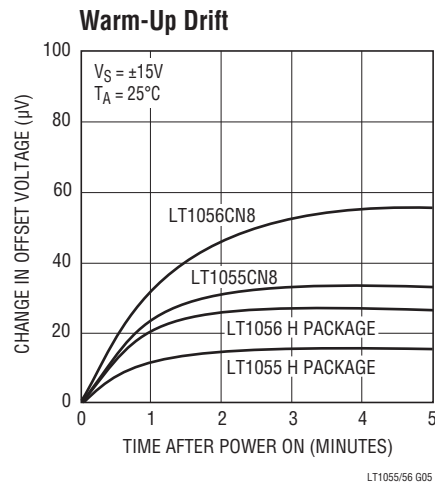
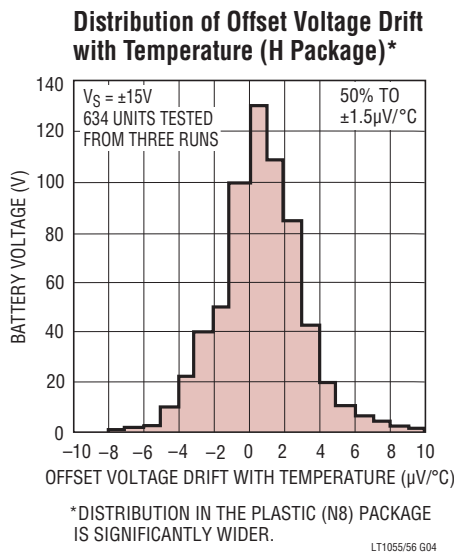
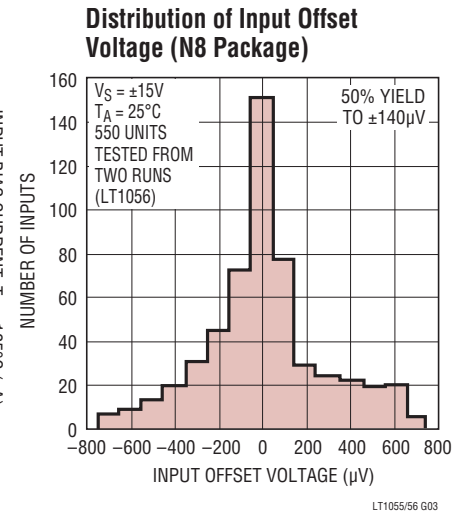
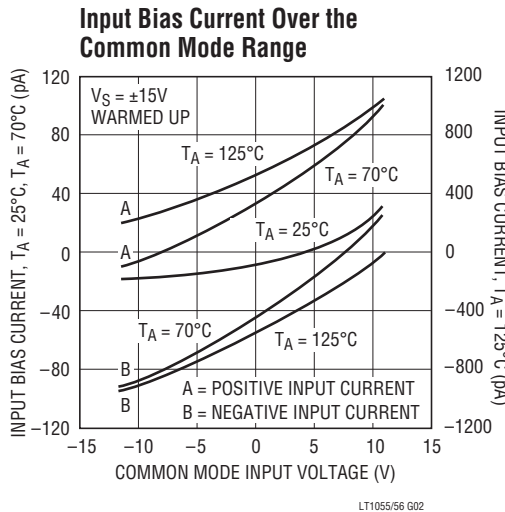
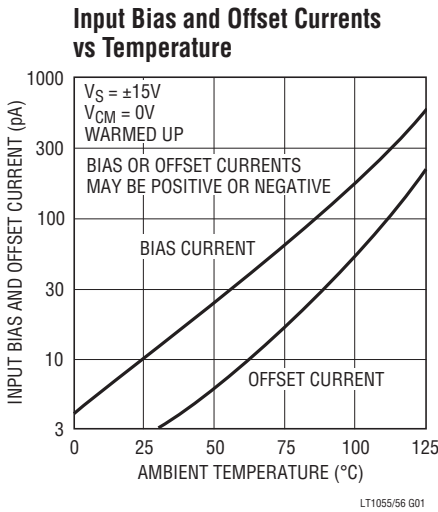
Note 3: 10Hz noise voltage density is sample tested on every lot of A grades. Devices 100% tested at 10Hz are available on request.

Note 4: This parameter is tested on a sample basis only.

Note 5: Current noise is calculated from the formula: $i_n = (2qI_B)^{1/2}$, where $q = 1.6 \cdot 10^{-19}$ coulomb. The noise of source resistors up to $1\text{G}\Omega$ swamps the contribution of current noise.

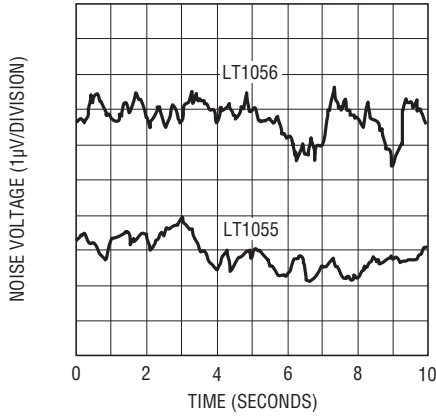
Note 6: Offset voltage drift with temperature is practically unchanged when the offset voltage is trimmed to zero with a 100k potentiometer between the balance terminals and the wiper tied to V^+ . Devices tested to tighter drift specifications are available on request.

TYPICAL PERFORMANCE CHARACTERISTICS



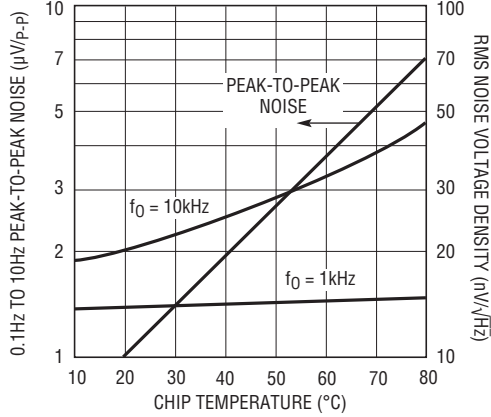
TYPICAL PERFORMANCE CHARACTERISTICS

0.1Hz to 10Hz Noise



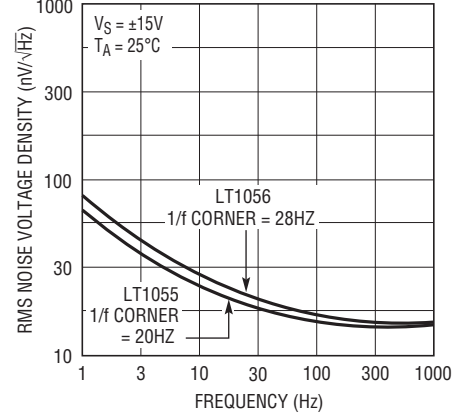
LT1055/56 G07

Noise vs Chip Temperature



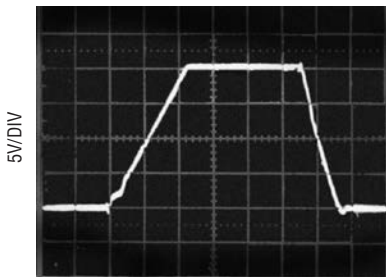
LT1055/56 G08

Voltage Noise vs Frequency



LT1055/56 G09

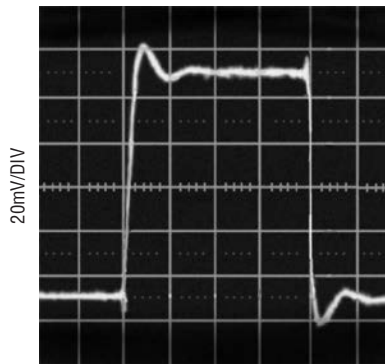
LT1056 Large-Signal Response



$A_V = 1, C_L = 100\text{pf}, 0.5\mu\text{s}/\text{DIV}$

LT1055/56 G10

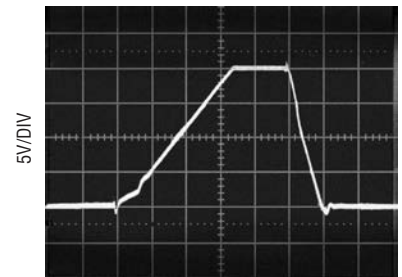
Small-Signal Response



$A_V = 1, C_L = 100\text{pf}, 0.2\mu\text{s}/\text{DIV}$

LT1055/56 G11

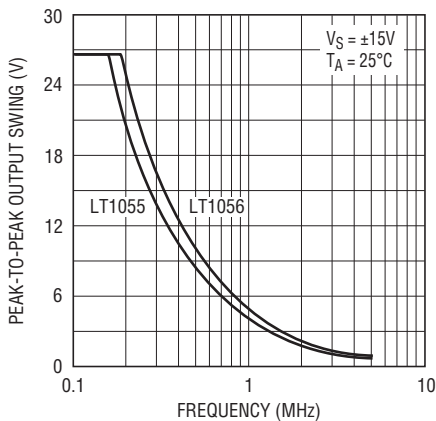
LT1055 Large-Signal Response



$A_V = 1, C_L = 100\text{pf}, 0.5\mu\text{s}/\text{DIV}$

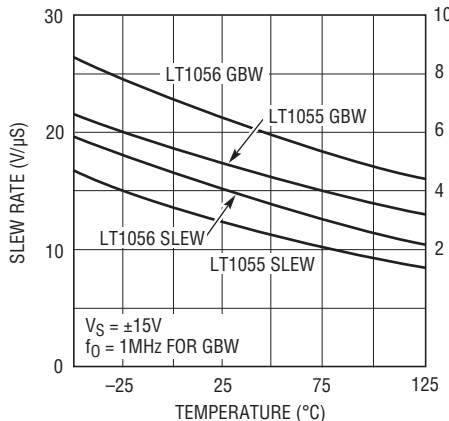
LT1055/56 G12

Undistorted Output Swing vs Frequency



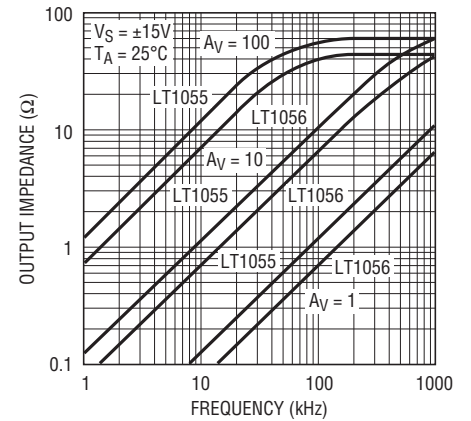
LT1055/56 G13

Slew Rate, Gain Bandwidth vs Temperature



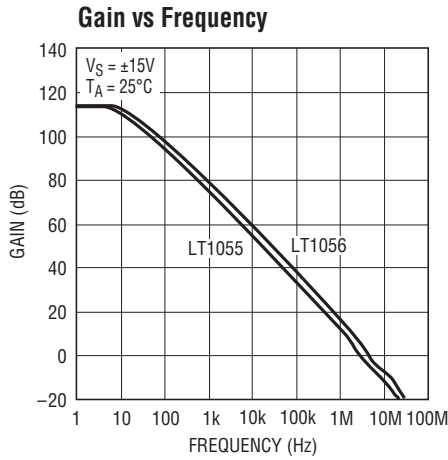
LT1055/56 G14

Output Impedance vs Frequency

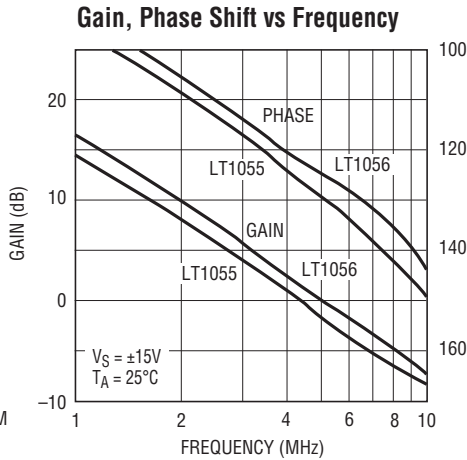


LT1055/56 G15

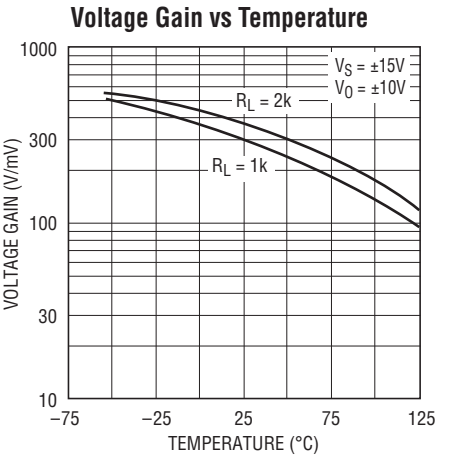
TYPICAL PERFORMANCE CHARACTERISTICS



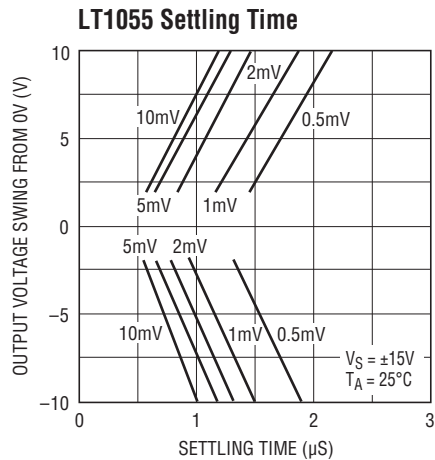
LT1055/56 G16



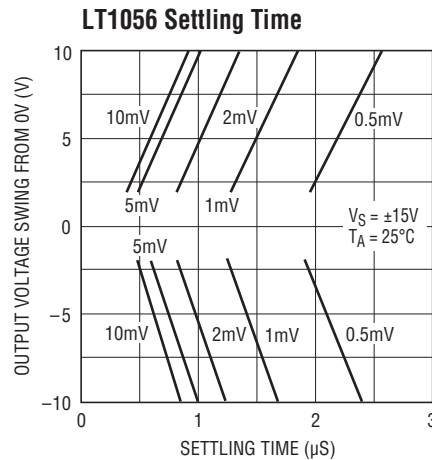
LT1055/56 G17



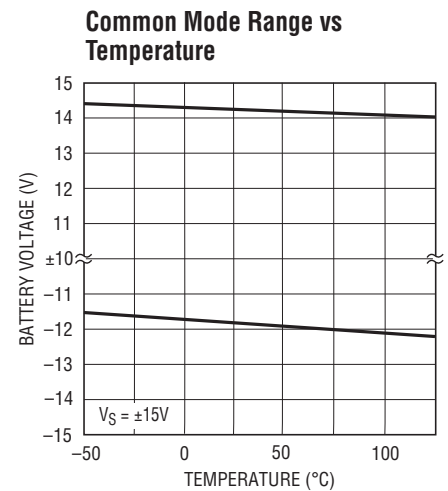
LT1055/56 G18



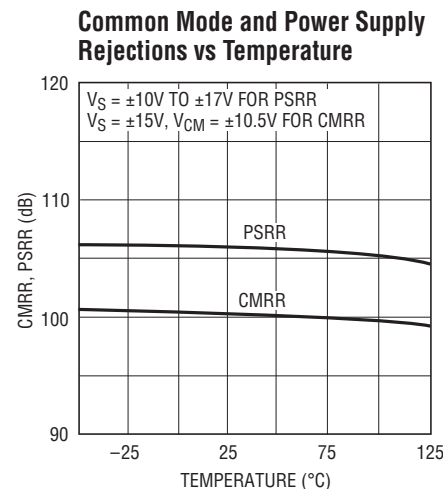
LT1055/56 G19



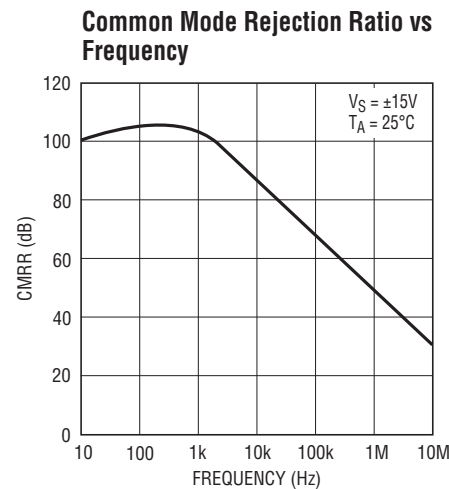
LT1055/56 G20



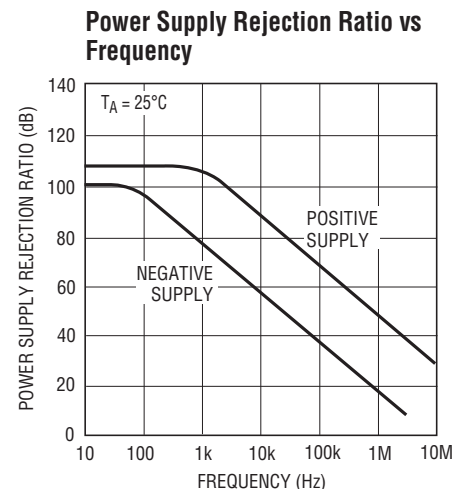
LT1055/56 G21



LT1055/56 G22

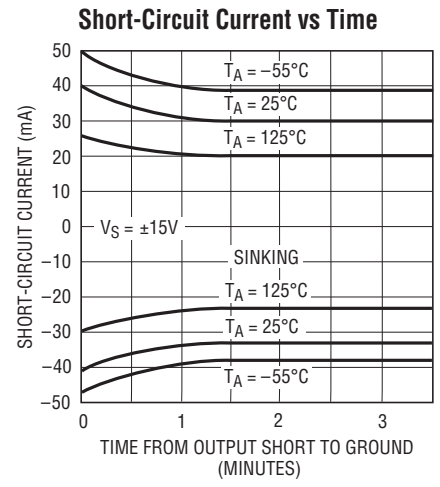
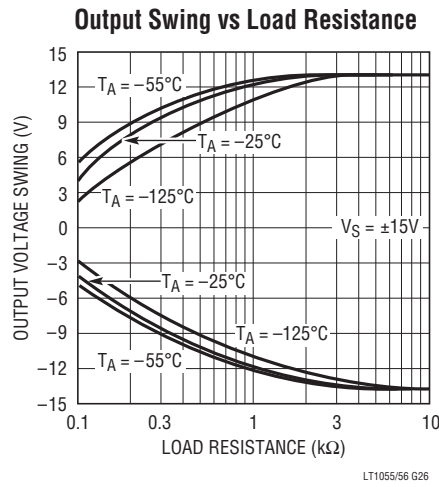
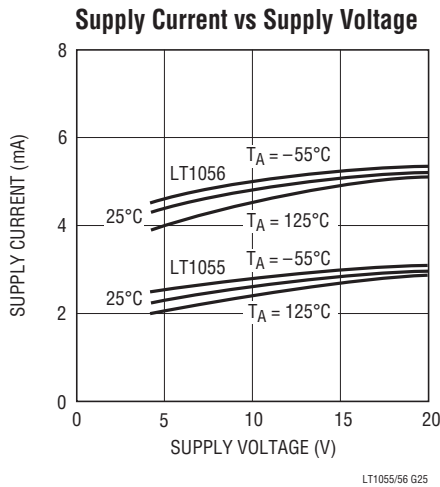


LT1055/56 G23



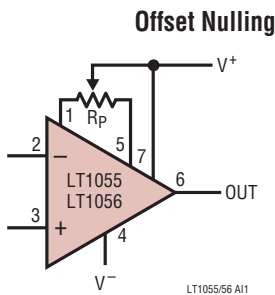
LT1055/56 G24

TYPICAL PERFORMANCE CHARACTERISTICS



APPLICATIONS INFORMATION

The LT1055/LT1056 may be inserted directly into LF155A/LT355A, LF156A/LT356A, OP-15 and OP-16 sockets. Offset nulling will be compatible with these devices with the wiper of the potentiometer tied to the positive supply.



No appreciable change in offset voltage drift with temperature will occur when the device is nulled with a potentiometer, R_P , ranging from 10k to 200k.

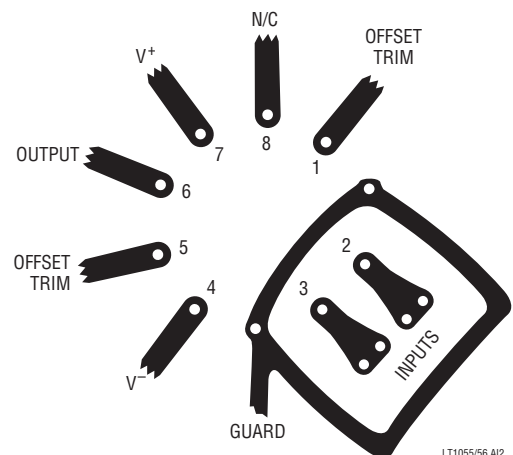
The LT1055/LT1056 can also be used in LF351, LF411, AD547, AD611, OPA-111, and TL081 sockets, provided that the nulling circuitry is removed. Because of the LT1055/LT1056's low offset voltage, nulling will not be necessary in most applications.

Achieving Picoampere/Microvolt Performance

In order to realize the picoampere-microvolt level accuracy of the LT1055/LT1056 proper care must be exercised. For

example, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation should be used (e.g. Teflon, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be required. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs: in inverting configurations the guard ring should be tied to ground, in noninverting connections to the inverting input at pin 2. Guarding both sides of the



APPLICATIONS INFORMATION

printed circuit board is required. Bulk leakage reduction depends on the guard ring width.

The LT1055/LT1056 has the lowest offset voltage of any JFET input op amp available today. However, the offset voltage and its drift with time and temperature are still not as good as on the best bipolar amplifiers because the transconductance of FETs is considerably lower than that of bipolar transistors. Conversely, this lower transconductance is the main cause of the significantly faster speed performance of FET input op amps.

Offset voltage also changes somewhat with temperature cycling. The AM grades show a typical $20\mu\text{V}$ hysteresis ($30\mu\text{V}$ on the M grades) when cycled over the -55°C to 125°C temperature range. Temperature cycling from 0°C to 70°C has a negligible (less than $10\mu\text{V}$) hysteresis effect.

The offset voltage and drift performance are also affected by packaging. In the plastic N8 package the molding compound is in direct contact with the chip, exerting pressure on the surface. While NPN input transistors are largely unaffected by this pressure, JFET device matching and drift are degraded. Consequently, for best DC performance, as shown in the typical performance distribution plots, the TO-5 H package is recommended.

Noise Performance

The current noise of the LT1055/LT1056 is practically immeasurable at $1.8\text{fA}/\sqrt{\text{Hz}}$. At 25°C it is negligible up to 1G of source resistance, R_S (compound to the noise of R_S). Even at 125°C it is negligible to 100M of R_S .

The voltage noise spectrum is characterized by a low $1/f$ corner in the 20Hz to 30Hz range, significantly lower than on other competitive JFET input op amps. Of particular interest is the fact that with any JFET IC amplifier, the frequency location of the $1/f$ corner is proportional to the square root of the internal gate leakage currents and, therefore, noise doubles every 20°C . Furthermore, as illustrated in the noise versus chip temperature curves, the 0.1Hz to 10Hz peak-to-peak noise is a strong function of temperature, while wideband noise ($f_0 = 1\text{kHz}$) is practically unaffected by temperature.

Consequently, for optimum low frequency noise, chip temperature should be minimized. For example, operat-

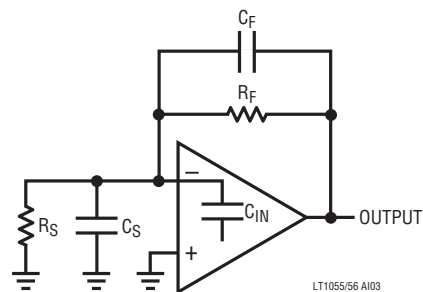
ing an LT1056 at $\pm 5\text{V}$ supplies or with a $20^\circ\text{C}/\text{W}$ case-to-ambient heat sink reduces 0.1Hz to 10Hz noise from typically $2.5\mu\text{V}_{\text{P-P}}$ ($\pm 15\text{V}$, free-air) to $1.5\mu\text{V}_{\text{P-P}}$. Similarly, the noise of an LT1055 will be $1.8\mu\text{V}_{\text{P-P}}$ typically because of its lower power dissipation and chip temperature.

High Speed Operation

Settling time is measured in the test circuit shown. This test configuration has two features which eliminate problems common to settling time measurements: (1) probe capacitance is isolated from the “false summing” node, and (2) it does not require a “flat top” input pulse since the input pulse is merely used to steer current through the diode bridges. For more details, please see Application Note 10.

As with most high speed amplifiers, care should be taken with supply decoupling, lead dress and component placement.

When the feedback around the op amp is resistive (R_F), a pole will be created with R_F , the source resistance and capacitance (R_S , C_S), and the amplifier input capacitance ($C_{\text{IN}} \approx 4\text{pF}$). In low closed-loop gain configurations and with R_S and R_F in the kilohm range, this pole can create excess phase shift and even oscillation. A small capacitor (C_F) in parallel with R_F eliminates this problem. With $R_S (C_S + C_{\text{IN}}) = R_F C_F$, the effect of the feedback pole is completely removed.



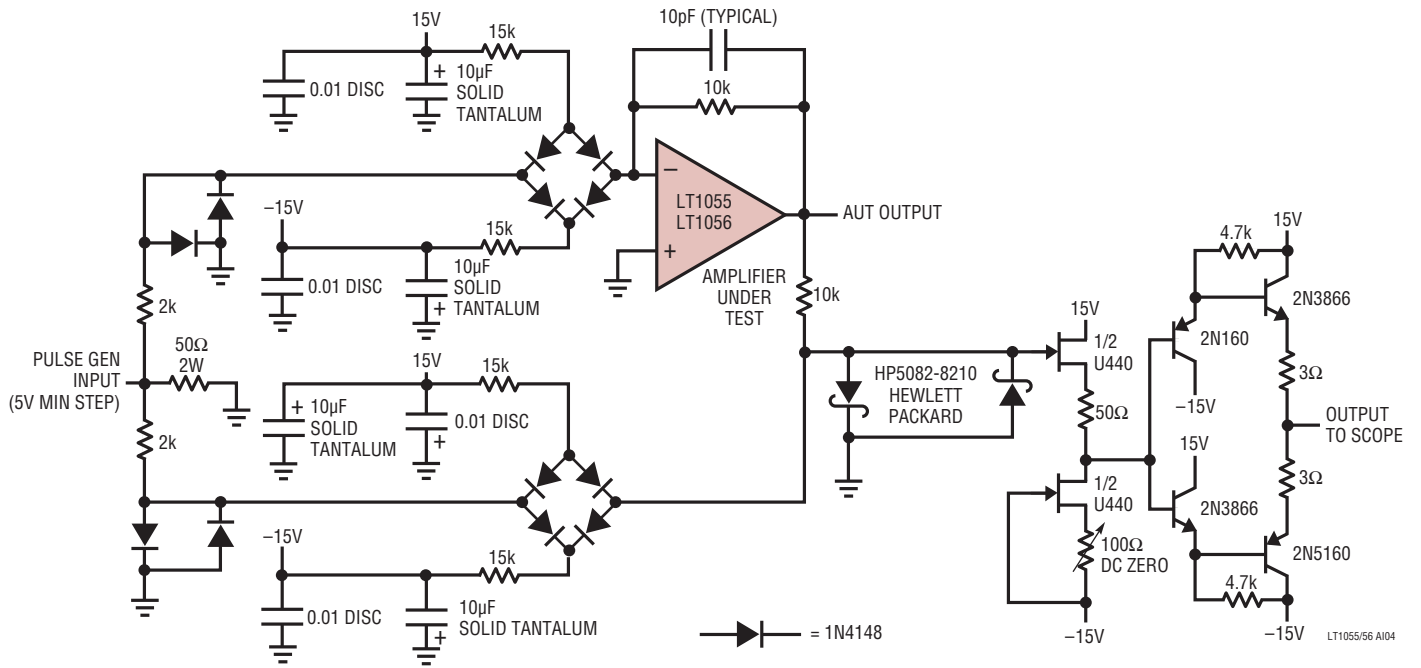
Phase Reversal Protection

Most industry standard JFET input op amps (e.g., LF155/LF156, LF351, LF411, OP15/16) exhibit phase reversal at the output when the negative common mode limit at the input is exceeded (i.e., from -12V to -15V with $\pm 15\text{V}$ supplies). This can cause lock-up in servo systems. As shown below, the LT1055/LT1056 does not have this problem due to unique phase reversal protection circuitry (Q1 on simplified schematic).

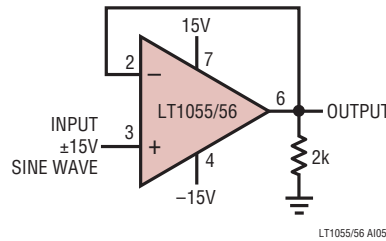
10556fd

APPLICATIONS INFORMATION

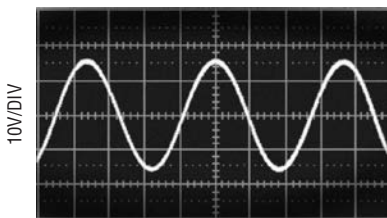
Settling Time Test Circuit



Voltage Follower with Input Exceeding the Negative Common Mode Range

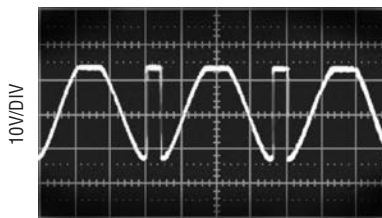


Input



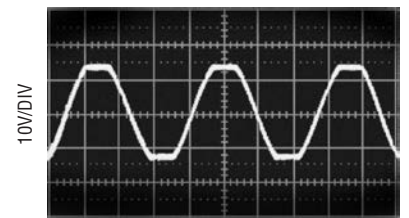
LT1055/56 A106

Output (LF155/LF56, LF441, OP-15/OP-16)



LT1055/56 A107

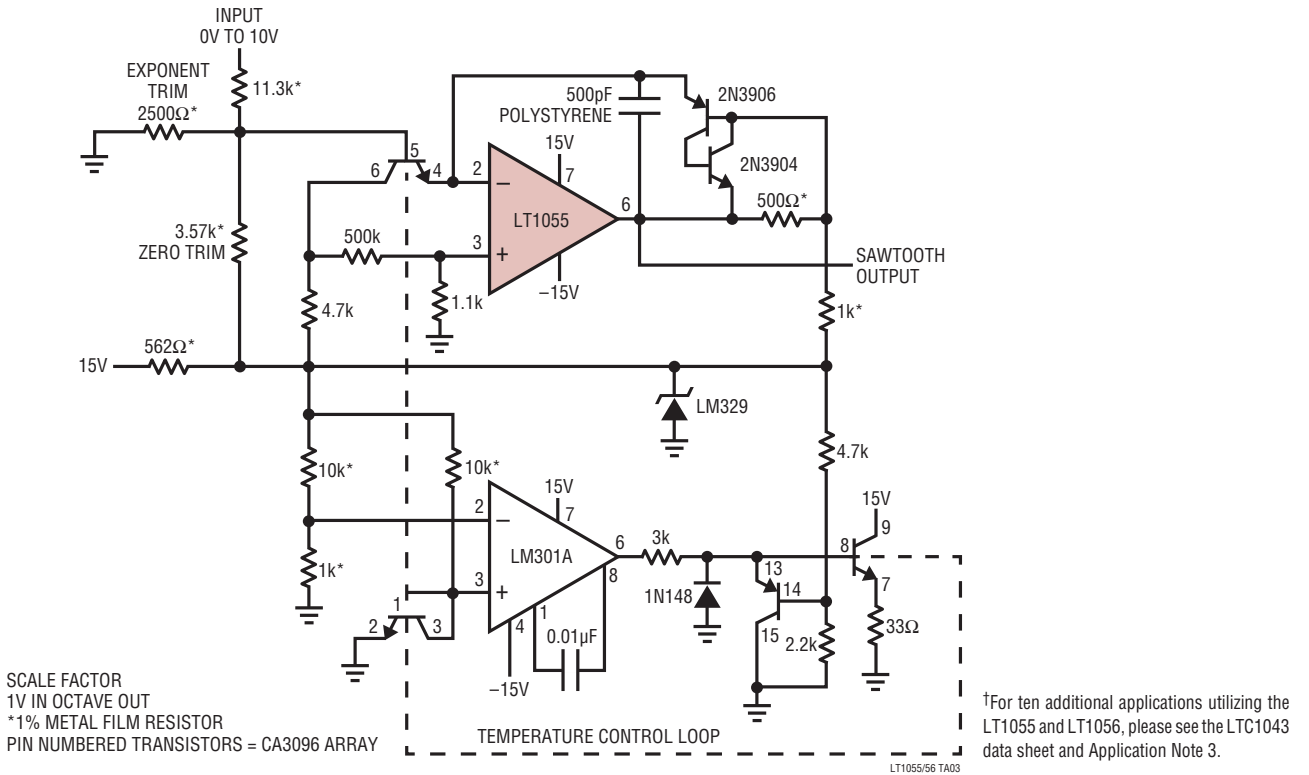
Output LT1055/LT1056



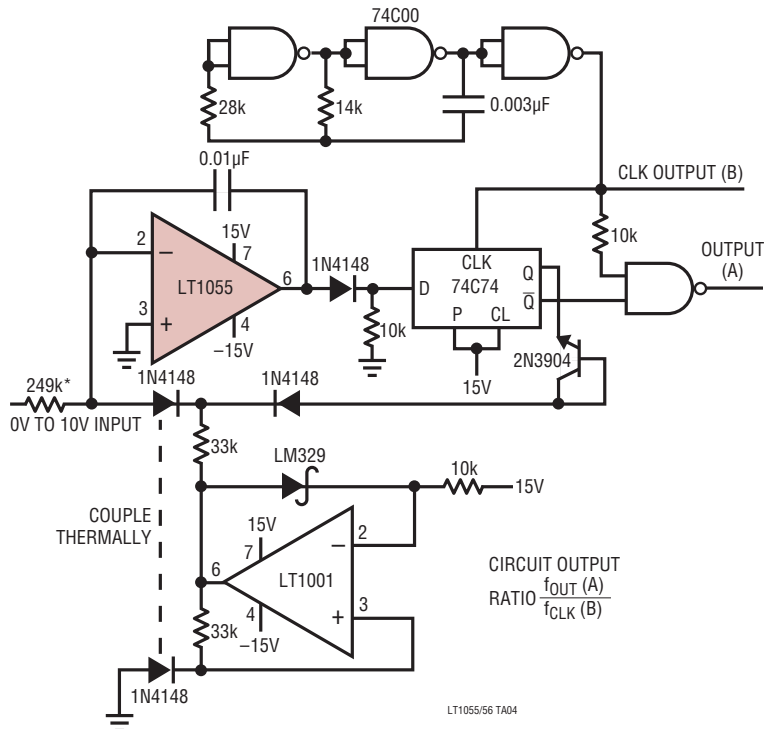
LT1055/56 A108

TYPICAL APPLICATIONS †

Exponential Voltage-to-Frequency Converter for Music Synthesizers

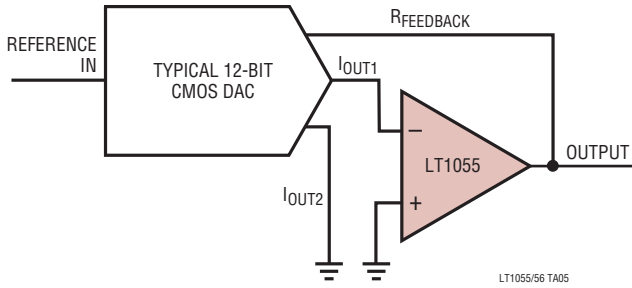


12-Bit Charge Balance A/D Converter



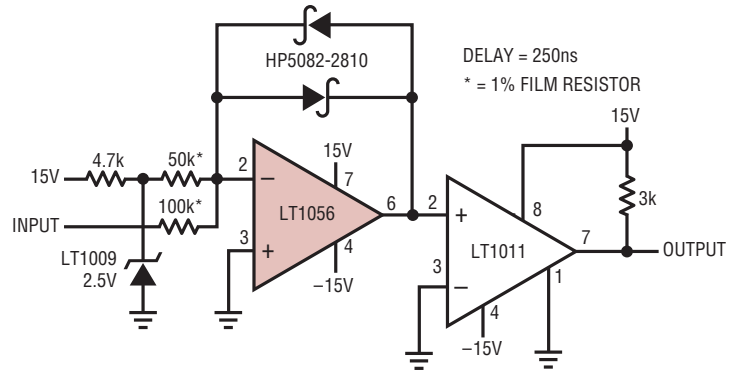
TYPICAL APPLICATIONS

Fast “No Trims” 12-Bit Multiplying CMOS DAC Amplifier



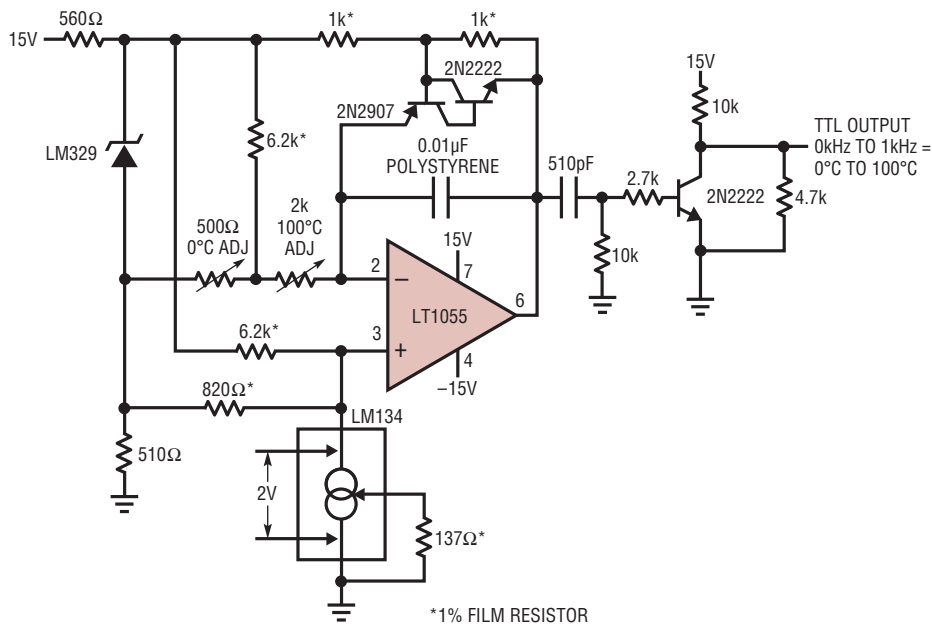
LT1055/56 TA05

Fast, 16-Bit Current Comparator



LT1055/56 TA06

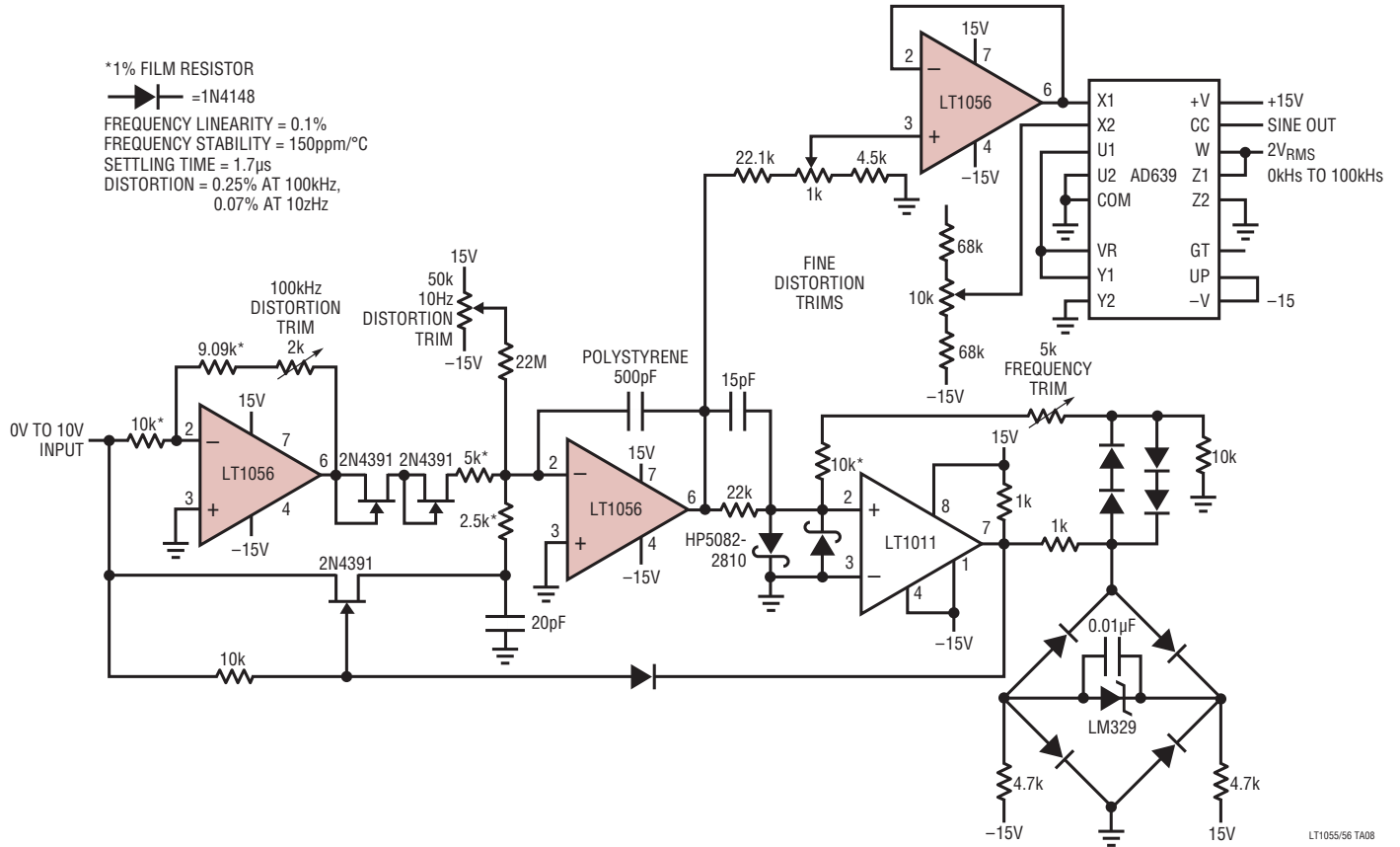
Temperature-to-Frequency Converter



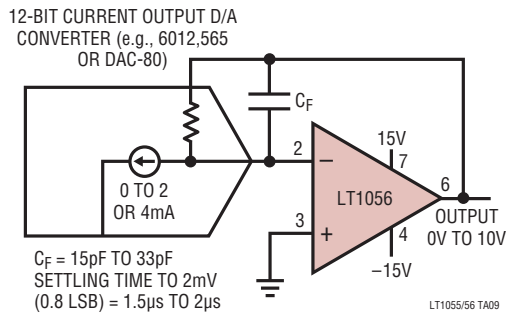
LT1055/56 TA07

TYPICAL APPLICATIONS

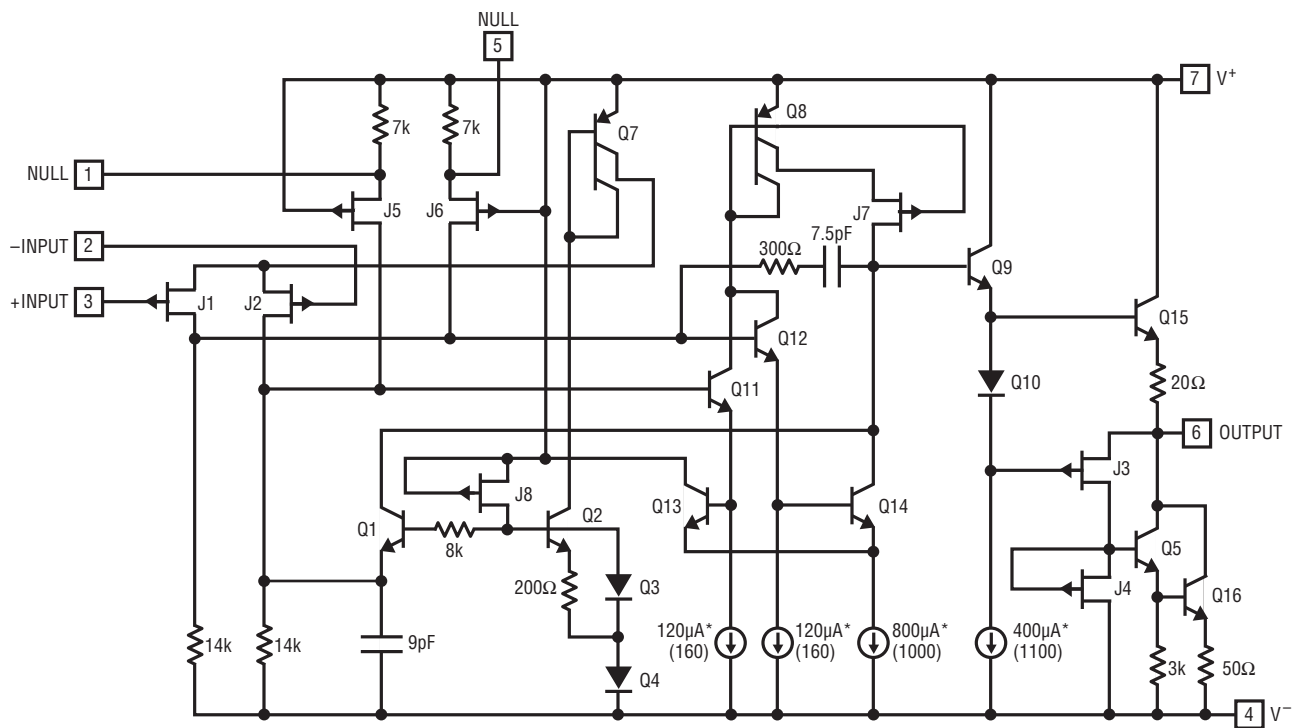
100kHz Voltage Controlled Oscillator



12-Bit Voltage Output D/A Converter



SIMPLIFIED SCHEMATIC



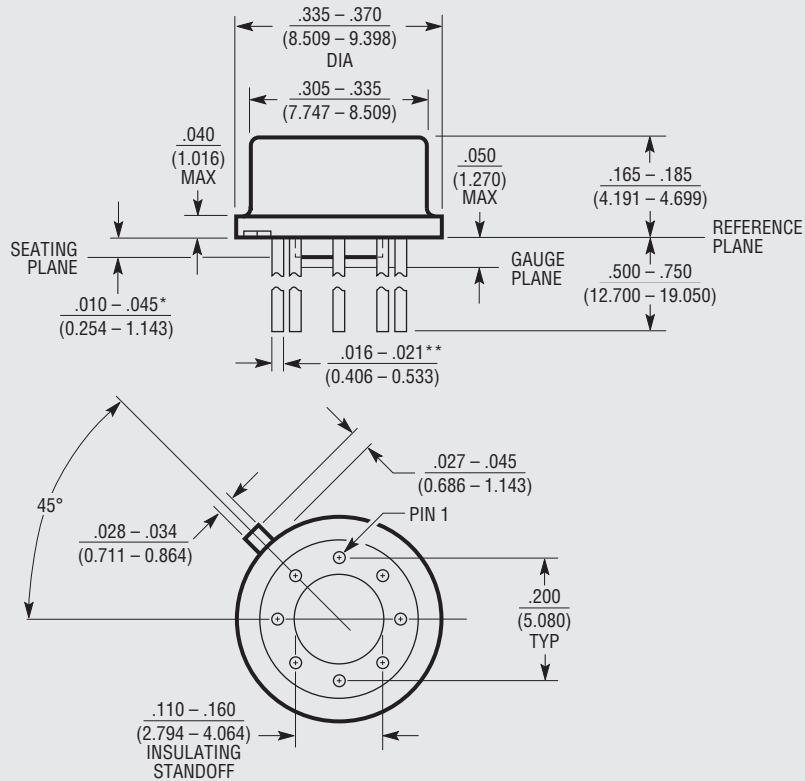
*CURRENTS AS SHOWN FOR LT1055. (X) = CURRENTS FOR LT1056.

LT1055/66 SCHM

PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

H Package
8-Lead TO-5 Metal Can (.200 Inch PCD)
 (Reference LTC DWG # 05-08-1320)



*LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND THE SEATING PLANE

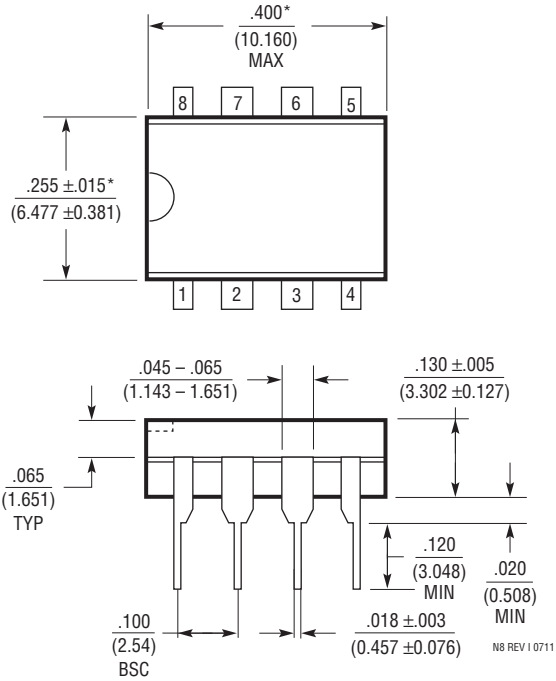
**FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS $\frac{.016 - .024}{(0.406 - 0.610)}$ H8(TO-5) 0.200 PCD 0204

OBsolete PACKAGE

PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

N Package 8-Lead PDIP (Narrow .300 Inch) (Reference LTC DWG # 05-08-1510 Rev I)

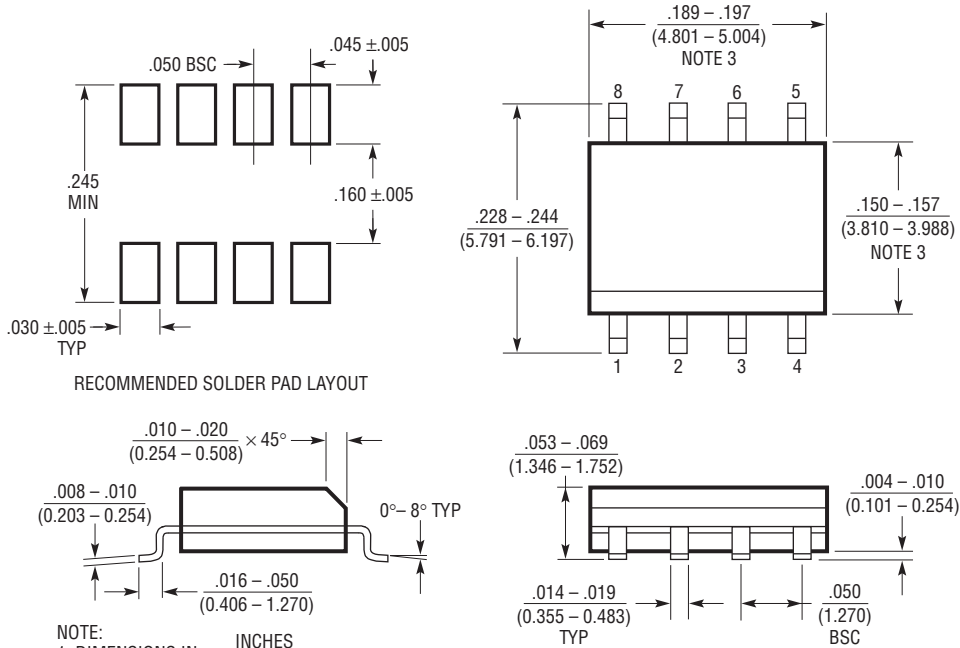


NOTE:
1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610 Rev G)



- NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
 2. DRAWING NOT TO SCALE
 3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED $.006''$ (0.15mm)
 4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

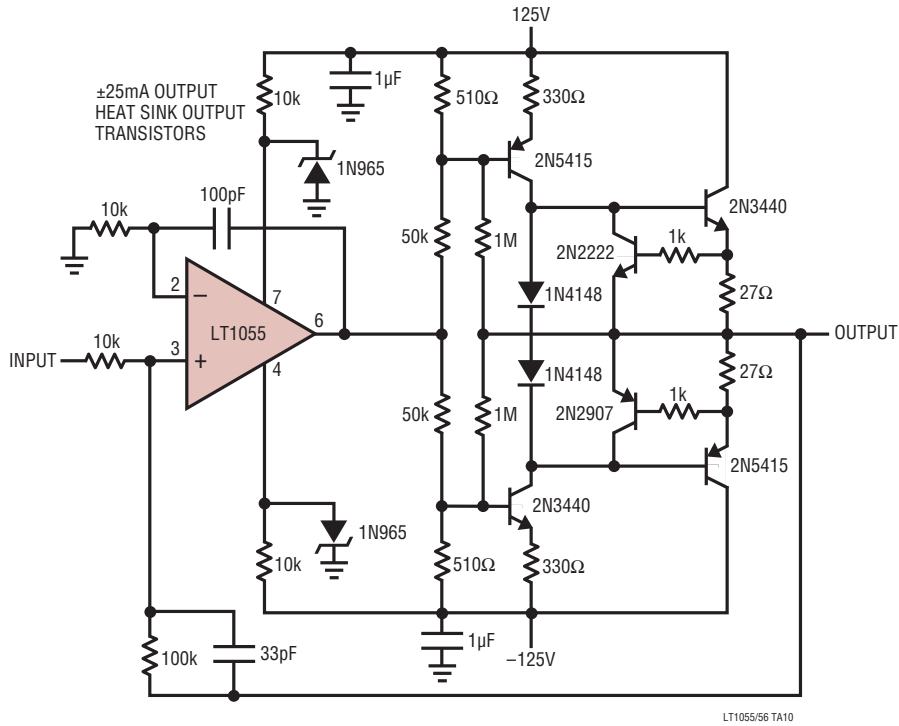
S08 REV G 0212

REVISION HISTORY (Revision history begins at Rev D)

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|-----|-------|--------------------------------|-------------|
| D | 08/15 | Corrected application circuit. | 20 |

TYPICAL APPLICATION

±120V Output Precision Op Amp



LT1055/56 TA10

RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|------------------------|---------------------------|---|
| LT1122 | Fast Settling JFET Op Amp | 340ns Settling Time, GBW = 14MHz, SR = 60V/μs |
| LT1792 | Low Noise JFET Op Amp | $e_n = 6nV/\sqrt{Hz}$ Max at $f = 1kHz$ |



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- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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