



# MOP-TFT800480-50A-BLM-TPN

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Hardware Manual

Revision 1.0

## Revision History

| Revision | Date         | Description     | Author |
|----------|--------------|-----------------|--------|
| 1.0      | May 26, 2017 | Initial Release | Divino |



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## 1 General Information

| No. | Item                           | Contents                                   | Unit |
|-----|--------------------------------|--|------|
| 1   | LCD size                       | 5.0 inch (Diagonal)                        | /    |
| 2   | LCD type                       | TN/Normally white/Transmissive(Anti-glare) | /    |
| 3   | Viewing direction(eye)         | 12 O'clock                                 | /    |
| 4   | Gray scale inversion direction | 6 O'clock                                  | /    |
| 5   | Resolution(H*V)                | 800 *480 Pixels                            | /    |
| 6   | Module size (L*W*H)            | 120.70*75.80*2.8                           | mm   |
| 7   | Active area (L*W)              | 108.00*64.80                               | mm   |
| 8   | Pixel pitch (L*W)              | 0.135*0.135                                | mm   |
| 9   | Interface type                 | RGB interface                              | /    |
| 10  | Module power consumption       | 1.297(with backlight)                      | W    |
| 11  | Back light type                | LED  | /    |
| 12  | Driver IC                      | ILI6122+ILI5960 OR COMPATIBLE              | /    |
| 13  | Weight                         | 56.1                                       | g    |

## 2 Absolute Maximum Ratings

| Item                                   | Symbol | Min. | Max.          | Unit |
|--|--------|------|---------------|------|
| Power supply input voltage(TFT Module) | VDD    | -0.3 | 5.0           | V    |
| Backlight current (normal temp.)       | ILED   | -    | 50            | mA   |
| Operation temperature                  | Top    | -20  | 70            | °C   |
| Storage temperature                    | Tst    | -30  | 80            | °C   |
| Humidity                               | RH     | -    | 90%(Max60 °C) | RH   |

## 3 Electrical Characteristics

### DC Characteristics (at Ta=25 °C)

| Item                                   | Symbol | Min.    | Typ.  | Max.    | Unit |
|--|--------|---------|-------|---------|------|
| Power supply input voltage(TFT Module) | VDD    | 3.0     | 3.3   | 3.6     | V    |
| I/O logic voltage                      | VDDIO  | N/A     | N/A   | N/A     | V    |
| Input voltage 'H' level                | VIH    | 0.7VDDI | -     | VDDI    | V    |
| Input voltage 'L' level                | VIL    | VSS     | -     | 0.3VDDI | V    |
| Power supply current                   | IVDD   | -       | 131.6 | -       | mA   |
| TFT gate on voltage                    | VGH    | -       | N/A   | -       | V    |
| TFT gate off voltage                   | VGL    | -       | N/A   | -       | V    |
| Analog power supply voltage            | AVDD   | -       | N/A   | -       | V    |
| Differential input common mode voltage | Vcom   | -       | N/A   | -       | V    |

## 4 Backlight Characteristics

(at Ta=25 °C, RH=60%)

| Item                  | Symbol | Min.                       | Typ.  | Max. | Unit | Note      |
|-----------------------|--------|----------------------------|-------|------|------|-----------|
| LED forward voltage   | VF     | -                          | 18.6  | 19.8 | V    | IF=20*2mA |
| LED forward current   | IF     | -                          | 40    | -    | mA   |           |
| LED power consumption | PLED   | -                          | 0.744 | -    | W    | Note1     |
| Number of LED         | -      | -                          | 12    | -    | PCS  |           |
| Connection mode       | -      | 6 in series, 2 in parallel |       |      | /    |           |
| LED life-time         | -      | 20000                      | -     | -    | Hrs  | Note2     |

**\*Note:** Calculate Value for reference  $IF \times VF = PLED$

**\*\*Note:** The LED Life-time is defined as the estimated time to 50% degradation of initial brightness at Ta=25°C and IF =40mA. The LED lifetime could be decreased if operating IF is larger than 40mA, and increased if IF is less than 40mA.



# 5 External Dimensions

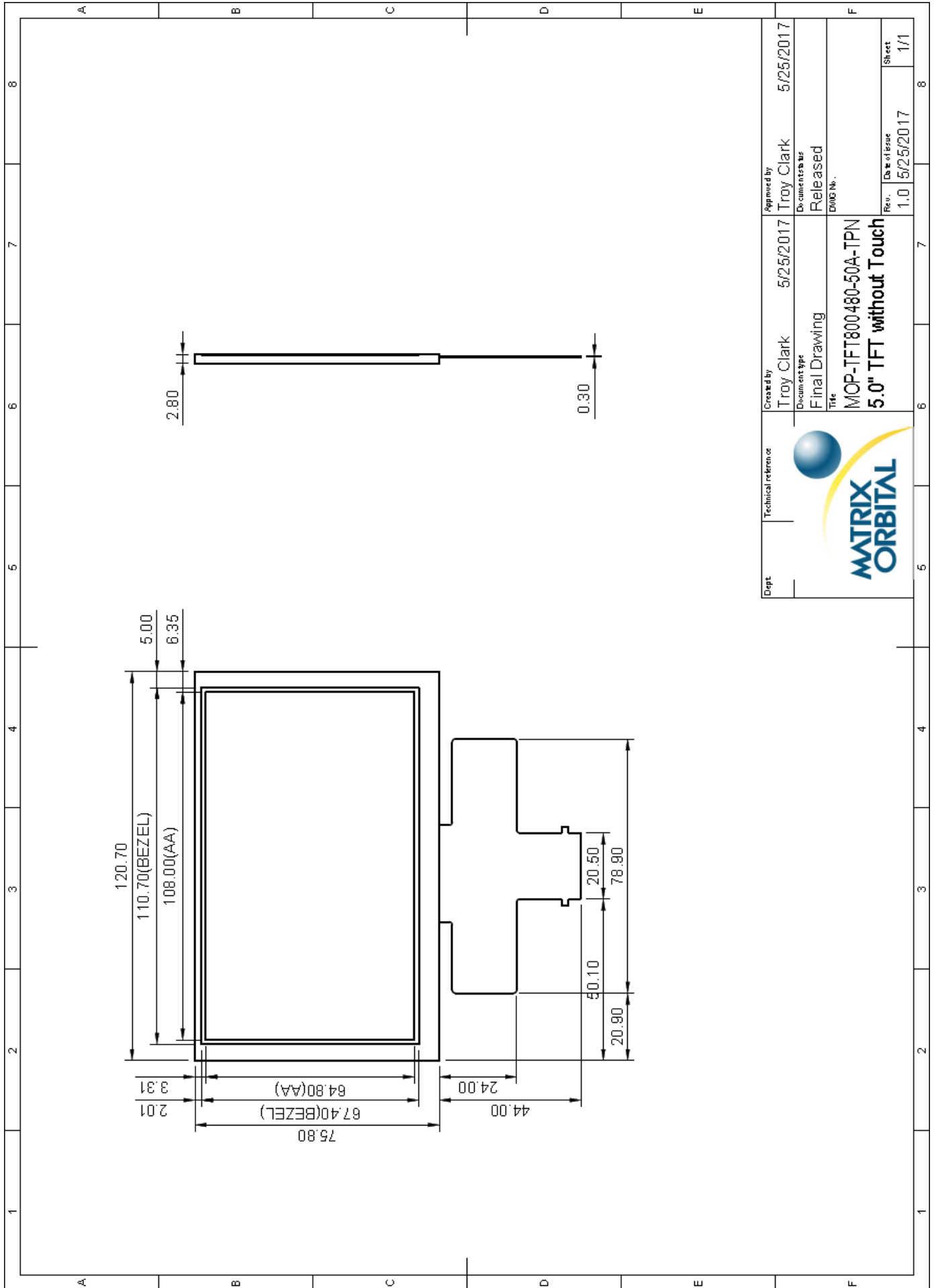


Figure 1: MOP-TFT800480-50A-BLM-TPN Drawing



## 6 Electro-Optical Characteristics

| Item                   | Symbol   | Condition  | Min.   | Typ.   | Max.   | Unit              | Remark           | Note   |
|------------------------|----------|--|--------|--------|--------|-------------------|------------------|--------|
| Response time          | Tr+ Tf   | -  | -      | 25     | 50     | ms                | FIG.1            | Note 4 |
| Contrast ratio         | Cr       |  | 400    | 500    | -      | -                 | FIG.2            | Note 1 |
| Surface luminance      | Lv       | $\theta=0^\circ$                                     | 380    | 480    | -      | cd/m <sup>2</sup> | FIG.2            | Note 2 |
| Luminance uniformity   | Yu       | $\theta=0^\circ$                                     | 75     | 80     | -      | %                 | FIG.2            | Note 3 |
| NTSC                   | -        | $\theta=0^\circ$                                     | -      | 50     | -      | %                 | FIG.2            | Note 5 |
| Viewing angle          | $\theta$ | $\varnothing=90^\circ$                               | 60     | 70     | -      | deg               | FIG.3            | Note 6 |
|                        |          | $\varnothing=270^\circ$                              | 40     | 50     | -      | deg               | FIG.3            |        |
|                        |          | $\varnothing=0^\circ$                                | 60     | 70     | -      | deg               | FIG.3            |        |
|                        |          | $\varnothing=180^\circ$                              | 60     | 70     | -      | deg               | FIG.3            |        |
| CIE (x,y) chromaticity | Red x    | $\theta=0^\circ$<br>$\varnothing=0^\circ$<br>Ta=25°C | 0.5212 | 0.5612 | 0.6012 | -                 | FIG.2<br>CIE1931 | Note 5 |
|                        | Red y    |  | 0.2959 | 0.3359 | 0.3759 | -                 |                  |        |
|                        | Green x  |  | 0.3055 | 0.3455 | 0.3855 | -                 |                  |        |
|                        | Green y  |  | 0.5450 | 0.5850 | 0.6250 | -                 |                  |        |
|                        | Blue x   |  | 0.1090 | 0.1490 | 0.1890 | -                 |                  |        |
|                        | Blue y   |  | 0.4833 | 0.5233 | 0.5633 | -                 |                  |        |
|                        | White x  |  | 0.2730 | 0.3130 | 0.3530 | -                 |                  |        |
|                        | White y  |  | 0.2969 | 0.3369 | 0.3769 | -                 |                  |        |

**\*Note 1:** Definition of contrast ratio

Contrast Ratio (CR) is defined mathematically by the following formula.

$$\text{CONTRAST RATIO} = \frac{\text{Luminance measured when LCD on the "White" State}}{\text{Luminance measured when LCD on the "Black" State}}$$

Measured at the center area of the LCD

**\*Note 2:** Definition of surface luminance

Surface luminance is the LCD luminance from the surface with all pixels displaying white.

$$L_v = \text{Average Surface Luminance with all white pixels (P1, P2, P3 ... Pn)}$$

**\*Note 3:** Definition of luminance uniformity

The luminance uniformity in surface luminance (Yu) is determined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n point's luminance by minimum luminance of n points luminance.

$$Y_u = \frac{\text{Minimum Surface Luminance with all white pixels (P1, P2, P3 ... Pn)}}{\text{Maximum Surface Luminance with all white pixels (P1, P2, P3 ... Pn)}}$$

**\*Note 4:** Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.

**\*Note 5:** Definition of color chromaticity (CIE1931)

CIE (x, y) chromaticity, the x, y value is determined by screen active area center position P5.

**\*Note 6:** Definition of Viewing angle.

Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface.

For Viewing angle and response time testing, the testing data is based on Autronic-Melchers's ConoScope or DMS series Instruments or compatible. For contrast ratio, Surface Luminance, Luminance uniformity and CIE, the testing data is based on TOPCON's BM-7 or BM-5 photo detector or compatible.

**\*Note 7:** For TFT module, Gray scale reverse occurs in the direction of panel viewing angle.



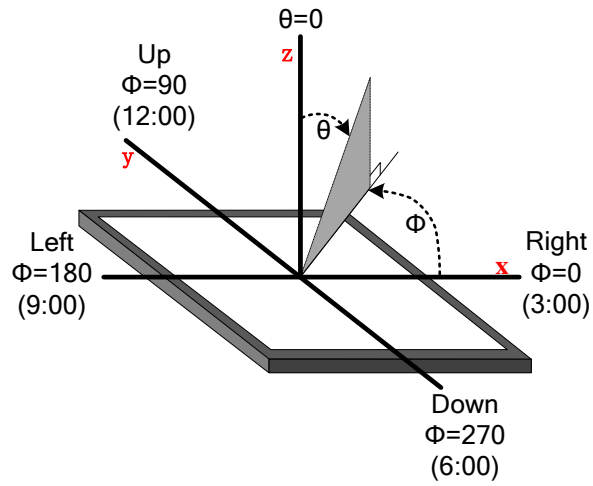


Figure 2: The definition of viewing angle

## 7 Interface Description

### 7.1 TFT Module Interface Description

| Interface No. | Name       | I/O or connect to | Description                      |
|---------------|------------|-------------------|----------------------------------|
| 1             | LEDK       | P                 | Power for LED backlight(Cathode) |
| 2             | LEDA       | P                 | Power for LED backlight(Anode)   |
| 3             | CS(NC)     | /                 | No connection                    |
| 4             | VDD        | P                 | Power for LCD                    |
| 5-12          | Red(0-7)   | I                 | Red data signal                  |
| 13-20         | Green(0-7) | I                 | Green data signal                |
| 21-28         | Blue(0-7)  | I                 | Blue data signal                 |
| 29            | GND        | I                 | Ground                           |
| 30            | DCLK       | I                 | Dot clock signal                 |
| 31            | DISP       | I                 | Display on/off                   |
| 32            | HSYNC      | I                 | Horizontal sync input.           |
| 33            | VSYNC      | I                 | Vertical sync input              |
| 34            | DE         | I                 | Data enable                      |
| 35            | SCL(NC)    | /                 | No connection                    |
| 36            | SDA(NC)    | /                 | No connection                    |
| 37            | XR(NC)     | /                 | No connection                    |
| 38            | YD(NC)     | /                 | No connection                    |
| 39            | XL(NC)     | /                 | No connection                    |
| 40            | YU(NC)     | /                 | No connection                    |

# 8 AC Characteristics

## 8.1 Pixel Timing

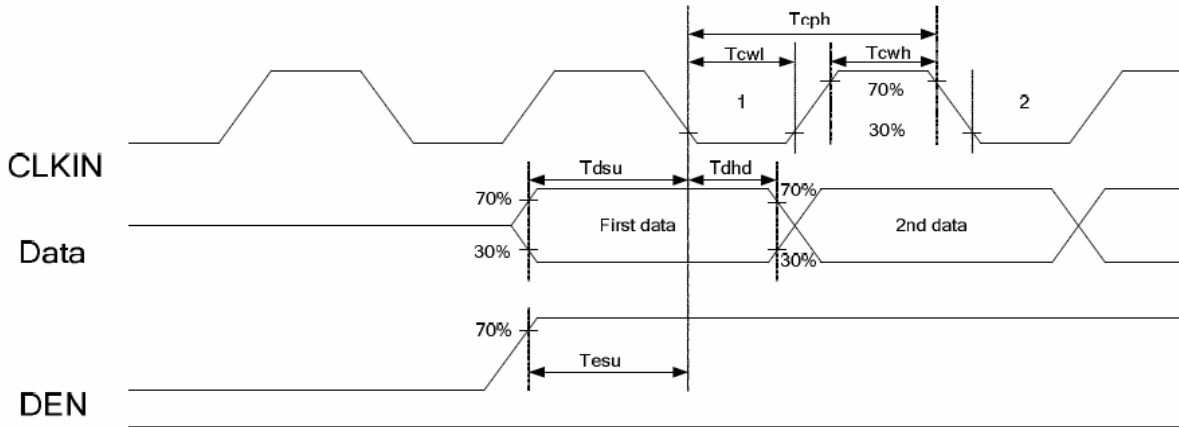


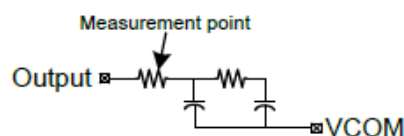
Figure 3: Pixel Timing

| Parameter                      | Symbol     | Spec. |      |      | Unit    | Conditions   |
|--------------------------------|------------|-------|------|------|---------|--|
|                                |            | Min.  | Typ. | Max. |         |  |
| VDD Power ON slew rate         | $t_{POR}$  | -     | -    | 20   | ms      | $0v \sim 0.9V_{DD}$                                    |
| RSTB pulse width               | $t_{RST}$  | 10    | -    | -    | $\mu s$ | $CLKIN = 50MHz$  |
| CLKIN cycle time               | $t_{CPH}$  | 20    | -    | -    | ns      |  |
| CLKIN pulse duty               | $t_{CWH}$  | 40    | 50   | 60   | %       |  |
| VSD setup time                 | $t_{VST}$  | 8     | -    | -    | ns      |  |
| VSD hold time                  | $t_{VHD}$  | 8     | -    | -    | ns      |  |
| HSD setup time                 | $t_{HST}$  | 8     | -    | -    | ns      |  |
| HSD hold time                  | $t_{HHD}$  | 8     | -    | -    | ns      |  |
| Data setup time                | $t_{DST}$  | 8     | -    | -    | ns      | D0[7:0], D1[7:0], D2[7:0] to CLKIN                     |
| Data hold time                 | $t_{DHD}$  | 8     | -    | -    | ns      | D0[7:0], D1[7:0], D2[7:0] to CLKIN                     |
| DE setup time                  | $t_{EST}$  | 8     | -    | -    | ns      |  |
| DE hold time                   | $t_{EHD}$  | 8     | -    | -    | ns      |  |
| Output stable time             | $t_{SST}$  | -     | -    | 6    | $\mu s$ | 10% to 90% target voltage.<br>CL=120pf, R=10k $\Omega$ |
| CLKIN frequency                | $f_{CLK}$  | -     | 40   | 50   | MHz     | $V_{DD}=3.0\sim 3.6V$                                  |
| CLKIN cycle time               | $t_{CLK}$  | 20    | 25   | -    | ns      |  |
| CLKIN pulse duty               | $t_{CWH}$  | 40    | 50   | 60   | %       | $T_{CLK}$  |
| Time from HSD to source output | $t_{HSO}$  | -     | 20   | -    | CLKIN   |  |
| Time from HSD to LD            | $t_{HLD}$  | -     | 20   | -    | CLKIN   | **Note   |
| Time from HSD to STV           | $t_{HSTV}$ | -     | 2    | -    | CLKIN   |  |
| Time from HSD to CKV           | $t_{HCKV}$ | -     | 20   | -    | CLKIN   |  |
| Time from HSD to OEV           | $t_{HOEV}$ | -     | 4    | -    | CLKIN   |  |
| LD pulse width                 | $t_{WLD}$  | -     | 10   | -    | CLKIN   | **Note   |
| CKV pulse width                | $t_{WCKV}$ | -     | 66   | -    | CLKIN   |  |
| OEV pulse width                | $t_{WOEV}$ | -     | 74   | -    | CLKIN   |  |

**\*Note:**  $V_{DD}=3.0\sim 3.6V$ ,  $V_{DDA}=6.5\sim 13.5V$ ,  $DGND=AGND=0V$ ,  $T_a=-20\sim +85^\circ C$

**\*\*Note:** The contents of the data register are transferred to the latch circuit at the rising edge of LD. Then the gray scale voltage is output from the device at the falling edge of LD

**\*\*\*Note:** Output loading condition:





## 8.2 Data Timing

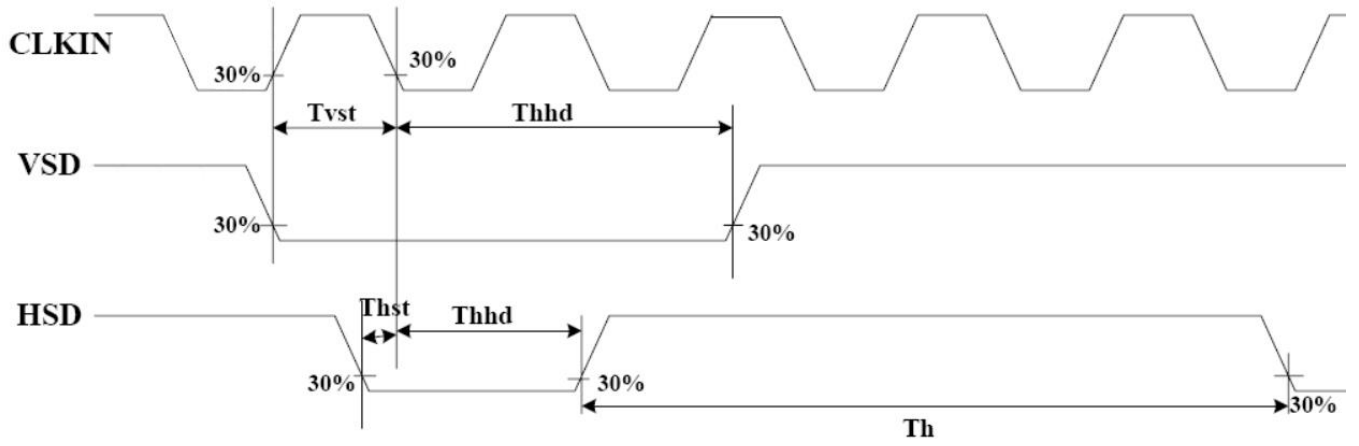


Figure 4: Data Transaction Timing in Parallel RGB (24Bit) interface (SYNC Mode)

| Horizontal Input Timing  |           |           |      |      |       |       |
|--------------------------|-----------|-----------|------|------|-------|-------|
| Parameter                | Symbol    | Value     |      |      | Unit  |       |
|                          |           | Min.      | Typ. | Max. |       |       |
| Horizontal display area  | $t_{HD}$  | -         | 800  | -    | CLKIN |       |
| CLKIN frequency          | $f_{CLK}$ | -         | 33.3 | 50   | MHz   |       |
| 1 Horizontal line period | $t_H$     | 862       | 1056 | 1200 | CLKIN |       |
| HSD Pulse Width          | Min.      | -         | 1    | -    | CLKIN |       |
|                          | Typ.      | -         | -    | -    | CLKIN |       |
|                          | Max.      | -         | 40   | -    | CLKIN |       |
| HSD back porch           | SYNC      | $t_{HBP}$ | 46   | 46   | 46    | CLKIN |
| HSD front porch          | SYNC      | $t_{HFP}$ | 16   | 210  | 354   | CLKIN |

| Vertical Input Timing |           |       |      |      |      |
|-----------------------|-----------|-------|------|------|------|
| Parameter             | Symbol    | Value |      |      | Unit |
|                       |           | Min.  | Typ. | Max. |      |
| Vertical display area | $t_{VD}$  | -     | 480  | -    | HSD  |
| VSD period time       | $t_V$     | 510   | 525  | 650  | HSD  |
| VSD pulse width       | $t_{VPW}$ | 1     | -    | 20   | HSD  |
| VSD back porch        | $t_{VBP}$ | 23    | 23   | 23   | HSD  |
| VSD front porch       | $t_{VFP}$ | 7     | 22   | 147  | HSD  |

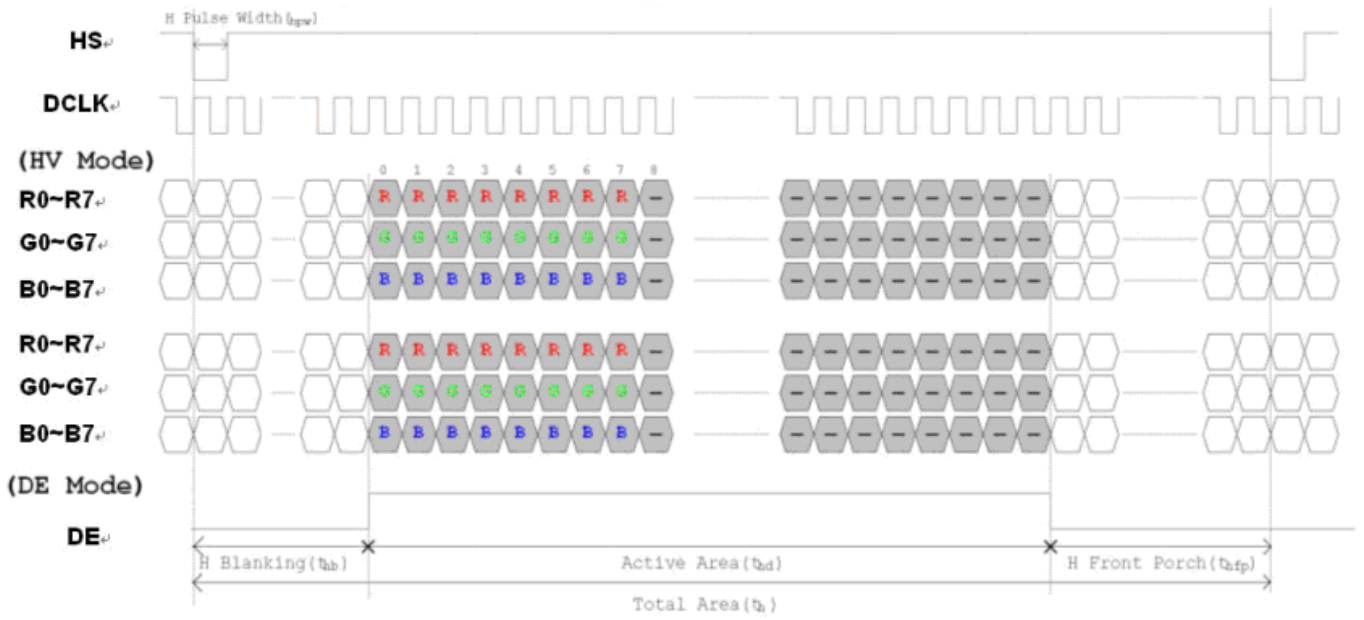


Figure 5: Horizontal Input Timing Diagram

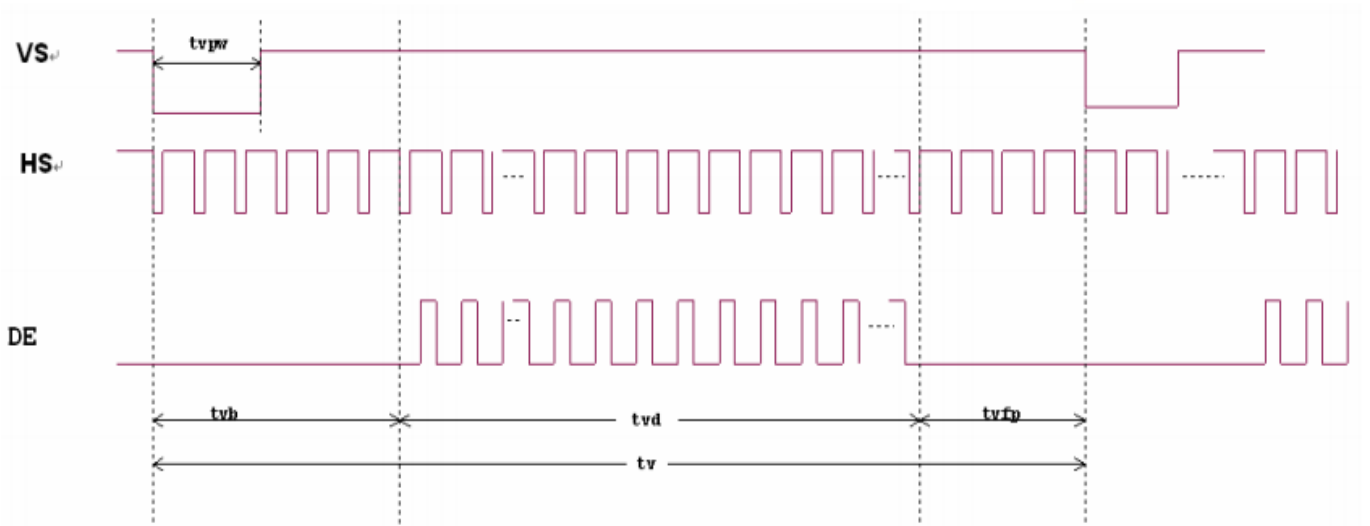


Figure 6: Vertical Input Timing Diagram



# 9 Power Sequence

## 9.1 Power Up Sequence

To prevent the device damage from latch up, the power ON/OFF sequence shown below must be followed.

Power On: VDD, DGND → VDDA, AGND, → V1 to V14

Power OFF: V1 to V14 → VDDA, AGND → VDD, DGND

In order to prevent ILI6122 from power ON reset fail, the rising time ( $t_{POR}$ ) of the digital power supply VDD should be maintained within given specifications. The power ON/OFF timing sequence is illustrated as below:

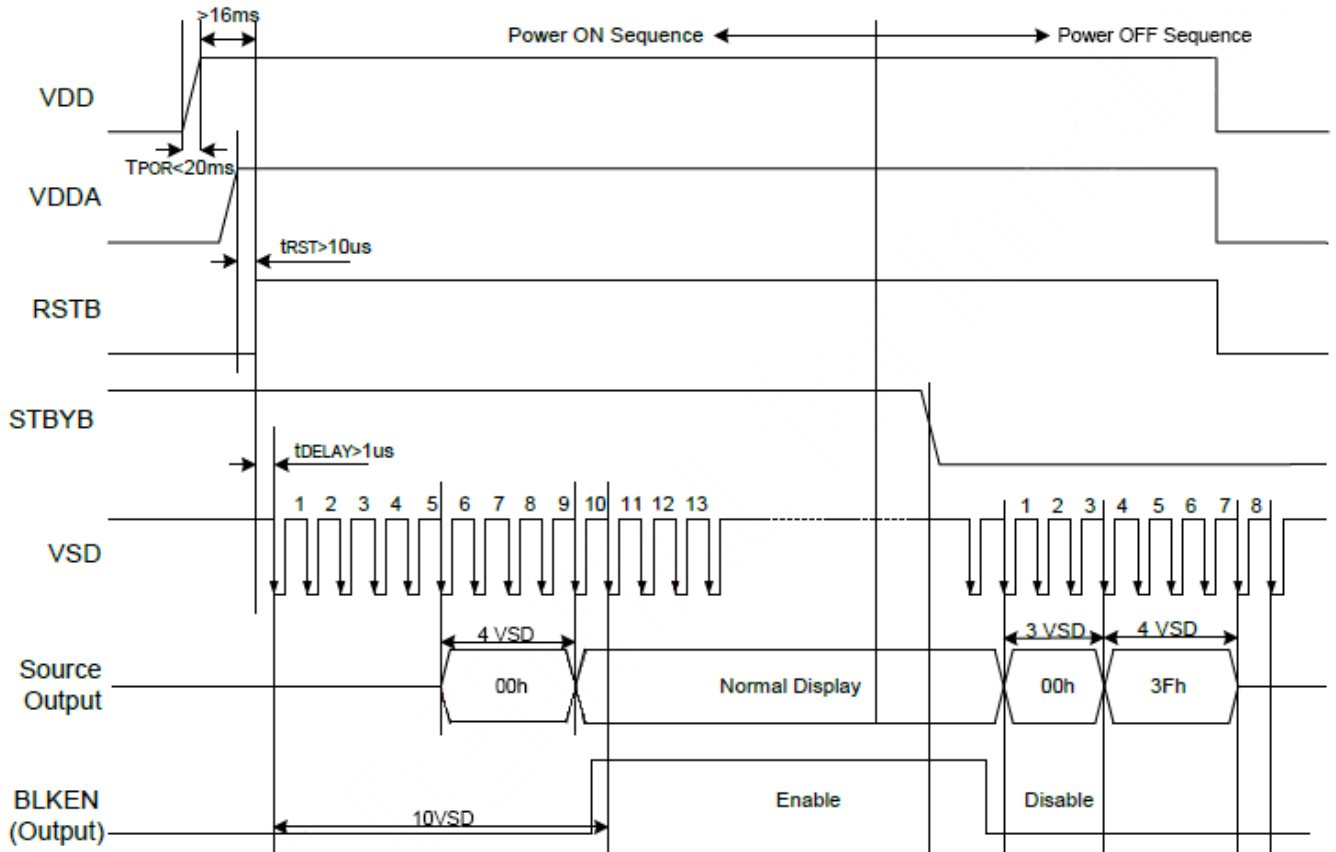


Figure 7: Power up sequence timing diagram

**\*Note:** To prevent abnormal operations,  $t_{RST}$  must be longer than 10 $\mu s$  during the Power ON sequence.

# 10 Inspection Criterion

## 10.1 Description

This specification is made to be used as the standard acceptance/rejection criteria for the MOP-TFT800480-50A-BLM-TPN.

## 10.2 Sampling Plan and Reference Standards

Sampling plan :

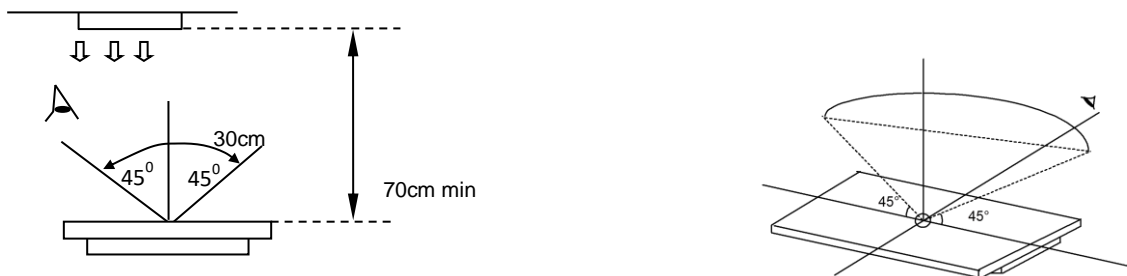
Refer to National Standard GB/T 2828.1---2012/ISO2859-1:1999, level II of normal levels:

Major defect: AQL 0.4

Minor defect: AQL 1.0

## 10.3 Inspection condition

- Cosmetic inspection: shall be done normally at  $23\pm 5^{\circ}\text{C}$  of the ambient temperature and 45~75%RH of relative humidity, under the ambient luminance between 500lux~1000lux and at the distance of 30cm apart between the inspector's eyes and the LCD panel and normally in reflected light. For backlight LCM, cosmetic inspection shall be done under the ambient luminance less than 100lux with the backlight on.
- The TFT shall be tested at the angle of  $45^{\circ}$  left and right and  $0-45^{\circ}$  top and bottom as the following picture showing:



## 10.4 Definition of Inspection Zone in LCD

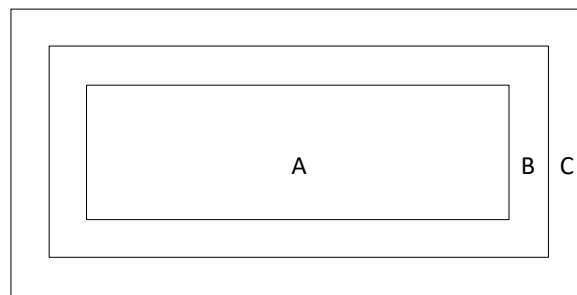


Figure 8: Inspection Zones in an LCD

Zone A: character/Digit area

Zone B: viewing area except Zone A (ZoneA + ZoneB=minimum Viewing area)

Zone C: Outside viewing area (invisible area after assembly in customer's product)

**\*Note:** As a general rule, visual defects in Zone C are permissible, if it does not affect display quality and assembly of customer's product.



## 10.5 Function Defect

| Items to be inspected  | Inspection criterion  | Classification of defects |
|------------------------|---|---------------------------|
| All Functional defects | 1)No Display<br>2)Display Abnormal<br>3)Missing Segment<br>4)Sealing Defects<br>5)No backlight, flickering and abnormal lighting<br>6)Obvious striation<br>7)Current beyond specification value | MA                        |
| Missing                | Missing Components  |                           |
| Outline Dimension      | Overall outline dimension exceed the drawing is not allowed   |                           |

## 10.6 LCD Pixel Defect

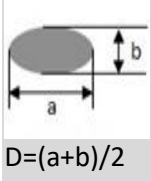
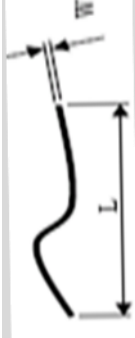
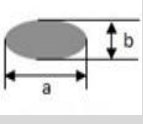
(Bad Dot) (Defect type: MI)

| Item   | Inspection criterion |
|--|----------------------|
| Color pixel dot defect(RGB dot)  | 2                    |
| 2 connected bright dot   | 1                    |
| 3 connected bright dot or more   | 0                    |
| Bright dot quantity  | 2                    |
| Random dark dot quantity   | 3                    |
| 2 connected dark dot   | 1                    |
| 3 connected dark dot or more   | 0                    |
| Dark dot quantity  | 4                    |
| Multi-bright dot   | ND 3%hidden, OK      |
| Remark: 2 bright dots distance $DS \geq 15mm$ 2 dark dots distance $DS \geq 5mm$                           |                      |
| 1) Bright dot: Power on TFT and RGB dot in black display   |                      |
| 2) Dark dot: Power on TFT and gray or black dot in RGB display   |                      |
| 3) Multi-bright dot: Power on TFT and fluorescent tiny dot in black display(only visible in black display) |                      |



## 10.7 Dot and line defect

(defect type: MI)

| Item   | Inspection criterion |                      | Picture  | Inspection method/tools   |  |
|--|----------------------|----------------------|--|---|--|
|  | Size                 | 5 Inch ≤ S < 10 Inch |  |   |  |
| Dot defect (black dot, white dot)  | D ≤ 0.15             | Not count            | <br>$D=(a+b)/2$ | Naked eyes<br>/film card<br>/magnifier  |  |
|  | 0.15 < D ≤ 0.25      | 3                    |  |   |  |
|  | 0.25 < D ≤ 0.30      | 2                    |  |   |  |
|  | 0.30 < D ≤ 0.35      | 1                    |  |   |  |
|  | 0.35 < D ≤ 0.50      | 0                    |  |   |  |
|  | D > 0.5              | 0                    |  |   |  |
| Remark: D ≤ 0.15mm, not count. Multi-dot as bulk is not accepted.<br>Count dot quantity ≤ 5<br>2 round dots or linear dots in 1 cm is judged as multi-dot.                       |                      |                      |  |   |  |
| Line defect (visible when power on)  | Length (mm)          | Width (mm)           | Judgement Criterion  |  | Naked eyes<br>/film card<br>/magnifier |
|  | Not count            | W ≤ 0.03             | Accepted   |   |  |
|  | L ≤ 5                | 0.03 ≤ W < 0.05      | 3  |   |  |
|  | L ≤ 5                | 0.05 ≤ W < 0.08      | 1  |   |  |
|  | L ≤ 8                | 0.05 ≤ W < 0.08      | 0  |   |  |
|  | L > 8                | W > 0.08             | 0  |   |  |
| Remark:<br>Invisible when power on, only visible in special angle against light, show as watermark/folding/scratch but cannot be touched, no control or refer to keeping sample. |                      |                      |  |   |  |
| Polarizer convex-concave dot defect, polarizer bubble defect   | Size(mm)             | Judgement Criterion  |               | Naked eyes<br>/film card<br>/magnifier  |  |
|  | D ≤ 0.20             | Not count            |  |   |  |
|  | 0.20 < D ≤ 0.5       | 2                    |  |   |  |
|  | 0.50 < D ≤ 0.8       | 1                    |  |   |  |
|  | 0.8 < D ≤ 1.5        | 0                    |  |   |  |
| D > 1.5mm  | 0                    |                      |  |   |  |



# 11 Handling Precautions

## 11.1 Mounting method

Do not make extra holes in the display or modify its shape. When mounting the display, ensure that the display does not flex, bend or twist. Extreme care should be used when handling the LCD modules.

## 11.2 LCD Handling and Cleaning Precaution

To clean the display surface, it is recommended to wipe lightly using a soft cloth with either Isopropyl alcohol or Ethyl alcohol.

Do not wipe the display surface with dry or hard materials as it may damage the polarizer surface.

Do not use Water or Aromatics to clean the display.

Do not wipe ITO pad area with dry or hard materials that will damage the ITO patterns

Do not use Soldering flux, Chlorine(Cl), and Sulfur(S) on the pad or prevent it from being contaminated.

If the display is sent without applying a silicon coat on the pad, the ITO patterns could be damaged due to corrosion as time goes on.

If ITO corrosion occurs due to customer miss-handling, or if the customer applies materials such as Chlorine (Cl), Sulfur (S) to the display, the responsibility is placed the customer.

## 11.3 Static Charge Precaution

The LCD module uses CMOS LSI drivers, so we recommend that you:

- Connect any unused input terminal to VDD or VSS
- Do not input any signals before power is turned on
- Ground your body, work/assembly areas, and assembly equipment to protect against static electricity.

## 11.4 Packing

The module employs LCD elements and must be treated as such.

- Avoid intense shock and falls from a height.
- To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity

## 11.5 Precautions during Operation

- It is an indispensable condition to drive the LCD module within the specified voltage limits. Applying voltage higher than the limit will reduce the life span of the LCD.
- Using direct drive current should be avoided, as it will induce an electrochemical reaction causing undesirable deterioration.
- The LCD's response time will be delayed when operating at a temperature lower than the suggested operating range. When operating at a temperature higher than the suggested range, the LCD will be noticeably darker. The display will return to normal when it is brought back to the specified operation temperature.
- If the display area is pushed hard during operation, some font may be abnormally drawn but the LCD will return to normal after it is reset.
- Slight dew depositing on terminals can cause an electro-chemical reaction, damaging traces and resulting in an open circuit.

Usage under the maximum operating temperature, 50%Rh or less is required.



## 11.6 Storage Recommendations

When storing the LCD for a prolonged period of time, the following recommendations will help prevent damage or deterioration

- Store the display in an ambient temperature range between 10°C to 30°C, and in a relative humidity of 45% to 75%.
- Do not leave the display exposed to sunlight or fluorescent light.
- Place the display in a polyethylene bag with the opening sealed.
- Ensure that nothing is making contact with the polarizer surface.
- It is recommended to store them in the same packaging that was provided upon purchase

## 11.7 Safety Precautions

In the case that the LCD glass has shattered, it is recommended to remove any glass pieces, wash off the liquid crystal using either acetone or ethanol, and proceed to burn any remaining display pieces.

If any liquid leaked out of a damaged glass cell, and comes in contact with your hands, please wash it off well with soap and water





## 12 Ordering

### 12.1 Part Numbering Scheme

Table 1: Parallel TFT Part Numbering Scheme

| MOP | TFT | 800 | 480 | 50 | A | BLM | TPN |
|-----|-----|-----|-----|----|---|-----|-----|
| 1   | 2   | 3   | 4   | 5  | 6 | 7   | 8   |

### 12.2 Options

Table 2: Parallel Part Options

| # | Designator          | Options  |
|---|---------------------|--|
| 1 | Product Line        | MOP: Matrix Orbital Parallel Display   |
| 2 | Screen Type         | TFT: Graphic TFT   |
| 3 | Display Columns     | 800: Eight Hundred Pixel Columns   |
| 4 | Display Rows        | 480: Four Hundred Eighty Pixel Columns   |
| 5 | Display Size        | 50: 5.0"   |
| 6 | Display Form Factor | A: A Form Factor   |
| 7 | Brightness Level    | -BLS: Brightness < 300 Nit<br>-BLM: 300 Nit < Brightness < 600 Nit<br>-BLH: 600 Nit < Brightness < 1000 Nit<br>-BLD: Brightness > 1000 Nit |
| 8 | Touch Panel Type    | TPN: None<br>TPR: Resistive<br>TPC: Capacitive   |

## 13 Contact

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### Online

Purchasing: [www.matrixorbital.com](http://www.matrixorbital.com)

Support: [www.matrixorbital.ca](http://www.matrixorbital.ca)





Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

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- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
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- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



#### Как с нами связаться

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