

16-Mbit (1M × 16/2M × 8) Static RAM

Features

- Ultra-low standby power
 - Typical standby current: 5.5 μA
 - Maximum standby current: 16 μA
- TSOP I package configurable as 1M × 16 or 2M × 8 SRAM
- Very high speed: 45 ns
- Temperature ranges
 - Industrial: -40 °C to +85 °C
- Wide voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, and 4.5 V to 5.5 V
- Easy memory expansion with \overline{CE}_1 , CE_2 , and \overline{OE} Features
- Automatic power-down when deselected
- CMOS for optimum speed and power
- Offered in Pb-free 48-ball VFBGA and 48-pin TSOP I packages

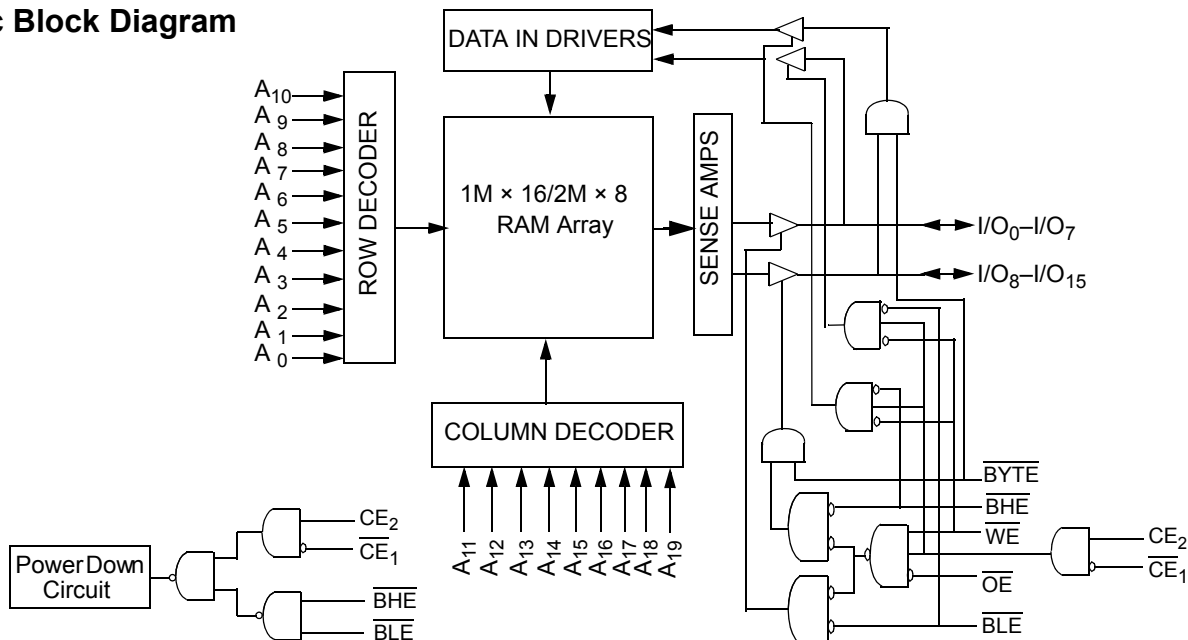
Functional Description

The CY62167GN is a high performance CMOS static RAM organized as 1M words by 16 bits or 2M words by 8 bits. This device features an advanced circuit design that provides an ultra low active current. Ultra low active current is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that reduces power consumption by 99 percent when addresses are not toggling. Place the device into standby mode when deselected (\overline{CE}_1 HIGH or CE_2 LOW or both \overline{BHE} and \overline{BLE} are HIGH). The input and output pins (I/O₀ through I/O₁₅) are placed in a high impedance state when: the device is deselected (\overline{CE}_1 HIGH or CE_2 LOW), outputs are disabled (\overline{OE} HIGH), both Byte High Enable and Byte Low Enable are disabled (\overline{BHE} , \overline{BLE} HIGH), or a write operation is in progress (\overline{CE}_1 LOW, CE_2 HIGH and \overline{WE} LOW).

To write to the device, take Chip Enables (\overline{CE}_1 LOW and CE_2 HIGH) and Write Enable (\overline{WE}) input LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O₀ through I/O₇) is written into the location specified on the address pins (A₀ through A₁₉). If Byte High Enable (\overline{BHE}) is LOW, then data from the I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₉).

To read from the device, take Chip Enables (\overline{CE}_1 LOW and CE_2 HIGH) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins appears on I/O₀ to I/O₇. If Byte High Enable (\overline{BHE}) is LOW, then data from memory appears on I/O₈ to I/O₁₅. See [Truth Table on page 13](#) for a complete description of read and write modes.

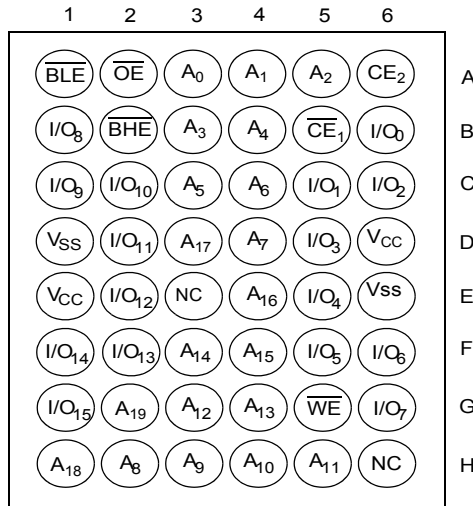
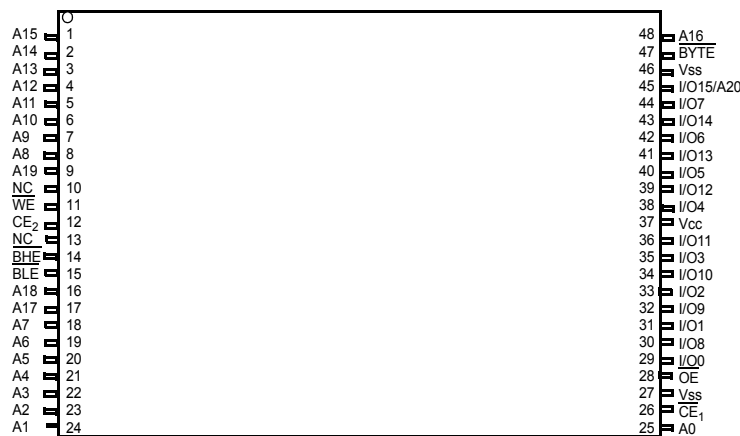
Logic Block Diagram



Contents

Pin Configuration	3	Ordering Information	14
Product Portfolio	3	Ordering Code Definitions	14
Maximum Ratings	4	Package Diagrams	15
Operating Range	4	Acronyms	17
Electrical Characteristics	4	Document Conventions	17
Capacitance	6	Units of Measure	17
Thermal Resistance	6	Document History Page	18
AC Test Loads and Waveforms	6	Sales, Solutions, and Legal Information	19
Data Retention Characteristics	7	Worldwide Sales and Design Support	19
Data Retention Waveform	7	Products	19
Switching Characteristics	8	PSoC® Solutions	19
Switching Waveforms	9	Cypress Developer Community	19
Truth Table	13	Technical Support	19

Pin Configuration

Figure 1. 48-ball VFBGA pinout (Top View) [1, 2]

Figure 2. 48-pin TSOP I pinout (Top View) [2, 3]


Product Portfolio

Product	Range	V _{CC} Range (V)			Speed (ns)	Power Dissipation								
						Operating I _{CC} (mA)				Standby I _{SB2} (μA)				
		f = 1 MHz		f = f _{max}										
		Min	Typ ^[4]	Max		Typ ^[4]	Max	Typ ^[4]	Max					
CY62167GN18	Industrial	1.65	1.8	2.2	55	7	9	29	32	7	26			
CY62167GN30		2.2	3.0	3.6				45	29			36	5.5	16
CY62167GN		4.5	5.0	5.5										

Notes

- Ball H6 for the VFBGA package can be used to upgrade to a 32M density.
- NC pins are not connected on the die.
- The BYTE pin in the 48-pin TSOP I package has to be tied to V_{CC} to use the device as a 1M × 16 SRAM. The 48-pin TSOP I package can also be used as a 2M × 8 SRAM by tying the BYTE signal to V_{SS}. In the 2M × 8 configuration, Pin 45 is A₂₀, while BHE, BLE and I/O₈ to I/O₁₄ pins are not used.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature	-65 °C to + 150 °C
Ambient temperature with power applied	-55 °C to + 125 °C
Supply voltage to ground potential ^[5, 6]	-0.3 V to $V_{CC(max)}$ + 0.3 V
DC voltage applied to outputs in High Z state ^[5, 6]	-0.3 V to $V_{CC(max)}$ + 0.3 V
DC input voltage ^[5, 6]	-0.3 V to $V_{CC(max)}$ + 0.3 V

Output current into outputs (LOW)	20 mA
Static discharge voltage (MIL-STD-883, Method 3015)	>2001 V
Latch-up current	>200 mA

Operating Range

Device Range	Ambient Temperature	$V_{CC}^{[7]}$
Industrial	-40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	45 ns/ 55 ns			Unit	
			Min	Typ ^[8]	Max		
V_{OH}	Output HIGH voltage	$1.65 \leq V_{CC} \leq 2.2$	$I_{OH} = -0.1$ mA	1.4	-	-	V
		$2.2 \leq V_{CC} \leq 2.7$	$I_{OH} = -0.1$ mA	2.0	-	-	
		$2.7 \leq V_{CC} \leq 3.6$	$I_{OH} = -1.0$ mA	2.4	-	-	
		$4.5 \leq V_{CC} \leq 5.5$	$I_{OH} = -1.0$ mA	2.4	-	-	
		$4.5 \leq V_{CC} \leq 5.5$	$I_{OH} = -0.1$ mA	$V_{OH} - 0.5^{[9]}$	-	-	
V_{OL}	Output LOW voltage	$1.65 \leq V_{CC} \leq 2.2$	$I_{OL} = 0.1$ mA	-	-	0.2	V
		$2.2 \leq V_{CC} \leq 2.7$	$I_{OL} = 0.1$ mA	-	-	0.4	
		$2.7 \leq V_{CC} \leq 3.6$	$I_{OL} = 2.1$ mA	-	-	0.4	
		$4.5 \leq V_{CC} \leq 5.5$	$I_{OL} = 2.1$ mA	-	-	0.4	
V_{IH}	Input HIGH voltage	$1.65 \leq V_{CC} \leq 2.2$		1.4	-	$V_{CC} + 0.2$	V
		$2.2 \leq V_{CC} \leq 2.7$		1.8	-	$V_{CC} + 0.3$	
		$2.7 \leq V_{CC} \leq 3.6$		2	-	$V_{CC} + 0.3$	
		$4.5 \leq V_{CC} \leq 5.5$		2.2	-	$V_{CC} + 0.5$	
V_{IL}	Input LOW voltage	$1.65 \leq V_{CC} \leq 2.2$		-0.2	-	0.4	V
		$2.2 \leq V_{CC} \leq 2.7$		-0.3	-	0.6	
		$2.7 \leq V_{CC} \leq 3.6$		-0.3	-	0.8	
		$4.5 \leq V_{CC} \leq 5.5$		-0.5	-	0.8	
I_{IX}	Input leakage current	$GND \leq V_I \leq V_{CC}$		-1	-	+1	μ A
I_{OZ}	Output leakage current	$GND \leq V_O \leq V_{CC}$, Output disabled		-1	-	+1	μ A
I_{CC}	V_{CC} operating supply current	$f = 22.22$ MHz (45 ns)	$V_{CC} = V_{CC(max)}$ $I_{OUT} = 0$ mA CMOS levels	-	29	36	mA
		$f = 18.18$ MHz (55 ns)		-	29	32	mA
		$f = 1$ MHz		-	7	9	mA

Notes

- $V_{IL(min)}$ = -2.0 V for pulse durations less than 20 ns.
- $V_{IH(max)}$ = $V_{CC} + 2$ V for pulse durations less than 20 ns.
- Full Device AC operation assumes a 100 μ s ramp time from 0 to $V_{CC(min)}$ and 200 μ s wait time after V_{CC} stabilization.
- Indicates the value for the center of distribution at 3.0 V, 25 °C and not 100% tested
- This parameter is guaranteed by design and not tested.

Electrical Characteristics (continued)

Over the Operating Range

Parameter	Description	Test Conditions	45 ns/ 55 ns			Unit	
			Min	Typ ^[8]	Max		
I_{SB1} ^[10]	Automatic power down current – CMOS inputs	$\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ or $CE_2 \leq 0.2 \text{ V}$ or $(\overline{BHE}$ and $\overline{BLE}) \geq V_{CC} - 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$, $V_{IN} \leq 0.2 \text{ V}$, $f = f_{max}$ (address and data only), $f = 0$ (\overline{OE} , and \overline{WE}), $V_{CC} = V_{CC(max)}$	–	5.5	16	μA	
I_{SB2} ^[10]	Automatic Power-down Current – CMOS Inputs $V_{CC} = 2.2 \text{ V}$ to 3.6 V and 4.5 V to 5.5 V	$\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ or $CE_2 \leq 0.2 \text{ V}$	25 °C ^[11]	–	5.5	6.5	μA
		or $(\overline{BHE}$ and $\overline{BLE}) \geq V_{CC} - 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$, $f = 0$, $V_{CC} = V_{CC(max)}$	40 °C ^[11]	–	6.3	8.0	
			70 °C ^[11]	–	8.4	12.0	
			85 °C	–	12.0	16.0	
	Automatic Power-down Current – CMOS Inputs $V_{CC} = 1.65 \text{ V}$ to 2.2 V	$\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ or $CE_2 \leq 0.2 \text{ V}$ or $(\overline{BHE}$ and $\overline{BLE}) \geq V_{CC} - 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$, $f = 0$, $V_{CC} = V_{CC(max)}$	–	7.0	26.0		

Notes

10. Chip enables (\overline{CE}_1 and CE_2), byte enables (\overline{BHE} and \overline{BLE}) and \overline{BYTE} must be tied to CMOS levels to meet the $I_{SB1}/I_{SB2} / I_{CCDR}$ spec. Other inputs can be left floating.
 11. Indicates the value for the center of distribution at 3.0 V, 25 °C and not 100% tested.

Capacitance

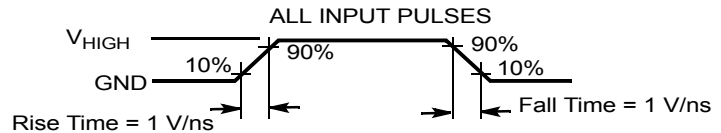
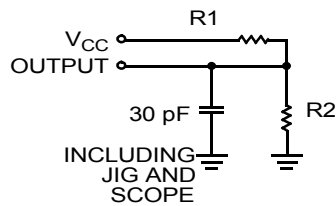
Parameter ^[12]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	$T_A = 25\text{ }^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = V_{CC(\text{typ})}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

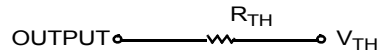
Parameter ^[12]	Description	Test Conditions	48-ball VFBGA	48-pin TSOP I	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	31.50	57.99	$^\circ\text{C/W}$
θ_{JC}	Thermal resistance (junction to case)		15.75	13.42	$^\circ\text{C/W}$

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Parameters	1.8 V	2.5 V	3.0 V	5.0 V	Unit
R_1	13500	16667	1103	1800	Ω
R_2	10800	15385	1554	990	Ω
R_{TH}	6000	8000	645	639	Ω
V_{TH}	0.80	1.20	1.75	1.77	V
V_{HIGH}	1.8	2.5	3.0	5.0	V

Note

12. Tested initially and after any design or process changes that may affect these parameters.

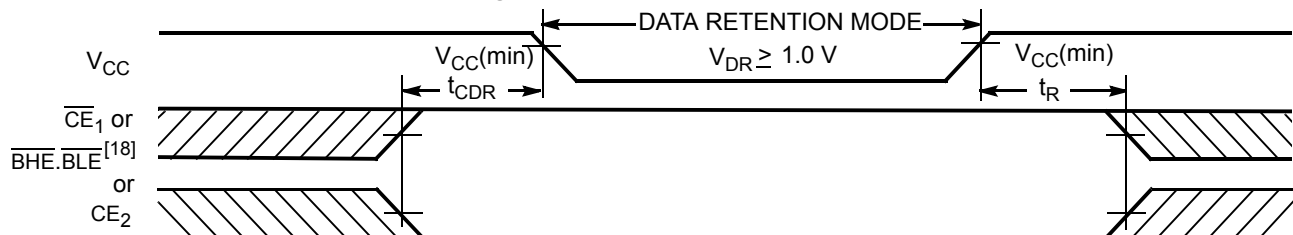
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ ^[13]	Max	Unit
V_{DR}	V_{CC} for data retention		1.0	–	–	V
I_{CCDR} ^[14, 15]	Data retention current	$V_{CC} = 2.2 \text{ V to } 3.6 \text{ V}$, $\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ or $CE_2 \leq 0.2 \text{ V}$ or $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$	–	5.5	16	μA
		$1.2 \text{ V} \leq V_{CC} \leq 2.2 \text{ V}$, $\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ or $CE_2 \leq 0.2 \text{ V}$ or $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$	–	7.0	26.0	
t_{CDR} ^[16]	Chip deselect to data retention time		0	–	–	–
t_R ^[17, 19]	Operation recovery time		45/55	–	–	ns

Data Retention Waveform

Figure 4. Data Retention Waveform



Notes

13. Indicates the value for the center of distribution at 3.0 V, 25 °C and not 100% tested.
14. Chip enables (\overline{CE}_1 and CE_2), byte enables (BHE and BLE) and BYTE must be tied to CMOS levels to meet the $I_{SB1} / I_{SB2} / I_{CCDR}$ spec. Other inputs can be left floating.
15. I_{CCDR} is guaranteed only after the device is first powered up to $V_{CC(min)}$ and then brought down to V_{DR} .
16. Tested initially and after any design or process changes that may affect these parameters.
17. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100 \mu\text{s}$ or stable at $V_{CC(min)} \geq 100 \mu\text{s}$.
18. BHE.BLE is the AND of both BHE and BLE. Deselect the chip by either disabling the chip enable signals or by disabling both \overline{BHE} and \overline{BLE} .
19. These parameters are guaranteed by design and are not tested.

Switching Characteristics

Parameter ^[20]	Description	45 ns		55 ns		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	45.0	–	55.0	–	ns
t_{AA}	Address to data valid	–	45.0	–	55.0	ns
t_{OHA}	Data hold from address change	10.0	–	10.0	–	ns
t_{ACE}	\overline{CE}_1 LOW and CE_2 HIGH to data valid	–	45.0	–	55.0	ns
t_{DOE}	\overline{OE} LOW to data valid	–	22.0	–	25.0	ns
t_{LZOE}	\overline{OE} LOW to Low Z ^[21, 22]	5.0	–	5.0	–	ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[21, 22, 23]	–	18.0	–	18.0	ns
t_{LZCE}	\overline{CE}_1 LOW and CE_2 HIGH to Low Z ^[21, 22]	10.0	–	10.0	–	ns
t_{HZCE}	\overline{CE}_1 HIGH and CE_2 LOW to High Z ^[21, 22, 23]	–	18.0	–	18.0	ns
t_{PU}	\overline{CE}_1 LOW and CE_2 HIGH to power-up ^[24]	0	–	0	–	ns
t_{PD}	\overline{CE}_1 HIGH and CE_2 LOW to power-down ^[24]	–	45.0	–	55.0	ns
t_{DBE}	BLE / BHE LOW to data valid	–	45.0	–	55.0	ns
t_{LZBE}	BLE / BHE LOW to Low Z ^[21, 22]	5.0	–	5.0	–	ns
t_{HZBE}	BLE / BHE HIGH to High Z ^[21, 22, 23]	–	18.0	–	18.0	ns
Write Cycle^[25, 26]						
t_{WC}	Write cycle time	45	–	55	–	ns
t_{SCE}	\overline{CE}_1 LOW and CE_2 HIGH to write end	35	–	40	–	ns
t_{AW}	Address setup to write end	35	–	40	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	\overline{WE} pulse width	35	–	40	–	ns
t_{BW}	BLE / BHE LOW to write end	35	–	40	–	ns
t_{SD}	Data setup to write end	25	–	25	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{HZWE}	\overline{WE} LOW to High Z ^[21, 22, 23]	–	18	–	20	ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[21, 22]	10	–	10	–	ns

Notes

20. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 V/ns, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in Figure 3 on page 6.

21. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.

22. Tested initially and after any design or process changes that may affect these parameters.

23. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high impedance state.

24. These parameters are guaranteed by design and are not tested.

25. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE}_1 = V_{IL}$, \overline{BHE} or \overline{BLE} or both = V_{IL} , and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.

26. The minimum write cycle pulse width for Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) should be equal to the sum of t_{HZWE} and t_{SD} .

Switching Waveforms

Figure 5. Read Cycle No. 1 (Address Transition Controlled)^[27, 28]

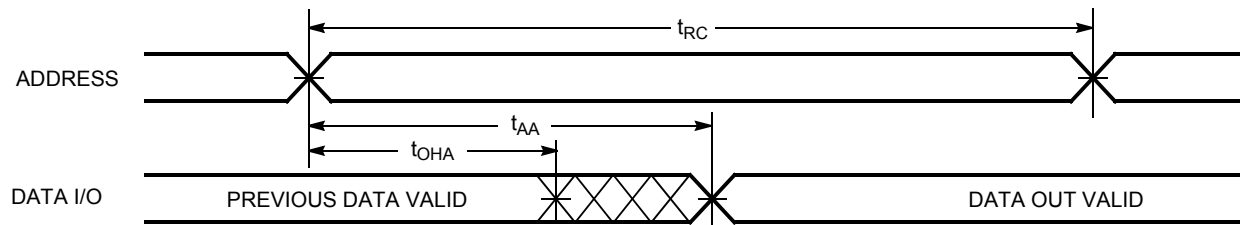
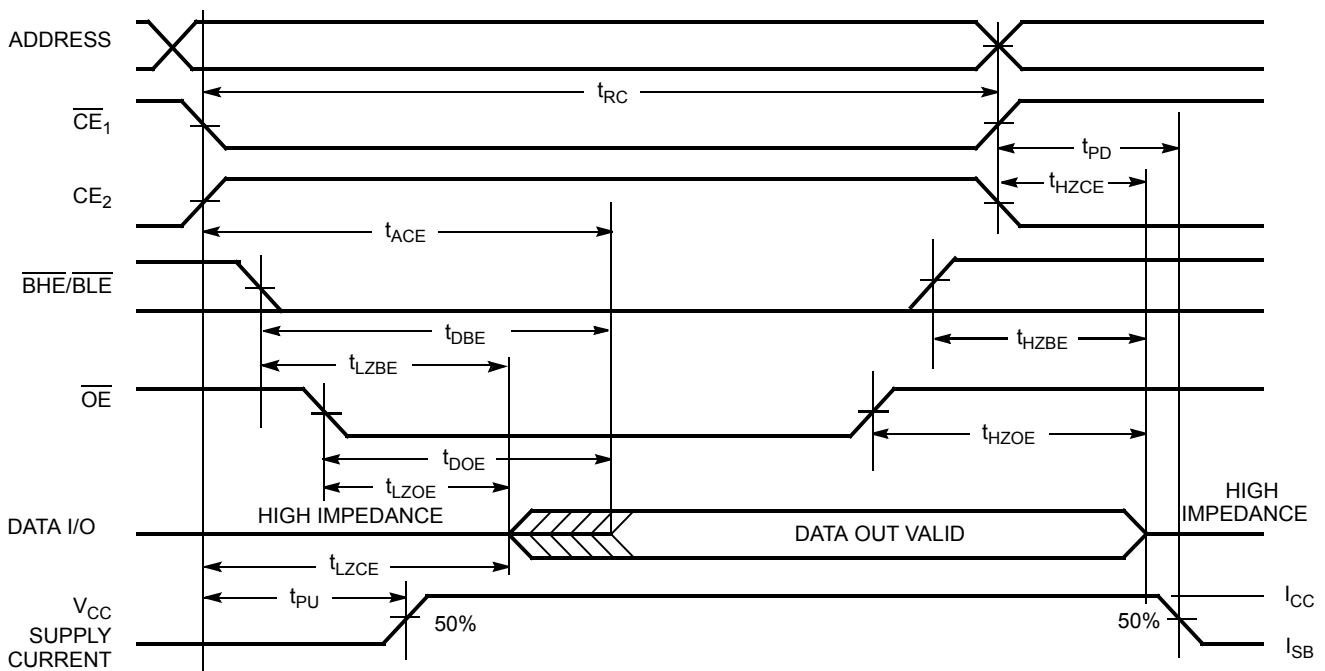


Figure 6. Read Cycle No. 2 (\overline{OE} Controlled)^[28, 29]



Notes

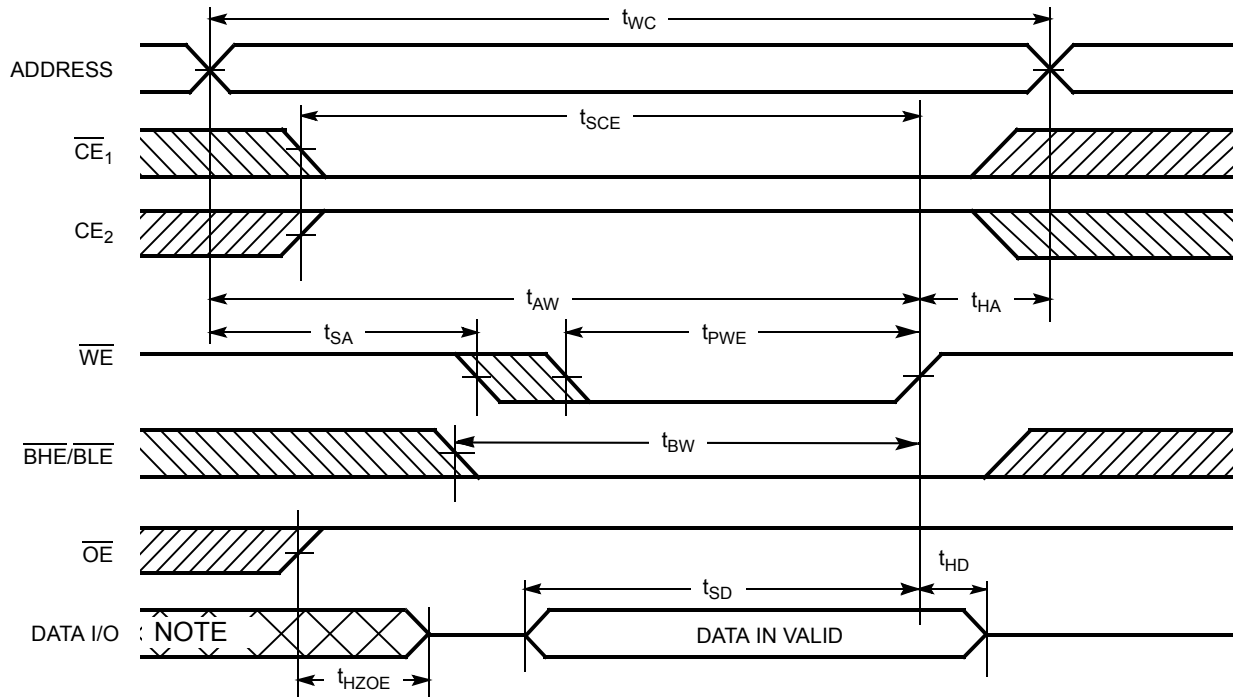
27. The device is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$, \overline{BHE} , \overline{BLE} or both = V_{IL} , and $CE_2 = V_{IH}$.

28. \overline{WE} is HIGH for read cycle.

29. Address valid before or similar to \overline{CE}_1 , \overline{BHE} , \overline{BLE} transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1 (\overline{WE} Controlled)^[30, 31, 32]

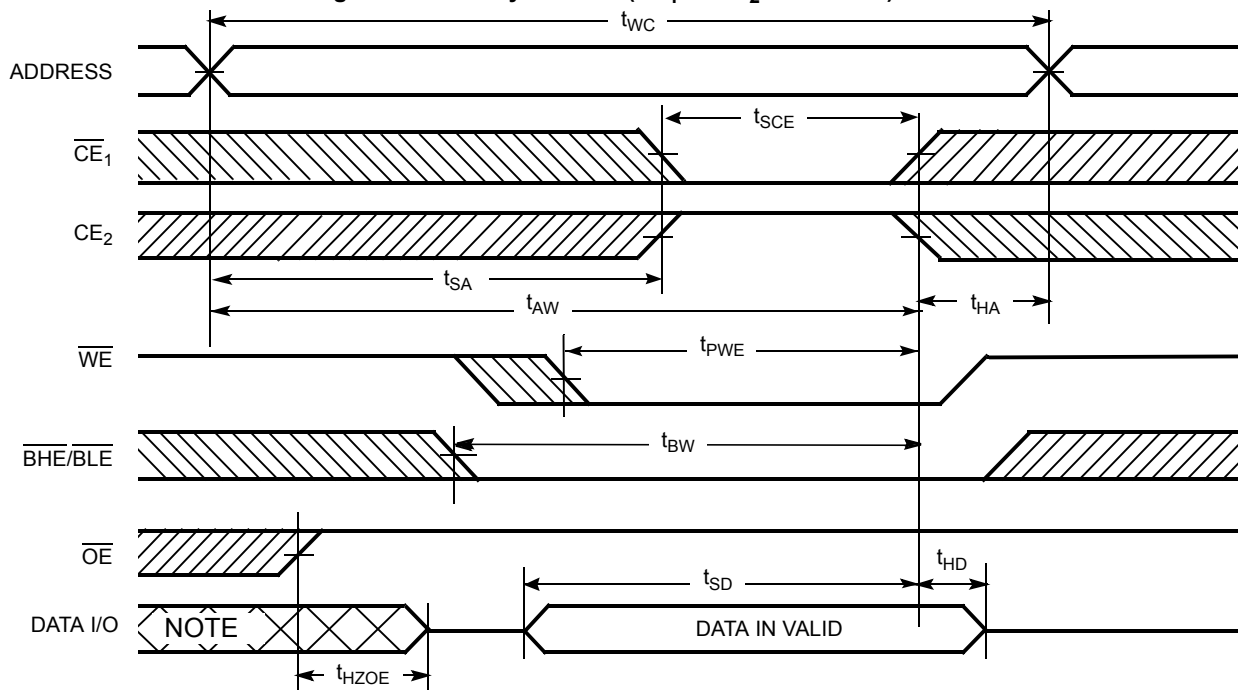


Notes

- 30. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE}_1 = V_{IL}$, \overline{BHE} or \overline{BLE} or both = V_{IL} , and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
- 31. Data I/O is high impedance if $OE = V_{IH}$.
- 32. If \overline{CE}_1 goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
- 33. During this period the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 2 (\overline{CE}_1 or CE_2 Controlled)^[34, 35]



Notes

- 34. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE}_1 = V_{IL}$, \overline{BHE} or \overline{BLE} or both = V_{IL} , and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
- 35. If \overline{CE}_1 goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
- 36. During this period the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)^[37, 38]

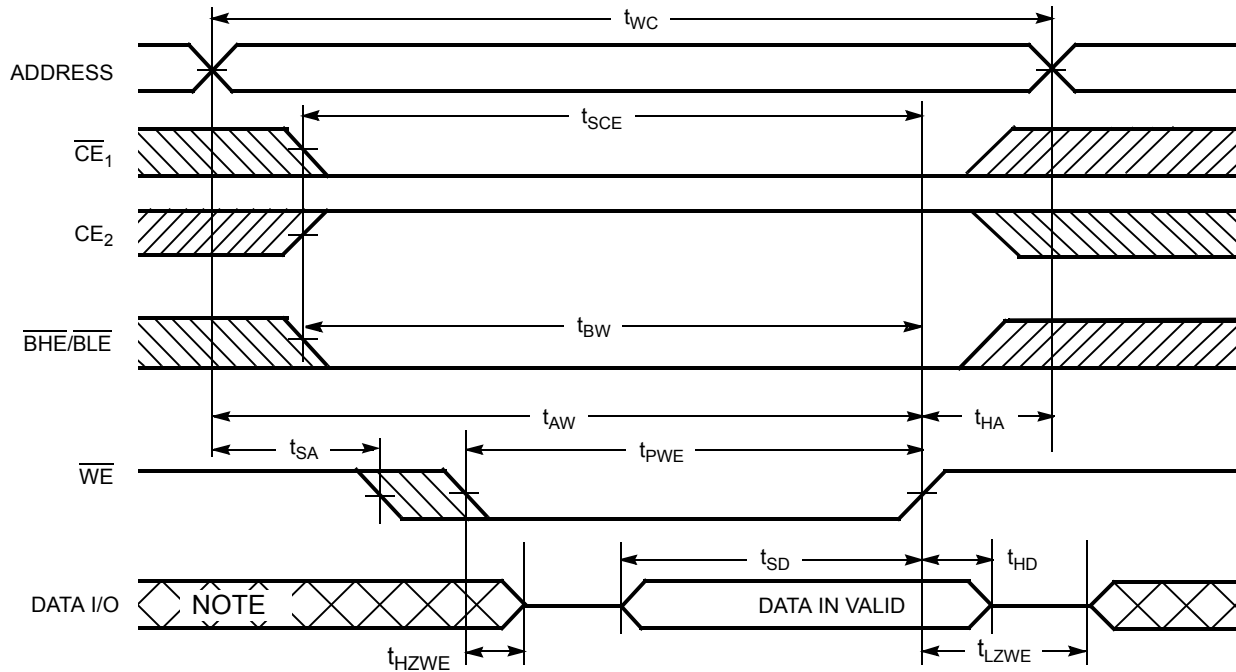
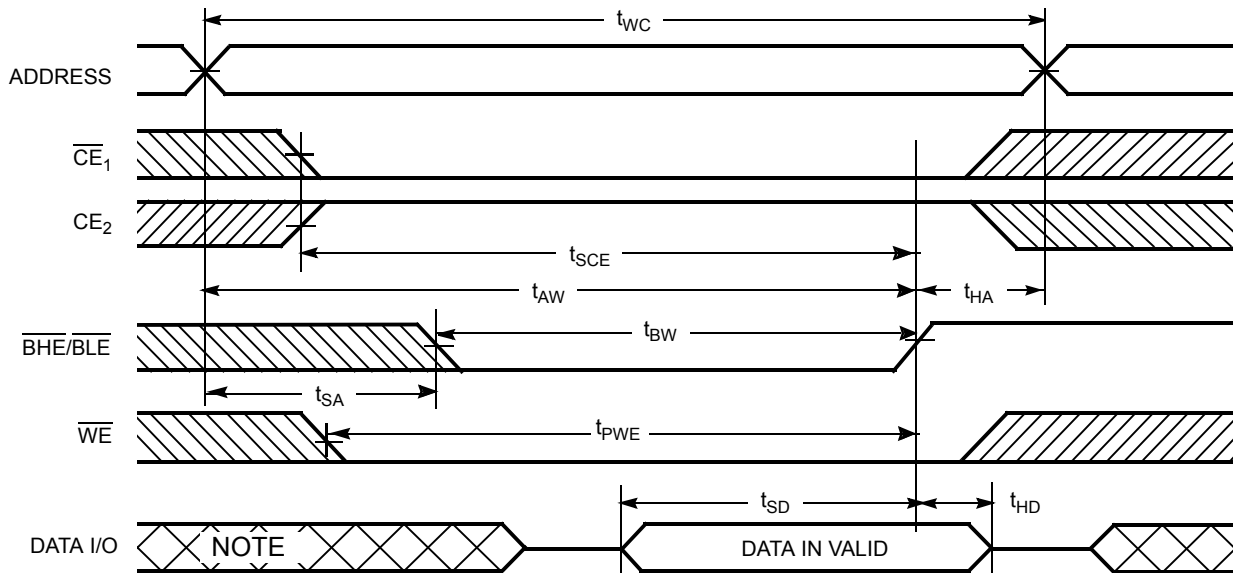


Figure 10. Write Cycle No. 4 ($\overline{BHE}/\overline{BLE}$ Controlled, \overline{OE} LOW)^[37, 38]



Notes

- 37. If \overline{CE}_1 goes HIGH and \overline{CE}_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
- 38. The minimum write cycle pulse width should be equal to the sum of t_{HZWE} and t_{SD} .
- 39. During this period the I/Os are in output state. Do not apply input signals.

Truth Table

\overline{CE}_1	CE_2	\overline{WE}	\overline{OE}	\overline{BHE}	\overline{BLE}	Inputs/Outputs	Mode	Power
H	X ^[40]	X	X	X ^[40]	X ^[40]	High Z	Deselect/Power-down	Standby (I_{SB})
X ^[40]	L	X	X	X ^[40]	X ^[40]	High Z	Deselect/Power-down	Standby (I_{SB})
X ^[40]	X ^[40]	X	X	H	H	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (I/O_0 – I/O_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	Data Out (I/O_0 – I/O_7); High Z (I/O_8 – I/O_{15})	Read	Active (I_{CC})
L	H	H	L	L	H	High Z (I/O_0 – I/O_7); Data Out (I/O_8 – I/O_{15})	Read	Active (I_{CC})
L	H	H	H	X	X	High Z	Output disabled	Active (I_{CC})
L	H	L	X	L	L	Data In (I/O_0 – I/O_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	Data In (I/O_0 – I/O_7); High Z (I/O_8 – I/O_{15})	Write	Active (I_{CC})
L	H	L	X	L	H	High Z (I/O_0 – I/O_7); Data In (I/O_8 – I/O_{15})	Write	Active (I_{CC})

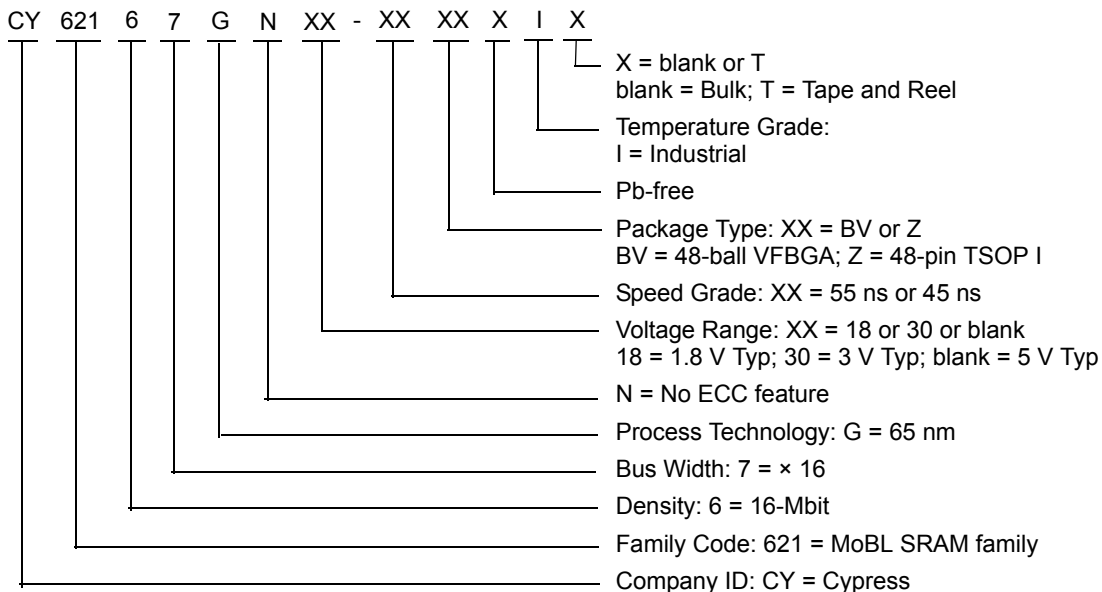
Note

40. The 'X' (Don't care) state for the chip enables and Byte enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

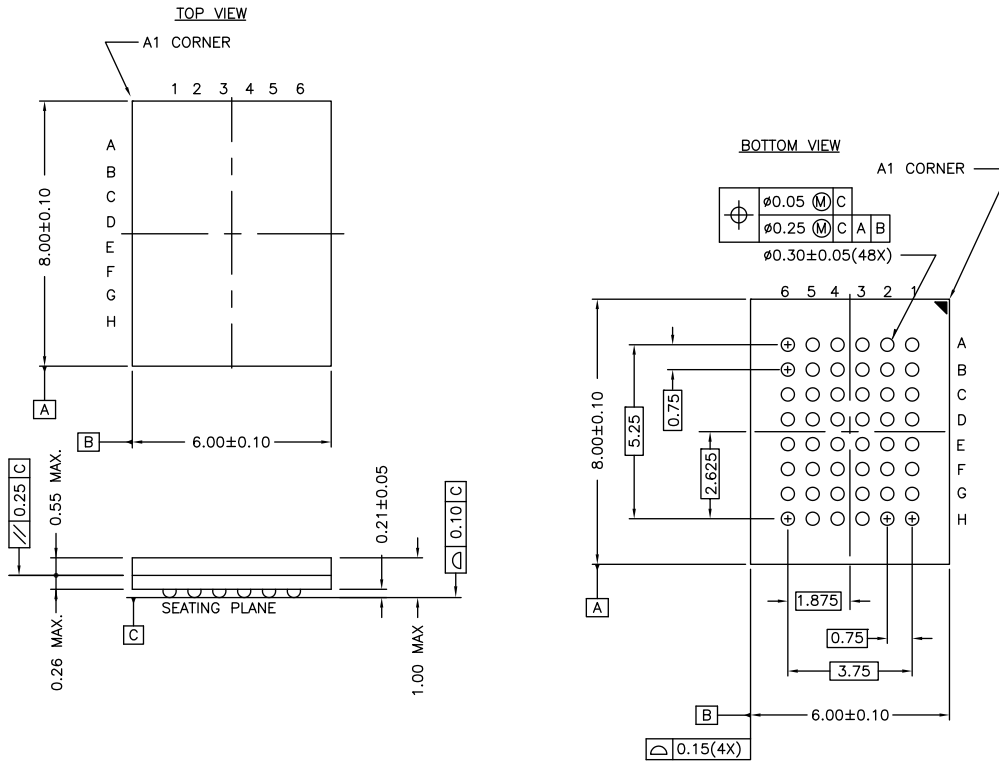
Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type	Operating Range
55	1.65 V–2.2 V	CY62167GN18-55BVXI	51-85150	48-ball VFBGA (6 × 8 × 1 mm), Package Code: BV48	Industrial
		CY62167GN18-55BVXIT			
45	2.2 V–3.6 V	CY62167GN30-45BVXI	51-85150	48-ball VFBGA (6 × 8 × 1 mm), Package Code: BV48	
		CY62167GN30-45BVXIT			
		CY62167GN30-45ZXI	51-85183	48-pin TSOP I (Pb-free)	
		CY62167GN30-45ZXIT			
4.5 V–5.5 V	CY62167GN-45ZXI	51-85183	48-pin TSOP I (Pb-free)		
				CY62167GN-45ZXIT	

Ordering Code Definitions



Package Diagrams

Figure 11. 48-ball VFBGA (6 × 8 × 1.0 mm) Package Outline, 51-85150

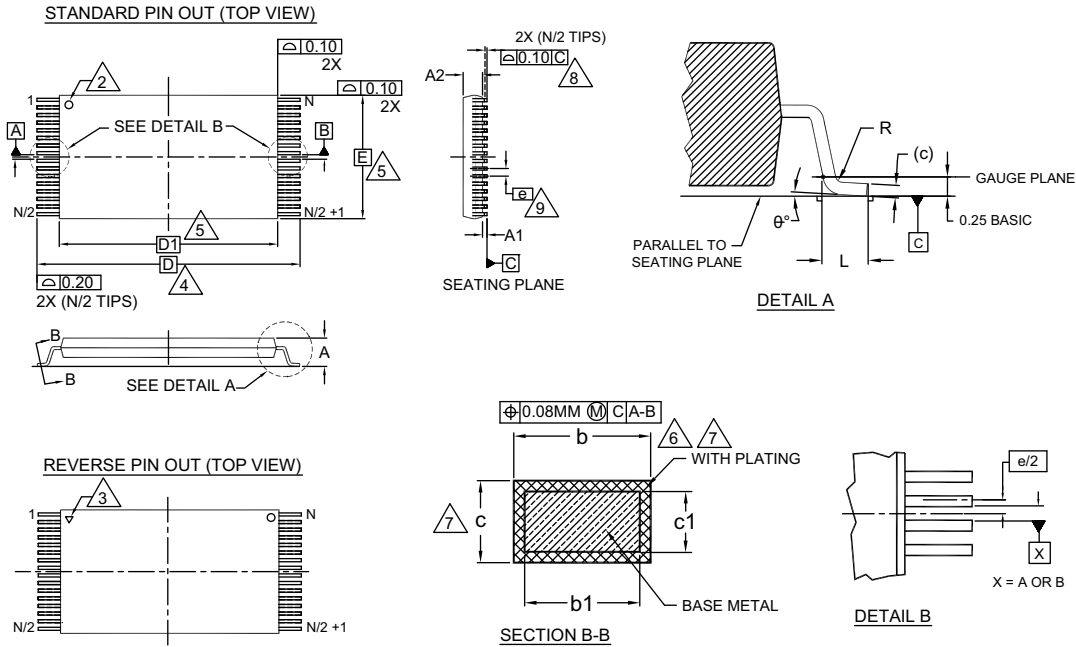


NOTE:
 PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

Package Diagrams (continued)

Figure 12. 48-pin TSOP I (12 × 18.4 × 1.0 mm) Package Outline, 51-85183



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	20.00 BASIC		
D1	18.40 BASIC		
E	12.00 BASIC		
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	—	8
R	0.08	—	0.20
N	48		

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS (mm).
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN); INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE [C]. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm.
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.
10. JEDEC SPECIFICATION NO. REF: MO-142(D)DD.

51-85183 *F

Acronyms

Acronym	Description
BHE	Byte High Enable
BLE	Byte Low Enable
CE	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
OE	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array
WE	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62167GN MoBL®, 16-Mbit (1M × 16/2M × 8) Static RAM Document Number: 001-93628				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*B	5210733	NILE	07/04/2016	Changed status from Preliminary to Final.
*C	5420388	VINI	09/08/2016	<p>Updated Electrical Characteristics: Changed minimum value of V_{OH} parameter corresponding to Test Condition "$2.7 \leq V_{CC} \leq 3.6, I_{OH} = -1.0 \text{ mA}$" from 2.2 V to 2.4 V. Changed minimum value of V_{IH} parameter corresponding to Test Condition "$2.2 \leq V_{CC} \leq 2.7$" from 2 V to 1.8 V. Updated Note 5 (Replaced 2 ns with 20 ns). Updated Note 6 (Replaced 2 ns with 20 ns). Updated Ordering Information: Updated part numbers. Added Tape and Reel parts. Updated to new template.</p>
*D	5783985	NILE	06/23/2017	<p>Updated Data Retention Characteristics: Changed typical value of I_{CCDR} parameter corresponding to Condition "$1.2 \text{ V} \leq V_{CC} \leq 2.2 \text{ V}$" from 5.5 μA to 7.0 μA. Changed maximum value of I_{CCDR} parameter corresponding to Condition "$1.2 \text{ V} \leq V_{CC} \leq 2.2 \text{ V}$" from 16.0 μA to 26.0 μA. Updated Package Diagrams: spec 51-85183 – Changed revision from *D to *F. Updated to new template.</p>

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

ARM [®] Cortex [®] Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC[®] Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6](#)

Cypress Developer Community

[Forums](#) | [WICED IOT Forums](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2014–2017. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.