



VNN3NV04P-E VNS3NV04P-E

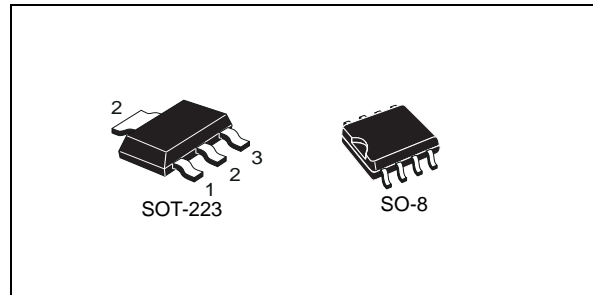
OMNIFET II fully autoprotected Power MOSFET

Datasheet – production data

Features

Type	$R_{DS(on)}$	I_{lim}	V_{clamp}
VNN3NV04P-E VNS3NV04P-E	120 m Ω	3.5 A	40 V

- Linear current limitation
- Thermal shutdown
- Short circuit protection
- Integrated clamp
- Low current drawn from input pin
- Diagnostic feedback through input pin
- ESD protection
- Direct access to the gate of the Power MOSFET (analog driving)
- Compatible with standard Power MOSFET in compliance with the 2002/95/EC European directive



Description

The VNN3NV04P-E, VNS3NV04P-E, are monolithic devices designed in STMicroelectronics® VIPower® M0-3 Technology, intended for replacement of standard Power MOSFETs from DC up to 50 kHz applications. Built in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments.

Fault feedback can be detected by monitoring the voltage at the input pin.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
SOT-223	—	VNN3NV04PTR-E
SO-8	VNS3NV04P-E	VNS3NV04PTR-E

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1 Block diagram and pin description

Figure 1. Block diagram

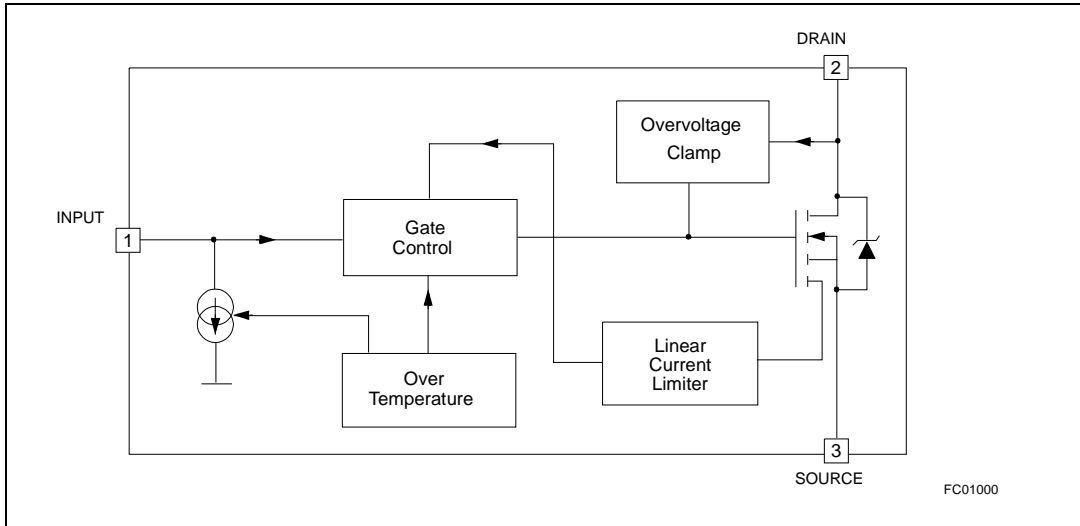
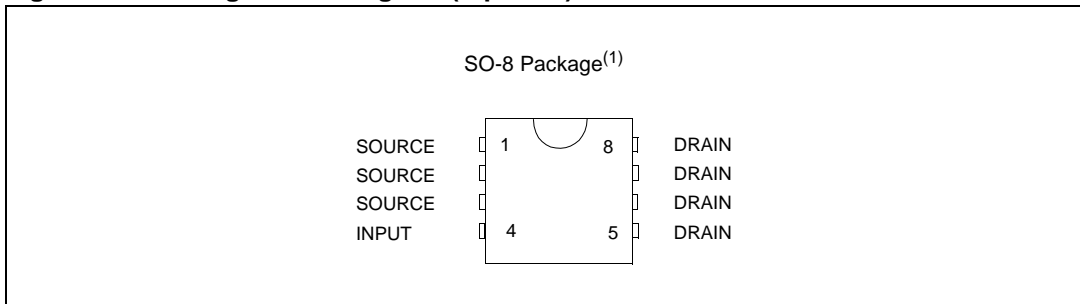


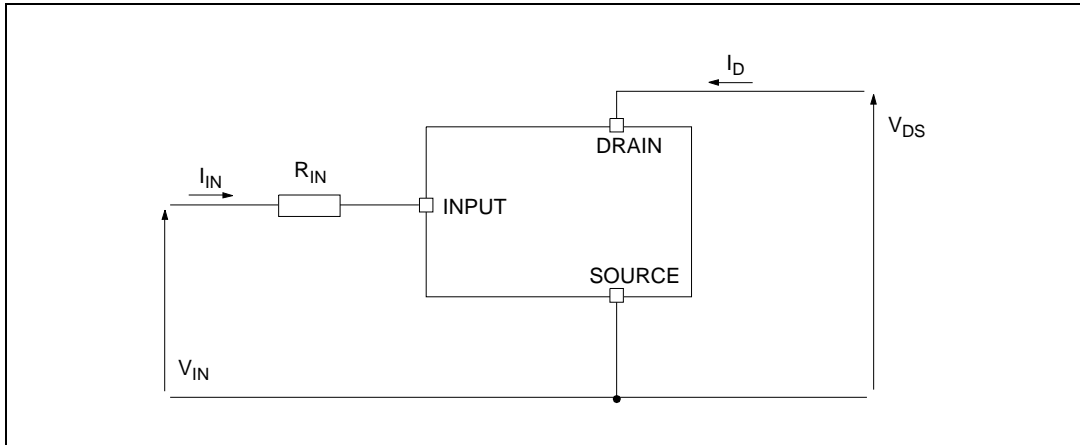
Figure 2. Configuration diagram (top view)



1. For the pins configuration related to SOT-223 see outlines at page 1.

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		SOT-223	SO-8	
V_{DS}	Drain-source voltage ($V_{IN} = 0\text{ V}$)	Internally clamped		V
V_{IN}	Input voltage	Internally clamped		V
I_{IN}	Input current	+/-20		mA
$R_{IN\text{ MIN}}$	Minimum input series impedance	220		Ω
I_D	Drain current	Internally limited		A
I_R	Reverse DC output current	-5.5		A
V_{ESD1}	Electrostatic discharge ($R = 1.5\text{ K}\Omega$, $C = 100\text{ pF}$)	4000		V
V_{ESD2}	Electrostatic discharge on output pin only ($R = 330\ \Omega$, $C = 150\text{ pF}$)	16500		V
P_{tot}	Total dissipation at $T_c = 25\text{ }^\circ\text{C}$	7	8.3	W
T_j	Operating junction temperature	Internally limited		$^\circ\text{C}$
T_c	Case operating temperature	Internally limited		$^\circ\text{C}$
T_{stg}	Storage temperature	-55 to 150		$^\circ\text{C}$

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		SOT-223	SO-8	
$R_{thj-case}$	Thermal resistance junction-case max	18		°C/W
$R_{thj-lead}$	Thermal resistance junction-lead max		15	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	70 ⁽¹⁾	65 ⁽¹⁾	°C/W

1. When mounted on a standard single-sided FR4 board with 50 mm² of Cu (at least 35 mm thick) connected to all DRAIN pins.

2.3 Electrical characteristics

-40°C < T_j < 150°C, unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Off						
V_{CLAMP}	Drain-source clamp voltage	$V_{IN} = 0\text{ V}; I_D = 1.5\text{ A}$	40	45	55	V
V_{CLTH}	Drain-source clamp threshold voltage	$V_{IN} = 0\text{ V}; I_D = 2\text{ mA}$	36			V
V_{INTH}	Input threshold voltage	$V_{DS} = V_{IN}; I_D = 1\text{ mA}$	0.5		2.5	V
I_{ISS}	Supply current from input pin	$V_{DS} = 0\text{ V}; V_{IN} = 5\text{ V}$		100	150	μA
V_{INCL}	Input-source clamp voltage	$I_{IN} = 1\text{ mA}$	6	6.8	8	V
		$I_{IN} = -1\text{ mA}$	-1.0		-0.3	V
I_{DSS}	Zero input voltage drain current ($V_{IN} = 0\text{ V}$)	$V_{DS} = 13\text{ V}; V_{IN} = 0\text{ V}; T_j = 25^\circ\text{C}$			30	μA
		$V_{DS} = 25\text{ V}; V_{IN} = 0\text{ V}$			75	μA
On						
$R_{DS(on)}$	Static drain-source on resistance	$V_{IN} = 5\text{ V}; I_D = 1.5\text{ A}; T_j = 25^\circ\text{C}$			120	mΩ
		$V_{IN} = 5\text{ V}; I_D = 1.5\text{ A}$			240	mΩ
Dynamic ($T_j = 25^\circ\text{C}$, unless otherwise specified)						
$g_{fs}^{(1)}$	Forward transconductance	$V_{DD} = 13\text{ V}; I_D = 1.5\text{ A}$		5.0		S
C_{OSS}	Output capacitance	$V_{DS} = 13\text{ V}; f = 1\text{ MHz}; V_{IN} = 0\text{ V}$		150		pF
Switching ($T_j = 25^\circ\text{C}$, unless otherwise specified)						
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{ V}; I_D = 1.5\text{ A}; V_{gen} = 5\text{ V}; R_{gen} = R_{IN\text{ MIN}} = 220\ \Omega$ (see Figure 4)		90	300	ns
t_r	Rise time			250	750	ns
$t_{d(off)}$	Turn-off delay time			450	1350	ns
t_f	Fall time			250	750	ns

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit	
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{ V}; I_D = 1.5\text{ A}; V_{gen} = 5\text{ V};$ $R_{gen} = 2.2\text{ K}\Omega$ (see Figure 4)		0.45	1.35	μs	
t_r	Rise time			2.5	7.5	μs	
$t_{d(off)}$	Turn-off delay time			3.3	10.0	μs	
t_f	Fall time			2.0	6.0	μs	
$(di/dt)_{on}$	Turn-on current slope	$V_{DD} = 15\text{ V}; I_D = 1.5\text{ A}; V_{gen} = 5\text{ V};$ $R_{gen} = R_{IN\text{ MIN}} = 220\ \Omega$		4.7		$\text{A}/\mu\text{s}$	
Q_i	Total input charge	$V_{DD} = 12\text{ V}; I_D = 1.5\text{ A}; V_{IN} = 5\text{ V};$ $I_{gen} = 2.13\text{ mA}$ (see Figure 7)		8.5		nC	
Source drain diode ($T_j=25^\circ\text{C}$, unless otherwise specified)							
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 1.5\text{ A}; V_{IN} = 0\text{ V}$		0.8		V	
t_{rr}	Reverse recovery time	$I_{SD} = 1.5\text{ A}; di/dt = 12\text{ A}/\mu\text{s};$ $V_{DD} = 30\text{ V}; L = 200\ \mu\text{H}$ (see Figure 5)		107		ns	
Q_{rr}	Reverse recovery charge				37		μC
I_{RRM}	Reverse recovery current				0.7		A
Protections ($-40^\circ\text{C} < T_j < 150^\circ\text{C}$, unless otherwise specified)							
I_{lim}	Drain current limit	$V_{IN} = 5\text{ V}; V_{DS} = 13\text{ V}$	3.5	5	7	A	
t_{dlim}	Step response current limit	$V_{IN} = 5\text{ V}; V_{DS} = 13\text{ V}$		10		μs	
T_{jsh}	Over temperature shutdown		150	175	200	$^\circ\text{C}$	
T_{jrs}	Over temperature reset		135			$^\circ\text{C}$	
I_{gf}	Fault sink current	$V_{IN} = 5\text{ V}; V_{DS} = 13\text{ V}; T_j = T_{jsh}$	10	15	20	mA	
E_{as}	Single pulse avalanche energy	starting $T_j = 25^\circ\text{C}; V_{DD} = 24\text{ V};$ $V_{IN} = 5\text{ V}; R_{gen} = R_{IN\text{ MIN}} = 220\ \Omega;$ $L = 24\text{ mH}$ (see Figure 6 and Figure 8)	100			mJ	

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

3 Protection features

During normal operation, the input pin is electrically connected to the gate of the internal Power MOSFET through a low impedance path.

The device then behaves like a standard Power MOSFET and can be used as a switch from DC up to 50 kHz. The only difference from the user's standpoint is that a small DC current I_{ISS} (typ. 100 μ A) flows into the input pin in order to supply the internal circuitry.

The device integrates:

- Overvoltage clamp protection: internally set at 45 V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.
- Linear current limiter circuit: limits the drain current I_D to I_{lim} whatever the input pin voltages. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the over temperature threshold T_{jsh} .
- Overtemperature and short circuit protection: these are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Overtemperature cutout occurs in the range 150°C to 190°C, a typical value being 170°C. The device is automatically restarted when the chip temperature falls of about 15°C below shutdown temperature.
- Status feedback: in the case of an overtemperature fault condition ($T_j > T_{jsh}$), the device tries to sink a diagnostic current I_{gf} through the input pin in order to indicate fault condition. If driven from a low impedance source, this current may be used in order to warn the control circuit of a device shutdown. If the drive impedance is high enough so that the input pin driver is not able to supply the current I_{gf} , the input pin will fall to 0 V. This will not however affect the device operation: no requirement is put on the current capability of the input pin driver except to be able to supply the normal operation drive current I_{ISS} .

Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL logic circuit.

Figure 4. Switching time test circuit for resistive load

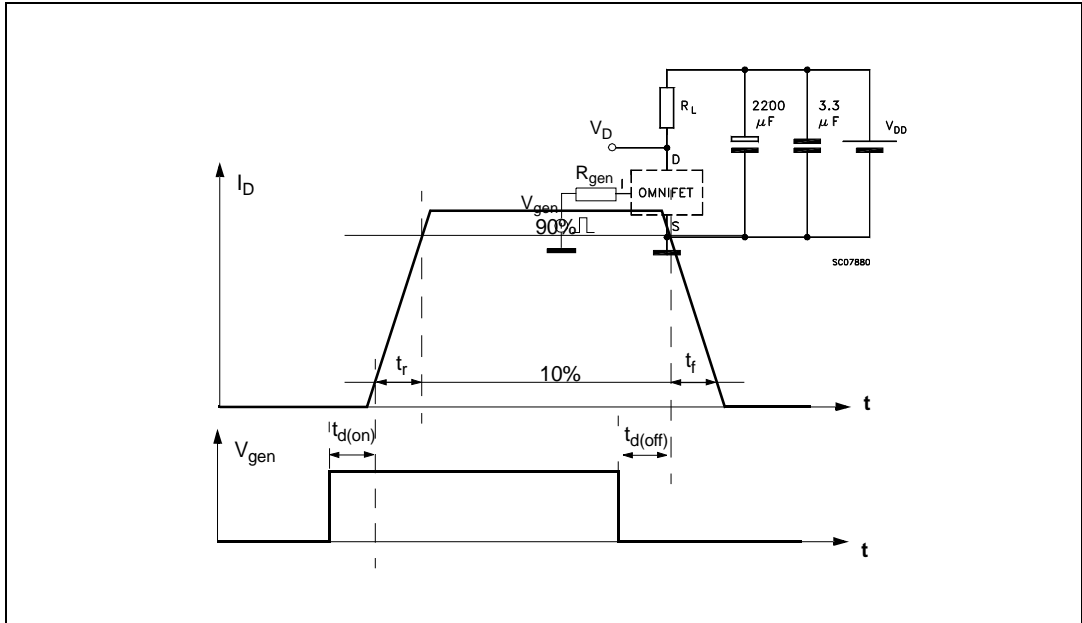


Figure 5. Test circuit for diode recovery times

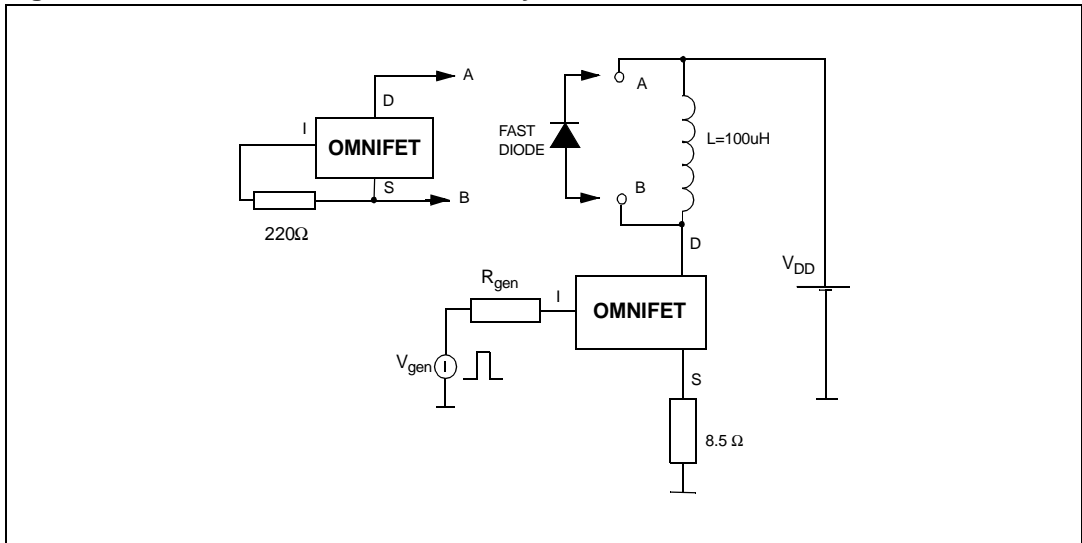


Figure 6. Unclamped inductive load test circuits

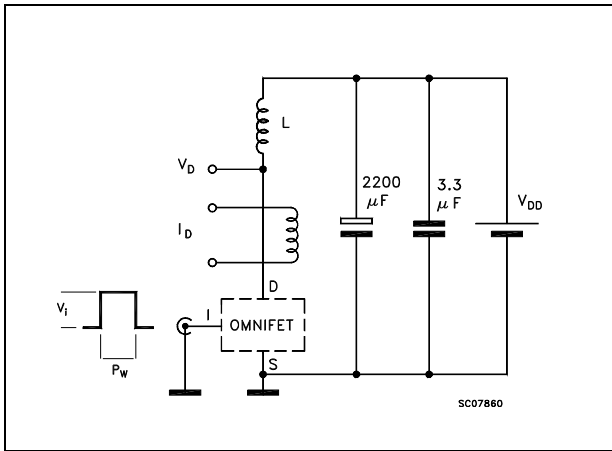


Figure 7. Input charge test circuit

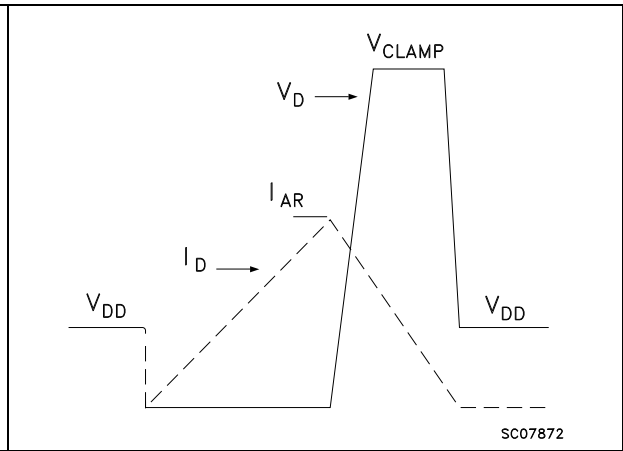
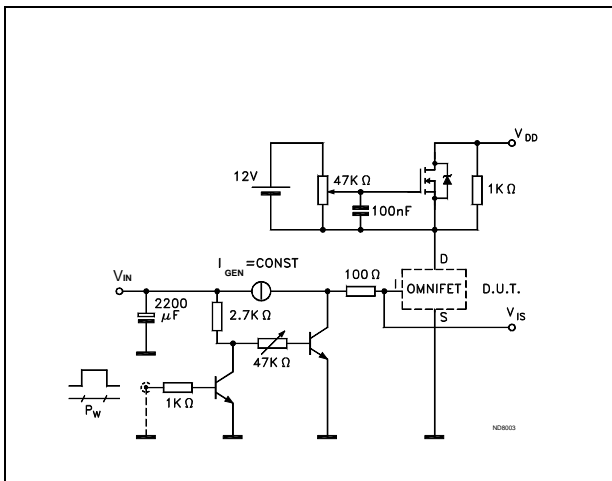


Figure 8. Unclamped inductive waveforms



3.1 Electrical characteristics curves

Figure 9. Thermal impedance for SOT-223

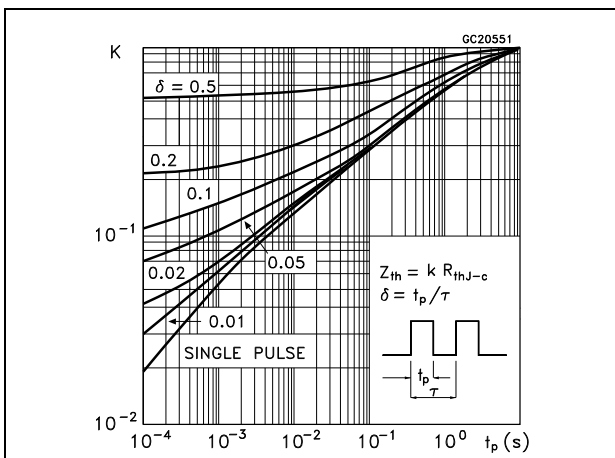


Figure 10. Derating curve

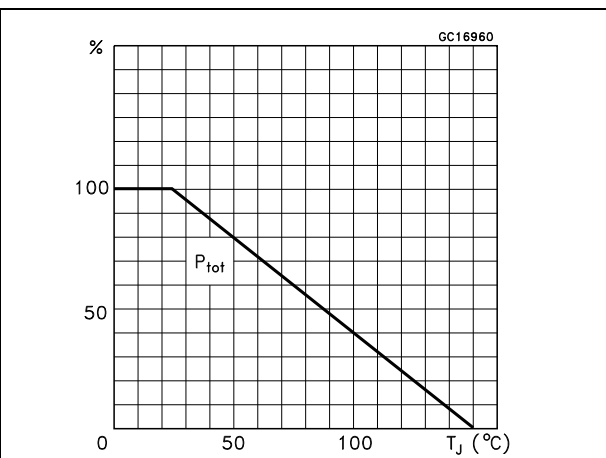


Figure 11. Transconductance

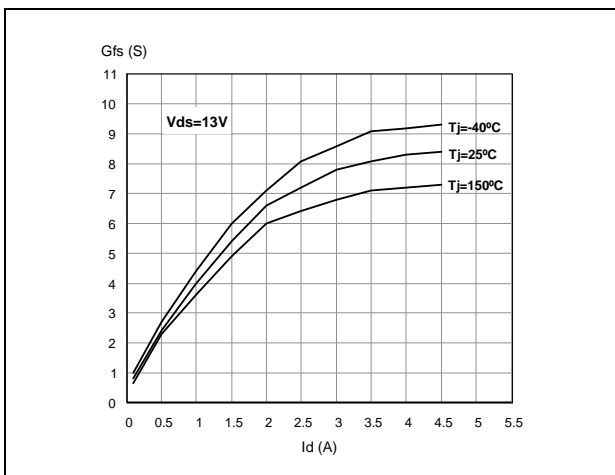


Figure 12. Static drain-source on resistance vs input voltage (part 1/2)

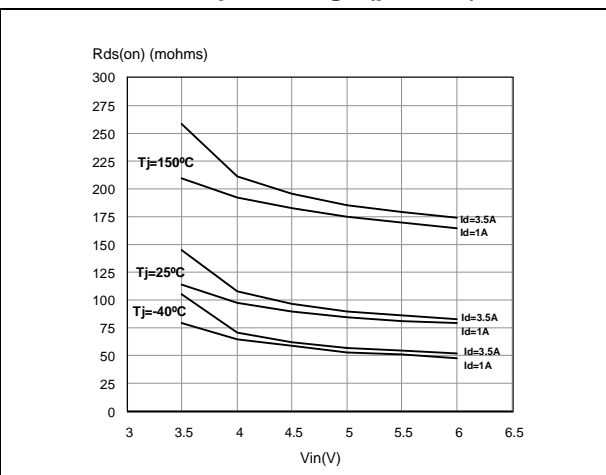


Figure 13. Static drain-source on resistance vs input voltage (part 2/2)

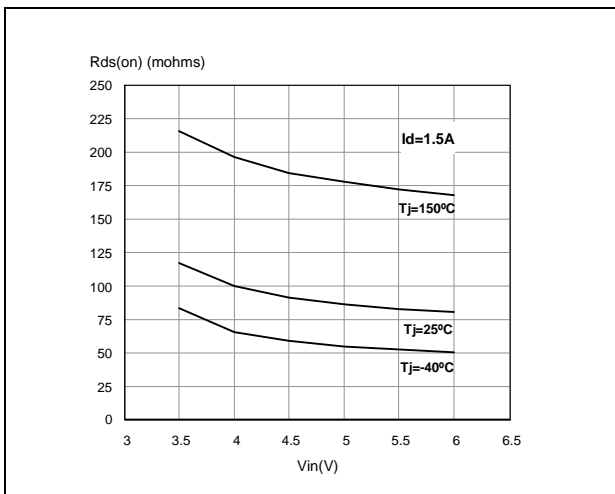


Figure 14. Source-drain diode forward characteristics

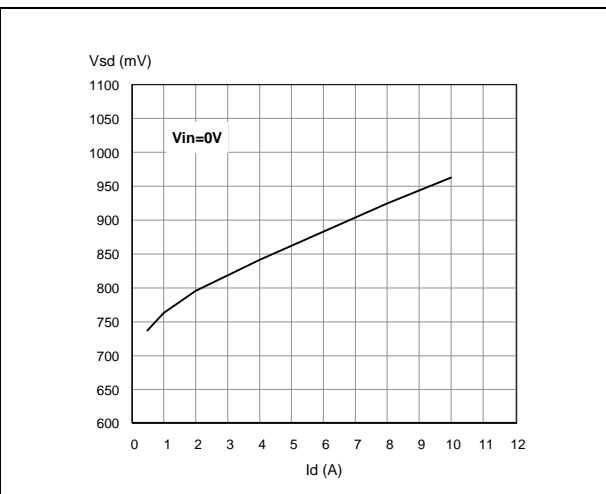


Figure 15. Static drain source on resistance

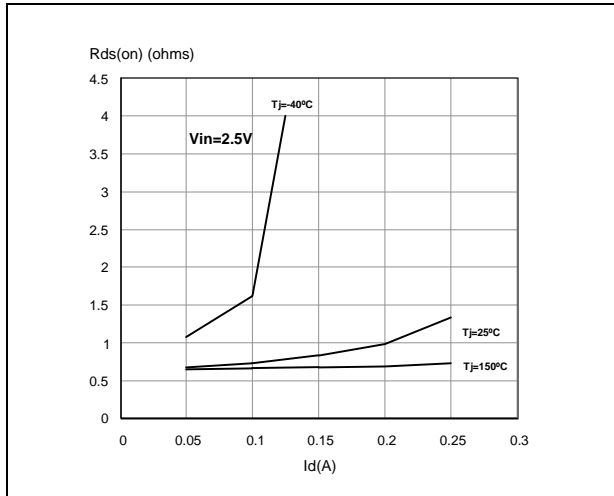


Figure 16. Turn-on current slope (part 1/2)

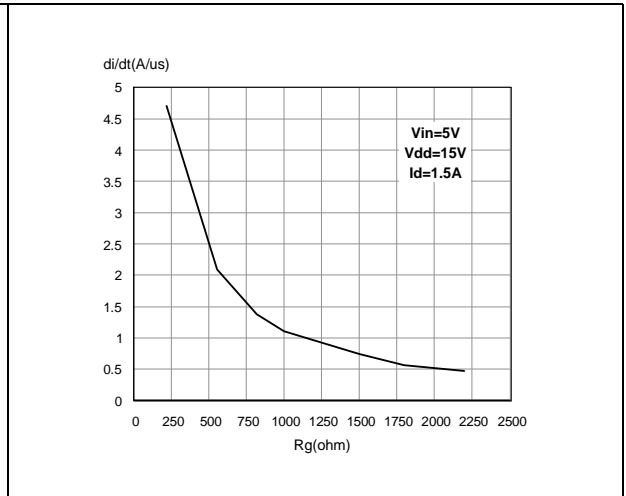


Figure 17. Turn-on current slope (part 2/2)

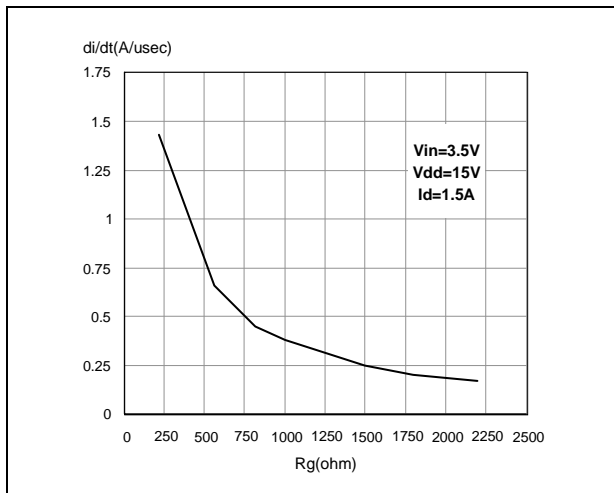


Figure 18. Transfer characteristics

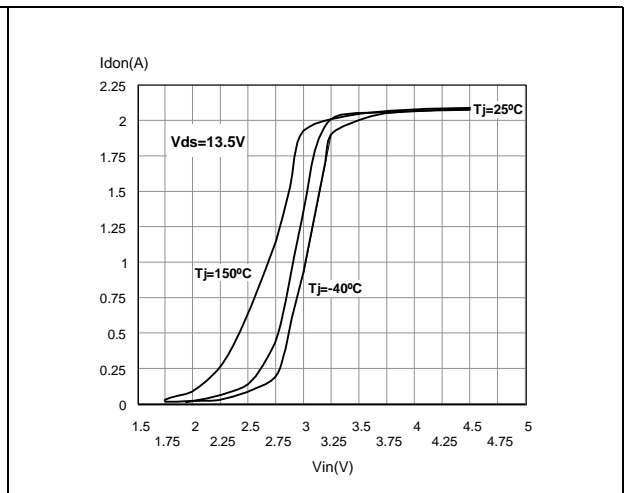


Figure 19. Static drain-source on resistance vs Id

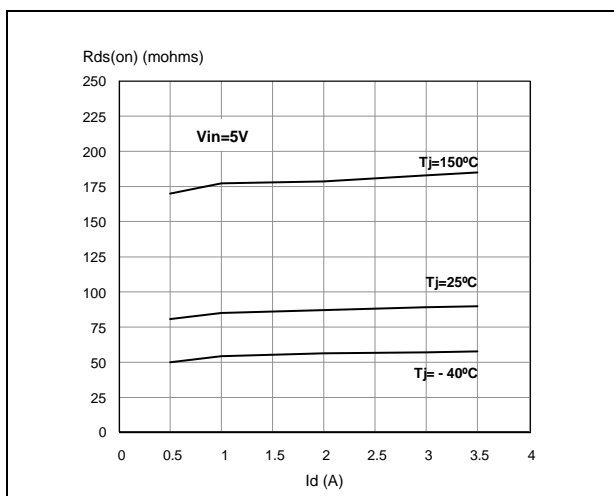


Figure 20. Input voltage vs input charge

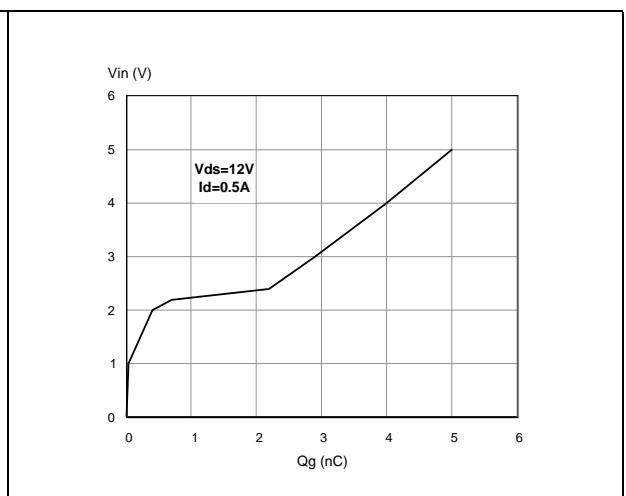


Figure 21. Turn-off drain source voltage slope (part 1/2)

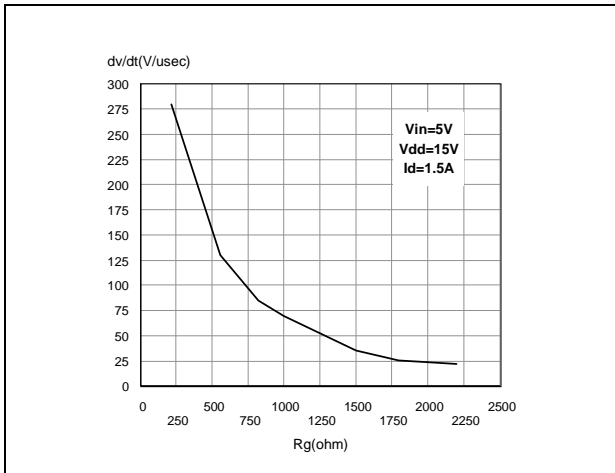


Figure 22. Turn-off drain source voltage slope (part 2/2)

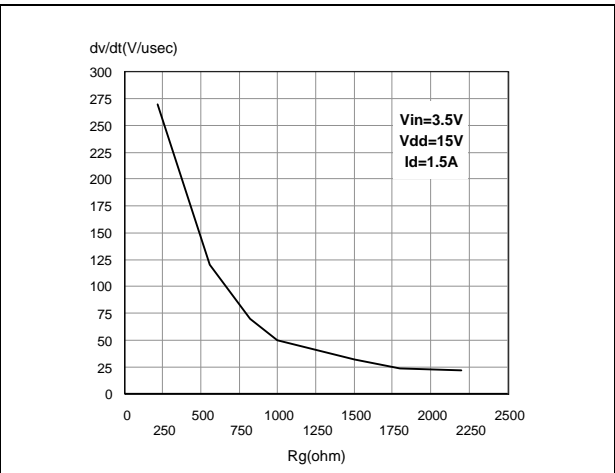


Figure 23. Capacitance variations

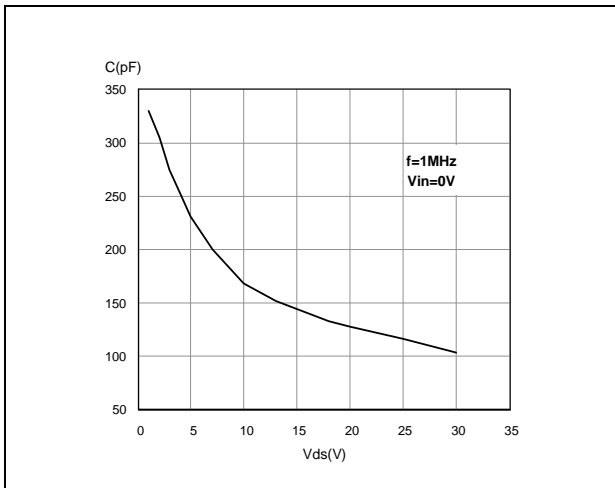


Figure 24. Output characteristics

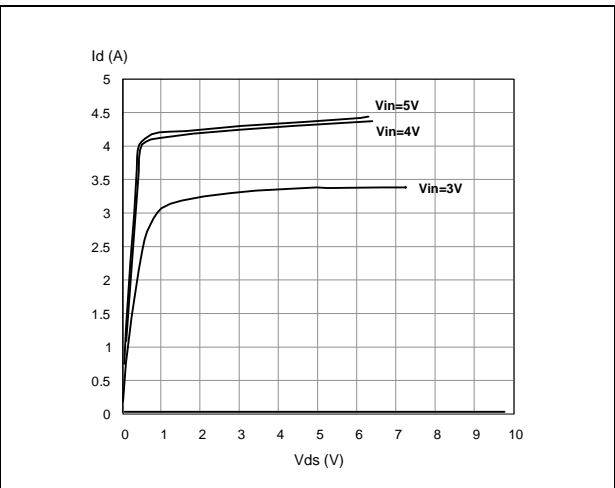


Figure 25. Normalized on resistance vs temperature

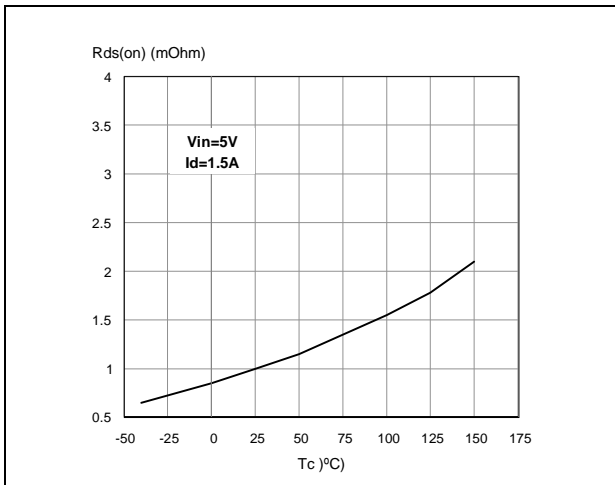


Figure 26. Switching time resistive load (part 1/2)

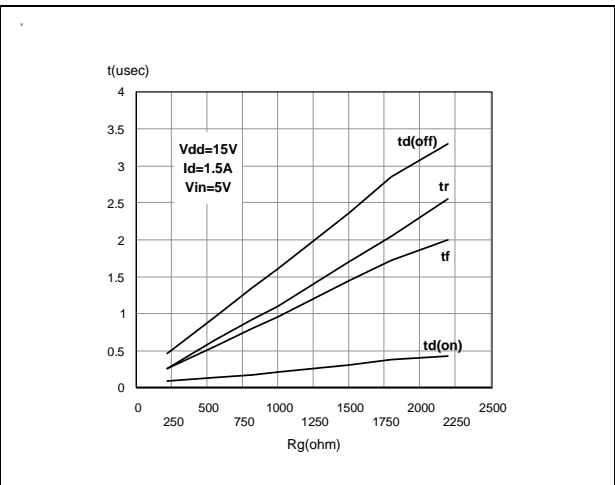


Figure 27. Switching time resistive load (part 2/2)

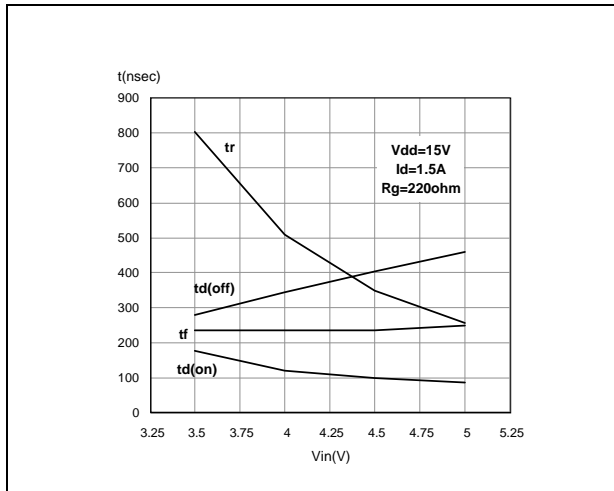


Figure 28. Normalized input threshold voltage vs temperature

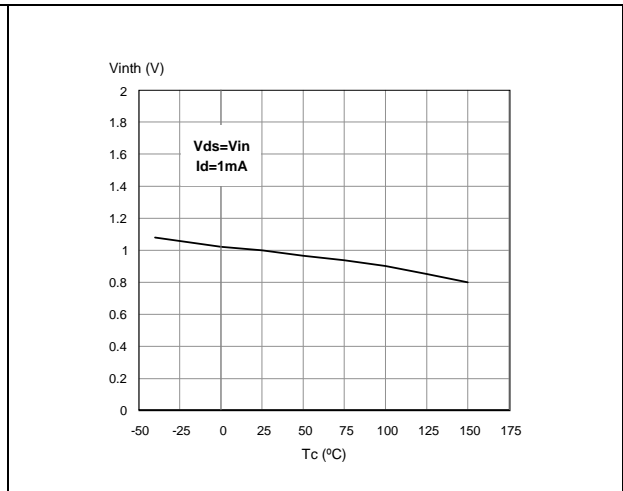


Figure 29. Normalized current limit vs junction temperature

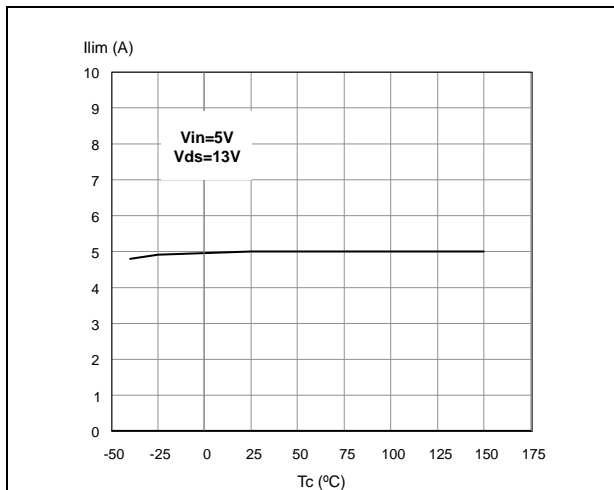
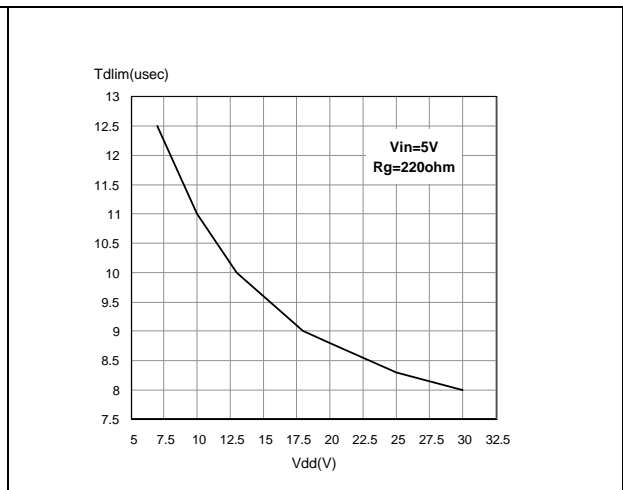


Figure 30. Step response current limit



4 Package and packing information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

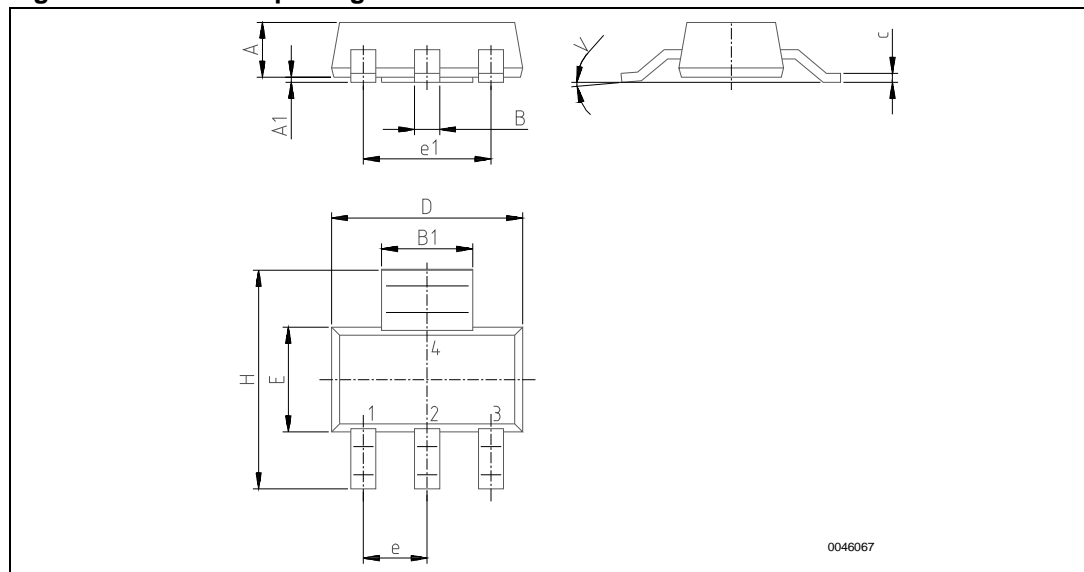
ECOPACK® is an ST trademark.

4.1 SOT-223 mechanical data

Table 5. SOT-223 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A			1.8
B	0.6	0.7	0.85
B1	2.9	3	3.15
c	0.24	0.26	0.35
D	6.3	6.5	6.7
e		2.3	
e1		4.6	
E	3.3	3.5	3.7
H	6.7	7	7.3
V	10 (max)		
A1	0.02		0.1

Figure 31. SOT-223 package dimensions



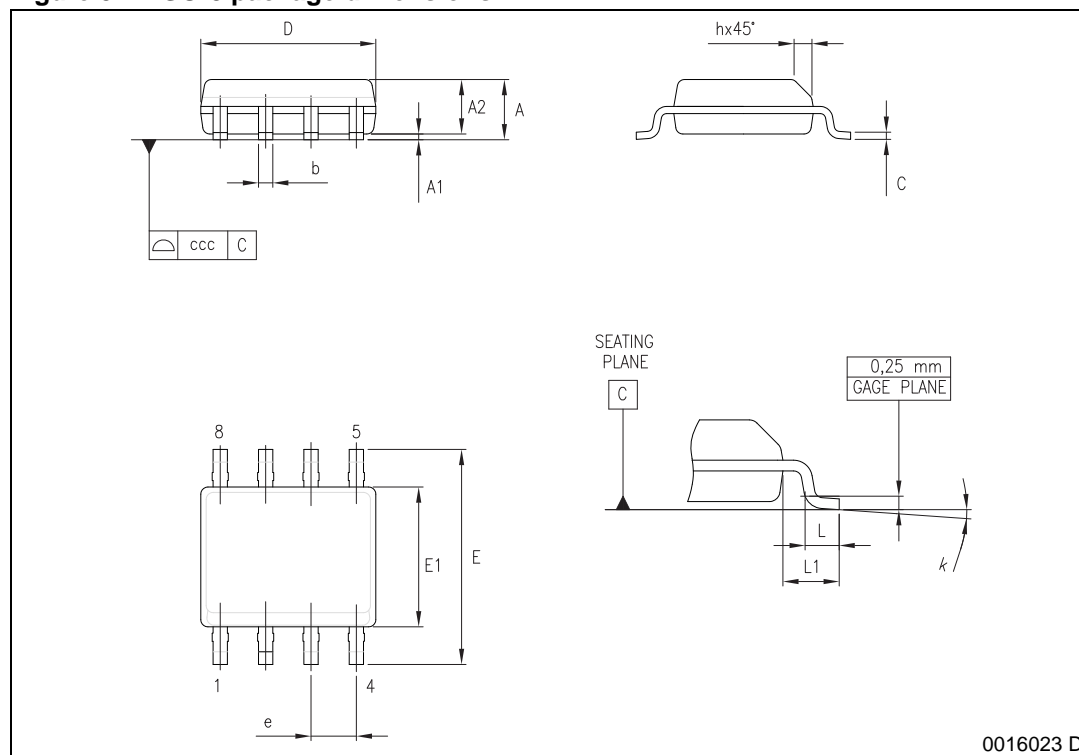
4.2 SO-8 mechanical data

Table 6. SO-8 mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A			1.75
a1	0.1		0.25
a2			1.65
a3	0.65		0.85
b	0.35		0.48
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D ⁽¹⁾	4.80	4.90	5.00
E	5.80	6.00	6.20
E1 ⁽²⁾	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

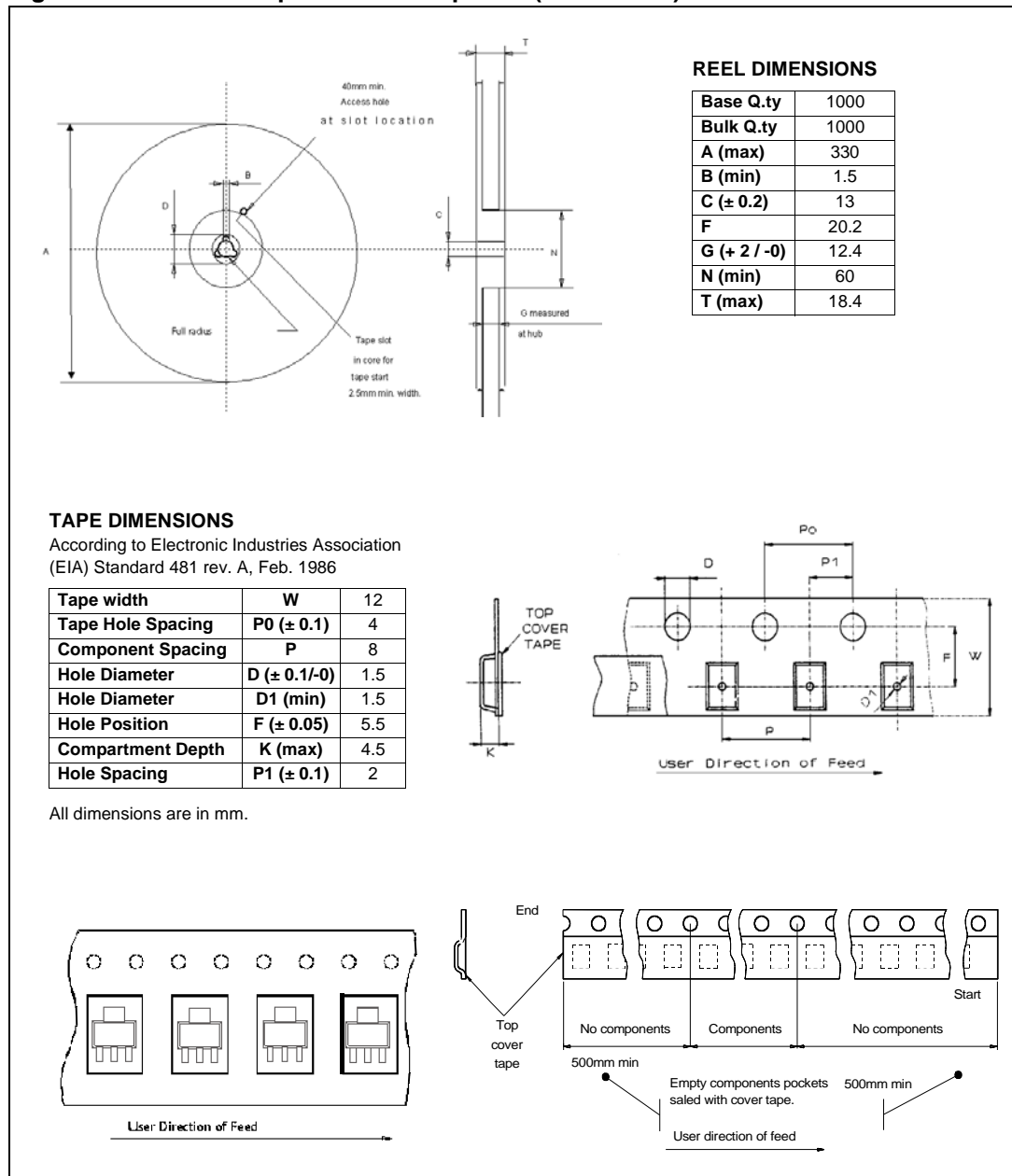
1. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total (both side).
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.

Figure 32. SO-8 package dimensions



4.3 SOT-223 packing information

Figure 33. SOT-223 tape and reel shipment (suffix “TR”)



4.4 SO-8 packing information

Figure 34. SO-8 tube shipment (no suffix)

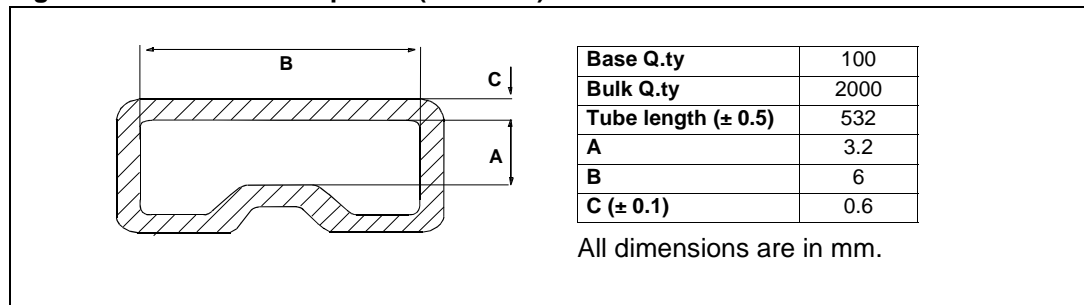
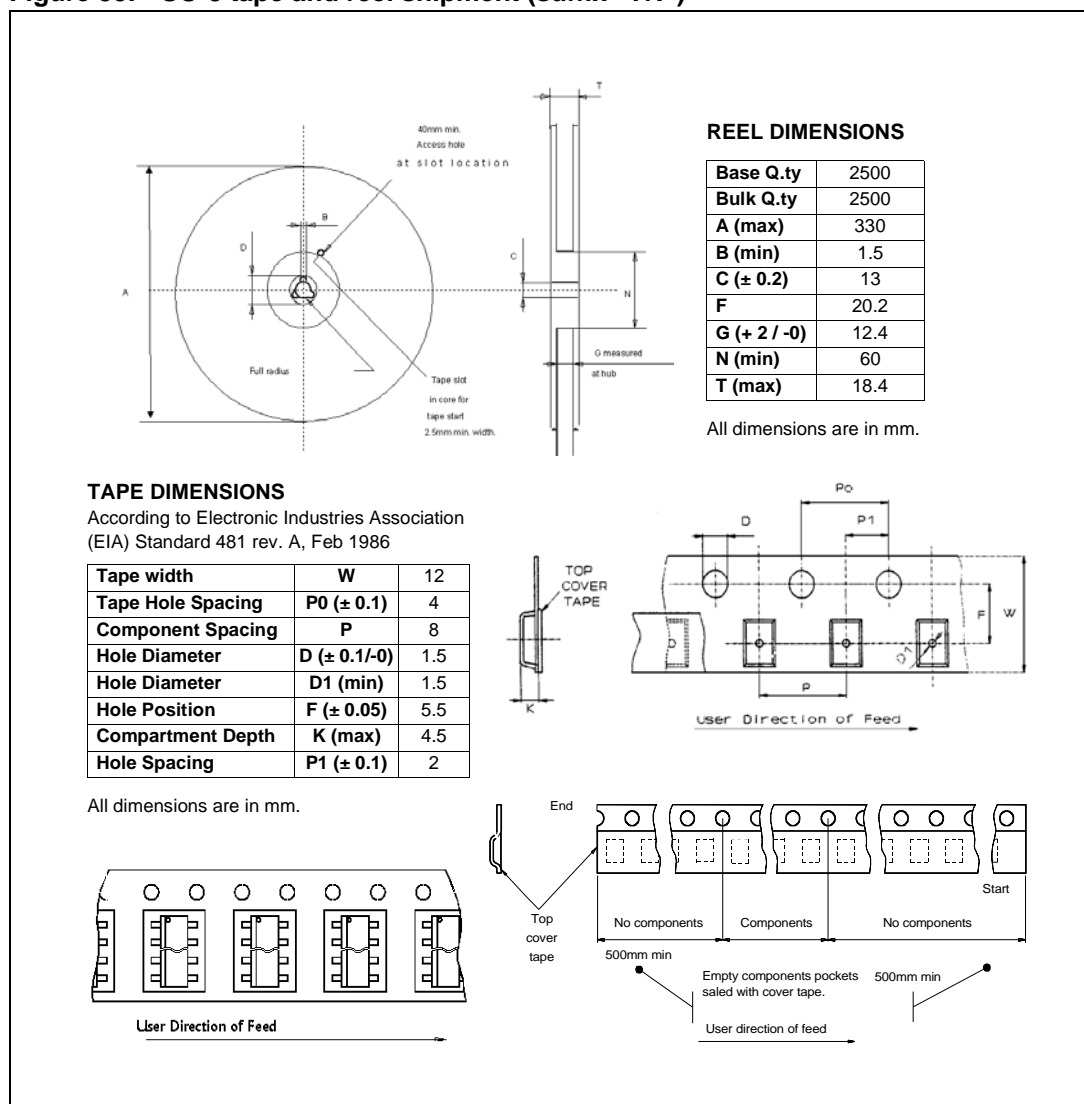


Figure 35. SO-8 tape and reel shipment (suffix "TR")



5 Revision history

Table 7. Document revision history

Date	Revision	Changes
24-May-2009	1	Initial release.
21-Jul-2009	2	Updated Table 1: Device summary .
29-Sep_2009	3	Removed target specification on cover page.
10-May-2012	4	Updated Table 1: Device summary Table 2: Absolute maximum ratings : – R _{IN MIN} : changed unit to Ω (it was W)
18-Sep-2013	5	Updated Disclaimer.

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