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November 2013

FDP150N10A

N-Channel PowerTrench[®] MOSFET 100 V, 50 A, 15 m Ω

Features

- $R_{DS(on)}$ = 12.5 m Ω (Typ.) @ V_{GS} = 10 V, I_D = 50 A
- · Fast Switching Speed
- Low Gate Charge, Q_G = 16.2 nC (Typ.)
- High Performance Trench Technology for Extremely Low $R_{DS(\text{on})}$
- · High Power and Current Handling Capability
- RoHS Compliant

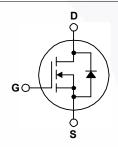
Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- · Motor Drives and Uninterruptible Power Supplies
- · Micro Solar Inverter





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol		Parameter		FDP150N10A_F102	Unit
V _{DSS}	Drain to Source Voltage			100	V
V _{GSS}	Gate to Source Voltage			±20	V
	Drain Current	- Continuous (T _C = 25°C)	50	Α	
ID	Dialii Current	- Continuous (T _C = 100°C)	- Continuous (T _C = 100°C)		
I _{DM}	Drain Current	- Pulsed	(Note 1)	200	Α
E _{AS}	Single Pulsed Avalanche E	Energy	(Note 2)	84.6	mJ
dv/dt	Peak Diode Recovery dv/c	lt	(Note 3)	6.0	V/ns
D	Power Dissipation	(T _C = 25°C)		91	W
P_{D}	Power Dissipation	- Derate Above 25°C		0.61	W/°C
T _J , T _{STG}	Operating and Storage Ter	mperature Range		-55 to +175	°C
T _L	Maximum Lead Temperatu	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds			°C

Thermal Characteristics

Symbol	Parameter FDP150N1		Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	*C/VV

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDP150N10A_F102	FDP150N10A	TO-220	Tube	N/A	N/A	50 units

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	cteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	100	-	-	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	-	0.08	-	V/°C
ı	Zero Gate Voltage Drain Current	V _{DS} = 80 V, V _{GS} = 0 V	-	-	1	
IDSS	Zero Gate voltage Drain Current	$V_{DS} = 80 \text{ V}, T_{C} = 150^{\circ}\text{C}$	-	-	500	μA
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	-	-	±100	nA

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	2.0	-	4.0	V
R _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 50 \text{ A}$	-	12.5	15.0	mΩ
9 _{FS}	Forward Transconductance	V _{DS} = 10 V, I _D = 50 A	-	40	-	S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 50.V.V 0.V	-	1080	1440	pF
C _{oss}	Output Capacitance	V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz		267	355	pF
C _{rss}	Reverse Transfer Capacitance			11	-	pF
C _{oss(er)}	Engry Related Output Capacitance	V _{DS} = 50 V, V _{GS} = 0 V	-	436	-	pF
Q _{g(tot)}	Total Gate Charge at 10V		-	16.2	21.0	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DS} = 50 \text{ V}$, $V_{GS} = 10 \text{ V}$,	-	5.3	-	nC
Q _{gs2}	Gate Charge Threshold to Plateau	I _D = 50 A	-	2.6	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	(Note 4)	-	3.7	-	nC
ESR	Equivalent Series Resistance (G-S)	f = 1 MHz	-	1.3	-	Ω

Switching Characteristics

t _{d(on)}	Turn-On Delay Time		-	13	36	ns
t _r		$V_{DD} = 50 \text{ V}, I_{D} = 50 \text{ A},$	-/	16	42	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_G = 4.7 \Omega$	-	21	52	ns
t _f	Turn-Off Fall Time	(Note 4)	-	5	20	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	50	Α
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	200	Α
V_{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 50 A	-	-	1.3	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, V _{DD} = 50 V, I _{SD} = 50 A,	-	50	-	ns
Q _{rr}	Reverse Recovery Charge dI _F /dt = 100 A/μs		-	55	-	nC

Notes

- ${\it 1. Repetitive\ rating: pulse-width\ limited\ by\ maximum\ junction\ temperature.}$
- 2. L = 2 mH, I_{AS} = 9.2 A, R_{G} = 25 Ω , starting T_{J} = 25°C.
- 3. I $_{SD} \leq$ 100 A, di/dt \leq 200 A/ μ s, V $_{DD} \leq$ BV $_{DSS}$, starting T $_{J}$ = 25°C.
- ${\it 4. Essentially independent of operating temperature typical characteristics.}\\$

Typical Performance Characteristics

Figure 1. On-Region Characteristics

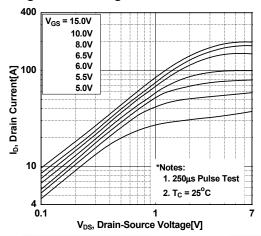


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

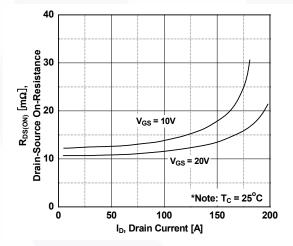


Figure 5. Capacitance Characteristics

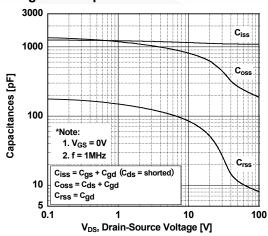


Figure 2. Transfer Characteristics

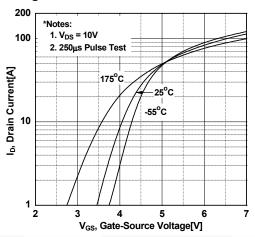


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

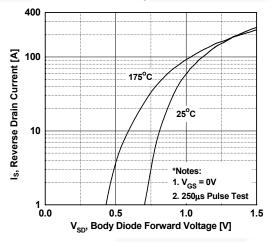
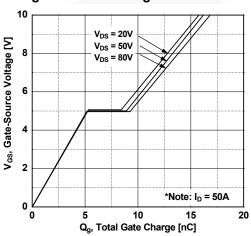


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

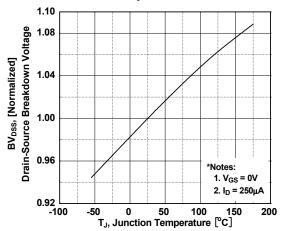


Figure 8. On-Resistance Variation vs. Temperature

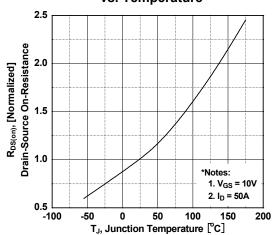


Figure 9. Maximum Safe Operating Area

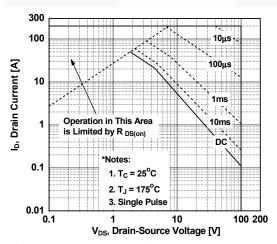


Figure 10. Maximum Drain Current vs. Case Temperature

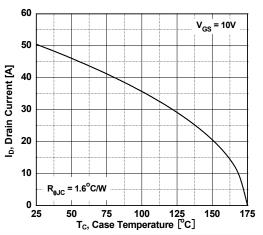


Figure 11. Eoss vs. Drain to Source Voltage

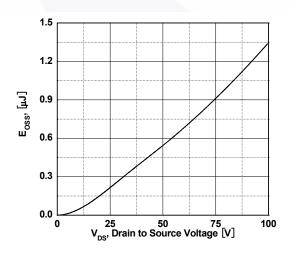
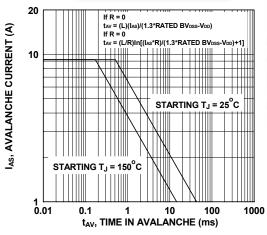
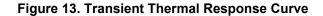
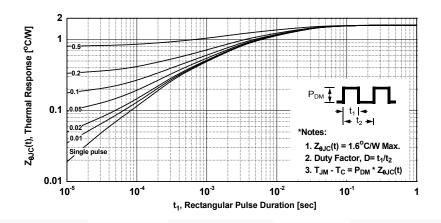


Figure 12. Unclamped Inductive Switching Capability



Typical Performance Characteristics (Continued)





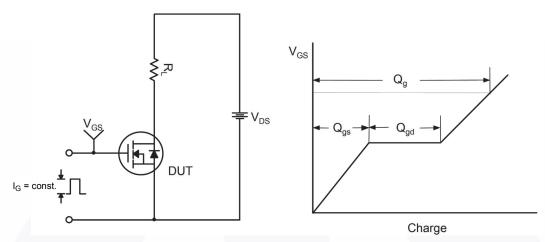


Figure 14. Gate Charge Test Circuit & Waveform



Figure 15. Resistive Switching Test Circuit & Waveforms

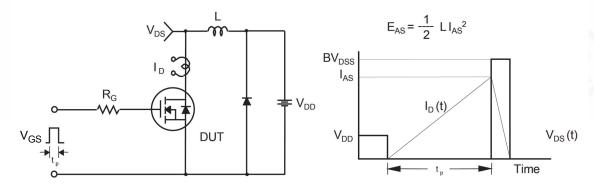


Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms

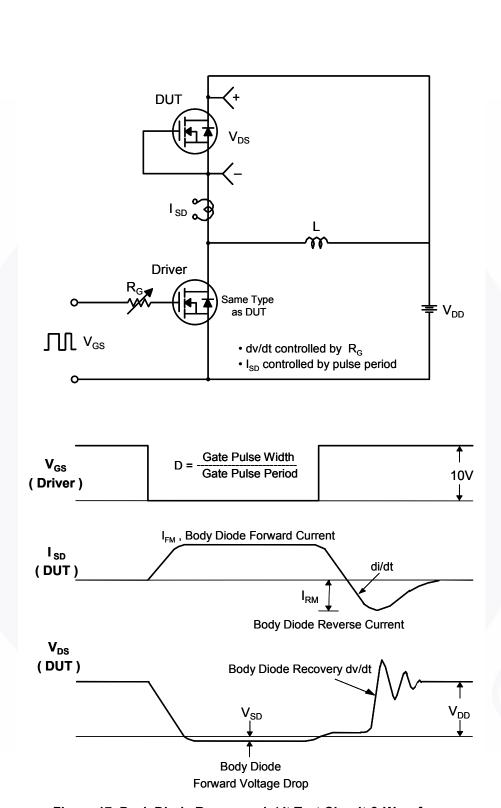


Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

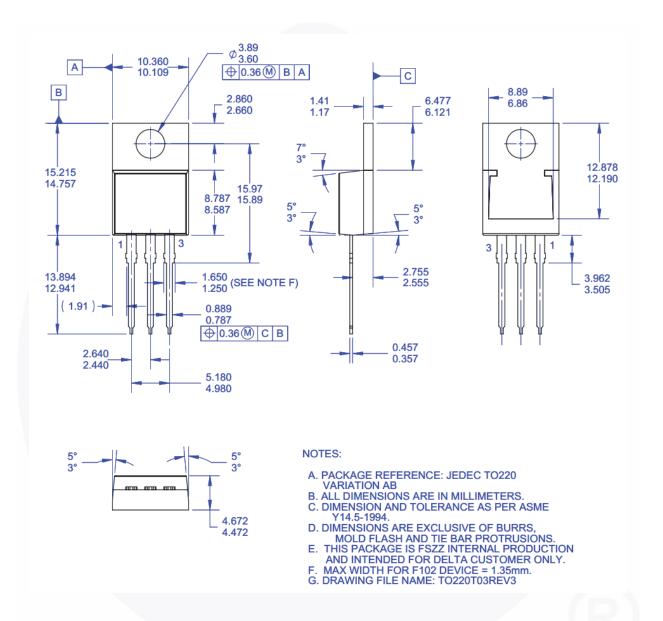


Figure 18. TO-220, Molded, 3-Lead, Jedec Variation AB (Delta)

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