INTEGRATED CIRCUITS

DATA SHEET

UBA2070
600 V CCFL ballast driver IC

Product specification
Supersedes data of 2001 Sep 27

2002 Oct 24

Philips Semiconductors

PHILIPS

FEATURES

- Current controlled operation
- Adaptive non-overlap time control
- Integrated high voltage level shift function
- Power-down function
- Protected against lamp failures or lamp removal
- Capacitive mode protection.

APPLICATION

- The circuit topology enables a broad range of backlight inverters.

GENERAL DESCRIPTION

The UBA2070 is a high voltage integrated circuit for driving electronically ballasted Cold Cathode Fluorescent Lamps (CCFL) at mains voltages up to 277 V (RMS) (nominal value). The circuit is made in a 650 V Bipolar CMOS DMOS (BCD) power logic process. The UBA2070 provides the drive function for the two discrete MOSFETs. Besides the drive function the UBA2070 also includes the level-shift circuit, the oscillator function, a lamp voltage monitor, a current control function, a timer function and protections.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UBA2070T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
UBA2070P	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
High voltage supply						
V_{hs}	high side supply voltage	I_{hs} < 30 μA; t < 1 s	–	–	600	V
Start-up state						
$V_{DD(high)}$	oscillator start voltage		12.4	13	13.6	V
$V_{DD(low)}$	oscillator stop voltage		8.6	9.1	9.6	V
$I_{DD(start)}$	start-up current	$V_{DD} < V_{DD(high)}$	–	170	200	μA
Reference voltage (pin V_{REF})						
V_{ref}	reference voltage	I_L = 10 μA	2.86	2.95	3.04	V
Voltage controlled oscillator						
$f_{bridge(max)}$	maximum bridge frequency		90	100	110	kHz
$f_{bridge(min)}$	minimum bridge frequency		38.9	40.5	42.1	kHz
Output drivers (pins GH and GL)						
I_{source}	source current	$V_{GH} - V_{SH} = 0$; $V_{GL} = 0$	135	180	235	mA
I_{sink}	sink current	$V_{GH} - V_{SH}$ = 13 V; V_{GL} = 13 V	265	300	415	mA
Lamp voltage sensor (pin LVS)						
$V_{LVS(fail)}$	fail voltage level		1.19	1.25	1.31	V
$V_{LVS(max)}$	maximum voltage level		1.67	1.76	1.85	V
Average current sensor (pin CS)						
V_{offset}	offset voltage	V_{CS} = 0 to 2.5 V	–2	0	+2	mV
g_m	transconductance	f = 1 kHz	100	200	400	μA/mV
Ignition timer (pin CT)						
V_{OL}	LOW-level output voltage		–	1.4	–	V
V_{OH}	HIGH-level output voltage		–	3.6	–	V

BLOCK DIAGRAM

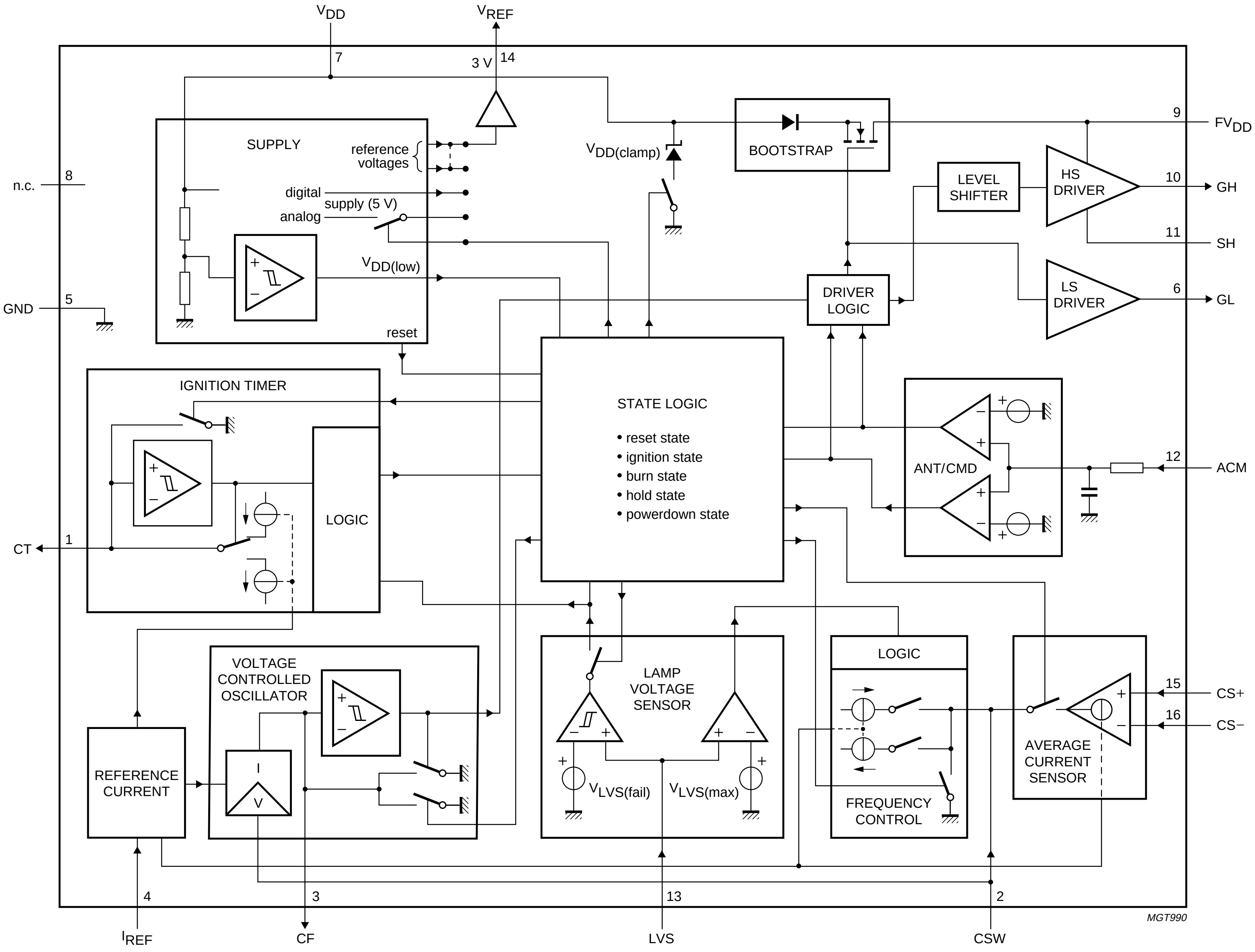


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CT	1	ignition timer output
CSW	2	voltage controlled oscillator input
CF	3	voltage controlled oscillator output
I_{REF}	4	internal reference current input
GND	5	ground
GL	6	gate of the low side switch output
V_{DD}	7	low voltage supply
n.c.	8	not connected
FV_{DD}	9	floating supply; supply for the high side switch
GH	10	gate of the high side switch output
SH	11	source of the high side switch
ACM	12	capacitive mode input
LVS	13	lamp voltage sensor input
V_{REF}	14	reference voltage output
CS+	15	average current sensor positive input
CS–	16	average current sensor negative input

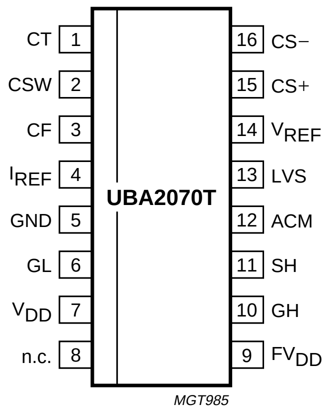


Fig.2 Pin configuration (SO16).

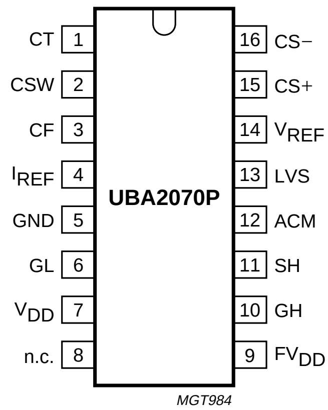


Fig.3 Pin configuration (DIP16).

FUNCTIONAL DESCRIPTION

Start-up state

Initial start-up can be achieved by charging C_{VDD} using an external start-up resistor. The start-up of the circuit is such, that the MOSFETs T_{ls} and T_{hs} shall be non-conductive. The circuit will be reset in the start-up state. If the V_{DD} supply reaches the value of $V_{DD(high)}$ the circuit starts oscillating. A DC reset circuit is incorporated in the high side (hs) driver. Below the lockout voltage at pin FV_{DD} the output voltage ($V_{GH} - V_{SH}$) is zero. The voltages at pins CF and CT are zero during the start-up state.

Oscillation

The internal oscillator is a Voltage Controlled Oscillator circuit (VCO) which generates a sawtooth waveform between the high level at pin CF and 0 V (see Fig.4). The frequency of the sawtooth is determined by C_{CF}, R_{IREF} and the voltage at pin CSW. The minimum and maximum frequencies are determined by C_{CF} and R_{IREF}. The minimum to maximum ratio is fixed internally. The sawtooth frequency is twice the half bridge frequency. The IC brings the MOSFETs T_{hs} and T_{ls} alternately into conduction with a duty factor of 50%.The oscillator starts oscillating at f_{max}. During the first switching cycle the MOSFET T_{ls} is switched on. To charge the bootstrap capacitor the first conduction time after the start-up state is made extra long. In all other cases the duty factor at the start is 50%.

Non-overlap time

The non-overlap time is realized with an Adaptive Non-Overlap circuit (ANT). By using this circuit, the application determines the duration of the non-overlap time (determined by the slope of the half bridge voltage and detected by the signal across R_{ACM}) and makes the non-overlap time optimum for each frequency (see Fig.4). The minimum non-overlap time is internally fixed. The maximum non-overlap time is internally fixed at approximately 25% of the bridge period time.

Timing circuit

A timing circuit is included (a clock generator) to determine the maximum ignition time. The ignition time is defined as 1 pulse at pin CT; the lamp has to ignite within the duration of this pulse. The timer circuit starts operating when a critical value of the lamp voltage [$V_{LVS(fail)}$] is exceeded. When the timer is not operating the capacitor at pin CT is discharged by 1 mA to 0 V.

Ignition state

After the start at f_{max} the frequency will decrease due to charging the capacitor at pin CSW with an internally fixed current. During this continuous decrease in frequency, the circuit approaches the resonant frequency of the lamp. This will cause a high voltage across the lamp, which ignites the lamp. The ignition voltage of the lamp is designed to be above the $V_{LVS(fail)}$ level. If the lamp voltage exceeds this voltage level the ignition timer is started (see Fig.5).

Burn state

If the lamp voltage does not exceed the $V_{LVS(max)}$ level the voltage at pin CSW will continue to increase until the clamp level at pin CSW is reached. As a consequence the frequency will decrease until the minimum frequency is reached. When the frequency reaches its minimum level it is assumed that the lamp has ignited, the circuit will enter the burn state and the Average Current Sensor (ACS) circuit will be enabled (see Fig.5). As soon as the average voltage across R_{sense} (measured at pin CS–) reaches the reference level at pin CS+, the average current sensor circuit will take over the control of the lamp current. The average current through R_{sense} is transferred to a voltage at the voltage controlled oscillator to regulate the frequency and, as a result, the lamp current.

Lamp failure

DURING IGNITION STATE

If the lamp fails to ignite, the voltage level increases. When the lamp voltage exceeds the $V_{LVS(max)}$ level, the voltage will be regulated at that level. The ignition timer is started when the $V_{LVS(fail)}$ level is exceeded. If the voltage at pin LVS is above the $V_{LVS(fail)}$ level at the end of the ignition time the circuit stops oscillation and is forced into a Power-down state (see Fig.6). This state is terminated by switching off the V_{DD} supply.

DURING BURN STATE

If the lamp fails during normal operation, the voltage across the lamp will increase and the lamp voltage will exceed the $V_{LVS(fail)}$ level. This forces the circuit to re-enter the ignition state and results in an attempt to re-ignite the lamp. If during restart the lamp still fails, the voltage remains high until the end of the ignition time. At the end of the ignition time the circuit stops oscillating and enters the Power-down state (see Fig.7).

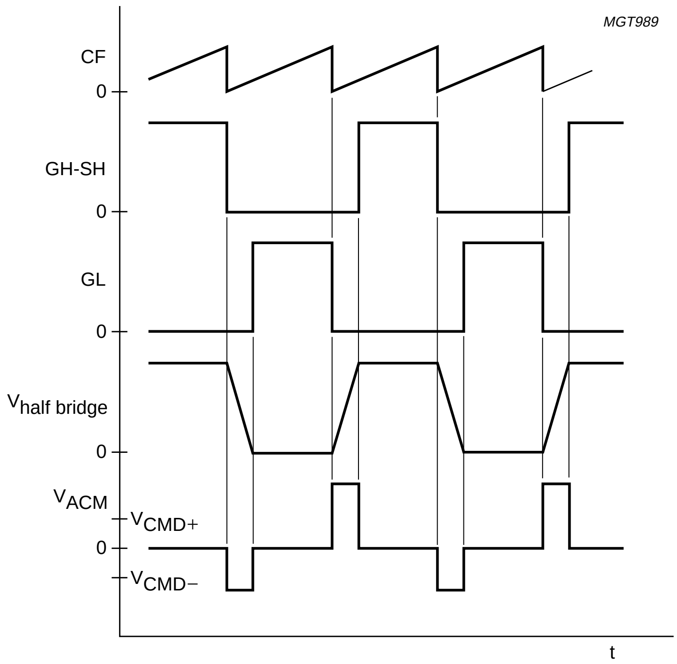


Fig.4 Oscillator and driver timing.

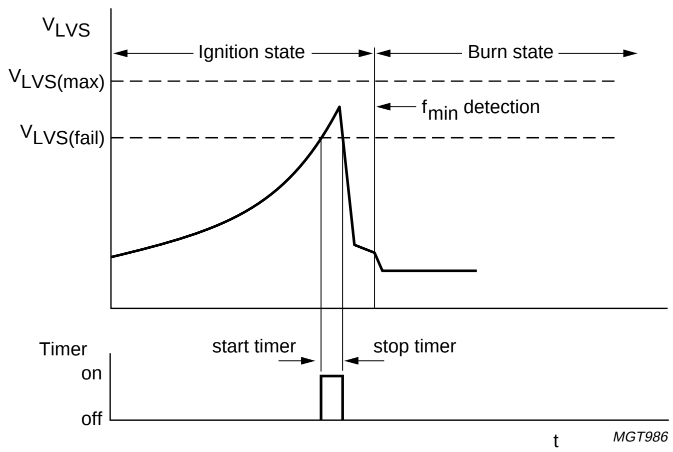


Fig.5 Normal ignition behaviour.

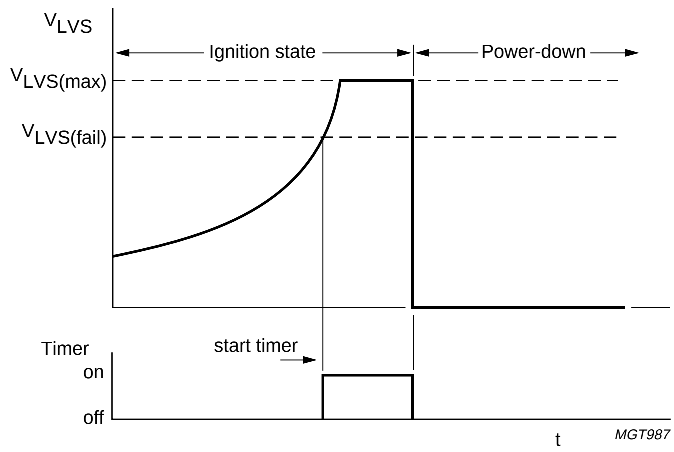


Fig.6 Lamp failure during ignition state.

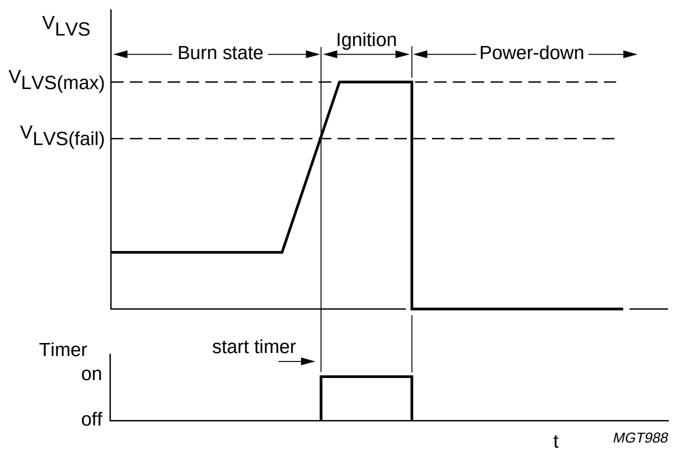


Fig.7 Lamp failure during burn state.

Power-down state

The Power-down state will be entered if, at the end of the ignition time, the voltage at pin LVS is above $V_{LVS(fail)}$. In the Power-down state the oscillation will be stopped and MOSFETs T_{hs} and T_{ls} will be non-conductive. The V_{DD} supply is internally clamped. The circuit is released from the Power-down state by reducing the supply voltage to below $V_{DD(reset)}$.

Capacitive mode protection

The signal across R_{ACM} also gives information about the switching behaviour of the half bridge. If the voltage at R_{ACM} does not exceed the V_{CMD} level during the non-overlap time (see Fig.4), the Capacitive Mode Detection (CMD) circuit assumes that the circuit is in capacitive mode of operation. Consequently the frequency will be directly increased to f_{max}. In this event the frequency behaviour is decoupled from the voltage at pin CSW until the voltage is discharged to zero. An internal filter of 30 ns is included at pin ACM to increase the noise immunity.

Charge coupling

Due to parasitic capacitive coupling to the high voltage circuitry all pins are charged with a repetitive charge injection. Given the typical application the pins I_{REF} and CF are sensitive to this charge injection. For charge coupling of ±8 pC, a safe functional operation of the IC is guaranteed, independent of the current level.

Charge coupling at current levels below 50 μA will not interfere with the accuracy of the V_{CS} and V_{ACM} levels.

Charge coupling at current levels below 20 μA will not interfere with the accuracy of any parameter.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); all voltages referenced to ground.

SYMBOL	PARAMETER	CONDITION	MIN.	MAX.	UNIT
V_{hs}	high side supply voltage	I_{hs} < 30 μA; t < 1 s	–	600	V
		I_{hs} < 30 μA	–	510	V
V_{ACM}	voltage on pin ACM		–5	+5	V
V_{LVS}	voltage on pin LVS		0	5	V
V_{CS+}	voltage on pin CS+		0	5	V
V_{CS-}	voltage on pin CS–		–0.3	+5	V
V_{CSW}	voltage on pin CSW		0	5	V
T_{amb}	ambient temperature		–25	+80	°C
T_j	junction temperature		–25	+150	°C
T_{stg}	storage temperature		–55	+150	°C
V_{esd}	electrostatic discharge voltage	note 1			
	pins FV_{DD}, GH, SH and V_{DD}		–1000	+1000	V
	pins GL, ACM, CS+, CS–, CSW, LVS, CF, I_{REF}, CT and V_{REF}		–2500	+2500	V

Note

1. In accordance with the human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	DESCRIPTION	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
	SO16		100	K/W
	DIP16		60	K/W
$R_{th(j-t)}$	thermal resistance from junction to tie-point			
	SO16		50	K/W
	DIP16		30	K/W

QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611D"*.

CHARACTERISTICS

V_{DD} = 13 V, $V_{FVDD} - V_{SH}$ = 13 V; T_{amb} = 25 °C; all voltages referenced to ground; see Fig.8; unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
High voltage supply						
I_L	leakage current on high voltage pins	voltage at pins FV_{DD}, GH and SH = 600 V	–	–	30	µA
Start-up state (pin V_{DD})						
V_{DD}	supply voltage for defined driver output	T_{hs} = off; T_{ls} = off	–	–	6	V
$V_{DD(high)}$	oscillator start voltage		12.4	13	13.6	V
$V_{DD(low)}$	oscillator stop voltage		8.6	9.1	9.6	V
$V_{DD(hys)}$	start-stop hysteresis voltage		3.5	3.9	4.4	V
$I_{DD(start)}$	start-up current	$V_{DD} < V_{DD(high)}$	–	170	200	µA
$V_{DD(clamp)}$	clamp voltage	Power-down mode	10	11	12	V
$I_{DD(pd)}$	Power-down current	V_{DD} = 9 V	–	170	200	µA
$V_{DD(reset)}$	reset voltage	T_{hs} = off; T_{ls} = off	4.5	5.5	7	V
I_{DD}	operating supply current	f_{bridge} = 40 kHz without gate drive	–	1.5	2.2	mA
Reference voltage (pin V_{REF})						
V_{ref}	reference voltage	I_L = 10 µA	2.86	2.95	3.04	V
I_{ref}	reference current	source	1	–	–	mA
		sink	1	–	–	mA
Z_o	output impedance	I_L = 1 mA source	–	3	–	Ω
$\Delta V_{ref}/\Delta T$	temperature coefficient of V_{ref}	I_L = 10 µA; T_{amb} = 25 to 150 °C	–	–0.64	–	%/K
Current supply (pin I_{REF})						
V_I	input voltage		–	2.5	–	V
I_I	input current		65	–	95	µA

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Voltage controlled oscillator						
t_{start}	first output oscillator stroke	after start-up state only	–	50	–	μs
$f_{bridge(max)}$	maximum bridge frequency		90	100	110	kHz
$f_{bridge(min)}$	minimum bridge frequency		38.9	40.5	42.1	kHz
Δf_{stab}	frequency stability	T_{amb} = –20 to +80 °C	–	1.3	–	%
$t_{no(min)}$	minimum non-overlap time	GH to GL	0.68	0.90	1.13	μs
		GL to GH	0.75	1	1.25	μs
$t_{no(max)}$	maximum non-overlap time	at f_{bridge} = 40 kHz; note 1	–	6.7	–	μs
PIN CSW						
V_i	input voltage		2.7	3	3.3	V
V_{clamp}	clamp voltage	burn state	2.8	3.1	3.4	V
PIN CF						
I_{start}	start current	V_{CF} = 1.5 V	3.8	4.5	5.2	μA
I_{min}	minimum current	V_{CF} = 1.5 V	–	21	–	μA
I_{max}	maximum current	V_{CF} = 1.5 V	–	54	–	μA
V_{OH}	HIGH-level output voltage	f = f_{min}	–	2.5	–	V
Output drivers						
V_{boot}	bootstrap diode forward drop	I = 5 mA	1.3	1.7	2.1	V
V_{FVDD}	lockout voltage on pin FV_{DD}		2.8	3.5	4.2	V
I_{FVDD}	floating well supply current on pin FV_{DD}	DC level at $V_{GH} - V_{SH}$ = 13 V	–	35	–	μA
PINS GH AND GL						
I_{source}	source current	$V_{GH} - V_{SH}$ = 0; V_{GL} = 0	135	180	235	mA
I_{sink}	sink current	$V_{GH} - V_{SH}$ = 13 V; V_{GL} = 13 V	265	300	415	mA
V_{OH}	HIGH-level output voltage	I_o = 10 mA	12.5	–	–	V
V_{OL}	LOW-level output voltage	I_o = 10 mA	–	–	0.5	V
HIGH SIDE AND LOW SIDE						
R_{on}	on resistance	I_o = 10 mA	32	39	45	Ω
R_{off}	off resistance	I_o = 10 mA	16	21	26	Ω
Adaptive non-overlap timing and capacitive mode detection (pin ACM)						
I_i	input current	V_{ACM} = 1.25 V	–	–	1	μA
V_{det}	capacitive mode detection voltage	positive	80	100	120	mV
		negative	–68	–85	–102	mV

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Lamp voltage sensor (pin LVS)						
I_i	input current	V_{LVS} = 1.25 V	–	–	1	µA
$V_{LVS(fail)}$	fail voltage		1.19	1.25	1.31	V
$V_{LVS(fail)(hys)}$	fail voltage hysteresis		112	140	168	mV
$\Delta V_{LVS(fail)(hys)}/\Delta T$	temperature coefficient hysteresis		–	0.65	–	mV/K
$V_{LVS(max)}$	maximum voltage		1.67	1.76	1.85	V
$I_{o(sink)}$	output sink current	V_{CSW} = 2 V	2.8	3.2	3.6	µA
$I_{o(source)(ign)}$	ignition output source current	V_{CSW} = 2 V	9.0	10	11	µA
Average current sensor (pins CS+ and CS–)						
I_i	input current	V_{CS} = 0 V	–	–	1	µA
V_{offset}	offset voltage	V_{CS} = 0 to 2.5 V	–2	0	+2	mV
$I_{o(source)}$	output source current	V_{CSW} = 2.0 V	9.0	10	11	µA
$I_{o(sink)}$	output sink current	V_{CSW} = 2.0 V	9.0	10	11	µA
g_m	transconductance	f = 1 kHz	100	200	400	µA/mV
Ignition timer (pin CT)						
I_o	output current	V_{CT} = 2.5 V	5.5	5.9	6.3	µA
V_{OL}	LOW-level output voltage		–	1.4	–	V
V_{OH}	HIGH-level output voltage		–	3.6	–	V
V_{hys}	output hysteresis		2.05	2.20	2.35	V
t_{ign}	ignition time		–	0.257	–	s

Note

1. The maximum non-overlap time is determined by the level of the CF signal. If this signal exceeds a level of 1.25 V the non-overlap will end. This equals a maximum non-overlap time of 6.7 µs at a bridge frequency of 40 kHz.

APPLICATION AND TEST INFORMATION

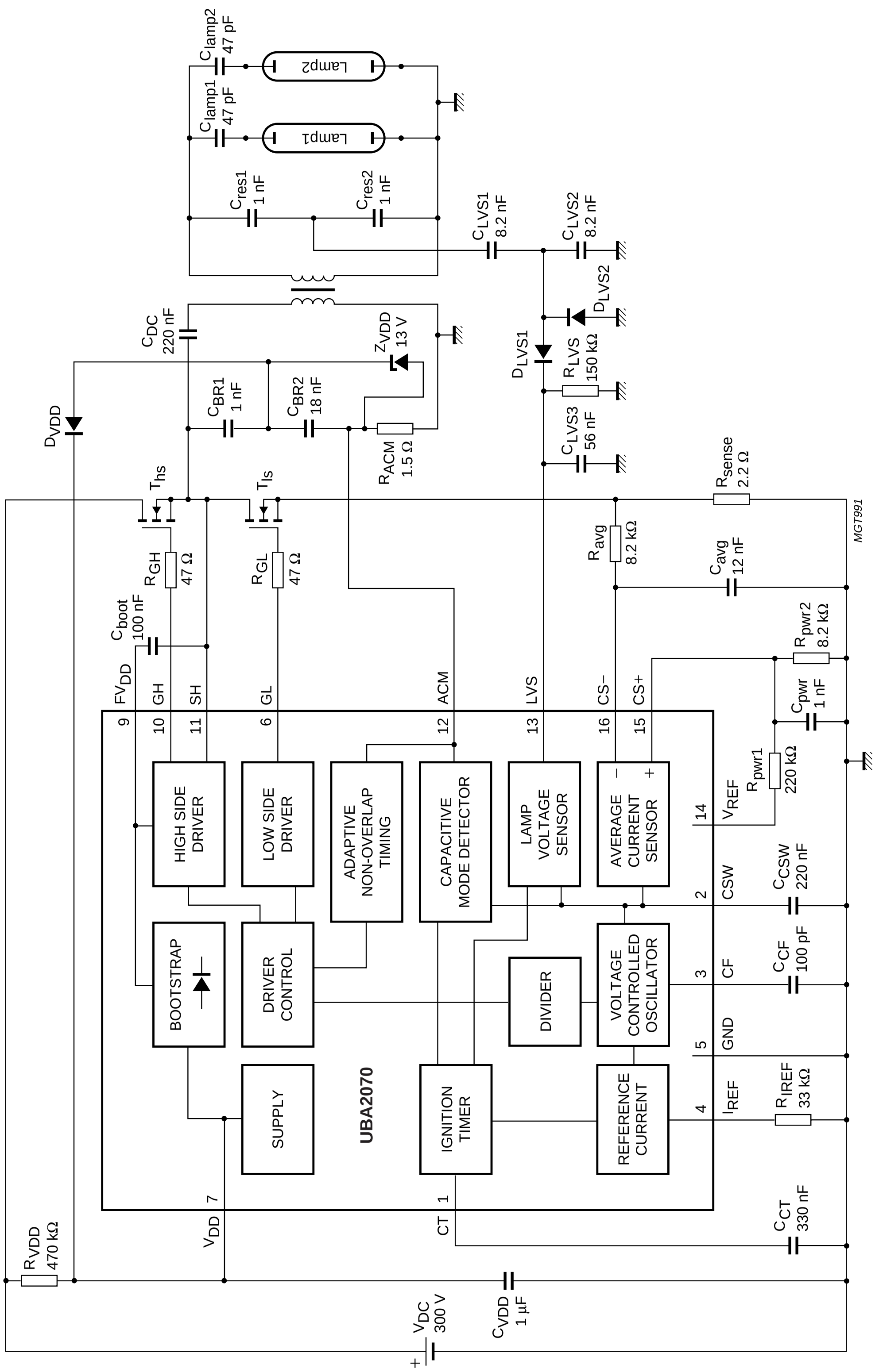
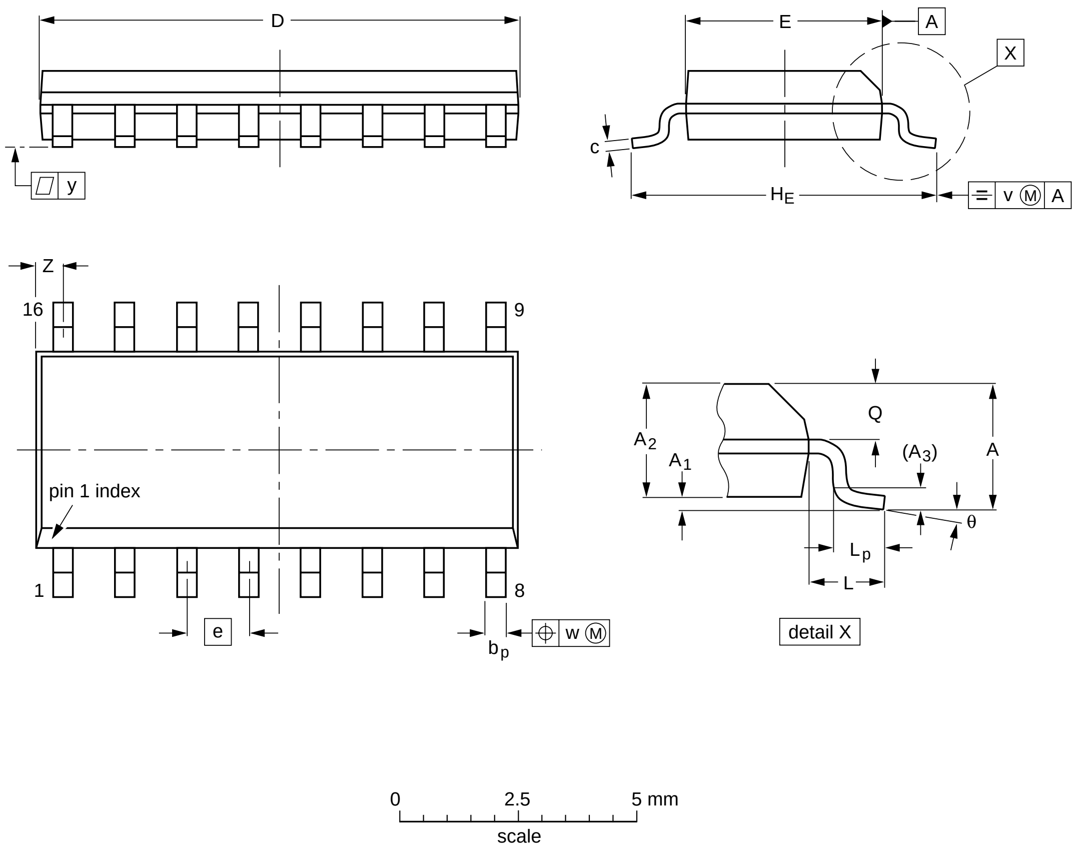


Fig.8 Test application circuit.

PACKAGE OUTLINES

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

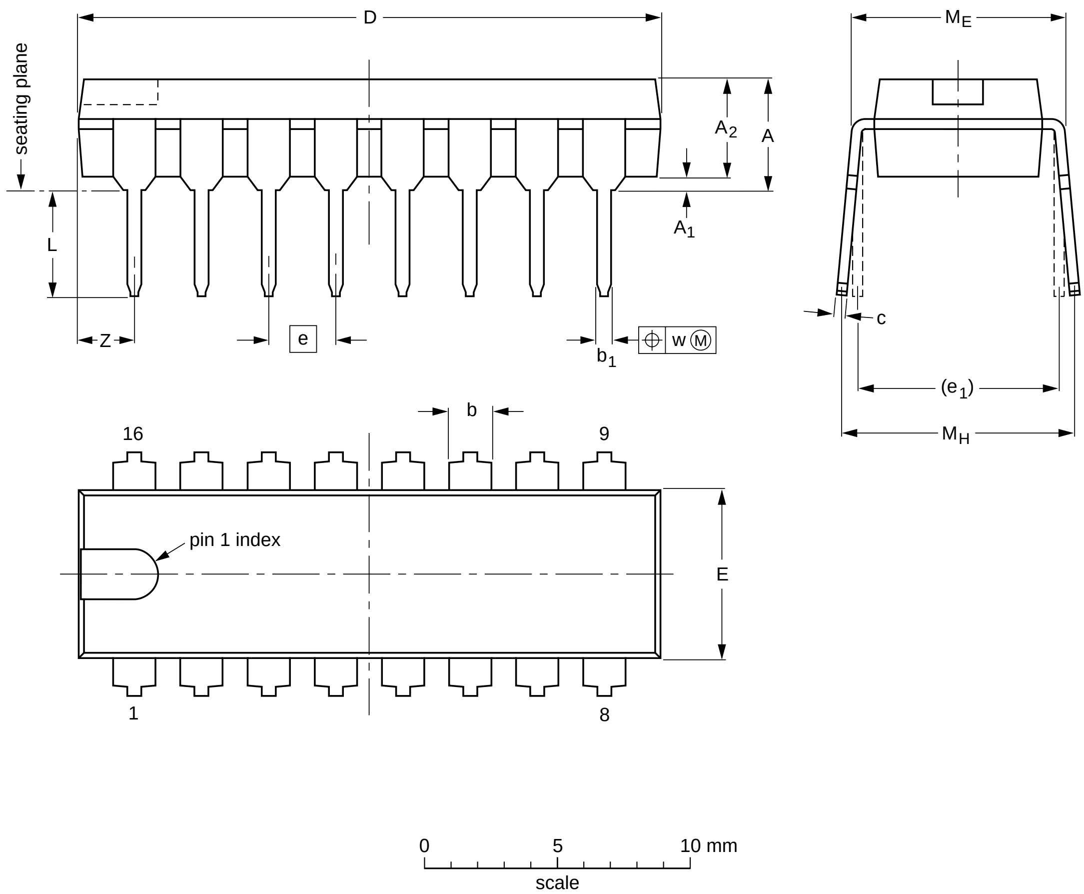
UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07	MS-012				~~97-05-22~~ 99-12-27

DIP16: plastic dual in-line package; 16 leads (300 mil); long body SOT38-1

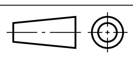


DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001	SC-503-16			~~95-01-19~~ 99-12-27

SOLDERING

Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Through-hole mount packages

SOLDERING BY DIPPING OR BY SOLDER WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

MANUAL SOLDERING

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Surface mount packages

REFLOW SOLDERING

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

WAVE SOLDERING

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

MANUAL SOLDERING

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of IC packages for wave, reflow and dipping soldering methods

MOUNTING	PACKAGE[1]	SOLDERING METHOD		
		WAVE	REFLOW[2]	DIPPING
Through-hole mount	DBS, DIP, HDIP, SDIP, SIL	suitable[3]	–	suitable
Surface mount	BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable	–
	HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable	–
	PLCC[5], SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended[5][6]	suitable	–
	SSOP, TSSOP, VSO	not recommended[7]	suitable	–

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
4. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
5. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
6. Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
7. Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS[1]	PRODUCT STATUS[2][3]	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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NOTES

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