WM8961

Ultra-Low Power Stereo CODEC with 1W Stereo Class D Speaker Drivers and Ground Referenced Headphone Drivers

DESCRIPTION

The WM8961 is a low power, high quality stereo CODEC designed for portable digital audio applications.

An integrated charge pump provides a ground referenced output which removes the need for DC-blocking capacitors on the output, and uses the Wolfson 'Class-W' amplifier techniques - incorporating an innovative dual-mode charge pump architecture - to optimise efficiency and power consumption during playback. A DC Servo is used to reduce DC ground offsets. This improves power consumption and minimises pops and clicks.

Stereo class D speaker drivers provide 1W per channel into 8Ω loads with a 5V supply. Low leakage, excellent PSRR and pop/click suppression mechanisms also allow direct battery connection to the speaker supply. Flexible speaker boost settings allow speaker output power to be maximised while minimising other analogue supply currents.

Control sequences for audio path setup can be pre-loaded and executed by an integrated sequencer to reduce software driver development and eliminate pops and clicks via Wolfson's SilentSwitch™ technology.

Flexible input configuration : a stereo input or two mono inputs on Lch or Rch ADC, with a complete microphone interface. External component requirements are drastically reduced as no separate microphone, speaker or headphone amplifiers are required. Advanced on-chip digital signal processing performs automatic level control for the microphone or line input.

Stereo 24-bit sigma-delta ADCs and DACs are used with low power over-sampling digital interpolation and decimation filters and a flexible digital audio interface.

The WM8961 operates at analogue supply voltages down to 1.71V, although the digital supplies can operate at voltages down to 1.62V to save power. The speaker supply can operate at up to 5.5V, providing 1W per channel into 8Ω loads. Unused functions can be disabled using software control to save power.

The WM8961 is supplied in a very small and thin 5x5mm QFN package, ideal for use in hand-held and portable systems.

FEATURES

- DAC SNR 98dB ('A' weighted), THD -83dB at 48kHz, 1.8V
- ADC SNR 88dB ('A' weighted), THD -75dB at 48kHz, 1.8V
- Stereo Class D Speaker Driver
  - 1W per channel into 8Ω BTL speakers.
  - Flexible internal switching clock
- Wolfson 'Class-W' ultra-low power headphone Driver
  - Up to 22mW per channel output power at -80dB THD+N into 16Ω at 1.8V
  - Ground Referenced
  - Low offset (+/- 1.5mV)
  - Pop and click suppression
  - Control sequencer for pop-minimised start-up and shut-down
  - Single register write for default start-up sequence
- Microphone Interface
  - Single ended stereo input
  - Integrated low noise MICBIAS
  - Programmable ALC / Limiter and Noise Gate
- Low Power Consumption
  - 6.99mW headphone playback (1.8V supplies, Low Power mode)
- Low Supply Voltages
  - Analogue 1.71V to 2.0V (Speaker supply up to 5.5V)
  - Charge pump 1.71V to 2.0V
  - MIC bias amp supply 1.71V to 3.6V
  - Digital 1.62V to 2.0V
- 2-wire serial control interface including read-back
- Sample rates: 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48
- 5x5x0.9mm 32 pin QFN package

APPLICATIONS

- Games consoles
- Portable media / DVD players
- Mobile multimedia

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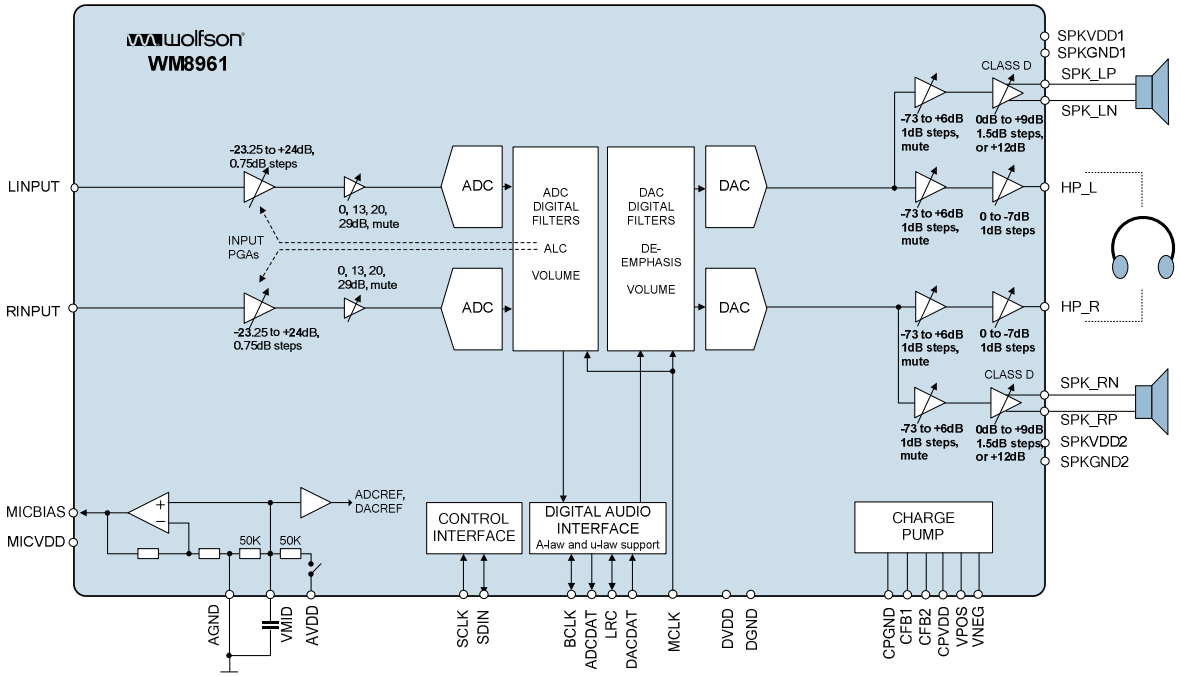
BLOCK DIAGRAM



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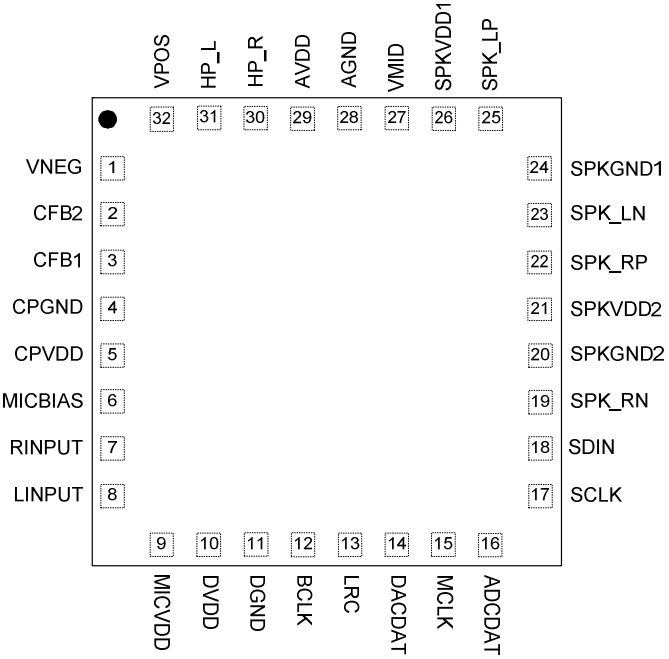
PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8961GEFL/V	-40°C to +85°C	32-pin QFN (5x5x0.9mm) (Pb-free)	MSL3	260°C
WM8961GEFL/RV	-40°C to +85°C	32-pin QFN (5x5x0.9mm) (Pb-free, Tape and reel)	MSL3	260°C

Note:
Reel quantity = 3500

PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
1	VNEG	Analogue Output	Charge pump negative supply decoupling (powers HP_L, HP_R)
2	CFB2	Analogue Output	Charge pump fly-back capacitor pin
3	CFB1	Analogue Output	Charge pump fly-back capacitor pin
4	CPGND	Supply	Charge pump ground (Return path for CPVDD)
5	CPVDD	Supply	Charge pump power supply
6	MICBIAS	Analogue Output	Microphone bias
7	RINPUT	Analogue Input	Right channel input
8	LINPUT	Analogue Input	Left channel input
9	MICVDD	Supply	Microphone bias amp supply
10	DVDD	Supply	Digital core and buffer (I/O) supply
11	DGND	Supply	Digital ground
12	BCLK	Digital Input / Output	Audio interface bit clock
13	LRC	Digital Input / Output	Audio interface left / right clock
14	DACDAT	Digital Input	DAC digital audio data
15	MCLK	Digital Input	Master clock
16	ADCDAT	Digital Output	ADC digital audio data
17	SCLK	Digital Input	Control interface clock input
18	SDIN	Digital Input/Output	Control interface data input / 2-wire acknowledge output
19	SPK_RN	Analogue Output	Right speaker negative output
20	SPKGND2	Supply	Ground for right speaker drivers
21	SPKVDD2	Supply	Supply for right speaker drivers
22	SPK_RP	Analogue Output	Right speaker positive output
23	SPK_LN	Analogue Output	Left speaker negative output
24	SPKGND1	Supply	Ground for left speaker drivers
25	SPK_LP	Analogue Output	Left speaker positive output
26	SPKVDD1	Supply	Supply for left speaker drivers
27	VMID	Analogue Output	Mid-rail voltage =AVDD/2 (requires decoupling capacitor)
28	AGND	Supply	Analogue ground (Return path for AVDD)
29	AVDD	Supply	Analogue supply
30	HP_R	Analogue Output	Right output (Line or headphone)
31	HP_L	Analogue Output	Left output (Line or headphone)
32	VPOS	Analogue Output	Charge pump positive supply decoupling (powers HP_L, HP_R)
	GND_PADDLE		Die Paddle (Note 1)

Note:

It is recommended that the QFN ground paddle should be connected to analogue ground on the application PCB.

Refer to the application note WAN_0118 on “Guidelines on How to Use QFN Packages and Create Associated PCB Footprints”

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
DVDD and AVDD	-0.3V	+2.5V
MICVDD	-0.3V	+4.5V
SPKVDD1, SPKVDD2	-0.3V	+7.0V
CPVDD	-0.3V	+2.2V
Voltage range digital inputs	DGND -0.3V	DVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Voltage range analogue outputs (HP_L, HP_R)	-CPVDD-0.3V	+CPVDD+0.3V
Temperature Range, T_A	-40°C	+85°C
Storage temperature after soldering	-65°C	+150°C

Notes

1. Analogue, digital and speaker grounds must always be within 0.3V of each other.
2. All digital and analogue supplies are completely independent from each other (i.e. not internally connected).
3. DVDD must be less than or equal to AVDD.
4. AVDD must be less than or equal to MICVDD.
5. AVDD must be less than or equal to SPKVDD1 and SPKVDD2.
6. SPKVDD1 and SPKVDD2 must be high enough to support the peak output voltage when using ACGAIN function, to avoid output waveform clipping. See the “Speaker Output Boost Control” section.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital supply range	DVDD	1.62	1.8V	2.0	V
Microphone bias supply range	MICVDD	1.71	2.5V	3.6	V
Analogue supplies range	AVDD	1.71	1.8V	2.0	V
Charge pump supply range (1.8V supply operation)	CPVDD	1.71	1.8V	2.0	V
Speaker supply range	SPKVDD1, SPKVDD2	2.7	5.0	5.5	V
Ground	DGND, AGND, CPGND, SPKGND1, SPKGND2		0		V
Operating Temperature		-40	+25	+85	°C

ELECTRICAL CHARACTERISTICS

Test Conditions

MICVDD = 2.5V, DVDD = 1.8V, CPVDD=1.8V, AVDD = 1.8V SPKVDD1 = SPKVDD2 = 5V, T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Inputs (LINPUT, RINPUT)						
Full-scale Input Signal Level – note this changes in proportion to AVDD	V_{INFS}	L/RINPUT Single-ended		500 -6.02		mVrms dBV
Mic PGA equivalent input noise		20Hz to 20kHz, +24dB gain		3		uV
Input resistance	L/R_{INPUT}	+24dB PGA gain		3.5		kΩ
	L/R_{INPUT}	0dB PGA gain		28		kΩ
	L/R_{INPUT}	-23.25dB PGA gain		53		kΩ
Input capacitance	Cin			10		pF
MIC Programmable Gain Amplifier (PGA)						
Programmable Gain		Input from L/RINPUT	-23.25		24	dB
Programmable Gain Step Size		Guaranteed monotonic		0.75		dB
Mute Attenuation				85		dB
Selectable Input Gain Boost						
Gain Boost Steps		Input from PGA		0, 13, 20, 29		dB
Analogue Inputs (LINPUT, RINPUT) to ADC out						
Signal to Noise Ratio (A-weighted)	SNR		80	88		dB
Total Harmonic Distortion Plus Noise	THD+N	-1dBFS input		-82	-75	dB
Total Harmonic Distortion	THD	-1dBFS input		-86	-75	dB
ADC Channel Separation		1kHz		97		dB
		10kHz		97		dB
PSRR		100mV(peak-peak) 1kHz applied to AVDD		60		dB
PSRR		100mV(peak-peak) 20kHz applied to AVDD		40		dB
Channel Matching		1kHz signal		+/-0.5		dB
DAC to HP_L, HP_R (used as Line output) with 10kΩ / 50pF load: standard headphone playback mode						
Full scale output voltage		L/ROUTVOL = 0dB		1.0		Vrms
Signal to Noise Ratio (A-weighted)	SNR		87	97		dB
Total Harmonic Distortion Plus Noise	THD+N	10kΩ load		-78	-67	dB
Total Harmonic Distortion	THD	10kΩ load		-79	-68	dB
Channel Separation		1kHz full scale signal		100		dB
		10kHz full scale signal		85		
PSRR (AVDD)		100mV(peak-peak) 1kHz		60		dB
		100mV(peak-peak) 20kHz		58		dB
DC offset		DC servo is enabled	-1.5		+1.5	mV

Test Conditions

MICVDD = 2.5V, DVDD = 1.8V, CPVDD=1.8V, AVDD = 1.8V SPKVDD1 = SPKVDD2 = 5V, T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to HP_L, HP_R (used as Line output) with 10kΩ / 50pF load: SNR optimised headphone playback mode (see note 1)						
Signal to Noise Ratio (A-weighted)	SNR		88	98		dB
Total Harmonic Distortion Plus Noise	THD+N	10kΩ load		-78		dB
Total Harmonic Distortion	THD	10kΩ load		-79		dB
DAC to Headphone Output (HP_L, HP_R) with headphone load: standard headphone playback mode						
Output Power at 1% THD+N	P_O	R_L=32Ω		26		mW
		R_L=16Ω		30		
Total Harmonic Distortion Plus Noise	THD+N	R_L=32Ω, P_O=2mW		-79 0.011		dB %
		R_L=32Ω, P_O=3.5mW		-79 0.011		
		R_L=32Ω, P_O=12mW		-78 0.012	-70 0.032	
		R_L=16Ω, P_O=2mW		-81 0.0089		
		R_L=16Ω, P_O=22mW		-80 0.01		
Total Harmonic Distortion	THD	R_L=32Ω, P_O=12mW		-82 0.0079		dB %
		R_L=16Ω, P_O=22mW		-84 0.0063		dB %
Noise Level			-87	-97		dBV
DC offset		DC servo is enabled	-1.5		+1.5	mV
Channel Separation		1kHz full scale signal		90		dB
		10kHz full scale signal		75		
DAC to Headphone Output (HP_L, HP_R) with headphone load: low power headphone playback mode						
Total Harmonic Distortion Plus Noise	THD+N	RL=32Ω, PO=12mW		-77 0.014		dB %
		RL=16Ω, PO=22mW		-79 0.011		
Noise Level				-97		dBV
DAC to Headphone Output (HP_L, HP_R) with headphone load: SNR optimised playback mode (see note 1)						
Total Harmonic Distortion Plus Noise	THD+N	RL=32Ω, PO=12mW		-81 0.0089	-70 0.032	dB %
		RL=16Ω, PO=22mW		-82 0.0079		
Noise Level			-88	-98		dBV
DAC to Speaker Outputs (DAC to SPK_LP, SPK_LN, SPK_RP, SPK_RN with stereo 8Ω bridge tied load)						
Output Power at 1% THD+N	P_O	R_L=8Ω, SPKVDD=5v5		1.26		W
Total Harmonic Distortion Plus Noise	THD+N	P_O =200mW, R_L = 8Ω, SPKVDD1=SPKVDD2 =3.3V; AVDD=1.8V		-64 0.063		dB %
		P_O =320mW, R_L = 8Ω, SPKVDD1=SPKVDD2 =3.3V; AVDD=1.8V		-72 0.025		dB %

Test Conditions

MICVDD = 2.5V, DVDD = 1.8V, CPVDD=1.8V, AVDD = 1.8V SPKVDD1 = SPKVDD2 = 5V, T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
		P_O =320mW, R_L = 8Ω, SPKVDD1=SPKVDD2 =5V; AVDD=1.8V		-61 0.089	-50 0.32	dB %
		P_O =1W, R_L = 8Ω, SPKVDD1=SPKVDD2 =5V; AVDD=1.8V		-58 0.13	-45 0.56	dB %
Signal to Noise Ratio (A-weighted) (DAC to speaker outputs)	SNR	SPKVDD1=SPKVDD2 =3.3V; AVDD=1.8V; R_L = 8Ω, ref=2.0Vrms		90		dB
		SPKVDD1=SPKVDD2 =5V; AVDD=1.8V; R_L = 8Ω, ref=2.8Vrms	82	92		dB
Speaker Supply Leakage current	I_{SPKVDD}	SPKVDD1=SPKVDD2 =5V; All other supplies disconnected		1	5	uA
		SPKVDD1=SPKVDD2 =5V; All other supplies 0V		1	5	uA
Power Supply Rejection Ratio (SPKVDD1/SPKVDD2)	PSRR	100mV(peak-peak) 217Hz		75		dB
		100mV(peak-peak) 1kHz		75		dB
SPKL/RVOL						
Volume Gain			-68		6	dB
Volume Gain Step Size		Guaranteed monotonic		1		dB
Mute Attenuation				87		dB
L/ROUTVOL						
Volume Gain			-68		6	dB
Volume Gain Step Size		Guaranteed monotonic		1		dB
Mute Attenuation				85		dB
Analogue Reference Levels						
Mid-rail Reference Voltage	VMID		–3%	AVDD/2	+3%	V
Microphone Bias						
Bias Voltage (Note that MBSEL=1 only allowed if MICVDD is greater than +2.40V)	$V_{MICBIAS}$	MICVDD=2.5V 2mA load current MBSEL=1	-10%	7/6×AVDD	+10%	V
		MICVDD=2.5V 2mA load current MBSEL=0	-10%	5/6×AVDD	+10%	V
Power Supply Rejection Ratio	PSRR	100mV ripple on MICVDD @1kHz, MBSEL=1		68		dB
		100mV ripple on AVDD @1kHz, MBSEL=1		51		
Bias Current Source	$I_{MICBIAS}$				2	mA
Output Noise spectral density @1KHz	Vst	1KHz, MBSEL=1		85		nV/√Hz
CHARGE PUMP						
Charge Pump switching frequency	CPFREQ				1	MHz
Flyback capacitor (between CFB1 and CFB2 pins)	C_{FB}	at 2V	1			µF

Test Conditions

MICVDD = 2.5V, DVDD = 1.8V, CPVDD=1.8V, AVDD = 1.8V SPKVDD1 = SPKVDD2 = 5V, T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VPOS capacitor		at 2V	2			µF
VNEG capacitor		at 2V	2			µF
Charge pump start-up time				300		µs
Digital Input / Output						
Input HIGH Level	V_{IH}		0.7×DVDD			V
Input LOW Level	V_{IL}				0.3×DVDD	V
Output HIGH Level	V_{OH}	I_{OL}=1mA	0.9×DVDD			V
Output LOW Level	V_{OL}	I_{OH}=-3mA			0.1×DVDD	V
Input capacitance				10		pF
Input leakage			-0.9		0.9	µA
CURRENT CONSUMPTION						
AVDD	I_{AVDD}	OFF: device powered down using register writes, TSENSEN=0, all clocks stopped.		5	20	µA
DVDD	I_{DVDD}			3	20	µA
CPVDD	I_{CPVDD}			5	20	µA
SPKVDD	I_{SPKVDD}			1	10	µA
MICVDD	I_{MICVDD}			1	20	µA

Note:

1. The measurement was made with HPL_VOL//HPR_VOL = 0dB. Normally, the recommended setting for SNR optimised HP playback mode (see “SNR optimised Mode”) includes -7dB HPL_VOL//HPR_VOL setting, to give a further noise floor improvement.

TYPICAL POWER CONSUMPTION

The WM8961 power consumption is dependent on many parameters. Most significantly, it depends on supply voltages, sample rates, mode of operation, and output loading.

The power consumption on each supply rail varies approximately with the square of the voltage. Power consumption is greater at fast sample rates than at slower ones. When the digital audio interface is operating in Master mode, the DVDD current is significantly greater than in Slave mode. (Note also that power savings can be made by using MCLK as the BCLK source in Slave mode.) The output load conditions (impedance, capacitance and inductance) can also impact significantly on the device power consumption.

COMMON TEST CONDITIONS

Unless otherwise stated, the following test conditions apply throughout the following sections:

- Ambient temperature = +25°C
- Audio signal = quiescent (zero amplitude)
- Sample rate = 48kHz
- MCLK = 12.288MHz

Additional, variant test conditions are quoted within the relevant sections below. Where applicable, power dissipated in the headphone or line loads is included.

All measurements given in this section are typical and derived from evaluation.

MEASUREMENTS

Stereo line record - LINPUT1 and RINPUT1 pins to ADC output.

Test conditions:
LINVOL = RINVOL = 011111b (0dB)

Variant test conditions	**AVDD**		**DVDD**		**SPKVDD**		**MICVDD**		**TOTAL (see note 1)**
	V	**mA**	**V**	**mA**	**V**	**mA**	**V**	**mA**	**mW**
48kHz sample rate, quiescent	1.8	7.08	1.8	1.8	5.0	0.001	2.5	0.001	16
48kHz sample rate, quiescent, MBSEL=1	1.8	7.08	1.8	1.8	5.0	0.001	2.5	0.258	16.7
48kHz sample rate, -1dBFS Input	1.8	7.12	1.8	1.8	5.0	0.001	2.5	0.001	16.1
8kHz sample rate (256fS i.e. MCLK = 2.048MHz)	1.8	6.85	1.8	0.30	5.0	0.001	2.5	0.001	12.9

Note:

1. CPVDD consumed 0.004mA in all cases.

Stereo Playback DAC to Headphones – Low Power Headphone Playback with 16Ω load.

Test conditions
CP_DYN_PWR[1:0] = 0b11 (Dynamic control of charge pump power)
48kHz sample rate

Variant test conditions	**AVDD**		**DVDD**		**SPKVDD**		**CPVDD**		**TOTAL**
	V	**mA**	**V**	**mA**	**V**	**mA**	**V**	**mA**	**mW**
Quiescent	1.8	1.79	1.8	1.55	5.0	0.002	1.8	0.54	6.99
P_o = 2mW/channel	1.8	1.79	1.8	1.57	5.0	0.002	1.8	18.0	38.2
P_o = 16mW/channel	1.8	1.82	1.8	1.57	5.0	0.002	1.8	59.8	114

Stereo Playback DAC to Headphones – Standard Headphone Playback with 16Ω load.

Test conditions
48kHz sample rate

Variant test conditions	AVDD		DVDD		SPKVDD		CPVDD		TOTAL
	V	mA	V	mA	V	mA	V	mA	mW
Quiescent	1.8	1.79	1.8	1.56	5.0	0.002	1.86	1.775	9.39
P_o = 2mW/channel	1.8	1.79	1.8	1.57	5.0	0.002	1.8	22.46	46.5
P_o = 16mW/channel	1.8	1.82	1.8	1.57	5.0	0.002	1.8	59.8	114

Stereo Playback DAC to Headphones – SNR Optimised Headphone Playback with 16Ω load.

Test conditions
48kHz sample rate

Variant test conditions	AVDD		DVDD		SPKVDD		CPVDD		TOTAL
	V	mA	V	mA	V	mA	V	mA	mW
Quiescent	1.8	2.1	1.8	1.72	5.0	0.002	1.8	1.46	9.52
P_o = 2mW/channel	1.8	2.12	1.8	1.73	5.0	0.002	1.8	22.4	47.25
P_o = 16mW/channel	1.8	2.14	1.8	1.73	5.0	0.002	1.8	59.4	114

Stereo Playback to Speaker - with 8.2Ω + 22uH load (see note 1).

Test conditions
48kHz sample rate
CLASSD_ACGAIN=111 (+12dB)

Variant test conditions	AVDD		DVDD		SPKVDD1+2		CPVDD		TOTAL
	V	mA	V	mA	V	mA	V	mA	
Quiescent	1.8	2.418	1.8	1.385	5.0	1.16	1.8	0.004	12.65mW
P_o = 200mW/channel	1.8	2.438	1.8	1.525	5.0	102	1.8	0.004	517mW
P_o = 1W/channel	1.8	2.458	1.8	1.750	5.0	480	1.8	0.004	2.4W

Note:

1. The load inductance will affect the efficiency: the Class D output is generally less efficient when driving a less inductive load.

SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK TIMING

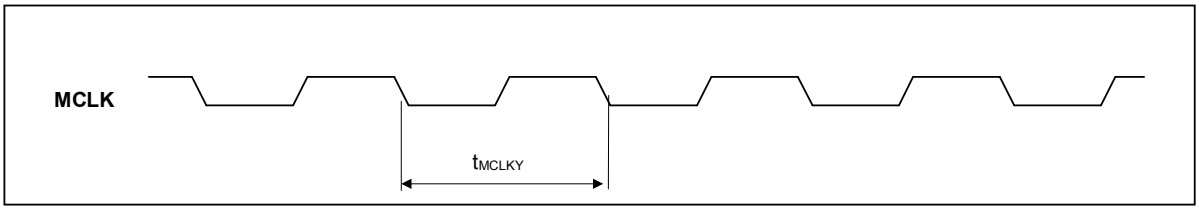


Figure 1 System Clock Timing Requirements

Test Conditions
MICVDD=2.5V, DVDD = CPVDD=AVDD =1.8V SPKVDD1 = SPKVDD2 = 5V,
DGND=AGND=CPGND=SPKGND1=SPKGND2=0V, T_A = +25°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
MCLK cycle time	T_{MCLKY}	MCLKDIV=1	40			ns
		MCLKDIV=0	80			ns
MCLK duty cycle	T_{MCLKDS}		60:40		40:60	

AUDIO INTERFACE TIMING – MASTER MODE

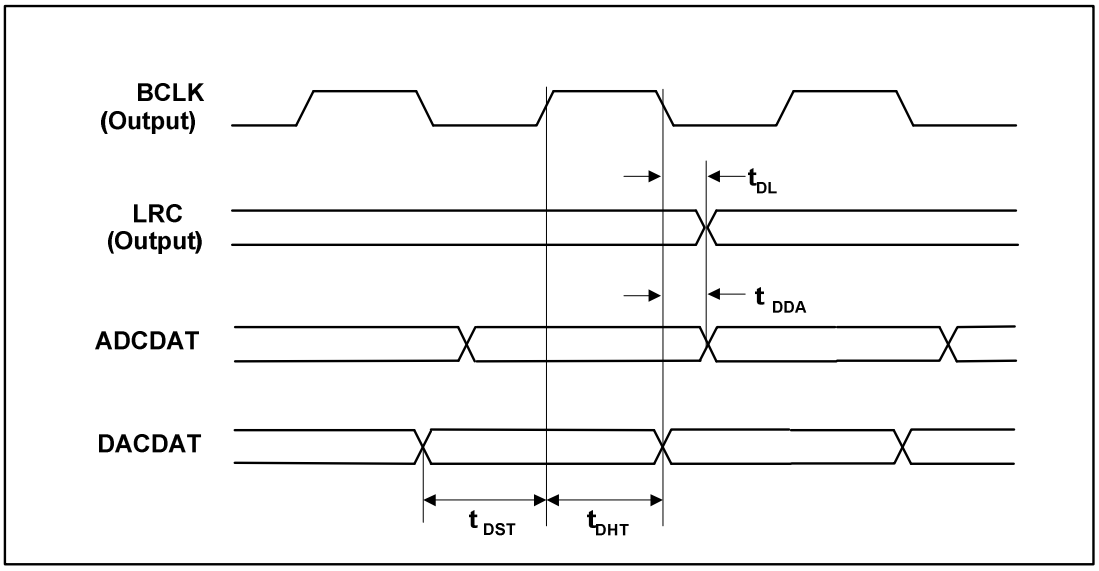


Figure 2 Digital Audio Data Timing – Master Mode (see Control Interface)

Test Conditions

MICVDD=2.5V, DVDD = CPVDD=AVDD =1.8V SPKVDD1 = SPKVDD2 = 5V,
DGND=AGND=CPGND=SPKGND1=SPKGND2=0V,

T_A=+25°C, Slave Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
LRC propagation delay from BCLK falling edge	t_{DL}			10	ns
ADCDAT propagation delay from BCLK falling edge	t_{DDA}			10	ns
DACDAT setup time to BCLK rising edge	t_{DST}	10			ns
DACDAT hold time from BCLK rising edge	t_{DHT}	10			ns

AUDIO INTERFACE TIMING – SLAVE MODE

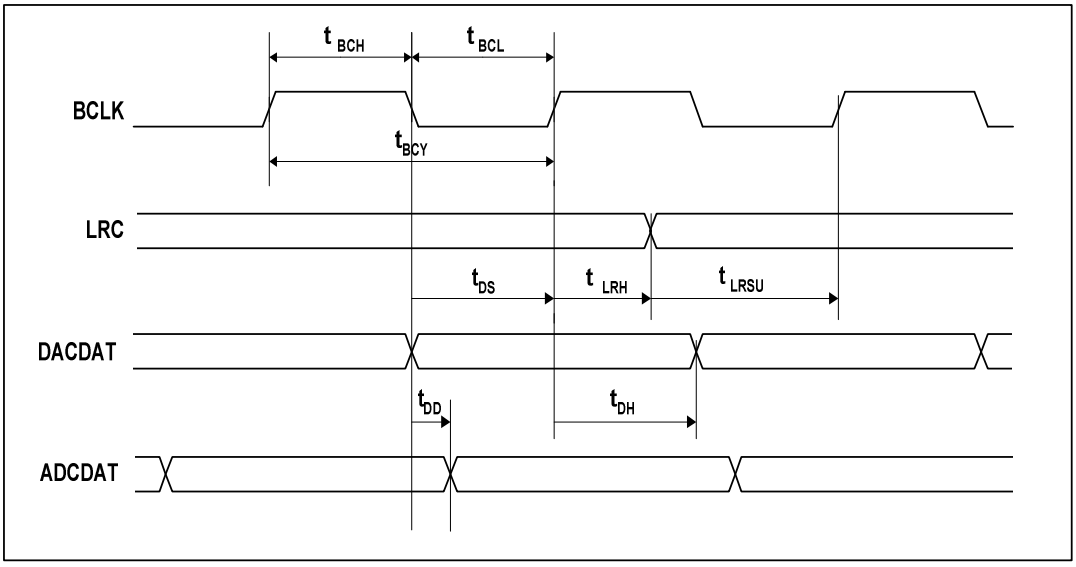


Figure 3 Digital Audio Data Timing – Slave Mode

Test Conditions

MICVDD=2.5V, DVDD = CPVDD=AVDD =1.8V SPKVDD1 = SPKVDD2 = 5V,
DGND=AGND=CPGND=SPKGND1=SPKGND2=0V,
T_A=+25°C, Slave Mode, fs=48kHz, MCLK= 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
BCLK cycle time	t_{BCY}	50			ns
BCLK pulse width high	t_{BCH}	20			ns
BCLK pulse width low	t_{BCL}	20			ns
LRC set-up time to BCLK rising edge	t_{LRSU}	10			ns
LRC hold time from BCLK rising edge	t_{LRH}	10			ns
DACDAT hold time from BCLK rising edge	t_{DH}	10			ns
ADCDAT propagation delay from BCLK falling edge	t_{DD}			10	ns
DACDAT set-up time to BCLK rising edge	t_{DS}	10			ns

Note:

BCLK period should always be greater than or equal to MCLK period.

CONTROL INTERFACE TIMING

The WM8961 is controlled via a 2-wire serial control interface.

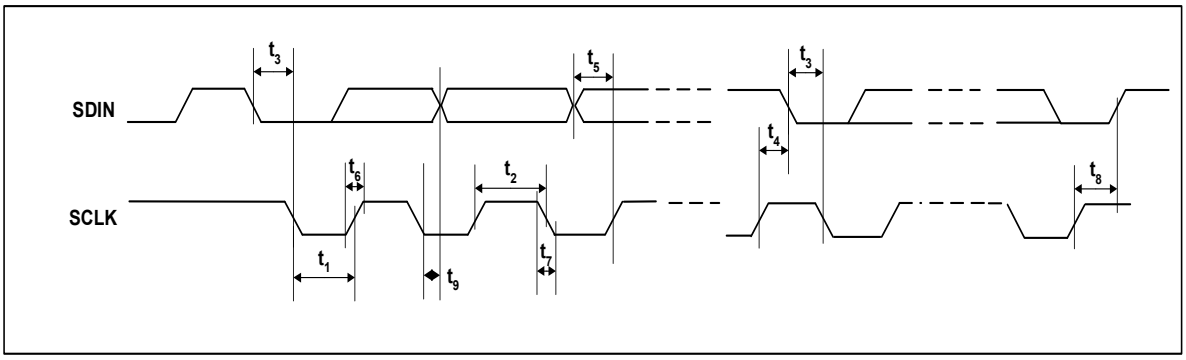


Figure 4 2-Wire Serial Control Interface Timing

Test Conditions

MICVDD=2.5V, DVDD = CPVDD=AVDD =1.8V SPKVDD1 = SPKVDD2 = 5V,
DGND=AGND=CPGND=SPKGND1=SPKGND2=0V,
T_A=+25°C, Slave Mode, fs=48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK Frequency				526	kHz
SCLK Low Pulse-Width	t_1	1.3			us
SCLK High Pulse-Width	t_2	600			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
SDIN, SCLK Rise Time	t_6			300	ns
SDIN, SCLK Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

Note:

Device Address = 0x94.

INTERNAL POWER ON RESET CIRCUIT

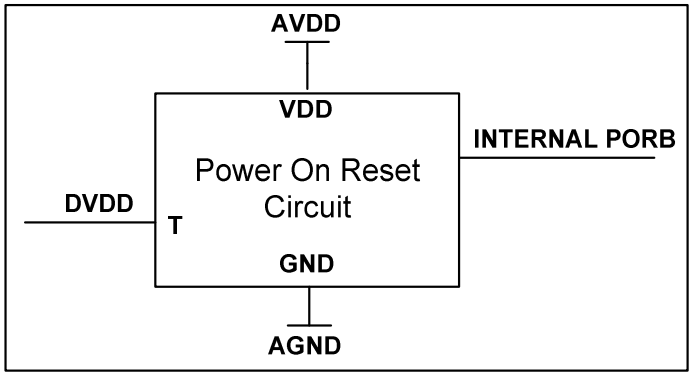


Figure 5 Internal Power-on Reset Circuit Schematic

The WM8961 includes an internal Power-On-Reset Circuit, as shown in Figure 5, which is used to reset the digital logic into a default state after power up. The POR circuit is powered from AVDD and monitors DVDD. It asserts PORB low if AVDD or DVDD is below a minimum threshold.

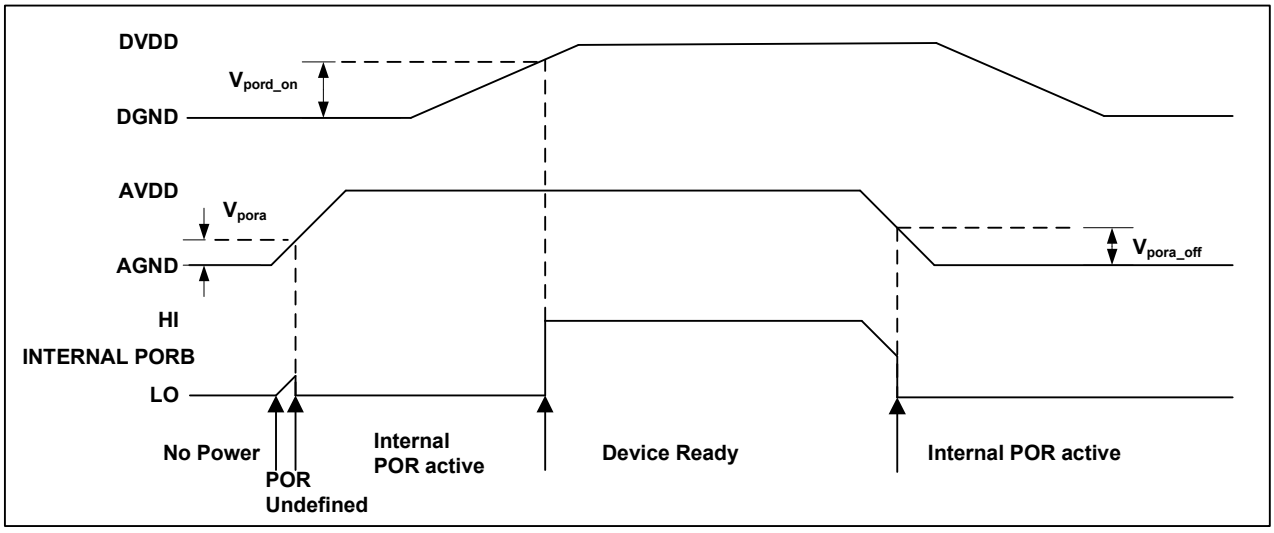


Figure 6 Typical Power up Sequence when AVDD is Applied before DVDD

Figure 6 shows a typical power-up sequence where AVDD comes up first. When AVDD goes above the minimum threshold, V_{pora}, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. Now AVDD is at full supply level. Next DVDD rises to V_{pord_on} and PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where AVDD falls first, PORB is asserted low whenever AVDD drops below the minimum threshold V_{pora_off}.

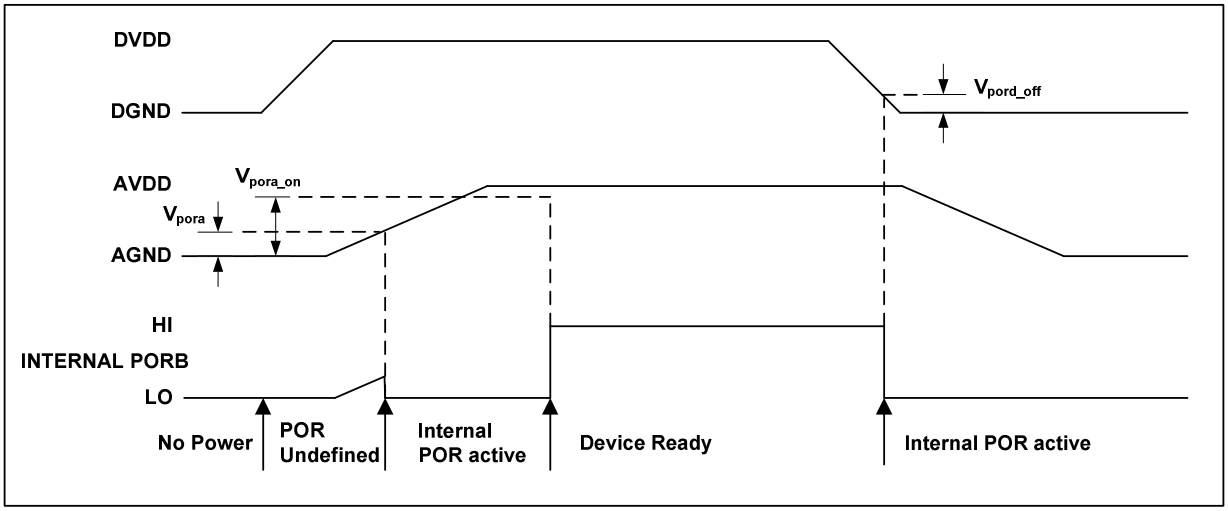


Figure 7 Typical Power up Sequence when DVDD is Applied before AVDD

Figure 7 shows a typical power-up sequence where DVDD comes up first. First it is assumed that DVDD is already up to specified operating voltage. When AVDD goes above the minimum threshold, V_{pora}, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. When AVDD rises to V_{pora_on}, PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where DVDD falls first, PORB is asserted low whenever DVDD drops below the minimum threshold V_{pord_off}.

SYMBOL	MIN	TYP	MAX	UNIT
V_{pora}		0.5		V
V_{pora_on}		1.1		V
V_{pora_off}		1.1		V
V_{pord_on}		0.9		V
V_{pord_off}		0.65		V

Table 1 Typical POR Operation

Notes:

1. If AVDD and DVDD suffer a brown-out (i.e. drops below the minimum recommended operating level but do not go below V_{pora_off} or V_{pord_off}) then the chip will not reset and will resume normal operation when the voltage is back to the recommended level again.
2. The chip will enter reset at power down when AVDD or DVDD falls below V_{pora_off} or V_{pord_off}. This may be important if the supply is turned on and off frequently by a power management system.
3. The minimum t_{por} period is maintained even if DVDD and AVDD have zero rise time. This specification is guaranteed by design rather than test.

DEVICE DESCRIPTION

INTRODUCTION

The WM8961 is a low power audio CODEC offering a combination of high quality audio, advanced features, low power and small size. These characteristics make it ideal for portable digital audio applications with stereo speaker and headphone outputs such as games consoles, portable media players and multimedia phones.

A flexible input configuration supports a single-ended stereo microphone interface. A boost amplifier is available for additional gain on the microphone inputs. A programmable gain amplifier (PGA) with an automatic level control (ALC) function can be used to maintain a constant microphone recording volume.

Stereo class D speaker drivers can provide >1W per channel into 8Ω loads. BTL configuration provides high power output and excellent PSRR.

Highly flexible output speaker boost settings provide fully internal level-shifting of analogue output signals, allowing speaker output power to be maximised while minimising other analogue supply currents, and requiring no additional components.

A dual mode (Level Shifting or Inverting Mode) charge pump generates split supplies for the headphone output amplifiers allowing these to be ground referenced.

A DC servo to remove offsets from the headphone outputs, low leakage and a user controlled power-up/power-down Control Sequencer provides powerful pop and click suppression mechanisms which enable direct battery connection. These anti-pop/click mechanisms, and no requirement for any external DC blocking capacitors to the headphone, results in a reduced external component count and reduced power consumption in portable battery-powered applications.

The hi-fi quality stereo ADC and DAC uses a 24-bit, low-order over-sampling architecture to deliver optimum performance. ADC and DAC operate at the same sample rate.

The WM8961 has a configurable digital audio interface where ADC data can be read and digital audio playback data fed to the DAC. It supports a number of audio data formats including I^2S, DSP Mode (a burst mode in which frame sync plus two data packed words are transmitted), MSB-First, left justified and MSB-First, right justified, and can operate in master or slave modes. In PCM mode A-law and μ-law companding is supported.

The SYSCLK (internal system clock) provides clocking for all internal functions. SYSCLK is derived directly from the MCLK pin. All MCLK frequencies typically used in portable systems are supported for sample rates between 8 kHz and 48 kHz. The ADC and DAC must be configured to operate at the same sample rate. A flexible switching clock for the class D speaker drivers (synchronous with the audio DSP clocks for best performance) is also derived from SYSCLK.

To allow full software control over all its features, the WM8961 uses a 2 wire serial control interface, with full read-back capability on all registers. It is fully compatible with, and an ideal partner to, a wide range of industry standard microprocessors, controllers and DSPs. Unused functions can be disabled via software to save power, while low leakage currents extend standby and off time in portable battery-powered applications.

CONTROL INTERFACE

The WM8961 is controlled by writing to registers through a 2-wire serial control interface. A control word consists of 24 bits. The first 8 bits (B23 to B16) are address bits that select which control register is accessed. The remaining 16 bits (B15 to B0) are data bits, corresponding to the 16 bits in each control register. Many devices can be controlled by the same bus, and each device has a unique 7-bit address (this is not the same as the 8-bit address of each register in the WM8961). The default device address is 1001010x (0x94h).

The WM8961 operates as a slave device only. The controller indicates the start of data transfer with a high to low transition on SDIN while SCLK remains high. This indicates that a device address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on SDIN (7-bit address + Read/Write bit, MSB first). If the device address received matches the address of the WM8961, then the WM8961 responds by pulling SDIN low on the next clock pulse (ACK). If the address is not recognised or the R/W bit is '1' when operating in write only mode, the WM8961 returns to the idle condition and wait for a new start condition and valid address.

By default, the WM8961 control interface requires an MCLK to be present before register writes are supported. To access the control interface without an MCLK, the user must set R8 (08h) Clocking2 bit 5 (CLK_SYS_ENA) =0. MCLK is not required to write to CLK_SYS_ENA.

Without MCLK, and with CLK_SYS_ENA=0, all registers can be updated and will maintain their settings, however any changes to functionality of the write sequencer, headphone PGAs, and headphone output stage will not take effect until MCLK is present. Enabling MCLK after the register writes to enable the headphone PGA and headphone output stage may produce audible pops and clicks, hence is not recommended.

The WM8961 supports several kinds of read and write operations, which are:

- Single write
- Single read
- Multiple write using auto-increment
- Multiple read using auto-increment

Auto-increment is enabled by default and can be disabled using the AUTO_INC bit as detailed in Table 3.

These modes are shown in the section below. Terminology used in the following figures is as follows:

TERMINOLOGY	DESCRIPTION	
S	Start Condition	
Sr	Repeated start	
A	Acknowledge	
P	Stop Condition	
$R\overline{W}$	ReadNotWrite	0 = Write 1 = Read

Table 2 Terminology

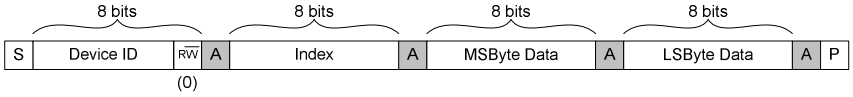


Figure 8 2-Wire Serial Control Interface (single write)

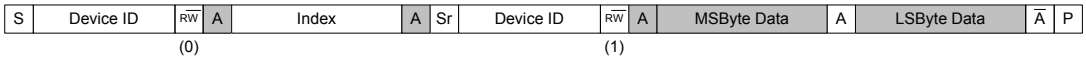


Figure 9 2-Wire Serial Control Interface (single read)

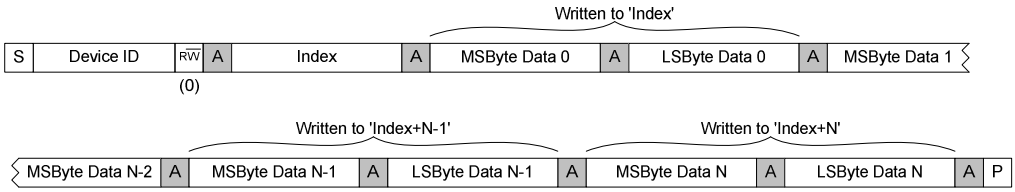


Figure 10 2-Wire Serial Control Interface (multiple write using auto-increment)

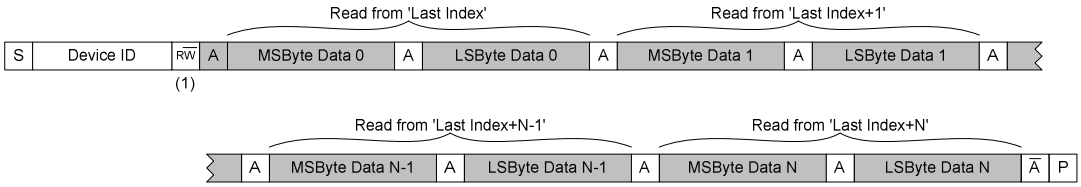


Figure 11 2-Wire Serial Control Interface (multiple read using auto-increment)

A Write Sequencer allows register write sequences to be stored in an area of memory on the WM8961 and then triggered by another register write. This allows complex sequences of updates to the WM8961 registers without the constant intervention of the processor. To use the write sequencer, an MCLK must be present and CLK_SYS_ENA=1. Refer to section headed "Control Write Sequencer" for operation of the Write Sequencer.

ALERT RESPONSES

By default WM8961 does not respond to Control interface alert response messages. This can be enabled by setting the ARA_ENA bit as detailed in Table 3.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R252 (FCh) General test 1	1	ARA_ENA	0	Alert Response Address Enable 0 : off 1 : on
	0	AUTO_INC	1	Enable Auto-Increment 0 : off 1 : on

Table 3 Control Interface Settings

INPUT SIGNAL PATH

The WM8961 has a flexible stereo analogue input channel which can be configured as line inputs or single-ended microphone inputs. The input signal path consists of an input volume control using a Programmable Gain Amplifier (PGA), followed by an input boost stage. The output of the boost stage drives a hi-fi stereo ADC. This is shown in Figure 12

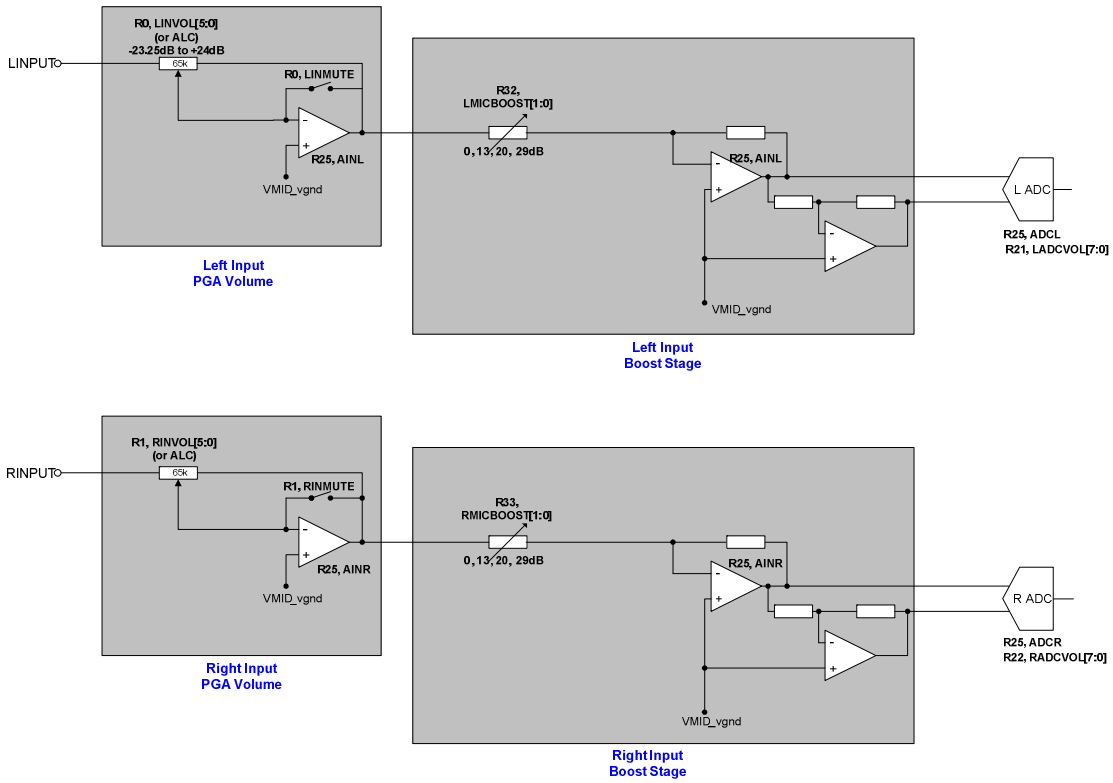


Figure 12 Analogue Input Stage

The input PGAs and boost stage are enabled by the AINL and AINR register bits.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R25 (19h) Power Management (1)	5	AINL	0	Left channel input PGA and boost stage enable 0 = PGA disabled, boost disabled 1 = PGA enabled boost enabled
	4	AINR	0	Right channel input PGA and boost stage enable 0 = PGA disabled, boost disabled 1 = PGA enabled boost enabled

Table 4 Input PGA and Boost Enable Register Settings

INPUT PGA VOLUME CONTROLS

The gain of the microphone PGAs can be manually configured, or automatically controlled using the ALC / Limiter. (Refer to section headed Automatic Level Control for more details).

The input PGA stage provide a general volume control for the LINPUT and RINPUT microphone inputs and have a gain range from -23.25dB to +24dB in 0.75dB steps. The gain of the PGAs is controlled by the register bits LINVOL[5:0] and RINVOL[5:0].

When the Automatic Level Control (ALC) is enabled the input PGA gains are controlled automatically and the LINVOL and RINVOL bits should not be used.

The left and right input PGAs can be independently muted using the LINMUTE and RINMUTE register bits.

To allow simultaneous volume updates of left and right channels, PGA gains are not altered until a 1 is written to the IPVU bit.

To prevent "zipper noise", a zero-cross function is provided, so that when enabled, volume updates will not take place until a zero-crossing is detected. This can be enabled using the LIZC and LIZC register bits. These bits must be written as a separate register write, before the volume setting is applied. For example, to change the left and right volumes simultaneously, with zero cross enabled, the sequence would be as detailed in Table 5.

It is recommended to perform a calibration of the DC Servo input channel before using the Input PGA Zero Cross Detector.

REGISTER	VALUE	COMMENT
R0 (00h) Left Channel PGA	0bxx1x_xxxx	LIZC = 1: Enable Left Input PGA Zero Cross Detector
R1 (01h) Right Channel PGA	0bxx1x_xxxx	RIZC = 1: Enable Right Input PGA Zero Cross Detector
R0 (00h) Left Channel PGA	0b001y_yyyy	IPVU = 0; LINMUTE = 0; LIZC = 1; LINVOL [5:0] = 0by_yyyy: Apply Left Input PGA volume setting, keep Zero Cross enabled, store update.
R1 (01h) Right Channel PGA	0b101y_yyyy	IPVU = 1; RINMUTE = 0; RLIZC = 1; RINVOL [5:0] = 0by_yyyy: Apply Right Input PGA volume setting, keep Zero Cross enabled, update left and right channel gains simultaneously.

Table 5 Simultaneous Volume update with Zero Cross

In the event of a long period without zero-crossings, a timeout function is available. When this function is enabled (using the TOEN register bit), the volume will update automatically after a timeout. The timeout period is set by CLK_TO_DIV[2:0] Note that SYSCLK must be running to use this function.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 (00h) Left Channel PGA	8	IPVU	0	Input PGA Volume Update 0 = Store LINVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = LINVOL, right = intermediate latch)
	7	LINMUTE	1	Left Input PGA Analogue Mute 1 = Enable Mute 0 = Disable Mute Note: IPVU must be set to un-mute.
	6	LIZC	0	Left Input PGA Zero Cross Detector. Requires separate register write before volume setting. 1 = Change gain on zero cross only 0 = Change gain immediately
	5:0	LINVOL [5:0]	011111 (0dB)	Left Input PGA Volume Control 111111 = +24dB 111110 = +23.25dB . . 0.75dB steps down to 000000 = -23.25dB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 (01h) Right Channel PGA	8	IPVU	0	Input PGA Volume Update 0 = Store RINVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (right = RINVOL, left = intermediate latch)
	7	RINMUTE	1	Right Input PGA Analogue Mute 1 = Enable Mute 0 = Disable Mute Note: IPVU must be set to un-mute.
	6	RIZC	0	Right Input PGA Zero Cross Detector. Requires separate register write before volume setting. 1 = Change gain on zero cross only 0 = Change gain immediately
	5:0	RINVOL [5:0]	011111 (0dB)	Right Input PGA Volume Control 111111 = +24dB 111110 = +23.25dB . . 0.75dB steps down to 000000 = -23.25dB
R23 (17h) Additional control(1)	0	TOEN	0	Timeout Enable 0 = Timeout disabled 1 = Timeout enabled
R30 (1Eh) Clocking 3	8:7	CLK_TO_DIV[1:0]	00	Timeout/slow clock divider setting 00 : 125Hz (timeout = 8ms) 01 : 250Hz (timeout = 4ms) 10 : 500Hz (timeout = 2ms) 11 : 1kHz (timeout = 1ms)

Table 6 Input PGA Volume Control

See "Volume Updates" section for a more detailed description of the volume update function, the zero cross function and the timeout operation

INPUT BOOST STAGE

The output of the PGA volume control stage is fed to the boost stage input. The input boost amplifier is a second order MFB active filter with selectable step gain. The boost stage provides the capability of adding large step gains to the output of the PGA. The output of the boost stage feeds into the ADC. To prevent large step outputs from the ADC, the boost gain should only be set during initial configuration.

The boost stage can provide up to +29dB additional gain from the PGA output to the ADC input, providing a total maximum available analogue gain of +53dB from microphone to ADC. Microphone PGA to boost gain settings are shown in Table 7.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32 (20h) ADCL signal path	5:4	LMICBOOST [1:0]	00	Left Channel Input PGA Boost Gain 00 = +0dB 01 = +13dB 10 = +20dB 11 = +29dB
R33 (21h) ADCR signal path	5:4	RMICBOOST [1:0]	00	Right Channel Input PGA Boost Gain 00 = +0dB 01 = +13dB 10 = +20dB 11 = +29dB

Table 7 Microphone PGA Boost Control

The output of the boost stage drives the ADC.

MICROPHONE INPUT CONNECTION EXAMPLE AND MICROPHONE BIASING

The input PGAs can be configured to use a single-ended input microphone. In the single ended microphone input configuration the microphone signal can be input to LINPUT. An example of this is shown in Figure 13 which also shows the microphone biasing.

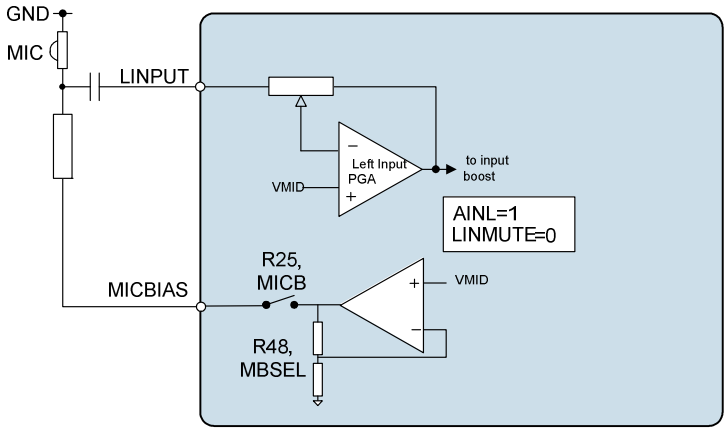


Figure 13 Single Ended Microphone Configuration Example

MICROPHONE BIASING CIRCUIT

The MICBIAS output pin provides a low noise reference voltage suitable for biasing electret type microphones and the associated external resistor biasing network. Refer to the Applications Information section for recommended external components. The MICBIAS voltage can be altered via the MBSEL register bit. When MBSEL=0, MICBIAS=5/6×AVDD and when MBSEL=1, MICBIAS=7/6×AVDD. The output can be enabled or disabled using the MICB control bit. (Note that MBSEL=1 only allowed if MICVDD is greater than +2.40V)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R25 (19h) Power management (1)	1	MICB	0	Microphone Bias Enable 0 = OFF (high impedance output) 1 = ON
R48 (30h) Additional Control (4)	0	MBSEL	1	Microphone Bias Voltage Control 1 = 7/6 * AVDD 0 = 5/6 * AVDD

Table 8 Microphone Bias Control

The internal MICBIAS circuitry is shown in Figure 14.

The maximum source current capability for MICBIAS is 2mA. The external biasing resistors therefore must be large enough to limit the MICBIAS current to 2mA.

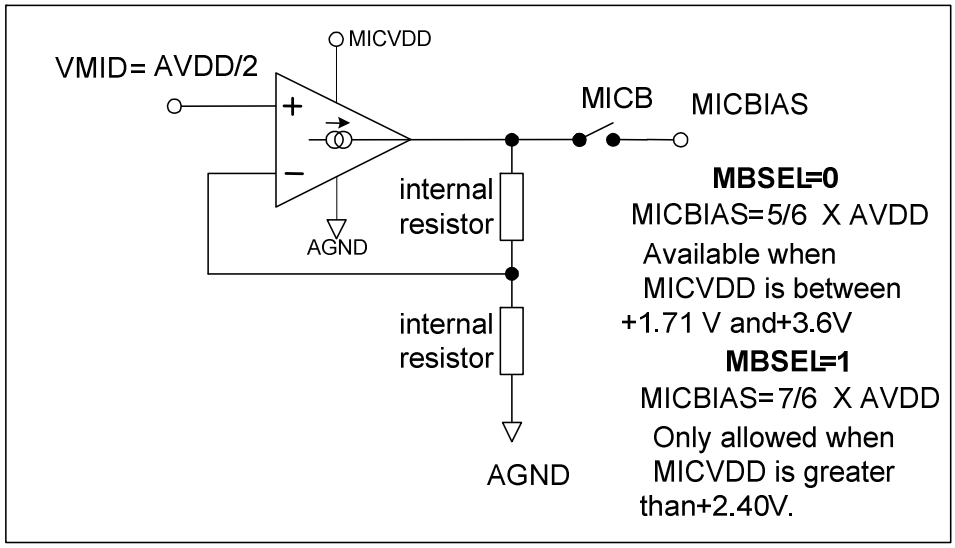


Figure 14 Microphone Bias Schematic

ANALOGUE TO DIGITAL CONVERTER (ADC)

The WM8961 uses stereo 24-bit, 128x over-sampled sigma-delta ADCs. The use of multi-bit feedback and high over-sampling rates reduce the effects of jitter and high frequency noise. The ADC Full Scale input level is proportional to AVDD. With a 1.8V supply voltage, the full scale level is $0.5V_{rms}$. Any voltage greater than full scale may overload the ADC and cause distortion.

The ADCs are enabled by the ADCL/R register bit. Note that when disabling the ADC, the digital volume control LADCVOL/RADCVOL[7:0] (R21 (15h)) should be muted (set to 00h), before clearing ADCL or ADCR to 0. This ensures that the last ADC code does not appear at the Audio Interface (ADCDAT) pin when ADCL/R are cleared.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R25 (19h) Power management (1)	3	ADCL	0	Enable ADC left channel: 0 = ADC disabled 1 = ADC enabled
	2	ADCR	0	Enable ADC right channel: 0 = ADC disabled 1 = ADC enabled

Table 9 ADC Enable Control

ADCDIV determines the ADC operating clock. The output of ADCDIV should be configured to output a clock of 256fs. The 256fs output of ADCDIV is further divided such that the ADC operates at 128fs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4 (04h) Clocking1	8:6	ADCDIV[2:0]	000	Defines the ADC 256fs clock, which is further divided by 2. 000 : 256fs = SYSCLK / 1.0 (default =12.288MHz, fs= 48 KHz) 001 : Reserved 010 : 256fs = SYSCLK / 2 011 : 256fs = SYSCLK / 3 100 : 256fs = SYSCLK / 4 101 : 256fs = SYSCLK / 5.5 110 : 256fs = SYSCLK / 6 111 : Reserved

The polarity of the output signal can be changed under software control using the ADCPOL[1:0] register bits.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) ADC and DAC Control 1	6:5	ADCPOL[1:0]	00	ADC Data invert 00 : Both Channels normal polarity 01 : Left Channel Inverted 10 : Right Channel Inverted 11 : Both Channels Inverted

Table 10 ADC Polarity Select

ADC DIGITAL VOLUME CONTROL

The output of the ADCs can be digitally amplified or attenuated over a range from -71.625dB to +17.625dB in 0.375dB steps. The volume of each channel can be controlled separately. The gain for a given eight-bit code X is given by:

$0.375 \times (X-192)$ dB for $1 \leq X \leq 239$; MUTE for $X = 0$ +17.625dB for $239 \leq X \leq 255$

The ADCVU bit controls the loading of digital volume control data. When ADCVU is set to 0, the LADCVOL or RADCVOL control data will be loaded into the respective control register, but will not actually change the digital gain setting. Both left and right gain settings are updated when a 1 is written to ADCVU. This makes it possible to update the gain of both channels simultaneously.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R21 (15h) Left ADC Digital Volume	7:0	LADCVOL [7:0]	1100_0000 (0dB)	ADC Left Channel Digital Volume. FFh -> Efh: +17.625dB EEh: +17.25dB …… in steps of -0.375dB to C0h : 0dB BFh : -0.375dB BEh: -0.75dB ….. in steps of -0.375dB to 02h: -71.25dB 01h: -71.625dB 00h: Digital Mute (refer to Table 12)
	8	ADCVU	0	ADC Volume Update 0 = Store LADCVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = LADCVOL, right = intermediate latch)
R22 (16h) Right ADC Digital Volume	7:0	RADCVOL [7:0]	1100_0000 (0dB)	ADC Right Channel Digital Volume. FFh -> Efh: +17.625dB EEh: +17.25dB …… in steps of -0.375dB to C0h : 0dB BFh : -0.375dB BEh: -0.75dB ….. in steps of -0.375dB to 02h: -71.25dB 01h: -71.625dB 00h: Digital Mute (refer to Table 12)
	8	ADCVU	0	ADC Volume Update 0 = Store RADCVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = intermediate latch, right = RADCVOL)

Table 11 ADC Digital Volume Control

Table 12 shows all possible ADC digital volume values.

LADCVOL or RADCVOL	Volume (dB)	LADCVOL or RADCVOL	Volume (dB)	LADCVOL or RADCVOL	Volume (dB)	LADCVOL or RADCVOL	Volume (dB)
0h	MUTE	40h	-48.000	80h	-24.000	C0h	0.000
1h	-71.625	41h	-47.625	81h	-23.625	C1h	0.375
2h	-71.250	42h	-47.250	82h	-23.250	C2h	0.750
3h	-70.875	43h	-46.875	83h	-22.875	C3h	1.125
4h	-70.500	44h	-46.500	84h	-22.500	C4h	1.500
5h	-70.125	45h	-46.125	85h	-22.125	C5h	1.875
6h	-69.750	46h	-45.750	86h	-21.750	C6h	2.250
7h	-69.375	47h	-45.375	87h	-21.375	C7h	2.625
8h	-69.000	48h	-45.000	88h	-21.000	C8h	3.000
9h	-68.625	49h	-44.625	89h	-20.625	C9h	3.375
Ah	-68.250	4Ah	-44.250	8Ah	-20.250	CAh	3.750
Bh	-67.875	4Bh	-43.875	8Bh	-19.875	CBh	4.125
Ch	-67.500	4Ch	-43.500	8Ch	-19.500	CCh	4.500
Dh	-67.125	4Dh	-43.125	8Dh	-19.125	CDh	4.875
Eh	-66.750	4Eh	-42.750	8Eh	-18.750	CEh	5.250
Fh	-66.375	4Fh	-42.375	8Fh	-18.375	CFh	5.625
10h	-66.000	50h	-42.000	90h	-18.000	D0h	6.000
11h	-65.625	51h	-41.625	91h	-17.625	D1h	6.375
12h	-65.250	52h	-41.250	92h	-17.250	D2h	6.750
13h	-64.875	53h	-40.875	93h	-16.875	D3h	7.125
14h	-64.500	54h	-40.500	94h	-16.500	D4h	7.500
15h	-64.125	55h	-40.125	95h	-16.125	D5h	7.875
16h	-63.750	56h	-39.750	96h	-15.750	D6h	8.250
17h	-63.375	57h	-39.375	97h	-15.375	D7h	8.625
18h	-63.000	58h	-39.000	98h	-15.000	D8h	9.000
19h	-62.625	59h	-38.625	99h	-14.625	D9h	9.375
1Ah	-62.250	5Ah	-38.250	9Ah	-14.250	DAh	9.750
1Bh	-61.875	5Bh	-37.875	9Bh	-13.875	DBh	10.125
1Ch	-61.500	5Ch	-37.500	9Ch	-13.500	DCh	10.500
1Dh	-61.125	5Dh	-37.125	9Dh	-13.125	DDh	10.875
1Eh	-60.750	5Eh	-36.750	9Eh	-12.750	DEh	11.250
1Fh	-60.375	5Fh	-36.375	9Fh	-12.375	DFh	11.625
20h	-60.000	60h	-36.000	A0h	-12.000	E0h	12.000
21h	-59.625	61h	-35.625	A1h	-11.625	E1h	12.375
22h	-59.250	62h	-35.250	A2h	-11.250	E2h	12.750
23h	-58.875	63h	-34.875	A3h	-10.875	E3h	13.125
24h	-58.500	64h	-34.500	A4h	-10.500	E4h	13.500
25h	-58.125	65h	-34.125	A5h	-10.125	E5h	13.875
26h	-57.750	66h	-33.750	A6h	-9.750	E6h	14.250
27h	-57.375	67h	-33.375	A7h	-9.375	E7h	14.625
28h	-57.000	68h	-33.000	A8h	-9.000	E8h	15.000
29h	-56.625	69h	-32.625	A9h	-8.625	E9h	15.375
2Ah	-56.250	6Ah	-32.250	AAh	-8.250	EAh	15.750
2Bh	-55.875	6Bh	-31.875	ABh	-7.875	EBh	16.125
2Ch	-55.500	6Ch	-31.500	ACh	-7.500	ECh	16.500
2Dh	-55.125	6Dh	-31.125	ADh	-7.125	EDh	16.875
2Eh	-54.750	6Eh	-30.750	AEh	-6.750	EEh	17.250
2Fh	-54.375	6Fh	-30.375	AFh	-6.375	EFh	17.625
30h	-54.000	70h	-30.000	B0h	-6.000	F0h	17.625
31h	-53.625	71h	-29.625	B1h	-5.625	F1h	17.625
32h	-53.250	72h	-29.250	B2h	-5.250	F2h	17.625
33h	-52.875	73h	-28.875	B3h	-4.875	F3h	17.625
34h	-52.500	74h	-28.500	B4h	-4.500	F4h	17.625
35h	-52.125	75h	-28.125	B5h	-4.125	F5h	17.625
36h	-51.750	76h	-27.750	B6h	-3.750	F6h	17.625
37h	-51.375	77h	-27.375	B7h	-3.375	F7h	17.625
38h	-51.000	78h	-27.000	B8h	-3.000	F8h	17.625
39h	-50.625	79h	-26.625	B9h	-2.625	F9h	17.625
3Ah	-50.250	7Ah	-26.250	BAh	-2.250	FAh	17.625
3Bh	-49.875	7Bh	-25.875	BBh	-1.875	FBh	17.625
3Ch	-49.500	7Ch	-25.500	BCh	-1.500	FCh	17.625
3Dh	-49.125	7Dh	-25.125	BDh	-1.125	FDh	17.625
3Eh	-48.750	7Eh	-24.750	BEh	-0.750	FEh	17.625
3Fh	-48.375	7Fh	-24.375	BFh	-0.375	FFh	17.625

Table 12 ADC Digital Volume Range

ADC DIGITAL FILTERS

The ADC filters perform true 24-bit signal processing to convert the raw multi-bit over-sampled data from the ADC to the correct sampling frequency to be output on the digital audio interface.

ADC HIGH PASS FILTER

A digital high pass filter is applied by default to the ADC path to remove DC offsets. This filter can also be programmed to remove low frequency noise in voice applications (e.g. wind noise or mechanical vibration).

This filter can be disabled using the ADCHPD register bit. The cut-off frequency of the filter is controlled by ADC_HPF_CUT.

In hi-fi mode the high pass filter is optimised for removing DC offsets without degrading the bass response and has a cut-off frequency of 3.7Hz at fs=44.1kHz.

In voice mode the high pass filter is optimised for voice communication and it is recommended to program the cut-off frequency below 300Hz (e.g. ADC_HPF_CUT=11 at fs=8kHz or ADC_HPF_CUT=10 at fs=16kHz)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) ADC and DAC Control (1)	0	ADCHPD	0	ADC High Pass Filter Disable 0 = Enable high pass filter on left and right channels 1 = Disable high pass filter on left and right channels
R6 (06h) ADC & DAC Control 2	8:7	ADC_HPF_CUT[1:0]	00	ADC High Pass Filter Cutoff 00: Hi-fi mode (fc=4Hz at fs=48kHz) 01: Voice mode 1 (fc=127 at fs=16kHz) 10: Voice mode 2 (fc=130 at fs=8kHz) 11: Voice mode 3 (fc=267Hz at fs=8kHz) (Note: fc scales with sample rate. See Table 14 for cut-off frequencies at all supported sample rates)

Table 13 ADC High Pass Filter

SAMPLE FREQUENCY (KHZ)	CUT-OFF FREQUENCY (HZ)			
	ADC_HPF_CUT =00	ADC_HPF_CUT =01	ADC_HPF_CUT =10	ADC_HPF_CUT =11
8.000	0.7	64	130	267
11.025	0.9	88	178	367
16.000	1.3	127	258	532
22.050	1.9	175	354	733
24.000	2.0	190	386	798
32.000	2.7	253	514	1063
44.100	3.7	348	707	1464
48.000	4.0	379	770	1594

Table 14 ADC High Pass Filter Cut-Off Frequencies

The high pass filter characteristics are shown in the “Digital Filter Characteristics” section.

AUTOMATIC LEVEL CONTROL (ALC)

The WM8961 has an automatic level control that aims to keep a constant recording volume irrespective of the input signal level. This is achieved by continuously adjusting the input PGA gain so that the signal level at the ADC input remains constant. A digital peak detector monitors the ADC output and changes the PGA gain if necessary. Note that when the ALC function is enabled, the settings of registers 0 and 1 (LINVOL, IPVU, LIZC, LINMUTE, RINVOL, RIZC and RINMUTE) are ignored.

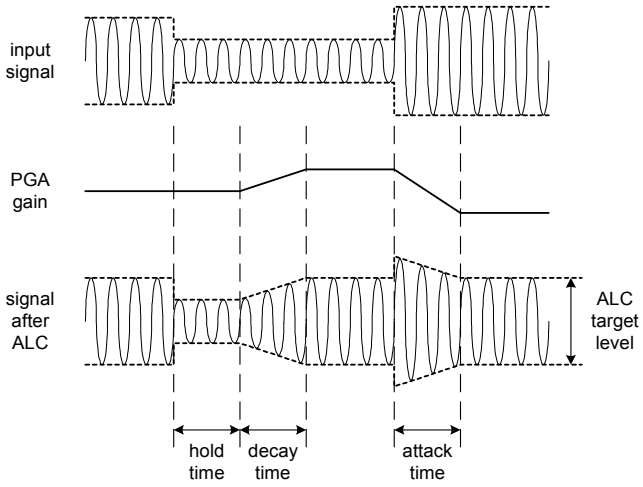


Figure 15 ALC Operation

The ALC function is enabled using the ALCSEL control bits. When enabled, the recording volume can be programmed between –6dB and –28.5dB (relative to ADC full scale) using the ALCL register bits. An upper limit for the PGA gain can be imposed by setting the MAXGAIN control bits. An lower limit for the PGA gain can be imposed by setting the MINGAIN control bits.

HLD, DCY and ATK control the hold, decay and attack times, respectively:

Hold time is the time delay between the peak level detected being below target and the PGA gain beginning to ramp up. It can be programmed in power-of-two (2^n) steps, e.g. 2.67ms, 5.33ms, 10.67ms etc. up to 43.7s. Alternatively, the hold time can also be set to zero. The hold time only applies to gain ramp-up; there is no delay before ramping the gain down when the signal level is above target.

Decay (Gain Ramp-Up) Time is the time that it takes for the PGA gain to ramp up across 90% of its range (for example from –21B up to 21.75dB). The time it takes for the recording level to return to its target value therefore depends on both the decay time and on the gain adjustment required. If the gain adjustment is small, it will be shorter than the decay time. The decay time can be programmed in power-of-two (2^n) steps, from 24ms, 48ms, 96ms, etc. to 24.58s.

Attack (Gain Ramp-Down) Time is the time that it takes for the PGA gain to ramp down across 90% of its range (for example from 21.75dB down to -21B gain). The time it takes for the recording level to return to its target value therefore depends on both the attack time and on the gain adjustment required. If the gain adjustment is small, it will be shorter than the attack time. The attack time can be programmed in power-of-two (2^n) steps, from 6ms, 12ms, 24ms, etc. to 6.14s.

When operating in stereo, the peak detector takes the maximum of left and right channel peak values, and any new gain setting is applied to both left and right PGAs, so that the stereo image is preserved. The input PGA and MICBOOST gain settings should be identical when entering ALC stereo mode in order for gain updates to be applied correctly.

The ALC function can also be enabled on one channel only. In this case, only one PGA is controlled by the ALC mechanism, while the other channel runs independently with its PGA gain set through the control register.

When one ADC channel is unused, the peak detector disregards that channel.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R17 (11h) ALC Control (1)	8:7	ALCSEL [1:0]	00 (OFF)	ALC Function Select 00 = ALC off (PGA gain set by register) 01 = Right channel only 10 = Left channel only 11 = Stereo (PGA registers unused) Note: ensure that LINVOL and RINVOL settings (reg. 0 and 1) are the same before entering this mode.
	6:4	MAXGAIN [2:0]	111 (+24dB)	Set Maximum Gain of PGA 111 : +24dB 110 : +18dB ….(-6dB steps) 001 : -12dB 000 : -18dB
	3:0	ALCL [3:0]	1011 (-12dB)	ALC Target (Sets signal level at ADC input) 0000 = -28.5dB FS 0001 = -27.0dB FS … (1.5dB steps) 1110 = -7.5dB FS 1111 = -6dB FS
R18 (12h) ALC Control (2)	6:4	MINGAIN [2:0]	000	Set Minimum Gain of PGA 000 = -23.25dB 001 = -17.25dB 010 = -11.25dB 011 = -5.25dB 100 = +0.75dB 101 = +6.75dB 110 = +12.75dB 111 = +18.75dB
	3:0	HLD [3:0]	0000 (0ms)	ALC hold time before gain is increased. 0000 = 0ms 0001 = 2.67ms 0010 = 5.33ms … (time doubles with every step) 1111 = 43.691s
R19 (13h) ALC Control (3)	8	ALCMODE	0	Determines the ALC mode of operation: 0 = ALC mode 1 = Limiter mode ALCSEL[1:0] bits must be set to 00 before changing this bit.
	7:4	DCY [3:0]	0011 (192ms)	ALC decay (gain ramp-up) time 0000 = 24ms 0001 = 48ms 0010 = 96ms … (time doubles with every step) 1010 or higher = 24.58s

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3:0	ATK [3:0]	0010 (24ms)	ALC attack (gain ramp-down) time 0000 = 6ms 0001 = 12ms 0010 = 24ms … (time doubles with every step) 1010 or higher = 6.14s
R27 (1Bh) Additional Control (3)	2:0	SAMPLE_RATE[2:0]	000	ALC Sample Rate 000 = 44.1k / 48k 001 = 32k 010 = 22.05k / 24k 011 = 16k 100 = 11.25k / 12k 101 = 8k 110 and 111 = Reserved

Table 15 ALC Control

ALC SAMPLE RATE CONTROL

The register bits R27[2:0],SAMPLE_RATE must be set correctly to ensure that the ALC attack, decay and hold times are correct for the chosen sample rate as shown in Table 15.

PEAK LIMITER

To prevent clipping when a large signal occurs just after a period of quiet, the ALC circuit includes a limiter function. If the ADC input signal exceeds 87.5% of full scale (–1.16dB), the PGA gain is ramped down at the maximum attack rate (as when ATK = 0000), until the signal level falls below 87.5% of full scale. This function is automatically enabled whenever the ALC is enabled.

Note:

If ATK = 0000, then the limiter makes no difference to the operation of the ALC. It is designed to prevent clipping when long attack times are used.

NOISE GATE

When the signal is very quiet and consists mainly of noise, the ALC function may cause “noise pumping”, i.e. loud hissing noise during silence periods. The WM8961 has a noise gate function that prevents noise pumping by comparing the signal level at the input pins against a noise gate threshold, NGTH. The noise gate cuts in when:

Signal level at ADC [dB] < NGTH [dB] + PGA gain [dB] + Mic Boost gain [dB]

This is equivalent to:

Signal level at input pin [dB] < NGTH [dB]

The PGA gain can then either be muted or held constant (preventing it from ramping up as it normally would when the signal is quiet) using the NGG bit.

The table below summarises the noise gate control register. The NGTH control bits set the noise gate threshold with respect to the ADC full-scale range. The threshold is adjusted in 1.5dB steps. Levels at the extremes of the range may cause inappropriate operation, so care should be taken with set–up of the function. Note that the noise gate only works in conjunction with the ALC function, and always operates on the same channel(s) as the ALC (left, right, both, or none).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R20 (14h) Noise Gate Control	7:3	NGTH [4:0]	00000	Noise gate threshold 00000 -76.5dBfs 00001 -75dBfs … 1.5 dB steps 11110 -31.5dBfs 11111 -30dBfs
	1	NGG	0	Noise gate mode 0 : Hold PGA gain static when noise gate triggers (recommended) 1 : Mute ADC output when noise gate triggers.
	0	NGAT	0	Noise gate function enable 0 = disable 1 = enable

Table 16 Noise Gate Control

OUTPUT SIGNAL PATH

The WM8961 DACs receive digital input data from the DACDAT pin of the AIF and via the digital side-tone path.

The digital filter block of the DACs process the data to provide the following functions:

- Digital volume control with soft mute and soft un-mute
- Mono mix
- De-emphasis
- Sigma-delta modulation

The analogue outputs from the DACs are fed to the analogue volume PGA control. The output from the analogue volume control is routed to the output drivers for headphone and speaker output. This output stage is shown in Figure 16.

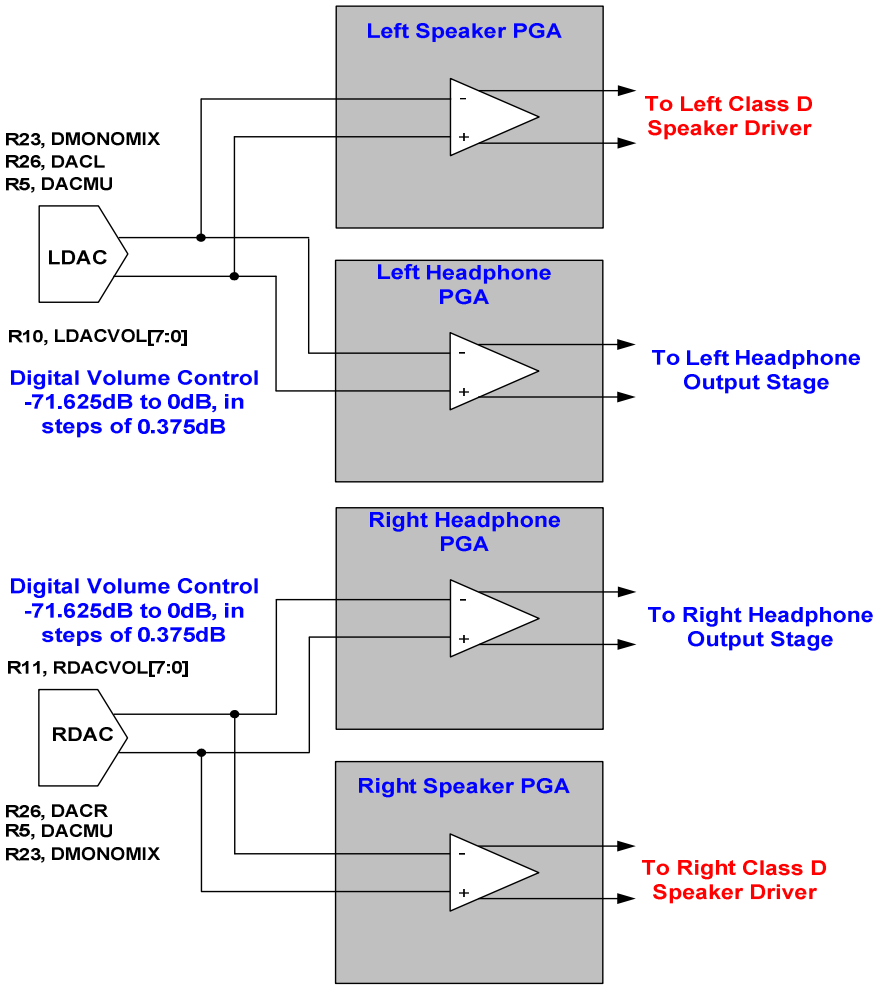


Figure 16 DAC Output Stage

DIGITAL TO ANALOGUE CONVERTER (DAC)

Digital data is passed to the WM8961 via the flexible audio interface to the hi-fi DACs. The digital audio data is converted to over-sampled bit streams in the on-chip, true 24-bit digital interpolation filters. The bit-stream data enters two multi-bit, sigma-delta DACs, which convert them to high quality analogue audio signals. The multi-bit DAC architecture reduces high frequency noise and sensitivity to clock jitter. It also uses a Dynamic Element Matching technique for high linearity and low distortion.

The DACs and digital filters are enabled by the DACL and DACR register bits.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R26 (1Ah) Power Management (2)	8	DACL	0	Left Channel DAC Enable 0 = DAC disabled 1 = DAC enabled
	7	DACR	0	Right Channel DAC Enable 0 = DAC disabled 1 = DAC enabled

Table 17 DAC Enable Control

DAC DIGITAL VOLUME CONTROL

The output level (digital volume) of each DAC can be controlled digitally over a range from -71.625dB to 0dB in 0.375dB steps. The level of attenuation for an eight-bit code X is given by:

$0.375 \times (X-192)$ dB for $1 \leq X \leq 192$; MUTE for $X = 0$ 0dB for $192 \leq X \leq 255$

The DACVU bit controls the loading of digital volume control data. When DACVU is set to 0, the LDACVOL or RDACVOL control data will be loaded into the respective control register, but will not actually change the digital gain setting. Both left and right gain settings are updated when a 1 is written to DACVU. This makes it possible to update the gain of both channels simultaneously.

See "Volume Updates" section for a description of the volume update function, the zero cross function and the timeout operation.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R10 (0Ah) Left Channel Digital Volume	8	DACVU	0	DAC Volume Update 0 = Store LDACVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = LDACVOL, right = intermediate latch)
	7:0	LDACVOL [7:0]	11111111 (0dB)	Left DAC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -71.625dB 0000 0010 = -71.250dB ... 0.375dB steps up to 1100 0000 = 0dB …. 1111 1111 = 0dB (See Table 19 for volume range)
R11 (0Bh) Right Channel Digital Volume	8	DACVU	0	DAC Volume Update 0 = Store RDACVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = intermediate latch, right = RDACVOL)
	7:0	RDACVOL [7:0]	11111111 (0dB)	Right DAC Digital Volume Control similar to LDACVOL (See Table 19 for volume range)

Table 18 Digital Volume Control

Table 19 shows the DAC Digital Volume Range.

LDACVOL or RDACVOL	Volume (dB)	LDACVOL or RDACVOL	Volume (dB)	LDACVOL or RDACVOL	Volume (dB)	LDACVOL or RDACVOL	Volume (dB)
0h	MUTE	40h	-48.000	80h	-24.000	C0h	0.000
1h	-71.625	41h	-47.625	81h	-23.625	C1h	0.000
2h	-71.250	42h	-47.250	82h	-23.250	C2h	0.000
3h	-70.875	43h	-46.875	83h	-22.875	C3h	0.000
4h	-70.500	44h	-46.500	84h	-22.500	C4h	0.000
5h	-70.125	45h	-46.125	85h	-22.125	C5h	0.000
6h	-69.750	46h	-45.750	86h	-21.750	C6h	0.000
7h	-69.375	47h	-45.375	87h	-21.375	C7h	0.000
8h	-69.000	48h	-45.000	88h	-21.000	C8h	0.000
9h	-68.625	49h	-44.625	89h	-20.625	C9h	0.000
Ah	-68.250	4Ah	-44.250	8Ah	-20.250	CAh	0.000
Bh	-67.875	4Bh	-43.875	8Bh	-19.875	CBh	0.000
Ch	-67.500	4Ch	-43.500	8Ch	-19.500	CCh	0.000
Dh	-67.125	4Dh	-43.125	8Dh	-19.125	CDh	0.000
Eh	-66.750	4Eh	-42.750	8Eh	-18.750	CEh	0.000
Fh	-66.375	4Fh	-42.375	8Fh	-18.375	CFh	0.000
10h	-66.000	50h	-42.000	90h	-18.000	D0h	0.000
11h	-65.625	51h	-41.625	91h	-17.625	D1h	0.000
12h	-65.250	52h	-41.250	92h	-17.250	D2h	0.000
13h	-64.875	53h	-40.875	93h	-16.875	D3h	0.000
14h	-64.500	54h	-40.500	94h	-16.500	D4h	0.000
15h	-64.125	55h	-40.125	95h	-16.125	D5h	0.000
16h	-63.750	56h	-39.750	96h	-15.750	D6h	0.000
17h	-63.375	57h	-39.375	97h	-15.375	D7h	0.000
18h	-63.000	58h	-39.000	98h	-15.000	D8h	0.000
19h	-62.625	59h	-38.625	99h	-14.625	D9h	0.000
1Ah	-62.250	5Ah	-38.250	9Ah	-14.250	DAh	0.000
1Bh	-61.875	5Bh	-37.875	9Bh	-13.875	DBh	0.000
1Ch	-61.500	5Ch	-37.500	9Ch	-13.500	DCh	0.000
1Dh	-61.125	5Dh	-37.125	9Dh	-13.125	DDh	0.000
1Eh	-60.750	5Eh	-36.750	9Eh	-12.750	DEh	0.000
1Fh	-60.375	5Fh	-36.375	9Fh	-12.375	DFh	0.000
20h	-60.000	60h	-36.000	A0h	-12.000	E0h	0.000
21h	-59.625	61h	-35.625	A1h	-11.625	E1h	0.000
22h	-59.250	62h	-35.250	A2h	-11.250	E2h	0.000
23h	-58.875	63h	-34.875	A3h	-10.875	E3h	0.000
24h	-58.500	64h	-34.500	A4h	-10.500	E4h	0.000
25h	-58.125	65h	-34.125	A5h	-10.125	E5h	0.000
26h	-57.750	66h	-33.750	A6h	-9.750	E6h	0.000
27h	-57.375	67h	-33.375	A7h	-9.375	E7h	0.000
28h	-57.000	68h	-33.000	A8h	-9.000	E8h	0.000
29h	-56.625	69h	-32.625	A9h	-8.625	E9h	0.000
2Ah	-56.250	6Ah	-32.250	AAh	-8.250	EAh	0.000
2Bh	-55.875	6Bh	-31.875	ABh	-7.875	EBh	0.000
2Ch	-55.500	6Ch	-31.500	ACh	-7.500	ECh	0.000
2Dh	-55.125	6Dh	-31.125	ADh	-7.125	EDh	0.000
2Eh	-54.750	6Eh	-30.750	AEh	-6.750	EEh	0.000
2Fh	-54.375	6Fh	-30.375	AFh	-6.375	EFh	0.000
30h	-54.000	70h	-30.000	B0h	-6.000	F0h	0.000
31h	-53.625	71h	-29.625	B1h	-5.625	F1h	0.000
32h	-53.250	72h	-29.250	B2h	-5.250	F2h	0.000
33h	-52.875	73h	-28.875	B3h	-4.875	F3h	0.000
34h	-52.500	74h	-28.500	B4h	-4.500	F4h	0.000
35h	-52.125	75h	-28.125	B5h	-4.125	F5h	0.000
36h	-51.750	76h	-27.750	B6h	-3.750	F6h	0.000
37h	-51.375	77h	-27.375	B7h	-3.375	F7h	0.000
38h	-51.000	78h	-27.000	B8h	-3.000	F8h	0.000
39h	-50.625	79h	-26.625	B9h	-2.625	F9h	0.000
3Ah	-50.250	7Ah	-26.250	BAh	-2.250	FAh	0.000
3Bh	-49.875	7Bh	-25.875	BBh	-1.875	FBh	0.000
3Ch	-49.500	7Ch	-25.500	BCh	-1.500	FCh	0.000
3Dh	-49.125	7Dh	-25.125	BDh	-1.125	FDh	0.000
3Eh	-48.750	7Eh	-24.750	BEh	-0.750	FEh	0.000
3Fh	-48.375	7Fh	-24.375	BFh	-0.375	FFh	0.000

Table 19 DAC Digital Volume Range

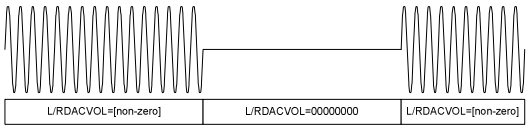
DAC SOFT MUTE AND SOFT UN-MUTE

The WM8961 also has a soft mute function, which, when enabled, gradually attenuates the volume of the digital signal to zero. When soft mute is disabled, the gain will either gradually ramp back up to the digital gain setting, or return instantly to the digital gain setting, depending on the DACSMM register bit.

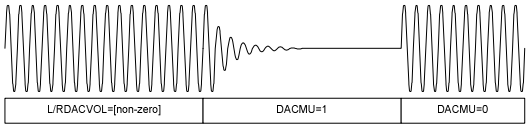
The DAC is soft-muted by default. To play back an audio signal, this function must first be disabled by setting the DACMU bit to zero.

DACSMM would typically be enabled when using soft mute during playback of audio data so that when soft mute is then disabled, the sudden volume increase will not create pop noise by jumping immediately to the previous volume level (e.g. resuming playback after pausing during a track).

DACSMM would typically be disabled when un-muting at the start of a digital music file, so that the first part of the track is not attenuated (e.g. when starting playback of a new track, or resuming playback after pausing between tracks).

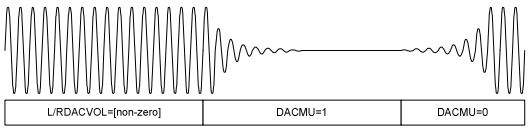


DAC muting and un-muting using volume control bits LDACVOL and RDACVOL.



DAC muting and un-muting using soft mute bit DACMU.

Soft un-mute not enabled (DACSMM = 0).



DAC muting and un-muting using soft mute bit DACMU.

Soft un-mute enabled (DACSMM = 1).

Figure 17 DAC Mute Control

The volume ramp rate during soft mute and un-mute is controlled by the DACMR bit. Ramp rates of fs/32 and fs/2 are selectable as shown in Table 20 (fs = DAC sample rate).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) ADC and DAC Control (1)	3	DACMU	1	Digital Soft Mute 1 = Mute 0 = No mute (signal active)
R6 (06h) ADC and DAC Control (2)	3	DACSMM	0	DAC Soft Mute Mode 0 = Disabling soft-mute (DACMU=0) will cause the volume to change immediately to the LDACVOL / RDACVOL settings 1 = Disabling soft-mute (DACMU=0) will cause the volume to ramp up gradually to the LDACVOL / RDACVOL settings
	2	DACMR	0	DAC Soft Mute Ramp Rate 0 = Fast ramp (fs/2 at fs=48k, providing maximum delay of 10.7ms) 1 = Slow ramp (fs/32 at fs=48k, providing maximum delay of 171ms)DAC Soft Mute Ramp Rate

Table 20 DAC Soft-Mute Control

DAC DE-EMPHASIS

Digital de-emphasis can be applied to the DAC playback data (e.g. when the data comes from a CD with pre-emphasis used in the recording). De-emphasis filtering is available for sample rates of 48kHz, 44.1kHz and 32kHz.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) ADC and DAC Control (1)	2:1	DEEMPH [1:0]	00	De-Emphasis Control 11 = 48kHz sample rate 10 = 44.1kHz sample rate 01 = 32kHz sample rate 00 = No de-emphasis

Table 21 DAC De-Emphasis Control

DAC MONO MIX

In normal operation, the left and right channel digital audio data is converted to analogue in two separate DACs. There is a mono-mix mode where the two audio channels are mixed together digitally and then converted to analogue using only one DAC (enabled DAC), while the other DAC must be disabled.

Only one DAC must be enabled in order to use this function.

A DAC digital mono-mix mode can be enabled using the DMONOMIX register bit.

To prevent clipping, a -6dB attenuation is automatically applied to the mono mix.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 (17h) Additional Control (1)	4	DMONOMIX	0	DAC Mono Mix 0 = Stereo 1 = Mono (Mono mix output on enabled DAC)

Table 22 DAC Mono Mix

DAC OUTPUT PHASE

The DAC output defaults to be non-inverted. Setting DACPOL[0] bit will invert the left DAC output phase and setting DACPOL[1] bit will invert the right DAC output phase.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 (06h) ADC and DAC Control (2)	6:5	DACPOL[1:0]	00	DAC Data invert 00 : Both Channels normal polarity 01 : Left Channel Inverted 10 : Right Channel Inverted 11 : Both Channels Inverted

Table 23 DAC Phase Invert Select

DAC SLOPING STOP-BAND FILTER

Two DAC filter types are available, selected by the register bit DACSLOPE. When operating at lower sample rates (e.g. during voice communication) it is recommended that the sloping stop-band filter type is selected (DACSLOPE =1) to reduce out-of-band noise which can be audible at low DAC sample rates. See "Digital Filter Characteristics" section for details of DAC filters characteristics.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 (06h) ADC & DAC Control 2	1	DACSLOPE	0	Selects DAC filter characteristics 0 = Normal mode 1 = Sloping stop-band mode

Table 24 DAC Sloping Stop-band Filter

DAC DIGITAL SIDETONE

A digital sidetone from the ADC is available at the DAC. Digital data from either left or right ADC can be mixed with the audio interface data on the left and right DAC channels. Sidetone data is taken from the ADC high pass filter output, to reduce low frequency noise which may be present in the sidetone (e.g. wind noise or mechanical vibration).

When using the digital sidetone, it is recommended that the ADCs are enabled before un-muting the DACs to prevent pop noise. The DAC volumes and sidetone volumes should be set to an appropriate level to avoid clipping at the DAC input.

Note that when the ADC sidetone is used for the headphone output, and dynamic (Class W) power saving is enabled (CP_DYN_PWR[1:0] = 0b11), the charge pump only monitors the DAC input level rather than the ADC sidetone level. An ADC sidetone signal which is louder than the DAC input signal could increase headphone output distortion because the charge pump settings are optimised for the quieter DAC input signal. Hence dynamic (Class W) power saving is not recommended when the ADC sidetone is louder than the DAC input. See also the 'Charge pump Clocking' section.

The digital sidetone is controlled as shown in Table 25.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R57 (39h) DSP Sidetone 0	7:4	ADCR_DAC_SVOL[3:0]	0000	Controls volume of ADC Right side tone, 3dB steps. 0000 : -36dB 0001 : -33dB … 1111 : 0dB (see Table 26)
	3:2	ADC_TO_DACR[1:0]	00	DAC Right Side-tone Control 11 = Unused 10 = Mix ADCR into DACR 01 = Mix ADCL into DACR 00 = No Side-tone mix into DACR
R58 (3Ah) DSP Sidetone 1	7:4	ADCL_DAC_SVOL[3:0]	0000	Controls volume of ADC Left side tone, 3dB steps. 0000 : -36dB 0001 : -33dB … 1111 : 0dB (see Table 26)
	3:2	ADC_TO_DACL[1:0]	00	DAC Left Side-tone Control 11 = Unused 10 = Mix ADCR into DACL 01 = Mix ADCL into DACL 00 = No Side-tone mix into DACL

Table 25 Digital Sidetone Control Registers

ADCL_DAC_SVOL or ADCR_DAC_SVOL	SIDETONE VOLUME
0000	-36
0001	-33
0010	-30
0011	-27
0100	-24
0101	-21
0110	-18
0111	-15
1000	-12
1001	-9
1010	-6
1011	-3
1100	0
1101	0
1110	0
1111	0

Table 26 Digital Sidetone Volume in dB

DAC OVERSAMPLING

In order to increase the signal to noise ratio (SNR) of the DAC output, the DAC_OSR128 register bit can be used to increase the oversampling rate of the DAC as shown in Table 31. The MANUAL_MODE register bit is detailed in "ADC and DAC Clocking and Sample Rates". There will be a slight increase in power consumption when 128OSR mode is selected.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 (06h) ADC & DAC Control 2	0	DAC_OSR128	0	DAC 128 Over Sampling Rate 0: 64x DAC oversampling 1: If MANUAL_MODE=0, automatically configure DACDIV[2:0] for 128OSR mode. This will give a SNR improvement at the expense of power

Table 27 DAC Oversampling Control

ANALOGUE OUTPUTS

WM8961 has 2 analogue output paths. One path drives a ground referenced headphone output which is powered by a charge pump. In this path, a DC servo is used to remove any offsets from the headphone outputs. The second path drives the Class D speaker outputs.

HEADPHONE OUTPUTS

The headphone output consists of 2 stages, a Volume PGA, followed by an output drive stage containing an integrated PGA, as illustrated in Figure 18. The headphone output stage must be enabled during normal operation, which permits power saving when not in use. The headphone bias current can be controlled to improve SNR. For details of the DC Servo, refer to the "DC Servo" section.

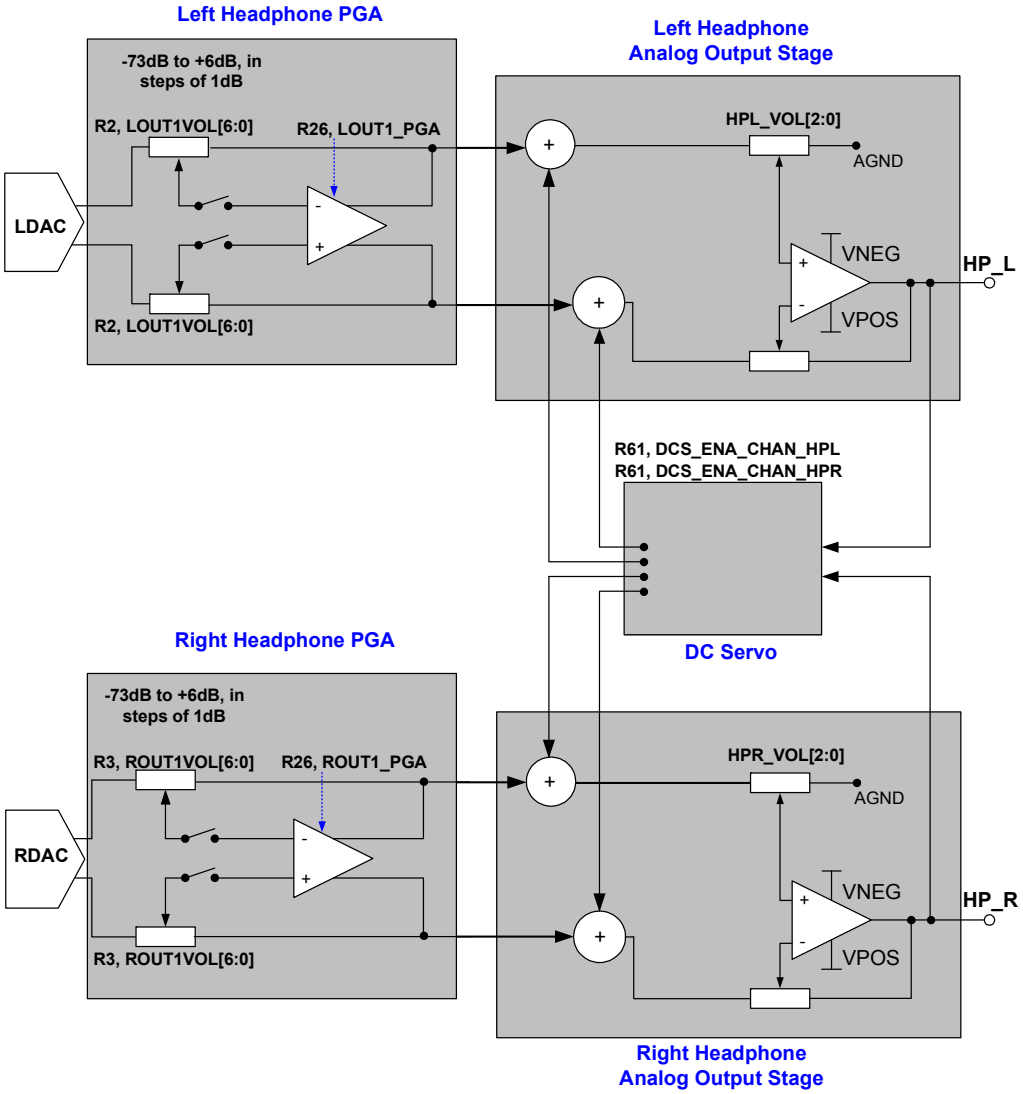


Figure 18 Headphone Analogue Output Stage

HEADPHONE VOLUME PGA

The signal volume on HP_L and HP_R can be independently adjusted under software control by writing to LOUT1VOL and ROUT1VOL, respectively. Note that gains over 0dB may cause clipping if the signal is large. Any gain setting below 0101111 (minimum) mutes the output driver.

The LOUT1VOL and ROUT1VOL register writes should only be carried out after the charge pump has been enabled, see the “Charge Pump” section for details.

A zero cross detect on the analogue output may also be enabled when changing the gain setting to minimize audible clicks and zipper noise as the gain updates. If zero cross is enabled a timeout is also available to update the gain if a zero cross does not occur. This function may be enabled by setting TOEN in register R23 (17h). The timeout period is set by CLK_TO_DIV[1:0]. The volume control PGAs are enabled using LOUT1_PGA and ROUT1_PGA.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h) LOUT1 Volume	8	OUT1VU	0	Headphone Volume Update 0 = Store LOUT1VOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = LOUT1VOL, right = intermediate latch)
	7	LO1ZC	0	Left zero cross enable 0 = Change gain immediately 1 = Change gain on zero cross only
	6:0	LOUT1VOL [6:0]	0000000 (MUTE)	LOUT1 Volume 1111111 = +6dB … 1dB steps down to 0110000 = -73dB 0101111 to 0000000 = Analogue MUTE
R3 (03h) ROUT1 Volume	8	OUT1VU	0	Headphone Volume Update 0 = Store ROUT1VOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = intermediate latch, right = ROUT1VOL)
	7	RO1ZC	0	Right zero cross enable 0 = Change gain immediately 1 = Change gain on zero cross only
	6:0	ROUT1VOL [6:0]	0000000 (MUTE)	ROUT1 Volume Similar to LOUT1VOL
R26 (1Ah) Power Management (2)	6	LOUT1_PGA	0	LOUT1 left headphone PGA Output Enable
	5	ROUT1_PGA	0	ROUT1 right headphone PGA Output Enable

Table 28 Headphone Output PGA Volume Control

See "Volume Updates" section for a description of the volume update function, the zero cross function and the timeout operation.

HEADPHONE OUTPUT DRIVE STAGE

The headphone output drive stage is a stereo differential to single-ended amplifier. It is capable of driving 16Ω or 32Ω headphones without the need for large AC coupling capacitors, which is achieved by having separate positive and negative supplies, generated by a charge pump, detailed in the “Charge Pump” section. It also permits power up and power down with minimised ‘pop’ operation through the use of a DC Servo to null out any offset on the outputs.

A secondary volume PGA in the output drive stage permits an improvement in SNR for applications that limit the maximum output voltage. This PGA can be set to attenuate by up to 7dB, as detailed in Table 29.

Because the secondary volume PGA controlled by HPL_VOL[2:0] and HPR_VOL[2:0] does not have a Zero Cross functionality, it is designed to be adjusted only during initialisation or periods of silence. For volume adjustments with a signal playing, it is recommended to use LOUT1VOL and ROUT1VOL.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R71 (47h) Analogue HP 2	8:6	HPL_VOL[2:0]	111	Secondary HPL PGA Volume 111 0dB (default) 110 -1dB 101 -2dB 100 -3dB 011 -4dB 010 -5dB 001 -6dB 000 -7dB
	5:3	HPR_VOL[2:0]	111	Secondary HPR PGA Volume 111 0dB (default) 110 -1dB 101 -2dB 100 -3dB 011 -4dB 010 -5dB 001 -6dB 000 -7dB

Table 29 Headphone Output Drive Volume Control

HEADPHONE OUTPUT ENABLE

The staged enabling of the headphone outputs can be controlled using register R69. The HPL_ENA and HPR_ENA enable the headphone amplifiers. The HPL_ENA_OUTP and HPR_ENA_OUTP should be enabled following any offset cancellation by the DC Servo.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R69 (45h) Analogue HP 0	7	HPL_RMV_SHORT	0	Left channel output short removal: set after output stage has been enabled
	6	HPL_ENA_OUTP	0	Enables left channel output stage; set after offset cancellation is done
	5	HPL_ENA_DLY	0	delayed left channel enable, set with at least 20us delay to HPL_ENA; reset together with HPL_ENA
	4	HPL_ENA	0	Enables left headphone amplifier channel
	3	HPR_RMV_SHORT	0	right channel output short removal: set after output stage has been enabled
	2	HPR_ENA_OUTP	0	enables right channel output stage; set after offset cancellation is done
	1	HPR_ENA_DLY	0	delayed right channel enable, set with at least 20us delay to HPR_ENA; reset together with HPR_ENA
	0	HPR_ENA	0	Enables right headphone amplifier channel

Table 30 Headphone Output Enable Control

HEADPHONE OUTPUT CIRCUIT

It is recommended that the HP-L and HP_R is connected to a zobel network consisting of a 20Ω resistor (5% tolerance) and a 100nF capacitor (20% tolerance). This ensures the stability of the headphone output amplifier. This is also illustrated in Figure 19.

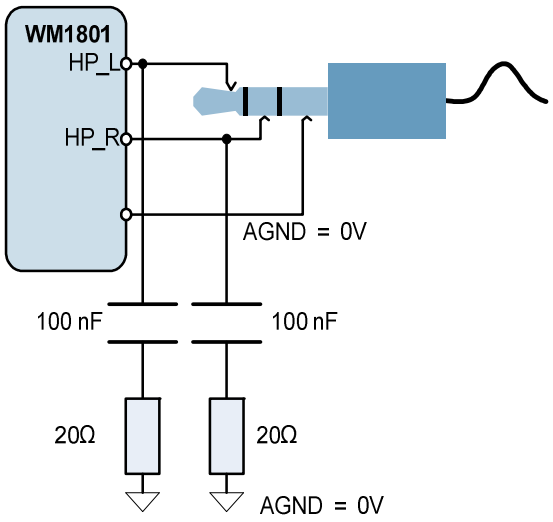


Figure 19 Recommended Headphone Output Configuration

HEADPHONE OUTPUT BIAS BOOST

In order to increase the signal to noise ratio (SNR) of the headphone output, the HP_PGAS_BIAS[2:0] and HP_BIAS_BOOST[2:0] register bits can be used to increase the bias current to the headphone output drive as shown in Table 31. There will be a slight increase in power consumption when a bias boost greater than x1 is selected.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R68 (44h) Analogue PGA Bias	2:0	HP_PGAS_BIAS[2:0]	011	Headphone PGA bias options 000 x 2 001 Reserved 010 Reserved 011 x 1 100-111 Reserved
R71 (47h) Analogue HP 2	2:0	HP_BIAS_BOOST[2:0]	011	Boost bias into headphone driver 000: x2 001: Reserved 010: Reserved 011: x1 100-111 Reserved

Table 31 Headphone Output Bias Boost

HEADPHONE PLAYBACK MODES

Headphone playback can be optimised for lowest power or best SNR, depending on the application requirements.

STANDARD MODE

Headphone playback with the best compromise between performance and power consumption can be enabled using the default DAC to Headphone Playback power on sequence as implemented at control write sequencer address 0, as detailed in “Control Write Sequencer”.

LOW POWER MODE

Headphone playback optimised for lower power consumption can be enabled. This results in a very slight reduction in headphone driver performance.

The register setting listed in Table 32 can be added to the power up sequence in order to implement this mode. Note that this register setting must take place before the charge pump is enabled. See the “Charge Pump” section. If the write sequencer is used to configure the DAC to HP path, this register write must take place before the write sequencer is enabled and triggered.

REGISTER ADDRESS	BITS	LABEL	SETTING	DESCRIPTION
R82 (52h) Charge Pump B	1:0	CP_DYN_PWR[1:0]	11	Enable dynamic (Class W) power saving

Table 32 Low Power Headphone Playback

SNR OPTIMISED MODE

Headphone playback optimised for best Signal to Noise Ratio (SNR) can be enabled, resulting in a slight increase in power consumption.

The register settings listed in Table 33 can be added at the start of the power up sequence in order to implement this mode. The LOUT1VOL and ROUT1VOL settings may require adjustment due to the additional attenuation of HPL_VOL[2:0] and HPR_VOL[2:0].

To partly offset the increase in power consumption due to selecting “SNR Optimised mode”, it is recommended to select Dynamic (Classs W) power saving) using CP_DYN_PWR=11. This saves power but only slightly impacts THD + noise performance.

REGISTER ADDRESS	BITS	LABEL	SETTING	DESCRIPTION
R30 (1Eh) Clocking 3	0	MANUAL_MODE	0	Automatic configuration of system clock dividers. Excludes master mode audio interface clocks.
R6 (06h) ADC & DAC Control 2	0	DAC_OSR128	1	Automatically configure DACDIV[2:0] for 128OSR mode. This will give a SNR improvement at the expense of power
R71 (47h) Analogue HP 2	8:6	HPL_VOL[2:0]	000	Secondary HPL PGA Volume -7dB
	5:3	HPR_VOL[2:0]	000	Secondary HPR PGA Volume -7dB
	2:0	HP_BIAS_BOOST[2:0]	000	Boost bias into headphone driver x2
R68 (44h) Analogue PGA Bias	2:0	HP_PGAS_BIAS[2:0]	000	Headphone PGA bias x 2
R82 (52h) Charge Pump B	1:0	CP_DYN_PWR[1:0]	11	Enable dynamic (Class W) power saving

Table 33 Low Power Headphone Playback

Note that the register write to CP_DYN_PWR[1:0] must take place before the charge pump is enabled. See the “Charge Pump” section.

SPEAKER OUTPUTS

The SPK_LP/SPK_LN and SPK_RP/SPK_RN output pins are class D speaker drivers. Each pair is independently controlled and can drive an 8Ω BTL speaker. Output PGA volume is relative to AVDD, while an additional boost stage (set by CLASSD_ACGAIN[2:0]) is available to accommodate higher SPKVDD1/SPKVDD2 supply voltages. This allows AVDD to be run at a lower voltage to save power, while maximum output power can be delivered to the load, utilising the full range of SPKVDD1 and SPKVDD2 supplies. The output gain stage automatically centers the analogue output about SPKVDD/2. This will avoid the analogue output clipping – except in the case of CLASSD_ACGAIN=12dB. The speaker output stage is illustrated in Figure *20*

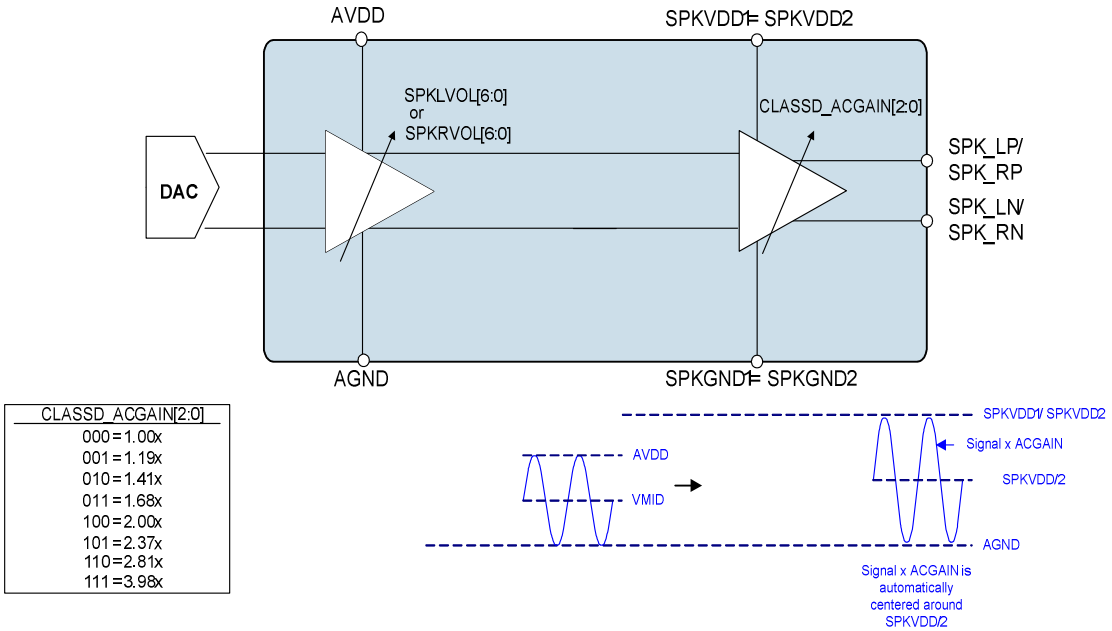


Figure *20* Speaker Output Stage

SPEAKER OUTPUT PGA VOLUME CONTROL

The signal volume on SPK_L and SPK_R can be independently adjusted under software control by writing to SPKLVOL and SPKRVOL, as shown in Figure 21.

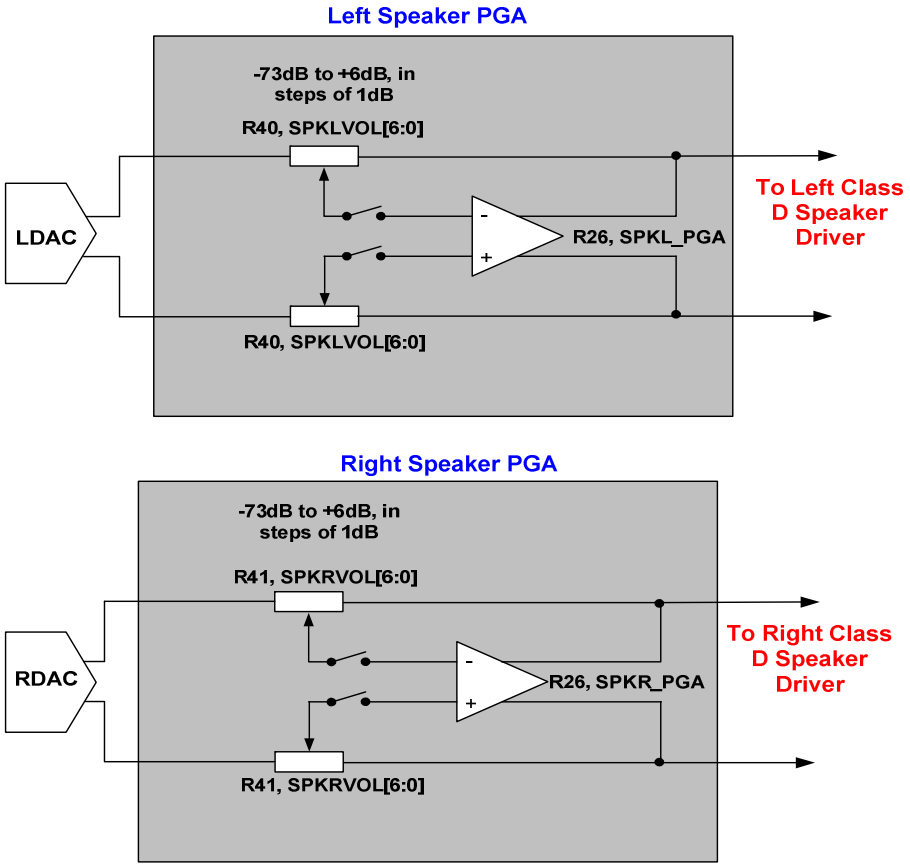


Figure 21 Speaker Volume PGA

A zero cross detect on the analogue output may also be enabled when changing the gain setting to minimize audible clicks and zipper noise as the gain updates. If zero cross is enabled a timeout is also available to update the gain if a zero cross does not occur. This function may be enabled by setting TOEN in register R23 (17h). The timeout period is set by CLK_TO_DIV[1:0]. The volume control PGAs are enabled using SPKL_PGA and SPKR_PGA.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R40 (28h) Left Speaker Volume	6:0	SPKLVOL [6:0]	0000000 (MUTE)	SPK_LP/SPK_LN Volume 1111111 = +6dB … 1dB steps down to 0110000 = -73dB 0101111 to 0000000 = Analogue MUTE
	7	SPKLZC	0	Left Speaker Zero Cross Enable 1 = Change gain on zero cross only 0 = Change gain immediately
	8	SPKVU	0	Speaker Volume Update 0 = Store SPKLVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = SPKLVOL, right = intermediate latch)
R41 (29h) Right Speaker Volume	6:0	SPKRVOL [6:0]	0000000 (MUTE)	SPK_RP/SPK_RN Volume 1111111 = +6dB … 1dB steps down to 0110000 = -73dB 0101111 to 0000000 = Analogue MUTE
	7	SPKRZC	0	Right Speaker Zero Cross Enable 1 = Change gain on zero cross only 0 = Change gain immediately
	8	SPKVU	0	Speaker Volume Update 0 = Store SPKRVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = intermediate latch, right = SPKRVOL)
R26 (1Ah) Pwr Mgmt (2)	4	SPKL_PGA	0	SPK_LP and SPK_LN left speaker PGA Enable
	3	SPKR_PGA	0	SPK_RP and SPK_RN right speaker PGA Enable

Table 34 SPK_L/SPK_R Analogue Volume Control

SPEAKER OUTPUT BOOST CONTROL

The speaker output boost stage allows AVDD to be run at a lower voltage to save power, while maximum output power can be delivered to the load, maximising the full range of SPKVDD1 and SPKVDD2 supplies. It is controlled by CLASSD_ACGAIN[2:0].

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R51 (33h) Class D Control 2	2:0	CLASSD_ACGAIN [2:0]	011 (1.68x)	AC Speaker Boost (Boosts speaker AC output signal by up to 3.98 x on left and right channels) 000 = 1.00x boost (+0dB) 001 = 1.19x boost (+1.5dB) 010 = 1.41x boost (+3.0dB) 011 = 1.68x boost (+4.5dB) 100 = 2.00x boost (+6.0dB) 101 = 2.37x boost (+7.5dB) 110 = 2.81x boost (+9.0dB) 111 = 3.98x boost (+12dB) Note that +12dB setting will cause a full scale output signal to clip.

Table 35 SPK_L/SPK_R Speaker Boost Control

To prevent pop noise, CLASSD_ACGAIN should not be modified while the speaker outputs are enabled.

To avoid clipping at speaker supply, SPKVDD1 and SPKVDD2 must be high enough to support the peak output voltage when using CLASSD_ACGAIN functions.

The maximum RMS output voltage is defined by the equation:

MAX. RMS OUTPUT VOLTAGE = AVDD/1.8* CLASSD_ACGAIN.

The above formula assumes there is 0.5dB loss (6%) due to PCB tracking. 0.5dB corresponds to 0.5Ω total tracking impedance with an 8Ω speaker. If the tracking impedance is greater than or less than 6% of the speaker impedance, the output voltage will differ slightly to the above formula.

CLASS D SPEAKER OUTPUT DRIVER

The class D speaker outputs SPK_LN/SPK_LP and SPK_RN/SPK_RP can drive 1W into 8Ω BTL speakers at SPKVDD=5v. The Class D output stage is shown in Figure 22.

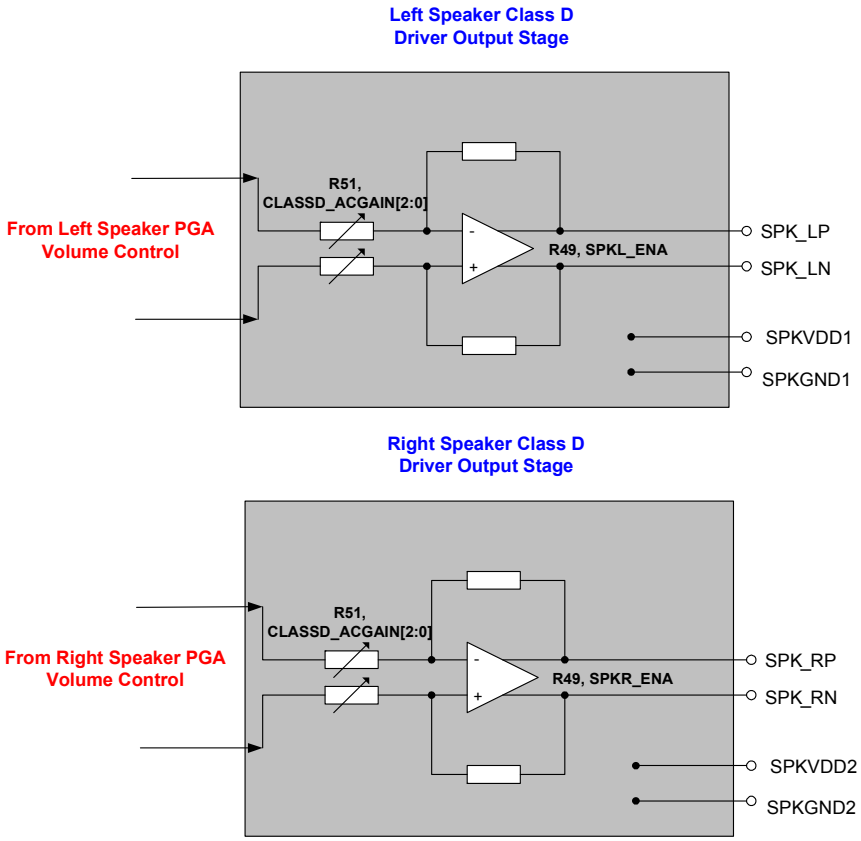


Figure 22 Class D Speaker Output Stage

Class D outputs reduce power consumption and maximise efficiency by reducing power dissipated in the output drivers, delivering most of the power directly to the load. This is achieved by pulse width modulation (PWM) of a high frequency square wave, allowing the audio signal level to be set by controlling the pulse width. The frequency of the output waveform is controlled by DCLKDIV, and is derived from SYSCLK.

The speaker output enable bits SPKR_ENA and SPKL_ENA should not be enabled until there is a valid switching clock to drive the Class D outputs. This means that SYSCLK must be active, and DCLKDIV set to an appropriate value to produce a Class D clock which runs at a nominal frequency of 384kHz when SYSCLK=12.288 MHz, or 352.8kHz when SYSCLK=11.2896MHz. This clock should not be altered or disabled while the Class D outputs are enabled.

If the speakers are located close to the WM8961 (less than about 100mm) then the internal filtering effects of the speaker can be used. Where speakers are located further away from the WM8961 and the speaker signals are routed over longer distances, it is recommended to use additional passive filtering. This additional filtering should be positioned as close as possible to the WM8961 to reduce EMI effects. See “Applications Information” for more information on EMI reduction.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 (08h) Clocking (2)	8:6	DCLKDIV[2:0]	111	Controls clock division from SYSCLK to generate suitable class D clock. 000 = SYSCLK / 1 001 = SYSCLK / 2 010 = SYSCLK / 3 011 = SYSCLK / 4 100 = SYSCLK / 6 101 = SYSCLK / 8 110 = SYSCLK / 12 111 = SYSCLK / 16 (Note that Class D function further divides by 2)
R49 (31h) Class D Control (1)	7	SPKR_ENA	0	Right channel class D enable 0= Disable Right Channel speaker output 1= Enable Right Channel speaker output
	6	SPKL_ENA	0	Left channel Class D enable 0= Disable Left Channel speaker output 1= Enable Left Channel speaker output

Table 36 Class D Speaker Control Registers

INPUT AND OUTPUT VOLUME UPDATES

Volume settings will not be applied to input or output PGAs until a ‘1’ is written to one of the update bits (IPVU, OUT1VU, SPKVU bits). This is to allow left and right channels to be updated at the same time, as shown in Figure 23.

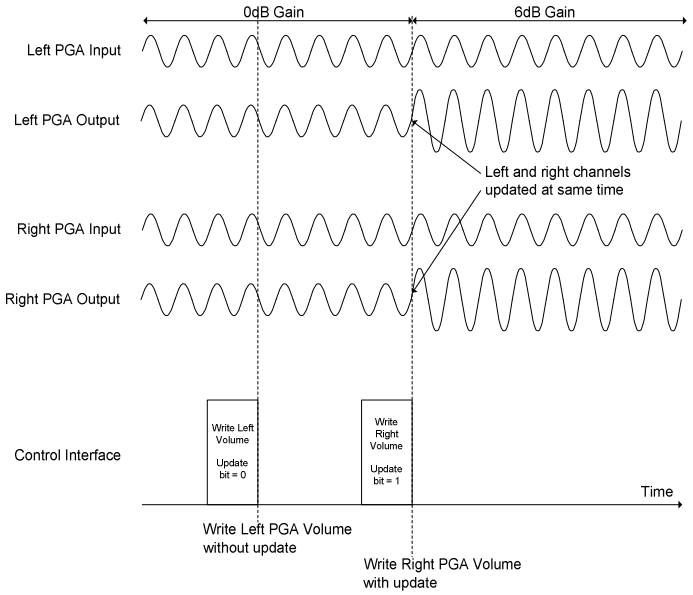


Figure 23 Simultaneous Left and Right Volume Updates

If a volume update is attempted while the signal is a non-zero value, an audible click could occur as shown in Figure 24.

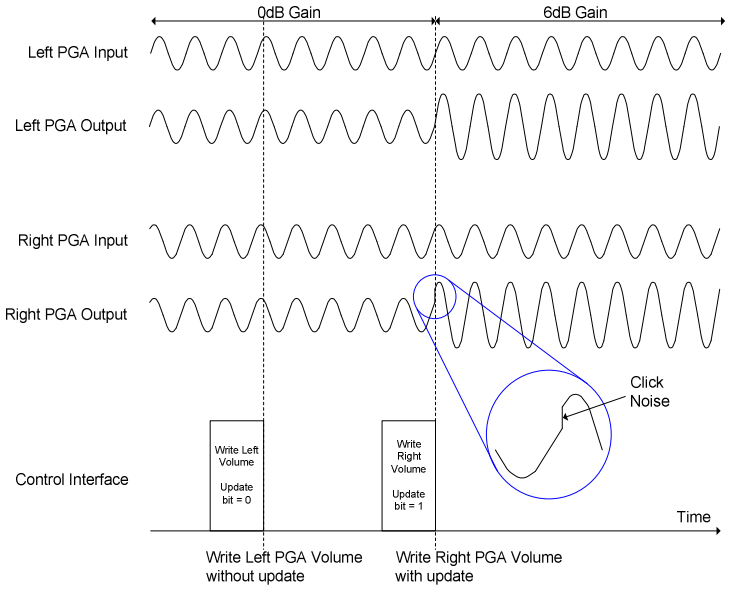


Figure 24 Click Noise during Volume Update

In order to prevent this click noise, a zero cross function is provided. When enabled, this will cause the PGA volume to update only when a zero crossing occurs, minimising click noise as shown in Figure 25.

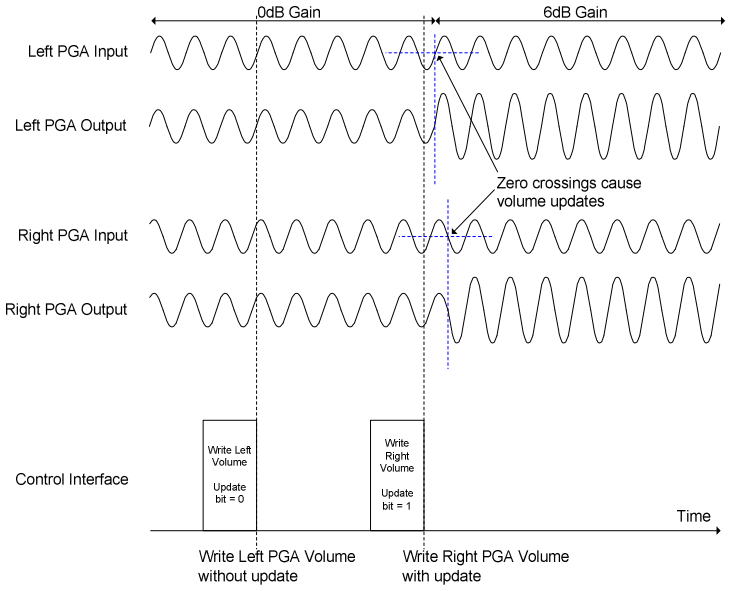


Figure 25 volume Update using Zero Cross Detection

If there is a long period where no zero-crossing occurs, a timeout circuit in the WM8961 will automatically update the volume. The volume updates will occur between one and two timeout periods, depending on when the volume update bit is set as shown in Figure 26. The TOEN register bit must be set to enable this timeout function. The timeout period is set by CLK_TO_DIV[1:0].

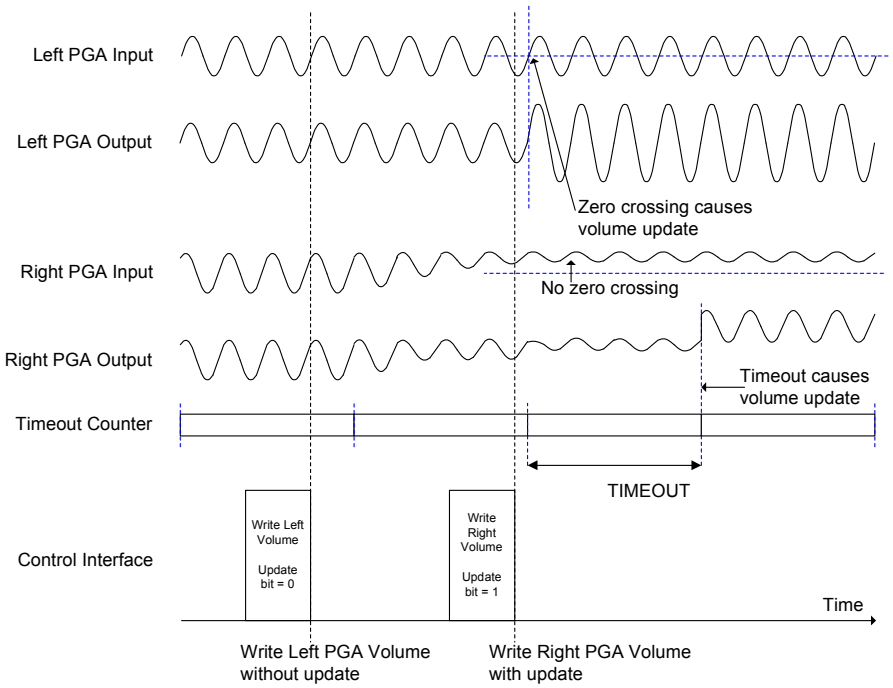


Figure 26 Volume Update after Timeout

DC SERVO

The DC servo reduces any DC offset from the ground referenced headphone output and the output of the microphone boost stage. The operation of the DC servo ensures that these outputs remain within 1.5mV of ground when enabled.

On the input stage the DC servo is used to null any DC offset at the input of the ADC (boost stage output). This optimises the zero cross detection, particularly when using ALC. The DC servo is referenced to the charge pump references VPOS and VNEG hence in order to permit the DC servo to be used when recording, the headphone charge pump must be enabled (CP_ENA = 1) and MCLK must be applied, see “Charge Pump” section. If the charge pump is not enabled or MCLK is not supplied, large offsets will be present within the Input Path and the zero cross function may not operate.

On the output stage the DC servo is used to null DC offsets at the headphone outputs. This results in reduced power consumption since any deviation from ground at the output pin results in a DC current flow through the load. Additionally, removal of DC offsets at these outputs helps to significantly reduce pops and clicks at power up and down.

A block diagram of the DC Servo is shown in Figure 27

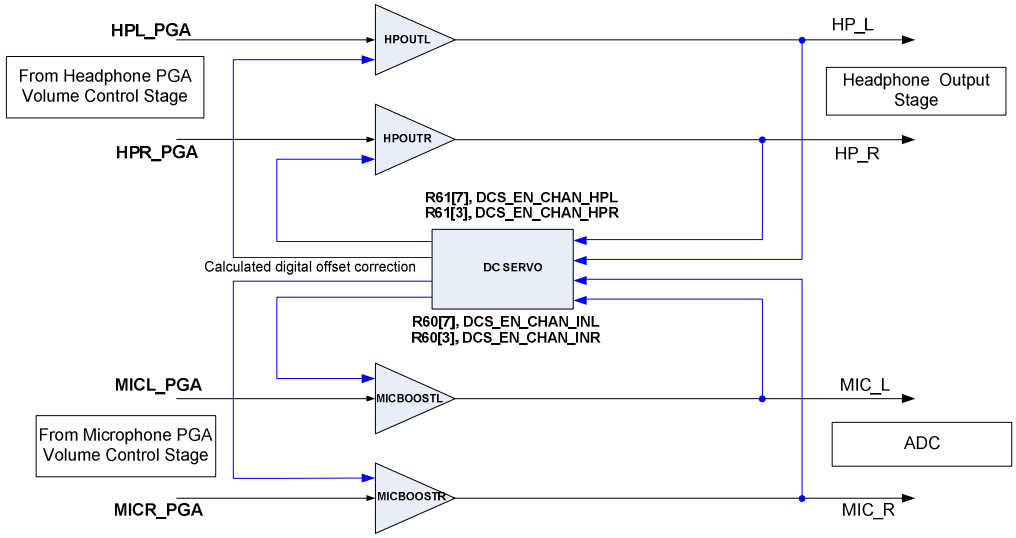


Figure 27 DC Servo Block Diagram

DC SERVO STARTUP OPERATION

The DC servo contains automatic control circuitry and can be configured using individual register writes.

The DC servo can also be configured by starting a sequence using the control write sequencer (see "Control Write Sequencer" section). Starting the pre-defined sequence from line 0 of the control write sequencer configures the DC servo by default.

The basic startup operation of the DC servo, for example for HP_R, is to

1. Enable the DC Servo operation on the HP_R output by configuring R61[3], DCS_ENA_CHAN_HPR. (The HP_L, INR/L have similar enables).
2. Trigger a start up sequence for the HP_R by configuring R61[2] DCS_TRIG_STARTUP_HPR (The HP_L, INR/L have similar start up sequence enables).

Additionally, to enable the DC servo for L/RINPUT, the headphone charge pump must be enabled (CP_ENA = 1) and MCLK must be applied.

Note that it is recommended to perform a calibration of the DC Servo input channel before using the Input PGA Zero Cross Detector.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R60 (3Ch) DC Servo 1	7	DCS_ENA_CHAN_INL	0	DC Servo enabled on channel INL
	6	DCS_TRIG_STARTUP_INL	0	Perform startup sequence on channel INL*see note 1
	3	DCS_ENA_CHAN_INR	0	DC Servo enabled on channel INR
	2	DCS_TRIG_STARTUP_INR	0	Perform startup sequence on channel INR *see note 1
R61 (3Dh) DC Servo 1	7	DCS_ENA_CHAN_HPL	0	DC Servo enabled on channel HPL
	6	DCS_TRIG_STARTUP_HPL	0	Perform startup sequence on channel HPL *see note 1
	3	DCS_ENA_CHAN_HPR	0	DC Servo enabled on channel HPR
	2	DCS_TRIG_STARTUP_HPR	0	Perform startup sequence on channel HPR *see note 1

Table 37 DC Servo Enable and Start-up Configuration

Note:

1. The "startup" bits are automatically reset to '0' after 1 clock cycle.

DC SERVO CONFIGURATION FOLLOWING A HEADPHONE PGA VOLUME UPDATE

When a PGA volume update is applied to the headphone output, its DC offset can change. To maintain sub 1.5mV DC offsets, it may be necessary to re-calibrate the DC correction factors when large changes are made to PGA settings in the signal path (6dB or greater). The DC Servo can be configured to do this automatically as a background task using the DCS_TRIG_SERIES_HPL/R. This function is not handled by the write control sequencer since it can happen at any time and is not part of a defined sequence.

This function is only available on the headphone outputs since it is not required for inputs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R61 (3Dh) DC Servo 1	4	DCS_TRIG_SERIES_HPL	0	0= do not perform any series of updates on HPL 1= Perform a DCS_SERIES_NO_HP series of LSB updates on channel HPL *see note 1 One channel completes before the next starts Reading this register returns status of this task. Read 0 = task completed. 1 = task being performed
	0	DCS_TRIG_SERIES_HPR	0	0= do not perform any series of updates on HPR 1= Perform a DCS_SERIES_NO_HP series of LSB updates on channel HPR *see note 1 One channel completes before the next starts Reading this register returns status of this task. Read 0 = task completed. 1 = task being performed

Table 38 DC Servo Series Updates following Volume Update

Note:

1. These bits are automatically reset to '0' after 1 clock cycle.

The DCS_TRIG_SERIES_X will update the channel a "number of times" before moving onto the next enabled channel. The "number of times" it updates a particular channel, is configured by DCS_SERIES_NO_HP.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R65 (41h) DC Servo 5	6:0	DCS_SERIES_NO_HP[6:0]	001_0000	Number of LSB updates in a series for channels HPL and HPR 000_0000-000_1111 : Reserved 001_0000 : 16 … 111_1111 : 127

Table 39 DC Servo Number of Updates Control

After any large gain update and volume updates have completed, the DCS_TRIG_SERIES_X bit should be set. The DC Servo will then examine each enabled output in order and apply any required offset correction to each.

To prevent any audible artifacts on the analogue outputs, the DC Servo only applies any necessary corrections in discreet 0.25mV steps. To allow this correction during audio playback, the DC Servo includes a high order, low pass filter which removes any AC signal content from each output before it measures the DC offset. This filter has a relatively long time constant which means that the servo will take approx 0.275 seconds for each 0.25mV correction on each enabled analogue channel. This means that the DC Servo may remain active, in the background, for several seconds after the DCS_TRIG_SERIES_X bit is set. Refer to "DC Servo Filter Bandwidth" section for more information.

DC SERVO FILTER BANDWIDTH

The DC Servo filter bandwidth can be modified to change the time taken to measure and correct the DC offset. The longer the time taken to measure the offset, then the more accurate the correction will be.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R63 (3Fh) DC Servo 3	5:4	DCS_FILT_BW_SERIES[1:0]	01	Bandwidth of filter during series updates. Determines how long a measurement takes. 00 : 6ms 01 : 275ms 10 : 1.2s 11 : 4.4s

Table 40 DC Servo Filter Bandwidth Control

CHARGE PUMP

The WM8961 incorporates a dual-mode Charge Pump which generates the +ve (VPOS) and –ve (VNEG) supply rails for the headphone output driver. The Charge Pump has a single supply input, CPVDD, and generates split rails VPOS and VNEG according to the selected mode of operation, which means that the headphone driver is capable of driving headphones without the need for large AC coupling capacitors. The Charge Pump connections are illustrated in Figure 28 (see 'applications information' for external component values). An input decoupling capacitor may also be required at CPVDD, depending upon the system configuration.

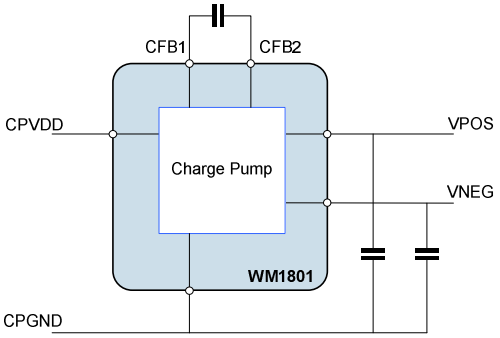


Figure 28 Charge Pump External Connections

Three external capacitors are needed for the charge pump. The fly-back pins (CFB1 and CFB2) require a 1µF capacitance or greater at 2V. The VPOS and VNEG supply pins each require a 2µF capacitance decoupling capacitor at 2V.

ENABLING THE CHARGE PUMP

An external clock (MCLK) input is required for the charge pump operation. The minimum MCLK frequency for the specified charge pump performance is 2.8224MHz.

The charge pump is enabled by setting the CP_ENA bit. DVDD and CPVDD must be active before the charge pump is enabled. The charge pump initialisation time is specified in the Electrical Characteristics. DVDD and CPVDD must be active before the charge pump is enabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R72 (48h) Charge Pump 1	0	CP_ENA	0	Enable charge-pump digits 0: disable 1: enable

Table 41 Charge Pump Enable

The Charge Pump can also be enabled by running the default Start-Up sequence as described in the "Control Write Sequencer" section. (Similarly, it will be disabled by running the Shut-Down sequence.) In these cases, the user does not need to write to the CP_ENA bit.

CHARGE PUMP CLOCKING

The charge pump clock is derived from SYSCLK, using a clock divider to generate a nominal 1MHz clock, as shown in Figure 43. The exact frequency depends on MCLK and the charge pump clock division ratio, which is based on the SAMPLE_RATE[2:0] and CLK_SYS_RATE[3:0] register settings.

For example, with MCLKDIV=0, SAMPLE_RATE[2:0]=000:

256fs: CLK_SYS_RATE[3:0]=0011 gives a charge pump clock division ratio of 12, hence

- MCLK=12.288MHz gives a charge pump frequency of 1.024MHz at full output power.
- MCLK=11.2896MHz gives a charge pump frequency of 940.8kHz at full output power.

128fs: CLK_SYS_RATE[3:0]=0001 gives a charge pump clock division ratio of 6, hence

- MCLK=6.144MHz gives a charge pump frequency of 1.024MHz at full output power.
- MCLK=5.6448MHz gives a charge pump frequency of 940.8kHz at full output power.

CHARGE PUMP CONTROL

In order to minimise power consumption, both the output voltages (VPOS and VNEG) and the switching frequency of the charge pump are automatically adjusted according to the operating conditions. This can take two forms:

1. Charge pump settings only depend on volume register settings (CP_DYN_PWR[1:0] = 0b00): the maximum of LOUT1VOL and ROUT1VOL volume register settings (excluding disabled or muted outputs) controls the charge pump mode of operation.
2. Dynamic (Class W) power saving: Charge pump settings depend on dynamic signal level (CP_DYN_PWR[1:0] = 0b11) *and* volume register settings: the audio signal input to the DAC, multiplied by the maximum of LOUT1VOL and ROUT1VOL volume register settings, is used to control the charge pump mode of operation. This is the Wolfson 'Class W' mode, which allows the power consumption to be optimised in real time.

The Charge Pump operating mode defaults to Register control. Dynamic (Class W) power saving may be selected by setting the CP_DYN_PWR[1:0] bits to 0b11. If dynamic power saving is to be selected, this register write must take place before the charge pump is enabled. If the write sequencer is used to configure the DAC to HP path, this register write must take place before the write sequencer is enabled and triggered. Dynamic power saving results in a very slight reduction in headphone driver performance.

When the ADC sidetone is used for the headphone output, and the charge pump settings depend on dynamic signal level CP_DYN_PWR[1:0] = 0b11), the charge pump will monitor the DAC output level rather than the ADC sidetone level. If the ADC sidetone signal is likely to exceed the DAC output level, to avoid clipping it is recommended to set the charge pump settings to depend on volume register settings (CP_DYN_PWR[1:0] = 0b00). See also the DAC Digital Sidetone section.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R82 (52h) Charge Pump B	1:0	CP_DYN_PWR[1:0]	0	Enable dynamic (Class W) power saving 00: dynamic power saving disabled 01: Reserved 10: Reserved 11: dynamic power saving enabled

Table 42 Charge Pump Configuration Registers

DIGITAL AUDIO INTERFACE

The digital audio interface is used for inputting DAC data into the WM8961 and outputting ADC data from it. It uses four pins:

- ADCDAT: ADC data output
- DACDAT: DAC data input
- LRC: DAC and ADC data alignment clock
- BCLK: Bit clock, for synchronisation

The clock signals BCLK and LRC can be an output when the WM8961 operates as a master, or an input when it is a slave (see Master and Slave Mode Operation, below).

Four different audio data formats are supported:

- Left justified
- Right justified
- I^2S
- DSP mode

All four of these modes are MSB first. They are described in Audio Data Formats, below. Refer to the Electrical Characteristic section for timing information.

MASTER AND SLAVE OPERATION

The WM8961 can be configured as either a master or slave mode device. As a master device the WM8961 generates BCLK and LRC and thus controls sequencing of the data transfer on ADCDAT and DACDAT. In slave mode, the WM8961 responds with data to clocks it receives over the digital audio interface. Master and slave modes are illustrated below.

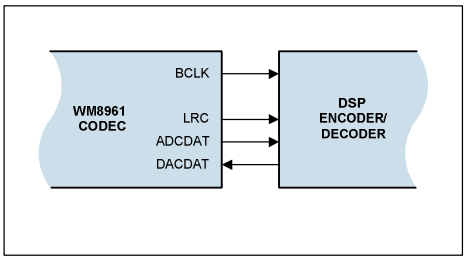


Figure 29 Master Mode

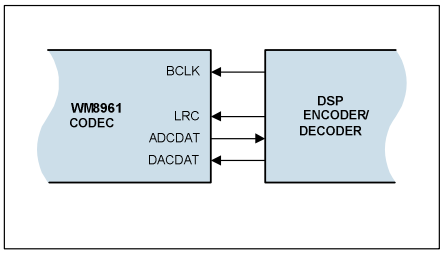


Figure 30 Slave Mode

MASTER MODE BCLK AND LRC GENERATION

The BCLK frequency is controlled by BCLKDIV[3:0] which must be set appropriately to support the ADC and DAC sample rate.

The LRC is set by the LRCLK_RATE[8:0] which is an integer division of the BCLK.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 (08h) Clocking2	3:0	BCLKDIV[3:0]	0100	BCLK Frequency (Master Mode) 0000 = SYSCLK 0001 = Reserved 0010 = SYSCLK / 2 0011 = SYSCLK / 3 0100 = SYSCLK / 4 (default) 0101 = Reserved 0110 = SYSCLK / 6 0111 = SYSCLK / 8 1000 = Reserved 1001 = SYSCLK / 12 1010 = SYSCLK / 16 1011 = SYSCLK / 24 1100 = Reserved 1101 to 1111 = SYSCLK / 32
R14 (0Eh) Audio Interface 2	8:0	LRCLK_RATE[8:0]	0_0100_0000	Integer divide of BCLK. 50:50 LRCLK duty cycle is only guaranteed with even values (4, 6, … … , 510). 0_0000_0000 to 0_0000_0011 : reserved 0_0000_0100 : 4 … 0_0100_0000 : 64 … 1_1111_1110 : 510 1_1111_1111: Reserved

Table 43 Master Mode BCLK and LRC Configuration

Internal clock divide and phase control mechanisms ensure that the BCLK and LRC edges will occur in a predictable and repeatable position relative to each other and to the data.

See Clocking and Sample Rates section for more information.

AUDIO DATA FORMATS

In Left Justified mode, the MSB is available on the first rising edge of BCLK following a LRC transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRC transition.

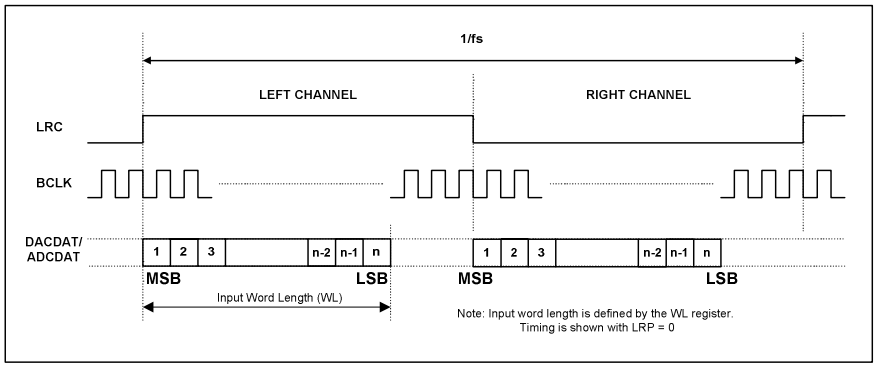


Figure 31 Left Justified Audio Interface (assuming n-bit word length)

In Right Justified mode, the LSB is available on the last rising edge of BCLK before a LRC transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each LRC transition.

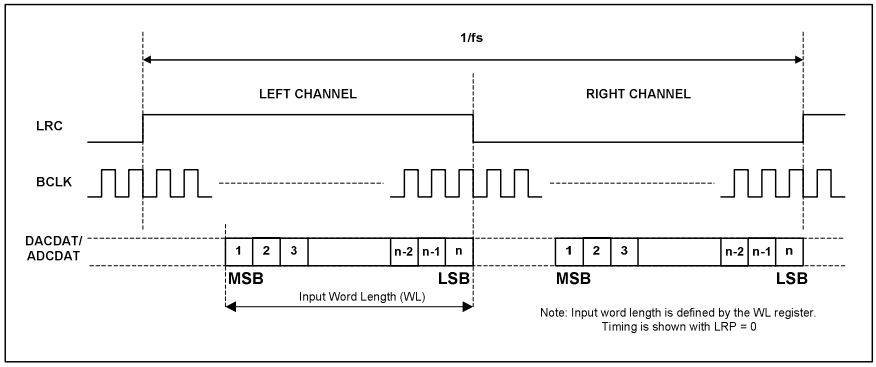


Figure 32 Right Justified Audio Interface (assuming n-bit word length)

In I^2S mode, the MSB is available on the second rising edge of BCLK following a LRC transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

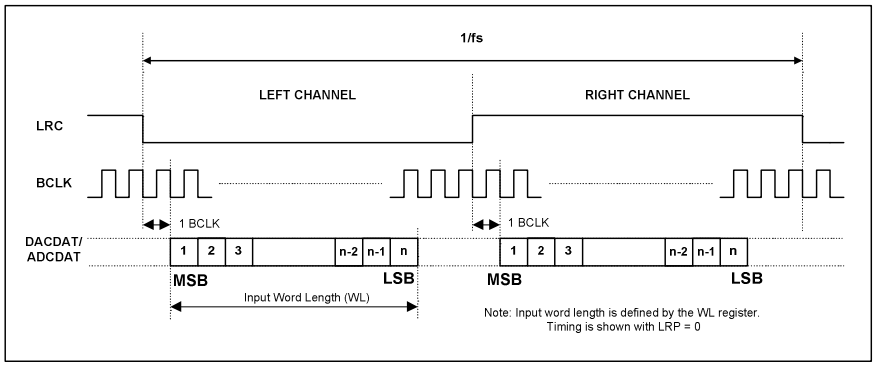


Figure 33 I^2S Justified Audio Interface (assuming n-bit word length)

In DSP mode, the left channel MSB is available on either the 1st (DSP mode B) or 2nd (DSP mode A) rising edge of BCLK (selectable by LRP) following a rising edge of LRC. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

In device master mode, the LRC output will resemble the frame pulse shown in Figure 34 and Figure 35. In device slave mode, Figure 36 and Figure 37, it is possible to use any length of frame pulse less than 1/fs, providing the falling edge of the frame pulse occurs greater than one BCLK period before the rising edge of the next frame pulse.

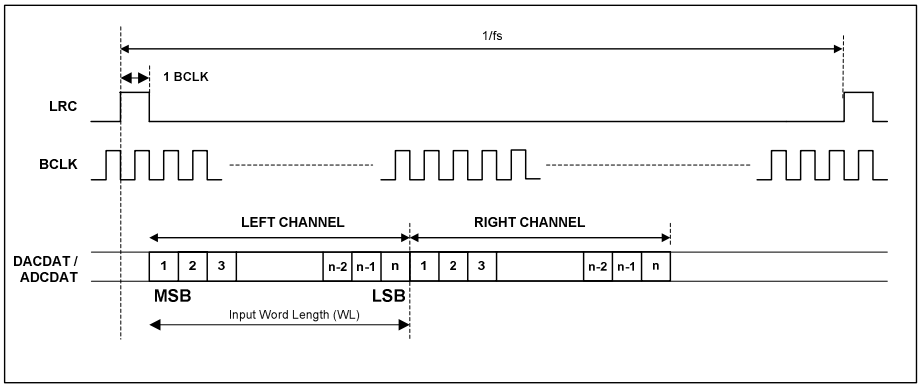


Figure 34 DSP Mode Audio Interface (mode A, LRP=0, Master)

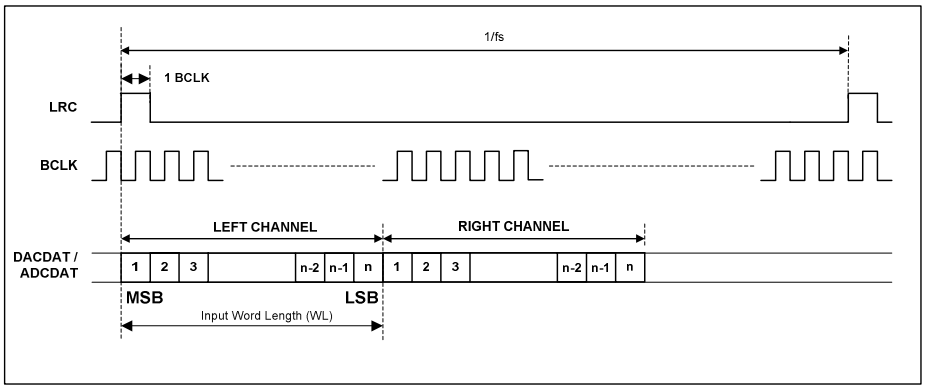


Figure 35 DSP Mode Audio Interface (mode B, LRP=1, Master)

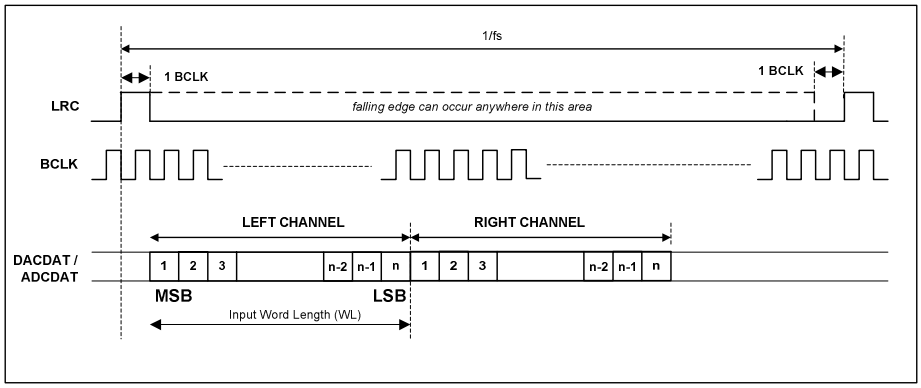


Figure 36 DSP Mode Audio Interface (mode A, LRP=0, Slave)

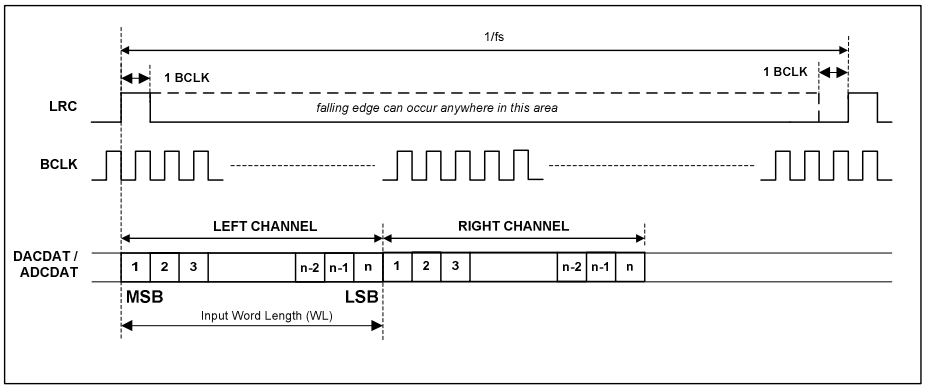


Figure 37 DSP Mode Audio Interface (mode B, LRP=0, Slave)

DIGITAL AUDIO INTERFACE CONTROL

The register bits controlling audio format, word length and master / slave mode are summarised in Table 44. MS selects audio interface operation in master or slave mode. In Master mode BCLK and LRC are outputs. The frequency of LRC is set by LRCLK_RATE and BCLK is set by the bits BCLKDIV (See "Clocking and Sample Rates"). In Slave mode BCLK and LRC are inputs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 (07h) Digital Audio Interface Format	8	ALRSWAP	0	Left/Right ADC channel swap 1 = Swap left and right ADC data in audio interface 0 = Output left and right data as normal
	7	BCLKINV	0	BCLK invert bit (for master and slave modes) 0 = BCLK not inverted 1 = BCLK inverted
	6	MS	0	Master / Slave Mode Control 0 = Enable slave mode 1 = Enable master mode
	5	DLRSWAP	0	Left/Right DAC Channel Swap 0 = Output left and right data as normal 1 = Swap left and right DAC data in audio interface
	4	LRP	0	Right, left and I^2S modes – LRC polarity 0 = normal LRC polarity 1 = invert LRC polarity
				DSP Mode – mode A/B select 0 = MSB is available on 2nd BCLK rising edge after LRC rising edge (mode A) 1 = MSB is available on 1st BCLK rising edge after LRC rising edge (mode B)
	3:2	WL[1:0]	10	Audio Data Word Length 00 = 16 bits 01 = 20 bits 10 = 24 bits 11 = 32 bits
	1:0	FORMAT[1:0]	10	Audio Data Format Select 00 = Right justified 01 = Left justified 10 = I^2S Format 11 = DSP Mode

Table 44 Audio Data Format Control

AUDIO INTERFACE OUTPUT TRISTATE

Register bit TRIS, register 24(18h) bit[3] can be used to tri-state the ADCDAT pin and switch LRC and BCLK to inputs. In Slave mode (MS=0) LRC and BCLK are by default configured as inputs and only ADCDAT will be tri-stated, (see Table 45).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24 (18h) Additional Control (2)	3	TRIS	0	Tri-states ADCDAT and switches LRC and BCLK to inputs. 0 = ADCDAT is an output; LRC and BCLK are inputs (slave mode) or outputs (master mode) 1 = ADCDAT is tri-stated; LRC and BCLK are inputs

Table 45 Tri-stating the Audio Interface

COMPANDING

The WM8961 supports A-law and μ-law companding on both transmit (ADC) and receive (DAC) sides. Companding can be enabled on the DAC or ADC audio interfaces by writing the appropriate value to the DACCOMP or ADCCOMP register bits respectively.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R9 (09h) Audio Interface (2)	2:1	ADCCOMP	00	ADC companding 00 = off 01 = reserved 10 = μ-law 11 = A-law
	4:3	DACCOMP	00	DAC companding 00 = off 01 = reserved 10 = μ-law 11 = A-law

Table 46 Companding Control

Companding involves using a piecewise linear approximation of the following equations (as set out by ITU-T G.711 standard) for data compression:

μ-law (where μ=255 for the U.S. and Japan):

$F(x) = \ln(1 + \mu|x|) / \ln(1 + \mu)$ $-1 \le x \le 1$

26 law (where A=87.6 for Europe):

$F(x) = A|x| / (1 + \ln A)$ } for $x \le 1/A$

$F(x) = (1 + \ln A|x|) / (1 + \ln A)$ } for $1/A \le x \le 1$

The companded data is also inverted as recommended by the G.711 standard (all 8 bits are inverted for μ-law, all even data bits are inverted for A-law). The data will be transmitted as the first 8 MSB's of data.

Companding converts 13 bits (μ-law) or 12 bits (A-law) to 8 bits using non-linear quantization. The input data range is separated into 8 levels, allowing low amplitude signals better precision than that of high amplitude signals. This is to exploit the operation of the human auditory system, where louder sounds do not require as much resolution as quieter sounds. The companded signal is an 8-bit word containing sign (1-bit), exponent (3-bits) and mantissa (4-bits).

8-bit mode is automatically selected during companding. That is whenever DACCOMP[2]=1 or ADCCOMP[2]=1. The use of 8-bit data allows samples to be passed using as few as 8 BCLK cycles per LRC frame. When using DSP mode B, 8-bit data words may be transferred consecutively every 8 BCLK cycles.

BIT7	BIT[6:4]	BIT[3:0]
SIGN	EXPONENT	MANTISSA

Table 47 8-bit Companded Word Composition

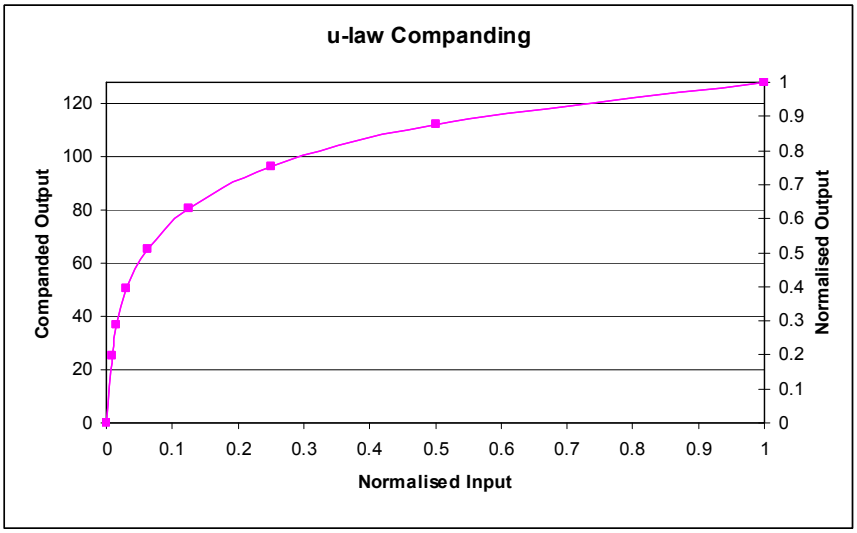


Figure 38 µ-Law Companding

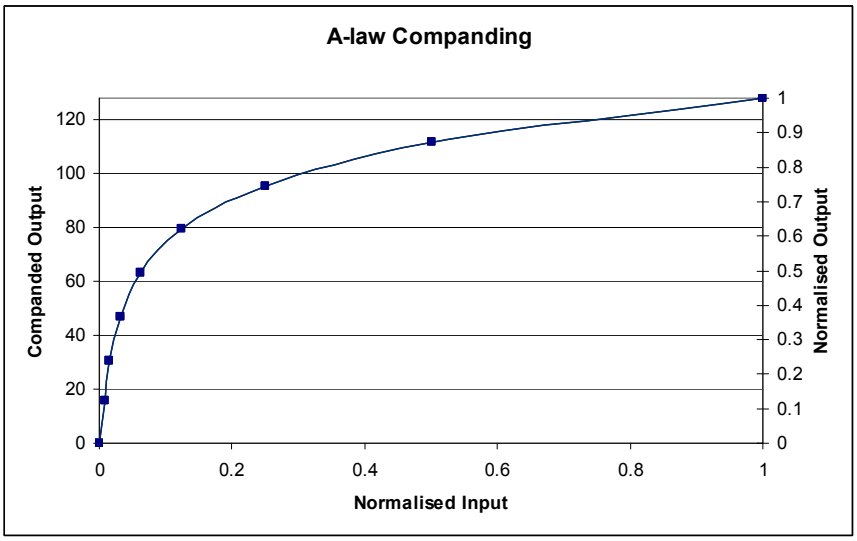


Figure 39 A-Law Companding

ADC-DAC LOOPBACK

Setting the LOOPBACK register bit enables digital loopback. When this bit is set the output data from the ADC audio interface is fed directly into the DAC data input..

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R9 Audio Interface	0	LOOPBACK	0	Digital Loopback Function 0 = No loopback. 1 = Loopback enabled, ADC data output is fed directly into DAC data input.

Table 48 Loopback Control

CONTROL WRITE SEQUENCER

The write sequencer allows register write sequences to be stored in an area of memory on the device and then triggered by another register write. In this way complex sequences of writes can be used to configure the device without the need for constant intervention by the main processor. This aids pop and click suppression and simplifies power-on and power-off sequences.

MCLK must be applied to the WM8961 while making use of the write sequencer.

The control write sequencer contains 2 memories. It contains a RAM (locations 0 to 31) and a ROM (locations 32 to 48). A number of pre-defined sequences are stored within both these areas of memory. This enables the most popular configurations to be selected via a single command. It also allows deployment of factory proven 'patches' into the field. The pre-defined sequences within the RAM can be overwritten by the user. This is done by loading new sequences via the control interface logic shown in Figure 40.

The control interface logic provides connectivity to the control interface and access to the control registers. In WM8961, a multiplexer has been added to allow switch over, such that the control write sequencer is connected to the registers instead.

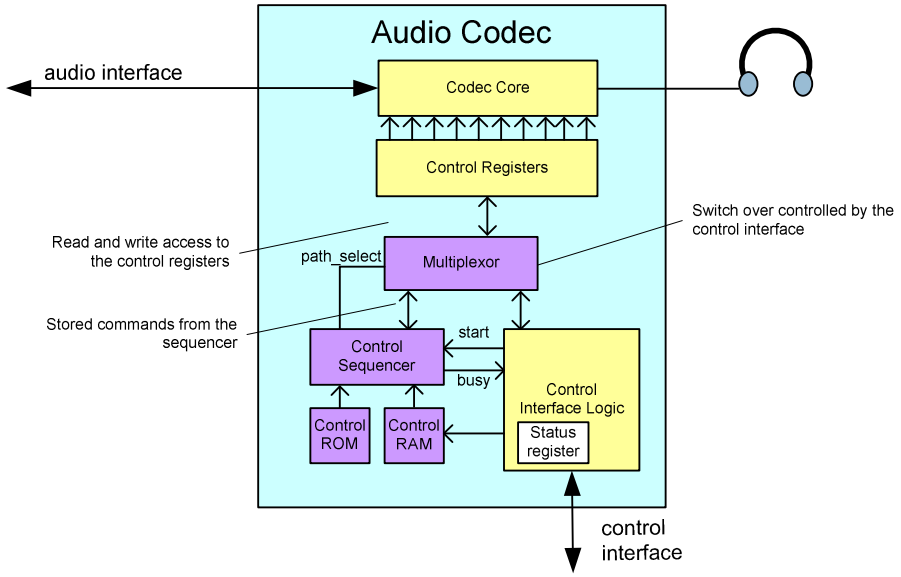


Figure 40 Location of the Control Sequencer in the Control Path

The sequencer allows the controlling processor to initiate a sequence of commands. The delays between each command in the sequence are controlled on-chip – and are not affected by activities elsewhere in the system. Once a sequence is initiated, the processor is then free to concentrate on other parts of the system. A status register is provided to allow the processor to check that one sequence is complete before starting another.

Although pop and click suppression is the most obvious application, there are other applications. Any sequence of control writes can be automated, enabling the processor to initiate a thread of asynchronous control events before performing other tasks or going into a power down mode.

Figure 41 is an example of how sequences of commands are stored and applied within the CODEC. A number of analogue functions requiring digital control are drawn across the bottom of the diagram. Each command contains an operation and a delay. The operation (e.g. Mute Left) contains data and address information to write a new value to a field within a CODEC control register. Each sequence is terminated with an EOS flag allowing several sequences at a time to be stored in RAM or ROM.

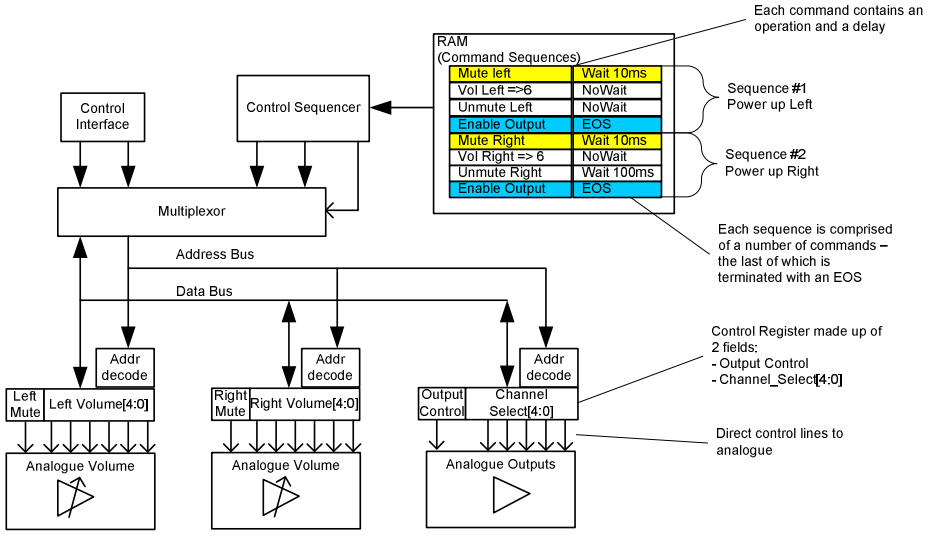


Figure 41 Definition of Sequences, Commands, Control Registers and Fields

The sequencer has the ability to write to only part of a word. This allows individual fields in the word to be written to while leaving others untouched. This capability also simplifies software access for direct command because the application processor no longer needs to perform a read-modify-write operation to ensure that only the field of interest is changed.

Each command in the sequence can includes a delay value which sets the time that execution will pause before executing the next command. To reduce memory overhead, the delay is stored as a 4-bit delay coefficient τ. The delay is proportional to k2τ , where k=62.5μs when MCLK=12.288MHz. This delay is added to the inherent time it takes to carry out a read-modify-write instruction (approximately 500 μs).

Figure 42 shows how the control words are arranged. Each word contains the details of the write: Address, Data and write enable. A delay value, τ, is included to control the time between writes. The EOS flag is used to indicate that the current command is the last in the sequence and that control should be returned to the control interface once that command is complete.

The start and length fields form a mask which allows the write to be restricted to an individual field within the write.

The mask byte comprises of (1) start = a pointer to the LSB of the field within the word, and (2) a field length indicating the number of bits in the field.

For example if the word format is 16-bits wide, an 8-bit mask can be used with a 4-bit bit pointer and a 3-bit length field. This would allow any 1 to 8-bit contiguous field within the word to be accessed. For example if start=0010, and length=011, then bits 2,3,4 will be modified.

Read/ Write	Address[6:0]	Data[7:0]	Delay[3:0]	Start[3:0]	Length[2:0]	EOS

Figure 42 Control Word format

The purpose of the write control sequencer default sequences is summarised in Table 49.

WSEQ START ADDRESS	WSEQ FINISH ADDRESS	PURPOSE
0	17	Power up DAC to HP out
18	26	Power up LRIN to ADC
27	48	Power down

Table 49 Write Sequencer Default Sequences

The default values of the write control sequencer are given in Table 50

WSEQ _LOCATION	WM8961 REG _INDEX	EOS	WIDTH	START	DATA	DELAY	COMMENT	CUMULATIVE DELAY	STARTUP TIME
0	8'h08	1'b0	3'h0	4'h4	8'h1	4'h0	CLK_DSP_ENA = 1	0.0005	0.0005
1	8'hFE	1'b0	3'h0	4'h0	8'h0	4'h0	Dummy Write for expansion	0.0005	0.0010
2	8'h1C	1'b0	3'h1	4'h3	8'h3	4'h0	BUFDCOPEN = 1, BUFIOEN = 1 ; Enable current bias circuits	0.0005	0.0015
3	8'h19	1'b0	3'h2	4'h6	8'h3	4'h0	VMIDSEL = 01, VREF = 1 ; VMID can be brought up fast, master bias enable	0.0005	0.0020
4	8'h48	1'b0	3'h0	4'h0	8'h01	4'h6	Enable Charge pump, wait 4.5ms	0.0045	0.0065
5	8'h1A	1'b0	3'h3	4'h5	8'hF	4'h0	LOUT1_PGA = 1, ROUT1_PGA = 1, DACL = 1, DACR = 1	0.0005	0.0070
6	8'h45	1'b0	3'h4	4'h0	8'h11	4'h0	Set HPL_ENA, HPR_ENA	0.0005	0.0075
7	8'h45	1'b0	3'h4	4'h1	8'h19	4'h0	Set HPL_EN_DLY, HPR_EN_DLY	0.0005	0.0080
8	8'h02	1'b0	3'h6	4'h0	8'h65	4'h0	LOUT1VOL to -20dB (7'b1100101)	0.0005	0.0085
9	8'h03	1'b0	3'h6	4'h0	8'h65	4'h0	ROUT1VOL to -20dB (7'b1100101)	0.0005	0.0090
10	8'h03	1'b0	3'h0	4'h8	8'h01	4'h0	OUT1VU	0.0005	0.0095
11	8'h3D	1'b0	3'h5	4'h2	8'h33	4'hC	Enable Servo on outputs, trigger startup, wait 256ms	0.2560	0.2655
12	8'hFE	1'b0	3'h0	4'h0	8'h0	4'h0	Dummy Write for expansion	0.0005	0.2660
13	8'h07	1'b0	3'h1	4'h2	8'h0	4'h0	AIF WL = 16 bit	0.0005	0.2665
14	8'h45	1'b0	3'h4	4'h2	8'h1D	4'h0	Set HPL_ENA_OUTP & HPR_ENA_OUTP	0.0005	0.2670
15	8'h45	1'b0	3'h4	4'h3	8'h1F	4'h0	Set HPL_RMV_SHRT & HPR_RMV_SHRT	0.0005	0.2675
16	8'hFE	1'b0	3'h0	4'h0	8'h0	4'h0	Dummy Write for expansion	0.0005	0.2680
17	8'h5	1'b1	3'h0	4'h3	8'h0	4'h8	DAC Soft unmute, wait 16.5ms	0.0165	0.2845
18	8'h20	1'b0	3'h1	4'h4	8'h03	4'h0	LMICBOOST = 11	0.0005	0.0005
19	8'h21	1'b0	3'h1	4'h4	8'h03	4'h0	RMICBOOST = 11	0.0005	0.0010
20	8'h19	1'b0	3'h4	4'h1	8'h19	4'h0	AINL = 1, AINR = 1, MICB = 1	0.0005	0.0015
21	8'h3C	1'b0	3'h5	4'h2	8'h33	4'hC	Enable Servo on inputs, trigger startup, wait 256ms	0.2560	0.2575
22	8'hFE	1'b0	3'h0	4'h0	8'h00	4'h0	Dummy Write for expansion	0.0005	0.2580
23	8'h19	1'b0	3'h1	4'h2	8'h3	4'h0	ADCL = 1, ADCR = 1	0.0005	0.2585
24	8'h20	1'b0	3'h1	4'h4	8'h0	4'h0	LMICBOOST = 00	0.0005	0.2590
25	8'h21	1'b0	3'h1	4'h4	8'h0	4'h0	RMICBOOST = 00	0.0005	0.2595
26	8'hFE	1'b1	3'h0	4'h0	8'h00	4'h0	Dummy Write for expansion	0.0005	0.2600
27	8'h5	1'b0	3'h0	4'h3	8'h1	4'h8	DAC Soft mute, wait 16.5ms	0.0165	0.0165
28	8'h00	1'b0	3'h0	4'h7	8'h01	4'h0	LINMUTE = 1	0.0005	0.0170
29	8'h01	1'b0	3'h1	4'h7	8'h03	4'h0	RINMUTE = 1, IPVU	0.0005	0.0175

WSEQ _LOCATION	WM8961 REG _INDEX	EOS	WIDTH	START	DATA	DELAY	COMMENT	CUMULATIVE DELAY	STARTUP TIME
30	8'h45	1'b0	3'h4	4'h3	8'h0E	4'h0	Clear RMV_SHRT on outputs	0.0005	0.0180
31	8'h45	1'b0	3'h4	4'h2	8'h0C	4'h0	Clear HPL_ENA_OUTP & HPR_ENA_OUTP	0.0005	0.0185
32	8'h02	1'b0	3'h6	4'h0	8'h00	4'h0	LOUTVOL to mute	0.0005	0.0190
33	8'h03	1'b0	3'h6	4'h0	8'h00	4'h0	ROUTVOL to mute	0.0005	0.0195
34	8'h03	1'b0	3'h0	4'h8	8'h01	4'h0	OUT1VU	0.0005	0.0200
35	8'h28	1'b0	3'h6	4'h0	8'h00	4'h0	SPKLVOL to mute	0.0005	0.0205
36	8'h29	1'b0	3'h6	4'h0	8'h00	4'h0	SPKRVOL to mute	0.0005	0.0210
37	8'h29	1'b0	3'h0	4'h8	8'h01	4'h0	SPKVU	0.0005	0.0215
38	8'h3C	1'b0	3'h4	4'h3	8'h00	4'h0	Disable Servo on inputs	0.0005	0.0220
39	8'h3D	1'b0	3'h4	4'h3	8'h00	4'h0	Disable Servo on outputs	0.0005	0.0225
40	8'h1A	1'b0	3'h5	4'h3	8'h00	4'h0	SPKL_PGA = 0, SPKR_PGA = 0, LOUT1_PGA = 0, ROUT1_PGA = 0, DACL = 0, DACR = 0	0.0005	0.0230
41	8'h31	1'b0	3'h1	4'h6	8'h00	4'h0	Disable Class D	0.0005	0.0235
42	8'h45	1'b0	3'h5	4'h0	8'h00	4'h0	Disable HPL_ENA, HPR_ENA, HPL_ENA_DLY, HPR_ENA_DLY	0.0005	0.0240
43	8'h48	1'b0	3'h0	4'h0	8'h00	4'h0	Disable Charge Pump	0.0005	0.0245
44	8'h19	1'b0	3'h5	4'h1	8'h00	4'h0	VREF = 0 ; ADCL = 0 ; ADCR = 0 ; MICB = 0 ; AINL = 0 ; AINR = 0	0.0005	0.0250
45	8'h1C	1'b0	3'h1	4'h3	8'h00	4'h0	BUFDCOPEN = 0, BUFIOEN = 0 ; Disable current bias circuits	0.0005	0.0255
46	8'h19	1'b0	3'h1	4'h7	8'h00	4'h0	VMIDSEL = 00, disable VMID	0.0005	0.0260
47	8'h08	1'b0	3'h0	4'h4	8'h00	4'h0	CLK_DSP_ENA = 0	0.0005	0.0265
48	8'hFE	1'b1	3'h0	4'h0	8'h00	4'h0	Dummy Write for expansion	0.0005	0.0270

Table 50 Write Sequencer Default Values (RAM =Locations 0-31, ROM = Locations 32-48)

The write sequencer control registers are explained in Table 51.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R87 (57h) Write Sequencer 1	5	WSEQ_ENA	0	Write Sequencer Enable. 0: off 1: on
	4:0	WSEQ_WRITE_ INDEX[4:0]	0_0000	Sets the current location in the Write Sequencer Memory. Writes to the following write sequencer registers will affect this memory location.
R88 (58h) Write Sequencer 2	8	WSEQ_EOS	0	Writes to the EOS field in the current write sequencer memory location (specified by last write to WSEQ_WRITE_INDEX). 0 – not end of current sequence 1 – end of current sequence. The write sequencer will stop after this write has been completed.
	7:0	WSEQ_ADDR[7:0]	0000_0000	This data will be written into the Register Address field of the current write sequencer memory location (specified by WSEQ_WRITE_INDEX).
R89 (59h) Write Sequencer 3	7:0	WSEQ_DATA[7:0]	0000_0000	The Data which is to be used to overwrite the current register bits. Only bits [WSEQ_DATA_WIDTH:0] of this register are used. The remaining bits should be set to 0.
R90 (5Ah) Write Sequencer 4	8	WSEQ_ABORT	0	Quit the current sequence and return control of the device back to the serial control interface
	7	WSEQ_START	0	Starts the write sequencer. The write sequencer will start writing the contents of its memory from WSEQ_START_INDEX until it reaches an end-of-sequence flag. Note, this bit will be reset by the Write Sequencer state machine at the end of each sequence
	5:0	WSEQ_START_ INDEX[5:0]	00_0000	Sequence Start Index. Gives the location in memory that the Write Sequencer will start executing from. 00_0000 -> 01_1111 : locations in RAM portion of memory 10_0000 -> 11_0000 : location in ROM portion of memory. 11_0001 -> 11_1111 : reserved.
R91 (5Bh) Write Sequencer 5	6:4	WSEQ_DATA_ WIDTH[2:0]	000	Sets the highest bit of the bit slice that the write sequencer will write to. Total width = value of this register + 1. For example: 000: Highest bit is 0. Data width 1 001: Highest bit is 1. Data width 2 … 111: Highest bit is 7. Data width 8.
	3:0	WSEQ_DATA_ START[3:0]	0000	Selects the bit in the register for WSEQ_DATA to replace. For example, if: WSEQ_ADDR = 2Eh WSEQ_DATA_WIDTH = 3 WSEQ_DATA_START = 5, In this example the write sequencer (when the sequence is activated) will replace bits [7:5] of register 2Eh with the data supplied in WSEQ_DATA[2:0].

R92 (5Ch) Write Sequencer 6	3:0	WSEQ_DELAY[3:0]	0000	The Delay to be inserted between the current write taking place and the next write taking place. 0000 : 0s 0001 : 125us 0010 : 250us 0011 : 500us 0100 : 1 ms 0101 : 2ms 0110 : 4ms 0111 : 8ms 1000 : 16ms 1001 : 32ms 1010 : 64ms 1011 : 128ms 1100 : 256ms 1101 : 512ms 1110 : 1.024s 1111 : 2.048s
R93 (5Dh) Write Sequencer 7	0	WSEQ_BUSY	0	Read-only Register to give Write Sequencer Status. 0: write sequencer idle, control interface is fully active 1: write sequencer busy, control interface is blocked.

Table 51 Write Sequencer Control

CLOCKING AND SAMPLE RATES

Clocks for the ADC and DAC, DSP core functions, the digital audio interface (AIF), the charge pump and the class D outputs are all derived from the MCLK clock input. This is as show in Figure 43.

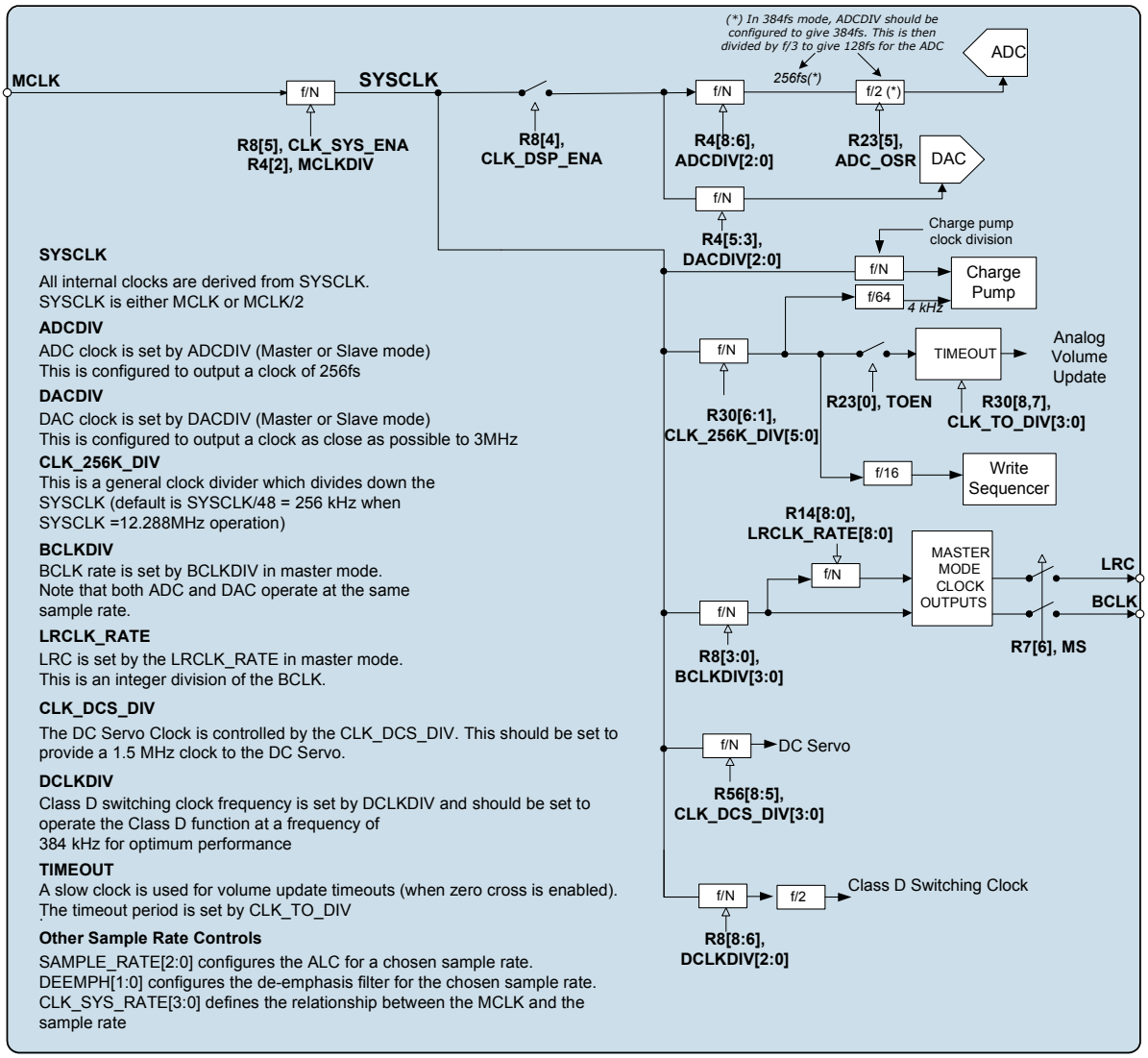


Figure 43 Clock Structure

AUTOMATIC MODE V'S MANUAL MODE CLOCK CONFIGURATION

The clock configuration for the WM8961 can be set automatically or manually (default). The mode of operation is set by MANUAL_MODE, R30[0].

In manual mode the user must configure all the clock registers (described in the following paragraphs) manually.

In automatic mode, SAMPLE_RATE and CLK_SYS_RATE are used to configure the following registers automatically: CLK_256_DIV, CLK_TO_DIV, ADCDIV, DACDIV, CLK_DCS_DIV and DCLKDIV. The BCLKDIV and LRCLK_RATE still require to be set manually in this mode.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R30 (1Eh) Clocking 3	0	MANUAL_MODE	1	Manual clock configuration Enable 0 = When low, use SAMPLE_RATE & CLK_SYS_RATE to allow automatic configuration of system clock dividers. Excludes master mode audio interface clocks. 1 = manual configuration of system clock dividers.
	6:1	CLK_256K_DIV[5:0]	10111	256kHz clock divider setting 000000 : SYSCLK/1 000001 : SYSCLK/2 … 101111 : SYSCLK/48 (default) … 111110 : SYSCLK/63 111111 : SYSCLK/64
R27 (1Bh) Additional Control (3)	2:0	SAMPLE_RATE[2:0]	000	Sample Rate Control for ALC and automatic configuration 000 : 44.1k/48k 001 : 32k 010 : 22.05k/24k 011 : 16k 100 : 11.25k/12k 101 : 8k 110-111 : reserved
R56 (38h) Clocking 4	4:1	CLK_SYS_RATE[3:0]	0011	Specifies the rate of SYSCLK with respect to the sample rate. 0000 : 64*fs 0001 : 128*fs 0010 : 192*fs 0011 : 256*fs 0100 : 384*fs 0101 : 512*fs 0110 : 768*fs 0111 : 1024 *fs 1000 : 1408*fs 1001: 1536*fs 1010 -> 1111 : reserved

Table 52 Clock Configuration: Automatic v's Manual

SYSCLK

SYSCLK is derived directly from MCLK. It is either MCLK or MCLK/2. The CLK_SYS_ENA enables the internal SYSCLK. The CLK_DSP_ENA allows the clock to the DSP, ADC and DAC to be disabled (for power reduction) while peripheral functions continue to be clocked by SYSCLK.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4 (04h) Clocking1	2	MCLKDIV	0	SYSCLK configuration. 0 : SYSCLK = MCLK/1 1 : SYSCLK = MCLK/2
R8 (08h) Clocking2	5	CLK_SYS_ENA	1	Enable system clock. Power saving feature to gate SYSTEM clock. When this bit is enabled, an MCLK must be provided to allow access to the control interface.
	4	CLK_DSP_ENA	1	DSP clock enable. Power saving feature to gate clock to DSP while allowing auxiliary functions to run.

Table 53 SYSCLK Configuration

ADC AND DAC CLOCKING AND SAMPLE RATES

The ADCDIV and DACDIV bits determine the ADC and DAC operating clock. The output of ADCDIV should be configured to output a clock of 256fs. The 256fs output of ADCDIV is further divided such that the ADC operates at 128fs.

The DAC should be configured to run at a clock frequency as close as possible to 3MHz. This requires setting the DACDIV divider to output a clock of at least 64fs.

ADC Example

SYSCLK=12.288 MHz, and fs=24 kHz. Then ADCDIV should be set to 010 (SYSCLK/2)..

This defines the output of the ADCDIV as 256fs = (12.288 MHz /2) = 6.144 MHz.

This 6.144 MHz is further divided by 2 (ADC runs at 128fs) to drive the ADC. Further examples are given in Table 55.

DAC Example

SYSCLK=11.2896 MHz and fs=44.1 kHz. Then DACDIV should be set to =100.

This defines the output of the DACDIV as 64fs = (11.2896 MHz /4) = 2.8224 MHz

Further examples are given in Table 55 (when both ADC and DAC used) and Table 56 (DAC only use).

In master mode the output BCLK is controlled by BCLKDIV, and the LRC is controlled by LRCLK_RATE. These are shown in Table 54 ADC, DAC and Master Mode BCLK and LRC Control.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4 (04h) Clocking1	8:6	ADCDIV[2:0]	000	Defines the ADC 256fs clock, which is further divided by 2. 000 : 256fs = SYSCLK / 1.0 (default =12.288MHz, fs= 48 KHz) 001 : Reserved 010 : 256fs = SYSCLK / 2 011 : 256fs = SYSCLK / 3 100 : 256fs = SYSCLK / 4 101 : 256fs = SYSCLK / 5.5 110 : 256fs = SYSCLK / 6 111 : Reserved
	5:3	DACDIV[2:0]	100	Defines the DAC clock. 000 : DAC clock = SYSCLK / 1 001 : Reserved 010 : DAC clock = SYSCLK / 2 011 : DAC clock = SYSCLK / 3 100 : DAC clock = SYSCLK / 4 (default =3.072 MHz when SYSCLK=12.288MHz) 101 : DAC clock = SYSCLK / 5.5 110 : DAC clock = SYSCLK / 6 111 : Reserved
R8 (08h) Clocking2	3:0	BCLKDIV[3:0]	0100	BCLK Frequency (Master Mode) 0000 = SYSCLK 0001 = Reserved 0010 = SYSCLK / 2 0011 = SYSCLK / 3 0100 = SYSCLK / 4 (default) 0101 = Reserved 0110 = SYSCLK / 6 0111 = SYSCLK / 8 1000 = Reserved 1001 = SYSCLK / 12 1010 = SYSCLK / 16 1011 = SYSCLK / 24 1100 = Reserved 1101 to 1111 = SYSCLK / 32
R14 (0Eh) Audio Interface 2	8:0	LRCLK_RATE[8:0]	0_0100_0000	Integer divide of BCLK. 50:50 LRCLK duty cycle is only guaranteed with even values (4, 6, … … , 510). 0_0000_0000 to 0_0000_0011 : reserved 0_0000_0100 : 4 … 0_0100_0000 : 64 … 1_1111_1110 : 510 1_1111_1111: Reserved

Table 54 ADC, DAC and Master Mode BCLK and LRC Control

EXAMPLE SAMPLE RATE CONFIGURATIONS

Using the registers shown in Table 51, some example ADCDIV and DACDIV settings have been calculated and detailed in Table 52 for various sample rates and SYSCLKs.

ADC / DAC SAMPLE RATE (kHz)	RECOMMENDED SYSCLK (MHZ)	DACDIV	ADCDIV
48	12.288	100 => DAC clk = 12.288 MHz/4.0 = 3.072MHz (=64fs)	000 => 256fs = 12.288 MHz/1.0 =12.288 MHz
32	8.192	100 => DAC clk = 8.192 MHz/4.0 = 2.048MHz (=64fs)	000 => 256fs = 8.192 MHz/1.0 = 8.192 MHz
24	6.144	010 => DAC clk = 6.144 MHz/2.0 = 3.072MHz (=128fs)	000 => 256fs = 6.144 MHz/ 1.0 = 6.144 MHz
12	3.072	000 => DAC clk = 3.072 MHz/1.0 = 3.072MHz (=256fs)	000 => 256fs = 3.072 MHz/ 1.0 = 3.072 MHz
44.1	11.2896	100 => DAC clk = 11.2896MHz/4.0 = 2.8224MHz (=64fs)	000 => 256fs = 11.2896MHz/1.0 =11.2896MHz
22.05	5.6448	010 => DAC clk = 5.6448 MHz/2.0 = 2.8224MHz (=128fs)	000 => 256fs = 5.6448 MHz/1.0 =5.6448 MHz
8	3.072	000 => DAC clk = 3.072 MHz/1.0 = 3.072MHz (=384fs)	000 => 256fs = 3.072 MHz/ 1.0 = 3.072 MHz

Table 55 ADC and DAC Recommended DACDIV and ADCDIV Configuration

If only the DAC is being used (ADC not used) then the SYSCLK can be reduced to save power. This is shown in Table 56.

DAC SAMPLE RATE (kHz)	RECOMMENDED SYSCLK (MHZ)	DACDIV
48	3.072	000 => DAC clk = 3.072 MHz /1.0 = 3.072 MHz (=64fs)
32	2.048	000 => DAC clk = 2.048 MHz/1.0 = 2.048 MHz (=64fs)
24	3.072	000 => DAC clk = 3.072 MHz/1.0 = 3.072 MHz (=128fs)
12	3.072	000 => DAC clk = 3.072 MHz/1.0 = 3.072 MHz (=256fs)
44.1	2.8224	000 => DAC clk = 2.8224 MHz/1.0 = 2.8224 MHz (=64fs)
22.05	2.8224	000 => DAC clk = 2.8224 MHz/1.0 = 2.8224MHz (=128fs)
8	3.072	000 => DAC clk = 3.072 MHz/1.0 = 3.072MHz (=384fs)

Table 56 Recommended DACDIV Configuration for DAC Playback Only

MASTER MODE BCLK CONFIGURATION

The ADC and DAC must be configured to operate at the same sample rate. In master mode the BCLK and LRCLK_RATE must be configured to support this sample rate. The following Table 57 shows example calculations of the maximum word length supported for the ADC and DAC running at different sample rates. Note that ADCDIV, DACDIV and LRCLK_RATE must be configured to be the same sample rate.

SYSCLK (MHz)	SAMPLE RATE	LRCLKRATE	BCLKDIV	BCLK RATE (MASTER MODE) (MHz)	MAXIMUM WORD LENGTH (AT ADC/DAC SAMPLE RATE)
12.288	fs=48 kHz	0x100 =BCLK/256 = 48 kHz	0000 (=1)	12.288	(12.288 MHz/48 kHz) / 2 = 128. => 32 bit word length supported.
		0x040 = BCLK/64 = 48 kHz	0100 (=4)	3.072	(3.072 MHz/48 kHz) / 2 = 32. => 32 bit word length supported.
	Fs=32 kHz	0x180 =BCLK/384 = 32 kHz	0000 (=1)	12.288	(12.288 MHz/32 kHz) / 2 = 192. => 32 bit word length supported.
		0x040 = BCLK/64 = 32 kHz	0110 (=6)	2.048	(2.048 MHz/32 kHz) / 2 = 32. => 32 bit word length supported.
		0x020 = BCLK/32 = 32 kHz	1001 (=12)	1.024	(1.024 MHz/32 kHz) / 2 = 16. => 16 bit word length supported.
11.2896	fs=44.1 kHz	0x100 =BCLK/256 = 44.1 kHz	0000 (=1)	11.2896	(11.2896MHz/44.1 kHz) / 2 = 128. => 32 bit word length supported.
		0x040 = BCLK/64 = 44.1 kHz	0100 (=4)	2.8224	(2.8224MHz/44.1 kHz) / 2 = 32. => 32 bit word length supported.
	Fs=22.05 kHz	0x080 =BCLK/128 = 22.05 kHz	0100 (=4)	2.8224	(2.8224MHz/22.05 kHz) / 2 = 64. => 32 bit word length supported.

Table 57 ADC and DAC Maximum Word Lengths Based on Valid BCLK (master mode) Configuration

ADDITIONAL SAMPLE RATE CONFIGURATION REQUIREMENTS

The DEEMPH[1:0], R5[2:1], should be configured to match the chosen DAC sample rate.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) ADC and DAC Control 1	2:1	DEEMPH[1:0]	00	DAC De-emphasis Filter Control 00: no de-emphasis 01: De-emphasis for 32kHz sample rate 10: De-emphasis for 44.1kHz sample rate 11: De-emphasis for 48kHz sample rate

Table 58 Additional Clock Configuration Register

DC SERVO CLOCK

The DC Servo requires to be clocked at a nominal 1.536MHz. It is controlled by the CLK_DCS_CLK configuration bits as shown in Table 59

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R56 (38h) Clocking 4	8:5	CLK_DCS_DIV[3:0]	1000	Clock divider control for DC Servo, set to get 1.5Mhz from SYSCLK 0000 : SYSCLK/1 0001 : SYSCLK/1.5 0010 : SYSCLK/2 0011 : Reserved 0100 : SYSCLK/3 0101 : SYSCLK/4 0110 : SYSCLK/5.5 0111 : SYSCLK/6 1000 : SYSCLK/8 (default for 12.288MHz/8 = 1.536MHz) 1001-1111 : Reserved

Table 59 DC Servo Clock Configuration

CLASS D CLOCK

The Class D clock is divided from SYSCLK.

When SYSCLK is 12.288 MHz, the Class D clock operates at an optimum frequency of 384 kHz

When SYSCLK is 11.2896 MHz, the Class D clock operates at an optimum frequency of 352.8 kHz

It is controlled using the DCLKDIV[2:0] configuration bits. For optimal operation, DCLKDIV[2:0] should be set to divide SYSCLK by 16, giving a clock of 768 KHz. This is further divided by 2 by the Class D function which runs at 384 KHz

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 (08h) Clocking2	8:6	DCLKDIV[2:0]	111	Divide of Class D clock from SYSCLK 000 : 1 001 : 2 010 : 3 011 : 4 100 : 6 101 : 8 110 : 12 111 : 16 (default for 12.288MHz/16 = 768 KHz) (Note that Class D function further divides by 2 to run at 384 KHz)

Table 60 Class D Clock Rate Configuration

CHARGE PUMP CLOCK

The Charge pump is driven from the SYSCLK plus a 4 kHz clock also generated from the SYSCLK, and requires a minimum SYSCLK of 2.8224 MHz. The charge pump internal clock is derived from SYSCLK, using a clock divider to generate a nominal 1MHz clock, as shown in Figure 43. The clock divider ratio depends on the SAMPLE_RATE[2:0] and CLK_SYS_RATE[3:0] register settings.

For example, with MCLKDIV=0, SAMPLE_RATE[2:0]=000:

256fs: CLK_SYS_RATE[3:0]=0011 gives a charge pump clock division ratio of 12, hence

- MCLK=12.288MHz gives a charge pump frequency of 1.024MHz at full output power.
- MCLK=11.2896MHz gives a charge pump frequency of 940.8kHz at full output power.

128fs: CLK_SYS_RATE[3:0]=0001 gives a charge pump clock division ratio of 6, hence

- MCLK=6.144MHz gives a charge pump frequency of 1.024MHz at full output power.
- MCLK=5.6448MHz gives a charge pump frequency of 940.8kHz at full output power

TIMEOUT CLOCK

The timeout clock triggers a volume update if a zero-cross has not been detected within the configured time-frame. The timeout is enabled by TOEN and the timeout period is controlled by the CLK_TO_DIV register as shown in Table 61

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R30 (1Eh) Clocking 3	8:7	CLK_TO_DIV[1:0]	00	Timeout/slow clock divider setting 00 : 125Hz (timeout = 8ms) 01 : 250Hz (timeout = 4ms) 10 : 500Hz (timeout = 2ms) 11 : 1kHz (timeout = 1ms)
R23 (17h) Additional control(1)	0	TOEN	0	Slow clock enable for volume update timeout

Table 61 Volume Update Timeout Control

VMID GENERATOR

An internal VMID generator generates AVDD/2 as a reference voltage to be used as the virtual ground for most internal analogue signal processing circuits. The internal VMID is output on the VMID pin. This pin requires a 4.7uF filtering capacitor.

VMIDSEL is the enable for the VMID reference, which defaults to disabled. VMIDSEL allows the charging and discharging of the external VMID capacitor to be controlled. It is recommended that the user use the fast start-up mode (VMIDSEL=11) when VMID is initially enabled. Then the user should switch to a lower power operating mode (VMIDSEL=01) for normal operation.

- **Fast Start Up:** use10kΩ divider
- **Normal Mode:** use 100kΩ divider
- **Standby:** use 500kΩ divider

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R25 (19h) Power Management (1)	8:7	VMIDSEL	00	VMID Divider Enable and Select 00 = VMID disabled (for OFF mode) 01 = 2 x 50kΩ divider enabled (for normal playback / record) 10 = 2 x 250kΩ divider enabled (for low-power standby) 11 = 2 x 5kΩ divider enabled (for fast start-up)
	6	VREF	0	Enable master bias current source 0 = Master bias current source disabled 1 = Master bias current source enabled
R28 (1Ch) Anti-pop	4	BUFDCOPEN	0	Enables fast startup bias generation
	3	BUFIOEN	0	Internal VMID and fast bias enable
	2	SOFT_ST	0	For anti-pops and clicks. VMID Slow start up. Ramp up voltage 0 = function disabled 1 = slow VMID slew rate selected

Table 62 VMIDSEL Control Registers

The BUFDCCOPEN and BUFIOEN are used internally to enable the internal VMID and to enable the internal fast start-up bias current. Users should enable both (set them to 1). The SOFT_ST bit can be used to give a slow VMID ramp up voltage to reduce possibility of pops and clicks at start-up.

THERMAL SHUTDOWN AND STATUS

The speaker outputs can drive very large currents. To protect the WM8961 from overheating a thermal shutdown circuit is included. If the device temperature reaches approximately 150^0C and the thermal shutdown circuit is enabled (TSDEN = 1; TSENSEN = 1) the speaker amplifiers (SPK_LP, SPK_LN, SPK_RP and SPK_RN) will be disabled.

TSENSEN must be set to 1 to enable the temperature sensor when using the TSDEN thermal shutdown function.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 (17h) Additional Control (1)	8	TSDEN	1	Thermal Shutdown Enable 0 = Thermal shutdown disabled 1 = Thermal shutdown enabled (TSENSEN must be enabled for this function to work)
R48 (30h) Additional Control (4)	1	TSENSEN	1	Temperature Sensor Enable 0 = Temperature sensor disabled 1 = Temperature sensor enabled

Table 63 Thermal Shutdown

In addition to the thermal shutdown registers, there are 2 status (read only) registers which can be used to check the status of the temperature sensor. These are the TEMP_WARN and TEMP_SHUT status bits

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R47 (2Fh) Pwr Mgmt (3)	1	TEMP_SHUT	0	Read only status of temperature sensor triggers at 145 degrees C
	0	TEMP_WARN	0	Read only status of temperature sensor – triggers at 125 degrees C

Table 64 Thermal Status

CHIP DEVICE ID

The device ID can be read back from register 1 bits [15:9]. (Note that writing to this register is also used to configure the Right Input Volume)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 (01h) Reset / ID	15:12	DEVICE_ID [3:0]	0000	Reading from this register will indicate device family ID Device ID: [3:0] 0000 = 1801 0001-1111 : unused
	11:9	CHIP_REV[2:0]	010	Device Revision: [2:0] 000 = Rev A 001 = Rev B 010 = Rev C 011-111 : unused

Table 65 Chip Device ID

CHIP SOFTWARE RESET

The device can be reset by writing any value to register 15.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R15 (0Fh) Software Reset	15:0	SW_RST_DEV_ID1 [15:0]	0x1801	Writing to this register resets all registers to their default state = Software Reset Read from register = Device number = 1801

Table 66 Chip Reset

REGISTER MAP

The complete register map is shown below. The detailed description can be found in the relevant text of the device description. The WM8961 can be configured using the Control Interface. All registers not listed and all unused bits should not be written to.
All registers can be read back. Registers R1[15:12] returns the device ID when read.

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R0 (0h)	Left Input volume	0	0	0	0	0	0	0	IPVU	LINMUTE	LIZC	LINVOL[5:0]						009Fh
R1 (1h)	Right Input volume	DEVICE_ID[3:0]				CHIP_REV[2:0]			IPVU	RINMUTE	RIZC	RINVOL[5:0]						029Fh
R2 (2h)	LOUT1 volume	0	0	0	0	0	0	0	OUT1VU	LO1ZC	LOUT1VOL[6:0]							0000h
R3 (3h)	ROUT1 volume	0	0	0	0	0	0	0	OUT1VU	RO1ZC	ROUT1VOL[6:0]							0000h
R4 (4h)	Clocking1	0	0	0	0	0	0	0	ADCDIV[2:0]			DACDIV[2:0]			MCLKDIV	0	0	0020h
R5 (5h)	ADC & DAC Control 1	0	0	0	0	0	0	0	0	0	ADCPOL[1:0]		0	DACMU	DEEMPH[1:0]		ADCHPD	0008h
R6 (6h)	ADC & DAC Control 2	0	0	0	0	0	0	0	DC_HPF_CUT[1:0]		DACPOL[1:0]		0	DACSMM	DACMR	ACSLOPE	AC_OSR128	0000h
R7 (7h)	Audio Interface 0	0	0	0	0	0	0	0	LRSWAP	BCLKINV	MS	LRSWAP	LRP	WL[1:0]		FORMAT[1:0]		000Ah
R8 (8h)	Clocking2	0	0	0	0	0	0	0	DCLKDIV[2:0]			CLK_SYS_ENA	CLK_DSP_ENA	BCLKDIV[3:0]				01F4h
R9 (9h)	Audio Interface 1	0	0	0	0	0	0	0	0	0	0	0	DACCOMP[1:0]		ADCCOMP[1:0]		LOOPBACK	0000h
R10 (Ah)	Left DAC volume	0	0	0	0	0	0	0	DACVU	LDACVOL[7:0]								00FFh
R11 (Bh)	Right DAC volume	0	0	0	0	0	0	0	DACVU	RDACVOL[7:0]								00FFh
R14 (Eh)	Audio Interface 2	0	0	0	0	0	0	0	LRCLK_RATE[8:0]									0040h
R15 (Fh)	Software Reset	SW_RST_DEV_ID1[15:0]																1801h
R17 (11h)	ALC1	0	0	0	0	0	0	0	ALCSEL[1:0]		MAXGAIN[2:0]			ALCL[3:0]				007Bh
R18 (12h)	ALC2	0	0	0	0	0	0	0	0	0	MINGAIN[2:0]			HLD[3:0]				0000h
R19 (13h)	ALC3	0	0	0	0	0	0	0	ALCMODE	DCY[3:0]				ATK[3:0]				0032h
R20 (14h)	Noise Gate	0	0	0	0	0	0	0	0	NGTH[4:0]					0	NGG	NGAT	0000h
R21 (15h)	Left ADC volume	0	0	0	0	0	0	0	ADCVU	LADCVOL[7:0]								00C0h
R22 (16h)	Right ADC volume	0	0	0	0	0	0	0	ADCVU	RADCVOL[7:0]								00C0h
R23 (17h)	Additional control(1)	0	0	0	0	0	0	0	TSDEN	0	0	0	MONOMIX	0	0	0	TOEN	0120h
R24 (18h)	Additional control(2)	0	0	0	0	0	0	0	0	0	0	0	0	TRIS	0	0	0	0000h
R25 (19h)	Pwr Mgmt (1)	0	0	0	0	0	0	0	VMIDSEL[1:0]		VREF	AINL	AINR	ADCL	ADCR	MICB	0	0000h
R26 (1Ah)	Pwr Mgmt (2)	0	0	0	0	0	0	0	DACL	DACR	OUT1_PGA	OUT1_PGA	KL_PGA	KR_PGA	0	0	0	0000h
R27 (1Bh)	Additional Control (3)	0	0	0	0	0	0	0	0	0	0	0	0	0	SAMPLE_RATE[2:0]			0000h
R28 (1Ch)	Anti-pop	0	0	0	0	0	0	0	0	0	0	0	UFDCOPEN	UFIOEN	SOFT_ST	0	0	0000h
R30 (1Eh)	Clocking 3	0	0	0	0	0	0	0	CLK_TO_DIV[1:0]		CLK_256K_DIV[5:0]						MANUAL_MODE	005Fh
R32 (20h)	ADCL signal path	0	0	0	0	0	0	0	0	0	0	LMICBOOST[1:0]		0	0	0	0	0000h
R33 (21h)	ADCR signal	0	0	0	0	0	0	0	0	0	0	RMICBOOST[1:0]		0	0	0	0	0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
	path																	
240 (28h)	LOUT2 volume	0	0	0	0	0	0	0	SPKVU	SPKLZC	SPKLVOL[6:0]							0000h
241 (29h)	ROUT2 volume	0	0	0	0	0	0	0	SPKVU	SPKRZC	SPKRVOL[6:0]							0000h
247 (2Fh)	Pwr Mgmt (3)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EMP_SHT	EMP_WARN	0000h
248 (30h)	Additional Control (4)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SENSEN	MBSEL	0023h
249 (31h)	Class D Control 1	0	0	0	0	0	0	0	0	PKR_ENA	PKL_ENA	0	0	0	0	0	0	0000h
251 (33h)	Class D Control 2	0	0	0	0	0	0	0	0	0	0	0	0	0	CLASSD_ACGAIN[2:0]			0003h
256 (38h)	Clocking 4	0	0	0	0	0	0	0	CLK_DCS_DIV[3:0]				CLK_SYS_RATE[3:0]				0	0106h
257 (39h)	DSP Sidetone 0	0	0	0	0	0	0	0	0	ADCR_DAC_SVOL[3:0]				DC_TO_DACR[1:0]		0	0	0000h
258 (3Ah)	DSP Sidetone 1	0	0	0	0	0	0	0	0	ADCL_DAC_SVOL[3:0]				DC_TO_DACL[1:0]		0	0	0000h
260 (3Ch)	DC Servo 0	0	0	0	0	0	0	0	0	CS_ENA_HAN_INL	CS_TRIG_STARTUP_INL	0	CS_TRIG_SERIES_NL *(K)*	CS_ENA_HAN_INR	CS_TRIG_STARTUP_INR	0	CS_TRIG_SERIES_NR *(K)*	0000h
261 (3Dh)	DC Servo 1	0	0	0	0	0	0	0	0	CS_ENA_HAN_HPL	CS_TRIG_STARTUP_HPL	0	CS_TRIG_SERIES_PL	CS_ENA_HAN_HPR	CS_TRIG_STARTUP_HPR	0	CS_TRIG_SERIES_PR	0000h
263 (3Fh)	DC Servo 3	0	0	0	0	0	0	0	0	0	0	CS_FILT_BW_SERIES[1:0]		0	0	0	0	015Eh
265 (41h)	DC Servo 5	0	0	0	0	0	0	0	0	0	DCS_SERIES_NO_HP[6:0]							0010h
268 (44h)	Analogue PGA Bias	0	0	0	0	0	0	0	0	0	0	0	0	0	HP_PGAS_BIAS[2:0]			0003h
269 (45h)	Analogue HP 0	0	0	0	0	0	0	0	0	HPL_RMV_SHORT	HPL_ENA_OUTP	HPL_ENA_DLY	HPL_ENA	HPR_RMV_SHORT	HPR_ENA_OUTP	HPR_ENA_DLY	HPR_ENA	0000h
271 (47h)	Analogue HP 2	0	0	0	0	0	0	0	HPL_VOL[2:0]			HPR_VOL[2:0]			HP_BIAS_BOOST[2:0]			01FBh
272 (48h)	Charge Pump 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CP_ENA	0000h
282 (52h)	Charge Pump B	0	0	0	0	0	0	0	0	0	0	0	0	0	0	P_DYN_PWR[1:0]		0000h
287 (57h)	Write Sequencer 1	0	0	0	0	0	0	0	0	0	0	WSEQ_ENA	WSEQ_WRITE_INDEX[4:0]					0000h
288 (58h)	Write Sequencer 2	0	0	0	0	0	0	0	WSEQ_ECS	WSEQ_ADDR[7:0]								0000h
289 (59h)	Write Sequencer 3	0	0	0	0	0	0	0	0	WSEQ_DATA[7:0]								0000h
290 (5Ah)	Write Sequencer 4	0	0	0	0	0	0	0	WSEQ_ABORT	WSEQ_START	0	WSEQ_START_INDEX[5:0]						0000h
291 (5Bh)	Write Sequencer 5	0	0	0	0	0	0	0	0	0	WSEQ_DATA_WIDTH[2:0]			WSEQ_DATA_START[3:0]				0000h
292 (5Ch)	Write Sequencer 6	0	0	0	0	0	0	0	0	0	0	0	0	WSEQ_DELAY[3:0]				0000h
293 (5Dh)	Write Sequencer 7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	WSEQ_BUSY	0000h
252 (FCh)	General test 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ARA_ENA	AUTO_INC	0001h

REGISTER BITS BY ADDRESS

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 (00h) Left Input volume	8	IPVU	0	Write 1 to do a volume update on inputs
	7	LINMUTE	1	Left Input PGA Analogue Mute 1 = Enable Mute 0 = Disable Mute Note: IPVU must be set to un-mute.
	6	LIZC	0	Zero cross enable. Requires separate register write before volume setting. 0 : Disable zero cross on left input PGA 1 : Enable zero cross
	5:0	LINVOL[5:0]	01_1111	Left input PGA gain, 0.75dB steps 000000 : -23.25dB 000001 : -22.50dB … 011111 : 0dB … 111110 : 23.25dB 111111 : 24.00dB

Register 00h Left Input volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 (01h) Right Input volume	15:12	DEVICE_ID [3:0]	0000	Reading from this register will indicate device family ID Device ID: [3:0] 0000 = 1801 0001-1111 : unused
	11:9	CHIP_REV[2:0]	010	Device Revision: [2:0] 000 = Rev A 001 = Rev B 010 = Rev C 011-111 : unused
	8	IPVU	0	Write 1 to do a volume update on inputs
	7	RINMUTE	1	Right Input PGA Analogue Mute 1 = Enable Mute 0 = Disable Mute Note: IPVU must be set to un-mute.
	6	RIZC	0	Zero cross enable. Requires separate register write before volume setting. 0 : Disable 1 : Enable
	5:0	RINVOL[5:0]	01_1111	Right input PGA gain, 0.75dB steps 000000 : -23.25dB 000001 : -22.50dB … 011111 : 0dB … 111110 : 23.25dB 111111 : 24.00dB

Register 01h Right Input volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h) LOUT1 volume	8	OUT1VU	0	Write 1 to do volume update on outputs
	7	LO1ZC	0	Left HP output zero cross enable
	6:0	LOUT1VOL[6:0]	000_0000	Left HP output PGA gain, 1dB steps 0000000 to 0101111 : Mute 0110000 : -73dB … 1111001 : 0dB … 1111111 : +6dB

Register 02h LOUT1 volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 (03h) ROUT1 volume	8	OUT1VU	0	Write 1 to do volume update on outputs
	7	RO1ZC	0	Right HP output zero cross enable
	6:0	ROUT1VOL[6:0]	000_0000	Right HP output PGA gain, 1dB steps 0000000 to 0101111 : Mute 0110000 : -73dB … 1111001 : 0dB … 1111111 : +6dB

Register 03h ROUT1 volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4 (04h) Clocking1	8:6	ADCDIV[2:0]	000	Defines the ADC 256fs clock, which is further divided by 2. 000 : 256fs = SYSCLK / 1.0 (default =12.288MHz, fs= 48 KHz) 001 : Reserved 010 : 256fs = SYSCLK / 2 011 : 256fs = SYSCLK / 3 100 : 256fs = SYSCLK / 4 101 : 256fs = SYSCLK / 5.5 110 : 256fs = SYSCLK / 6 111 : Reserved
	5:3	DACDIV[2:0]	100	Defines the DAC clock. 000 : DAC clock = SYSCLK / 1 001 : Reserved 010 : DAC clock = SYSCLK / 2 011 : DAC clock = SYSCLK / 3 100 : DAC clock = SYSCLK / 4 (default =3.072 MHz when SYSCLK=12.288MHz) 101 : DAC clock = SYSCLK / 5.5 110 : DAC clock = SYSCLK / 6 111 : Reserved
	2	MCLKDIV	0	Pre-divide MCLK to get SYSCLK. 0 : Divide by 1 1 : Divide by 2

Register 04h Clocking1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) ADC and DAC Control 1	6:5	ADCPOL[1:0]	00	ADC Data invert 00 : Both Channels normal polarity 01 : Left Channel Inverted 10 : Right Channel Inverted 11 : Both Channels Inverted
	3	DACMU	1	Digital DAC mute
	2:1	DEEMPH[1:0]	00	DAC De-emphasis Filter Control 00: no de-emphasis 01: De-emphasis for 32kHz sample rate 10: De-emphasis for 44.1kHz sample rate 11: De-emphasis for 48kHz sample rate
	0	ADCHPD	0	Disables high pass filter

Register 05h ADC and DAC Control 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 (06h) ADC and DAC Control 2	8:7	ADC_HPF_CUT[1:0]	00	ADC High Pass Filter Cutoff 00: Hi-fi mode (fc=4Hz at fs=48kHz) 01: Voice mode 1 (fc=127 at fs=16kHz) 10: Voice mode 2 (fc=130 at fs=8kHz) 11: Voice mode 3 (fc=267Hz at fs=8kHz) (Note: fc scales with sample rate. See Table 14 for cut-off frequencies at all supported sample rates)
	6:5	DACPOL[1:0]	00	DAC Data invert 00 : Both Channels normal polarity 01 : Left Channel Inverted 10 : Right Channel Inverted 11 : Both Channels Inverted
	3	DACSMM	0	0=No soft mute 1=slow volume ramp when DAC muted/un-muted.
	2	DACMR	0	Select fast or slow volume ramp up and down 0: Fast Ramp Rate (24kHz at fs=48k, providing maximum delay of 10.7ms) 1: Slow ramp rate (1.5kHz at fs=48kHz, providing maximum delay of 171ms)
	1	DACSLOPE	0	Sloping stop band enable
	0	DAC_OSR128	0	DAC 128 Over Sampling Rate 0: 64x DAC oversampling 1: If MANUAL_MODE=0, automatically configure DACDIV[2:0] for 128OSR mode. This will give a SNR improvement at the expense of power

Register 06h ADC and DAC Control 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 (07h) Audio Interface 0	8	ALRSWAP	0	Swaps L and R ADC data in interface
	7	BCLKINV	0	BCLK invert bit (for master and slave modes) 0 : BCLK not inverted 1 : BCLK inverted
	6	MS	0	Master / Slave Mode Control 0 : Enable slave mode 1 : Enable master mode
	5	DLRSWAP	0	Swap Left/Right channels on DAC path
	4	LRP	0	Right, Left and I2S modes – LRC polarity 0 : normal LRC polarity 1 : invert LRC polarity DSP Mode – mode A/B select 0 : MSB is available on 2nd BCLK rising edge after LRC rising edge (mode A) 1 : MSB is available on 1st BCLK rising edge after LRC rising edge (mode B)
	3:2	WL[1:0]	10	Audio Interface Word Length 00 : 16 bit 01 : 20 bit 10 : 24 bit 11 : 32 bit
	1:0	FORMAT[1:0]	10	Audio Interface Format 00: Right Justified 01: Left Justified 10: I2S 11: DSP

Register 07h Audio Interface 0

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 (08h) Clocking2	8:6	DCLKDIV[2:0]	111	Class D switching clock divider. 000 = SYSCLK / 1 001 = SYSCLK / 2 010 = SYSCLK / 3 011 = SYSCLK / 4 100 = SYSCLK / 6 101 = SYSCLK / 8 110 = SYSCLK / 12 111 = SYSCLK / 16 (default for 12.288MHz/16 = 768 KHz) (Note that Class D function further divides by 2 to run at 384 KHz)
	5	CLK_SYS_ENA	1	Enable system clock. Power saving feature to gate clock to digital. When this bit is enabled, an MCLK must be provided to allow access to the control interface.
	4	CLK_DSP_ENA	1	DSP clock enable. Power saving feature to gate clock to DSP while allowing auxiliary functions to run
	3:0	BCLKDIV[3:0]	0100	BCLK Frequency (Master Mode) 0000 = SYSCLK 0001 = Reserved 0010 = SYSCLK / 2 0011 = SYSCLK / 3 0100 = SYSCLK / 4 (default) 0101 = Reserved 0110 = SYSCLK / 6 0111 = SYSCLK / 8

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
				1000 = Reserved 1001 = SYSCLK / 12 1010 = SYSCLK / 16 1011 = SYSCLK / 24 1100 = Reserved 1101 to 1111 = SYSCLK / 32

Register 08h Clocking2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R9 (09h) Audio Interface 1	4:3	DACCOMP[1:0]	00	DAC data companding mode 00 : off 01 : reserved 10 : µ-law 11 : A-law
	2:1	ADCCOMP[1:0]	00	ADC data companding mode 00 : off 01 : reserved 10 : µ-law 11 : A-law
	0	LOOPBACK	0	Audio interface loopback mode enable 0 : No loopback 1 : Loopback enabled, ADC data output is fed directly into DAC data input

Register 09h Audio Interface 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R10 (0Ah) Left DAC volume	8	DACVU	0	DAC digital volume update Writing 1 to this bit will cause left and right DAC volumes to be updated (LDACVOL and RDACVOL)
	7:0	LDACVOL[7:0]	1111_1111	Left DAC digital volume FFh -> C0h : 0dB BFh : -0.375dB Beh: -0.75dB ….. in steps of -0.375dB to 02h: -71.25dB 01h: -71.625dB 00h: Digital Mute

Register 0Ah Left DAC volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R11 (0Bh) Right DAC volume	8	DACVU	0	DAC digital volume update Writing 1 to this bit will cause left and right DAC volumes to be updated (LDACVOL and RDACVOL)
	7:0	RDACVOL[7:0]	1111_1111	Right DAC digital volume FFh -> C0h : 0dB BFh : -0.375dB Beh: -0.75dB ….. in steps of -0.375dB to 02h: -71.25dB 01h: -71.625dB 00h: Digital Mute

Register 0Bh Right DAC volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R14 (0Eh) Audio Interface 2	8:0	LRCLK_RATE[8:0]	0_0100_0000	Integer divide of BCLK. 50:50 LRCLK duty cycle is only guaranteed with even values (4, 6, … … , 510). 0_0000_0000 to 0_0000_0011 : reserved 0_0000_0100 : 4 … 0_0100_0000 : 64 … 1_1111_1110 : 510 1_1111_1111: Reserved

Register 0Eh Audio Interface 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R15 (0Fh) Software Reset	15:0	SW_RST_DEV_ID1[15:0]	0001_1000_0000_0001	Software Reset

Register 0Fh Software Reset

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R17 (11h) ALC1	8:7	ALCSEL[1:0]	00	ALC Function Select 00 : ALC off (PGA gain set by register) 01 : Right channel only 10: Left channel only 11 : Stereo (PGA registers unused). Note: ensure that LINVOL and RINVOL settings are the same before entering this mode.
	6:4	MAXGAIN[2:0]	111	ALC Max Gain 000 : -18dB 001 : -12dB 010 : -6dB 011 : 0dB 100 : 6dB 101 : 12dB 110 : 18dB 111 : 24dB
	3:0	ALCL[3:0]	1011	ALC Target Level (dB FS) 0000 : -28.5 0001 : -27 …1.5dB steps… 1111 : -6

Register 11h ALC1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R18 (12h) ALC2	6:4	MINGAIN[2:0]	000	Min gain setting 000 : -23.25dB 001 : -17.25dB 010 : -11.25dB 011 : -5.25dB 100 : +0.75dB 101 : +6.75dB 110 : +12.75dB 111 : +18.75dB
	3:0	HLD[3:0]	0000	ALC Hold time 0000 : 0ms 0001 : 2.67ms 0010 : 5.33ms Doubling with each step up to… 1111 : 43.691s

Register 12h ALC2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R19 (13h) ALC3	8	ALCMODE	0	Determines the ALC mode of operation: 0 = ALC mode 1 = Limiter mode ALCSEL[1:0] bits must be set to 00 before changing this bit.
	7:4	DCY[3:0]	0011	ALC Decay (gain ramp-up) time 0000 : 24ms 0001 : 48ms Doubling each step… 1010-1111 : 24.58s
	3:0	ATK[3:0]	0010	ALC Attack (gain ramp-down) time 0000 : 6ms 0001 : 12ms 0010 : 24ms … (time doubles with every step) 1010 to 1111 : 6.14s

Register 13h ALC3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R20 (14h) Noise Gate	7:3	NGTH[4:0]	0_0000	Noise Gate Threshold 00000 : -76.5dB FS 00001 : -75dB FS 1.5dB steps… 1111-30dB FS
	1	NGG	0	Noise gate mode 0 : Hold PGA gain static (recommended) 1 : Mute ADC output
	0	NGAT	0	Noise Gate Enable

Register 14h Noise Gate

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R21 (15h) Left ADC volume	8	ADCVU	0	ADC digital volume update Writing 1 to this bit will cause left and right ADC volumes to be updated (LADCVOL and RADCVOL)
	7:0	LADCVOL[7:0]	1100_0000	ADC Left Channel Digital Volume. FFh -> Efh: +17.625dB EEh: +17.25dB …… in steps of -0.375dB to C0h : 0dB BFh : -0.375dB Beh: -0.75dB ….. in steps of -0.375dB to 02h: -71.25dB 01h: -71.625dB 00h: Digital Mute

Register 15h Left ADC Volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R22 (16h) Right ADC volume	8	ADCVU	0	ADC digital volume update Writing 1 to this bit will cause left and right ADC volumes to be updated (LADCVOL and RADCVOL)
	7:0	RADCVOL[7:0]	1100_0000	ADC Right Channel Digital Volume. FFh -> Efh: +17.625dB EEh: +17.25dB …… in steps of -0.375dB to C0h : 0dB BFh : -0.375dB Beh: -0.75dB ….. in steps of -0.375dB to 02h: -71.25dB 01h: -71.625dB 00h: Digital Mute

Register 16h Right ADC volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 (17h) Additional control(1)	8	TSDEN	1	Enable auto shutdown of speaker driver on temperature overheat condition 0 : Thermal Shutdown disabled 1 : Thermal Shutdown enabled (TSENSEN must be enabled for this function to work)
	4	DMONOMIX	0	DAC Mono Mix 0 : Stereo 1 : Mono (Mono MIX output on enabled DAC) Note: Only one DAC can be enabled when using this feature
	0	TOEN	0	Slow clock enable for volume update timeout

Register 17h Additional control(1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24 (18h) Additional control(2)	3	TRIS	0	Tristates ADCDAT and switches LRC and BCLK to inputs. 0 : ADCDAT is an output; LRC and BCLK are inputs (slave mode) or outputs (master mode) 1 : ADCDAT is tristated; LRC and BCLK are inputs

Register 18h Additional Control (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R25 (19h) Pwr Mgmt (1)	8:7	VMIDSEL[1:0]	00	00 = off 01 = 2x50k 10 = 2x250k 11 = 2x5k
	6	VREF	0	Enable master bias current source
	5	AINL	0	Enables Left PGA and boost mixer
	4	AINR	0	Enables Right PGA and boost mixer
	3	ADCL	0	Enable ADC Left channel
	2	ADCR	0	Enable ADC Right channel
	1	MICB	0	Enable MICBIAS circuit

Register 19h Pwr Mgmt (1)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R26 (1Ah) Pwr Mgmt (2)	8	DACL	0	Enable left DAC channel
	7	DACR	0	Enable right DAC channel
	6	LOUT1_PGA	0	Enable left headphone PGA
	5	ROUT1_PGA	0	Enable right headphone PGA
	4	SPKL_PGA	0	Enable left speaker PGA
	3	SPKR_PGA	0	Enable right speaker PGA

Register 1Ah Pwr Mgmt (2)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R27 (1Bh) Additional control (3)	2:0	SAMPLE_RATE[2:0]	000	Sample Rate Control for ALC and auto configuration 000 : 44.1k/48k 001 : 32k 010 : 22.05k/24k 011 : 16k 100 : 11.25k/12k 101 : 8k 110-111 : reserved

Register 1Bh Additional control (3)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R28 (1Ch) Anti-pop	4	BUFDCOPEN	0	Enables fast startup bias gen
	3	BUFIOEN	0	Enables fast startup bias and vmid buffers
	2	SOFT_ST	0	Enables VMID soft start 0 : Disabled 1 : Enabled

Register 1Ch Anti-pop

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R30 (1Eh) Clocking 3	8:7	CLK_TO_DIV[1:0]	00	Timeout/slow clock divider setting 00 : 125Hz 01 : 250Hz 10 : 500Hz 11 : 1kHz
	6:1	CLK_256K_DIV[5:0]	10_1111	256kHz clock divider setting 000000 : SYSCLK/1 000001 : SYSCLK/2 … 101111 : SYSCLK/48 (default) … 111110 : SYSCLK/63 111111 : SYSCLK/64
	0	MANUAL_MODE	1	Manual clock configuration Enable 0 = When low, use SAMPLE_RATE & CLK_SYS_RATE to allow automatic configuration of system clock dividers. Excludes master mode audio interface clocks. 1 = manual configuration of system clock dividers.

Register 1Eh Clocking 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32 (20h) ADCL signal path	5:4	LMICBOOST[1:0]	00	Left microphone boost control 00 : 0dB 01 : 13dB 10 : 20dB 11 : 29dB

Register 20h ADCL signal path

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R33 (21h) ADCR signal path	5:4	RMICBOOST[1:0]	00	Right microphone boost control 00 : 0dB 01 : 13dB 10 : 20dB 11 : 29dB

Register 21h ADCR signal path

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R40 (28h) LOUT2 volume	8	SPKVU	0	Speaker PGA volume update
	7	SPKLZC	0	Left Speaker PGA zero cross enable
	6:0	SPKLVOL[6:0]	000_0000	Left Speaker output PGA gain, 1dB steps 0000000 to 0101111 : Mute 0110000 : -73dB … 1111001 : 0dB … 1111111 : +6dB

Register 28h LOUT2 volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R41 (29h) ROUT2 volume	8	SPKVU	0	Speaker PGA volume update
	7	SPKRZC	0	Right speaker PGA zero cross enable
	6:0	SPKRVOL[6:0]	000_0000	Right Speaker output PGA gain, 1dB steps 0000000 to 0101111 : Mute 0110000 : -73dB … 1111001 : 0dB … 1111111 : +6dB

Register 29h ROUT2 volume

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R47 (2Fh) Pwr Mgmt (3)	1	TEMP_SHUT	0	Read only status of temperature sensor triggers at 145 degrees C
	0	TEMP_WARN	0	Read only status of temperature sensor – triggers at 125 degrees C

Register 2Fh Pwr Mgmt (3)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R48 (30h) Additional Control (4)	1	TSENSEN	1	Enable overheat temp sensor
	0	MBSEL	1	0: MICBIAS = 5/6 AVDD 1: MICBIAS = 7/6 AVDD

Register 30h Additional Control (4)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R49 (31h) Class D Control 1	7	SPKR_ENA	0	Right channel class D enable
	6	SPKL_ENA	0	Left channel Class D enable

Register 31h Class D Control 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R51 (33h) Class D Control 2	2:0	CLASSD_ACGAIN[2:0]	011	AC speaker boost (Boosts speaker AC output signal on both left and right channels) 000 – 1.00 x boost (+0dB) 001 – 1.19 x boost (+1.5dB) 010 – 1.41 x boost (+3dB) 011 – 1.68 x boost (+4.5B) 100 – 2.00 x boost (+6B) 101 – 2.37 x boost (+7.5dB) 110 – 2.81 x boost (+9dB) 111 – 3.98 x boost (+12dB) Note that +12dB setting will cause a full scale output signal to clip.

Register 33h Class D Control 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R56 (38h) Clocking 4	8:5	CLK_DCS_DIV[3:0]	1000	Clock divider control for DC Servo, set to get 1.5Mhz from SYSCLK 0000 : SYSCLK/1 0001 : SYSCLK/1.5 0010 : SYSCLK/2 0011 : Reserved 0100 : SYSCLK/3 0101 : SYSCLK/4 0110 : SYSCLK/5.5 0111 : SYSCLK/6 1000 : SYSCLK/8 1001-1111 : Reserved
	4:1	CLK_SYS_RATE[3:0]	0011	Specifies the rate of SYSCLK with respect to the sample rate. 0000 : 64*fs 0001 : 128*fs 0010 : 192*fs 0011 : 256*fs 0100 : 384*fs 0101 : 512*fs 0110 : 768*fs 0111 : 1024 *fs 1000 : 1408*fs 1001 : 1536*fs 1010 -> 1111 : reserved

Register 38h Clocking 4

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R57 (39h) DSP Sidetone 0	7:4	ADCR_DAC_SVOL[3:0]	0000	Controls volume of ADC Right side tone, 3dB steps. 0000 : -36dB 0001 : -33dB … 1111 : 0dB
	3:2	ADC_TO_DACR[1:0]	00	DAC Right Side-tone Control 11 = Unused 10 = Mix ADCR into DACR 01 = Mix ADCL into DACR 00 = No Side-tone mix into DACR

Register 39h DSP Sidetone 0

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R58 (3Ah) DSP Sidetone 1	7:4	ADCL_DAC_SVOL[3:0]	0000	Controls volume of ADC Left side tone, 3dB steps. 0000 : -36dB 0001 : -33dB … 1111 : 0dB
	3:2	ADC_TO_DACL[1:0]	00	DAC Left Side-tone Control 11 = Unused 10 = Mix ADCR into DACL 01 = Mix ADCL into DACL 00 = No Side-tone mix into DACL

Register 3Ah DSP Sidetone 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R60 (3Ch) DC Servo 0	7	DCS_ENA_CHAN_INL	0	DC Servo enabled on channel INL
	6	DCS_TRIG_STARTUP_INL	0	Perform startup sequence on channel INL
	3	DCS_ENA_CHAN_INR	0	DC Servo enabled on channel INR
	2	DCS_TRIG_STARTUP_INR	0	Perform startup sequence on channel INR

Register 3Ch DC Servo 0

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R61 (3Dh) DC Servo 1	7	DCS_ENA_CHAN_HPL	0	DC Servo enabled on channel HPL
	6	DCS_TRIG_STARTUP_HPL	0	Perform startup sequence on channel HPL
	4	DCS_TRIG_SERIES_HPL	0	Perform a series of LSB updates on channel HPL
	3	DCS_ENA_CHAN_HPR	0	DC Servo enabled on channel HPR
	2	DCS_TRIG_STARTUP_HPR	0	Perform startup sequence on channel HPR
	0	DCS_TRIG_SERIES_HPR	0	Perform a series of LSB updates on channel HPR

Register 3Dh DC Servo 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R63 (3Fh) DC Servo 3	5:4	DCS_FILT_BW_SERIES[1:0]	01	Bandwidth of filter during series updates. Determines how long a measurement takes. 00 : 6ms 01 : 275ms 10 : 1.2s 11 : 4.4s

Register 3Fh DC Servo 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R65 (41h) DC Servo 5	6:0	DCS_SERIES_NO_HP[6:0]	001_0000	Number of LSB updates in a series for channels HPL and HPR 000_0000-000_1111 : Reserved 001_0000 : 16 … 111_1111 : 127

Register 41h DC Servo 5

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R68 (44h) Analogue PGA Bias	2:0	HP_PGAS_BIAS[2:0]	011	Headphone PGA bias options 000 x 2 001 Reserved 010 Reserved 011 x 1 100-111 Reserved

Register 44h Analogue PGA Bias

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R69 (45h) Analogue HP 0	7	HPL_RMV_SHORT	0	Left channel output short removal: set after output stage has been enabled
	6	HPL_ENA_OUTP	0	Enables left channel output stage; set after offset cancellation is done
	5	HPL_ENA_DLY	0	delayed left channel enable, set with at least 20us delay to HPL_ENA; reset together with HPL_ENA
	4	HPL_ENA	0	enables left headphone amplifier. Channel
	3	HPR_RMV_SHORT	0	right channel output short removal: set after output stage has been enabled
	2	HPR_ENA_OUTP	0	enables right channel output stage; set after offset cancellation is done
	1	HPR_ENA_DLY	0	delayed right channel enable, set with at least 20us delay to HPR_ENA; reset together with HPR_ENA
	0	HPR_ENA	0	enables right headphone amplifier. Channel

Register 45h Analogue HP 0

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R72 (48h) Charge Pump 1	0	CP_ENA	0	Enable charge-pump digits 0: disable 1: enable

Register 48h Charge Pump 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R71 (47h) Analogue HP 2	8:6	HPL_VOL[2:0]	111	Secondary HPL PGA Volume 111 0dB (default) 110 -1dB 101 -2dB 100 -3dB 011 -4dB 010 -5dB 001 -6dB 000 -7dB
	5:3	HPR_VOL[2:0]	111	Secondary HPR PGA Volume 111 0dB (default) 110 -1dB 101 -2dB 100 -3dB 011 -4dB 010 -5dB 001 -6dB 000 -7dB
	2:0	HP_BIAS_BOOST[2:0]	011	Boost bias into headphone driver 000: x2 001: Reserved 010: Reserved 011: x1 100-111: Reserved

Register 47h Analogue HP 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R82 (52h) Charge Pump B	1:0	CP_DYN_PWR[1:0]	0	Enable dynamic (Class W) power saving 00: dynamic power saving disabled 01: Reserved 10: Reserved 11: dynamic power saving enabled

Register 52h Charge Pump B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R87 (57h) Write Sequencer 1	5	WSEQ_ENA	0	Write Sequencer Enable. 0: off 1: on
	4:0	WSEQ_WRITE_INDEX[4:0]	0_0000	Sets the current Index in the Write Sequencer Memory. Writes to the following write sequencer registers will affect this memory location.

Register 57h Write Sequencer 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R88 (58h) Write Sequencer 2	8	WSEQ_EOS	0	Writes to the EOS field in the current write sequencer memory location (specified by last write to WSEQ_WRITE_INDEX). 0 – not end of current sequence 1 – end of current sequence. The write sequencer will stop after this write has been completed.
	7:0	WSEQ_ADDR[7:0]	0000_0000	This data will be written into the Register Address field of the current write sequencer memory location (specified by WSEQ_WRITE_INDEX).

Register 58h Write Sequencer 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R89 (59h) Write Sequencer 3	7:0	WSEQ_DATA[7:0]	0000_0000	The Data which is to be used to overwrite the current register bits. Only bits [WSEQ_DATA_WIDTH:0] of this register are used. The remaining bits should be set to 0.

Register 59h Write Sequencer 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R90 (5Ah) Write Sequencer 4	8	WSEQ_ABORT	0	Quit the current sequence and return control of the device back to the serial control interface.
	7	WSEQ_START	0	Starts the write sequencer. The write sequencer will start writing the contents of its memory from WSEQ_START_INDEX until it reaches an end-of-sequence flag. Note that this bit will be reset by the Write Sequencer state machine at the end of each sequence.
	5:0	WSEQ_START_INDEX[5:0]	00_0000	Sequence Start Index. Gives the location in memory that the Write Sequencer will start executing from. 00_0000 -> 01_1111 : locations in RAM portion of memory 10_0000 -> 11_0000 : location in ROM portion of memory. 11_0001 -> 11_1111 : reserved.

Register 5Ah Write Sequencer 4

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R91 (5Bh) Write Sequencer 5	6:4	WSEQ_DATA_WIDTH[2:0]	000	Sets the highest bit of the bit slice that the write sequencer will write to. Total width = value of this register + 1. For example: 000: Highest bit is 0. Data width 1 001: Highest bit is 1. Data width 2 … 111: Highest bit is 7. Data width 8
	3:0	WSEQ_DATA_START[3:0]	0000	Selects the bit in the register for WSEQ_DATA to replace. For example, if: WSEQ_ADDR = 2Eh WSEQ_DATA_WIDTH = 3 WSEQ_DATA_START = 5, the write sequencer (when the sequence is activated) will replace bits [7:5] of register 2Eh with the data supplied in WSEQ_DATA[2:0].

Register 5Bh Write Sequencer 5

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R92 (5Ch) Write Sequencer 6	3:0	WSEQ_DELAY[3:0]	0000	The Delay to be inserted between the current write taking place and the next write taking place. 0000 : 0s 0001 : 125us 0010 : 250us 0011 : 500us 0100 : 1 ms 0101 : 2ms 0110 : 4ms 0111 : 8ms 1000 : 16ms 1001 : 32ms 1010 : 64ms 1011 : 128ms 1100 : 256ms 1101 : 512ms 1110 : 1.024s 1111 : 2.048s

Register 5Ch Write Sequencer 6

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R93 (5Dh) Write Sequencer 7	0	WSEQ_BUSY	0	Read-only Register to give Write Sequencer Status. 0: write sequencer idle, control interface is fully active 1: write sequencer busy, control interface is blocked.

Register 5Dh Write Sequencer 7

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R252 (FCh) General test 1	1	ARA_ENA	0	Alert Response Address Enable 0 : off 1 : on
	0	AUTO_INC	1	Enable Auto-Increment 0 : off 1 : on

Register FCh General Test 1

DIGITAL FILTER CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Filter					
Passband	+/- 0.05dB	0		0.454 fs	
	-6dB		0.5fs		
Passband Ripple				+/- 0.05	dB
Stopband		0.546s			
Stopband Attenuation	f > 0.546 fs	-60			dB
DAC Normal Filter					
Passband	+/- 0.05dB	0		0.454 fs	
	-6dB		0.5 fs		
Passband Ripple	0.454 fs			+/- 0.03	dB
Stopband		0.546 fs			
Stopband Attenuation	F > 0.546 fs	-50			dB
DAC Sloping Stopband Filter					
Passband	+/- 0.03dB	0		0.25 fs	
	+/- 1dB	0.25 fs		0.454 fs	
	-6dB		0.5 fs		
Passband Ripple	0.25 fs			+/- 0.03	dB
Stopband 1		0.546 fs		0.7 fs	
Stopband 1 Attenuation	f > 0.546 fs	-60			dB
Stopband 2		0.7 fs		1.4 fs	
Stopband 2 Attenuation	f > 0.7 fs	-85			dB
Stopband 3		1.4 fs			
Stopband 3 Attenuation	F > 1.4 fs	-55			dB

DAC FILTERS		ADC FILTERS	
Mode	**Group Delay**	**Mode**	**Group Delay**
Normal	16.5 / fs	Normal	16.5 / fs
Sloping Stopband	18 / fs		

TERMINOLOGY

1. Stop Band Attenuation (dB) – the degree to which the frequency spectrum is attenuated (outside audio band)
2. Pass-band Ripple – any variation of the frequency response in the pass-band region

DAC FILTER RESPONSES

This series of plots shows the filter response for the entire DAC channel for different signal rates. The full path, has a nominal gain of 3.01dB (1V input, 1.414V output), this means that the highest nodes in the 48kHz case are at 47.5dB (rather than below the 50dB specification).

Sample Rate (kHz)	Sloping Stop-band	MCLK recommended rate for DAC only playback (CODEC mode) (Hz)
8	Yes	3072000 (3072000)
11.025	Yes	2822400 (2822400)
12	Yes	3072000 (3072000)
16	Yes	2048000 (6144000)
22.05	Yes	2822400 (5644800)
24	Yes	3072000 (6144000)
32	No	2048000 (8192000)
44.1	No	2822400 (11289600)
48	No	3072000 (12288000)

Table 67 Recommended Filter Configurations for Supported Sample Rates

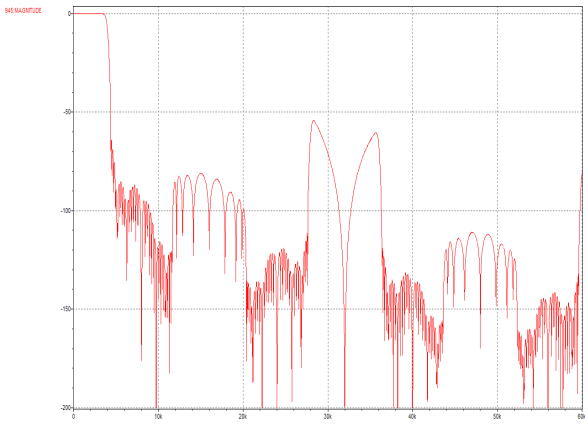


Figure 44 DAC Filter Response 8k Sampling Rate

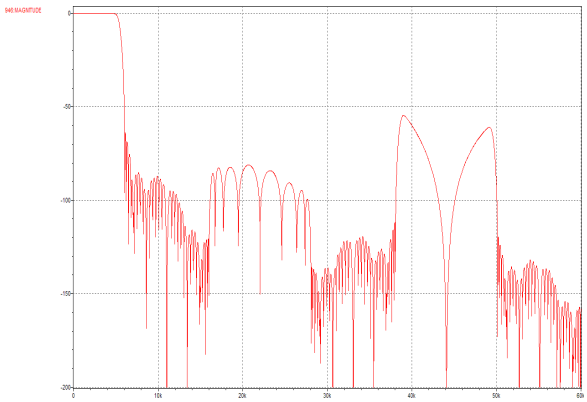


Figure 45 DAC Filter Response for 11.025k Sample Rate

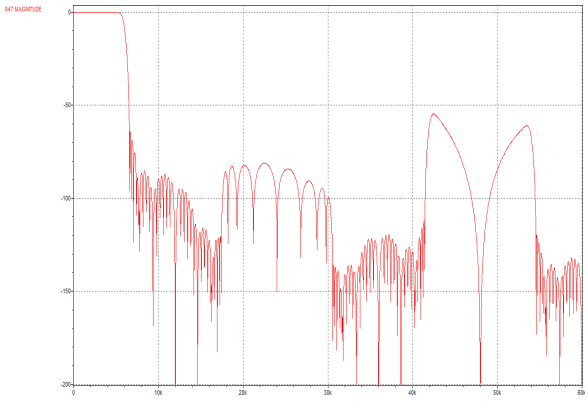


Figure 46 DAC Filter Response for 12k Sample Rate

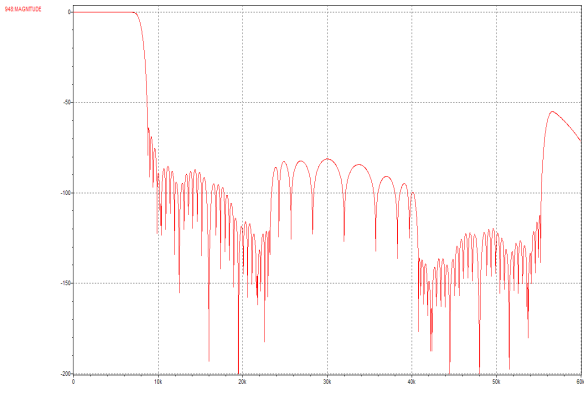


Figure 47 DAC Filter Response for 16k Sample Rate

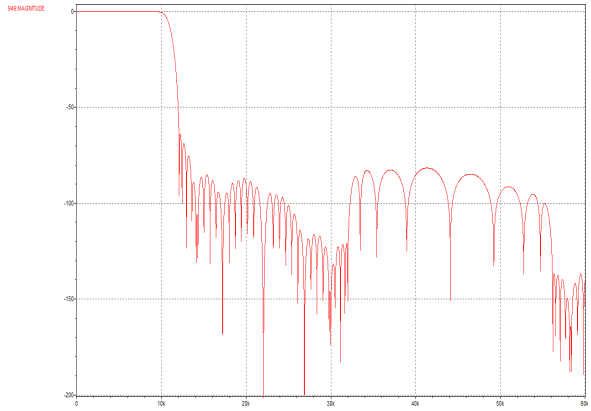


Figure 48 DAC Filter Response 22.05k Sample Rate

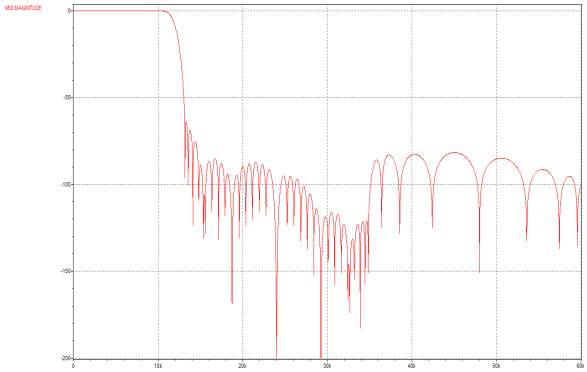


Figure 49 DAC Playback Filter Response for 24k Sample Rate

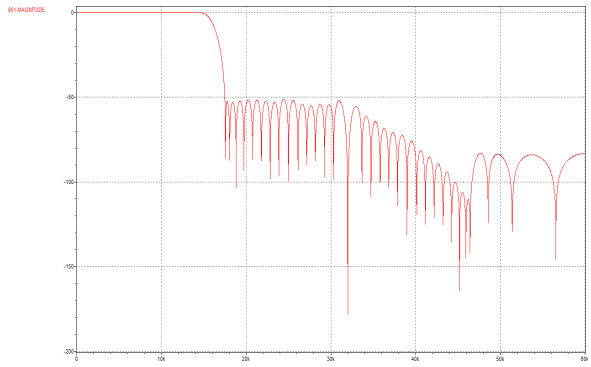


Figure 50 DAC Playback Filter Response for 32k Sample Rate

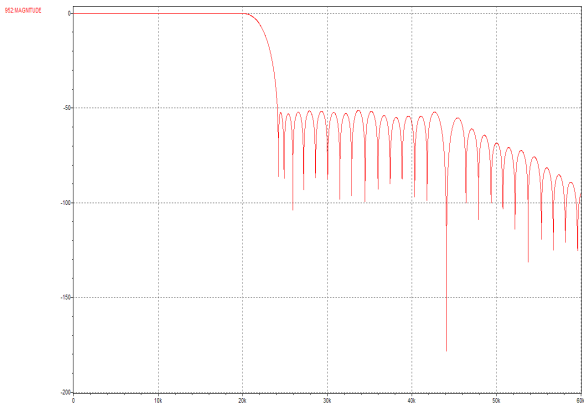


Figure 51 DAC Playback Filter Response for 44.1k Sample Rate

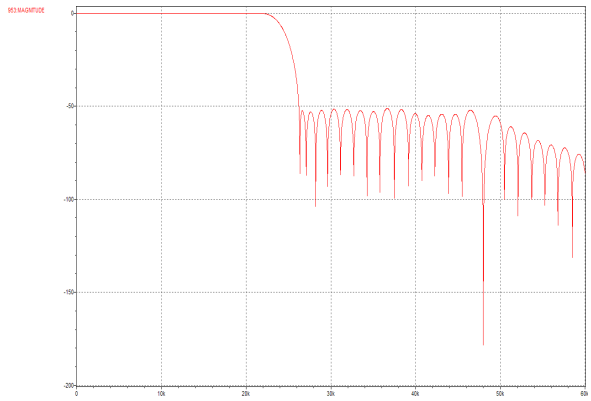


Figure 52 DAC Playback Filter Response for 48k Sample Rate

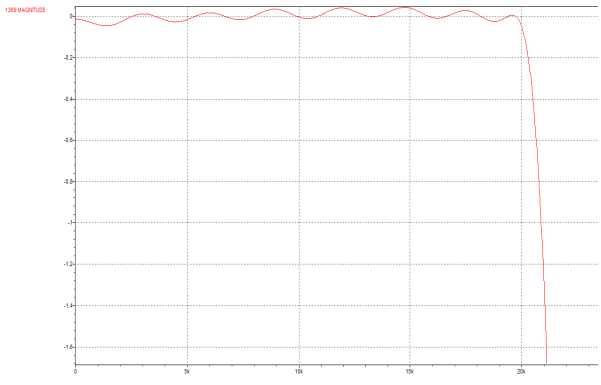


Figure 53 DAC Playback Filter Passband Ripple for 44.1k Sample Rate (MCLK=11.2896MHZ)

ADC FILTER RESPONSES

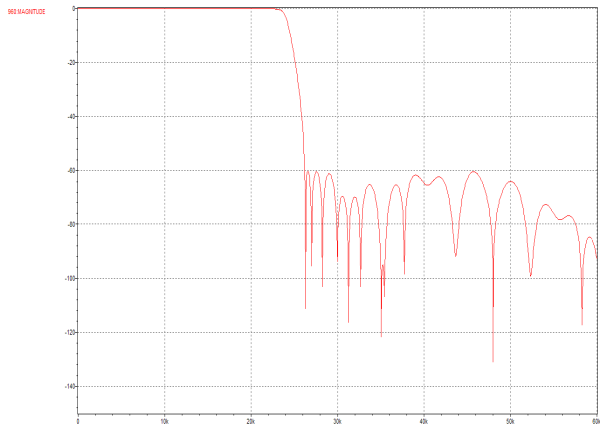


Figure 54 ADC Digital Filter Frequency Response (128OSR)

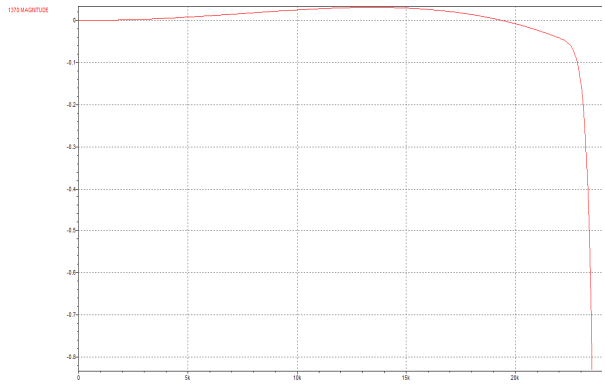


Figure 55 ADC Digital Filter Passband Ripple (128OSR)

ADC HIGH PASS FILTER RESPONSES

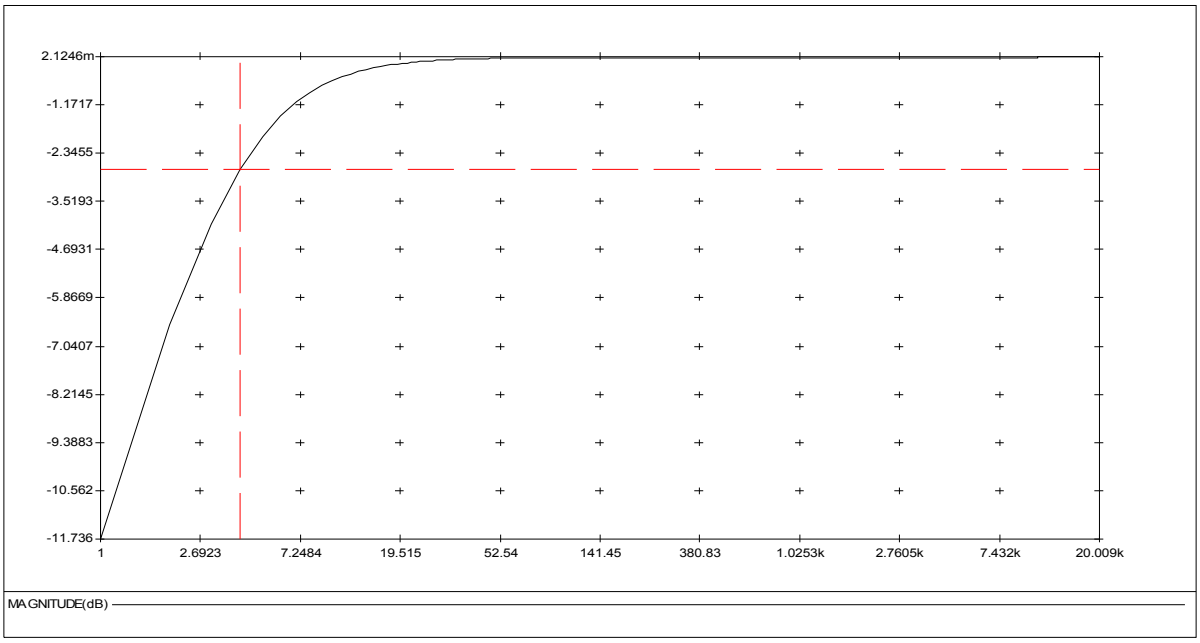


Figure 56 ADC Digital High Pass Filter Frequency Response (48kHz, Hi-Fi Mode, ADC_HPF_CUT[1:0]=00)

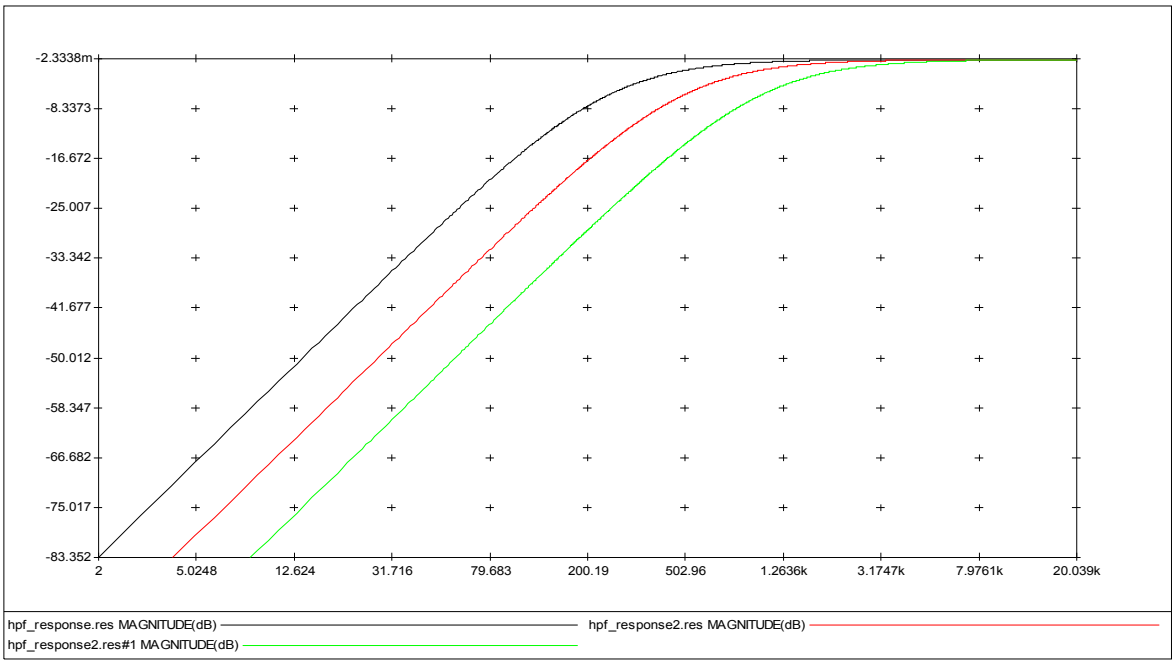


Figure 57 ADC Digital High Pass Filter Ripple (48kHz, Voice Mode, ADC_HPF_CUT=01, 10 and 11)

DE-EMPHASIS FILTER RESPONSES

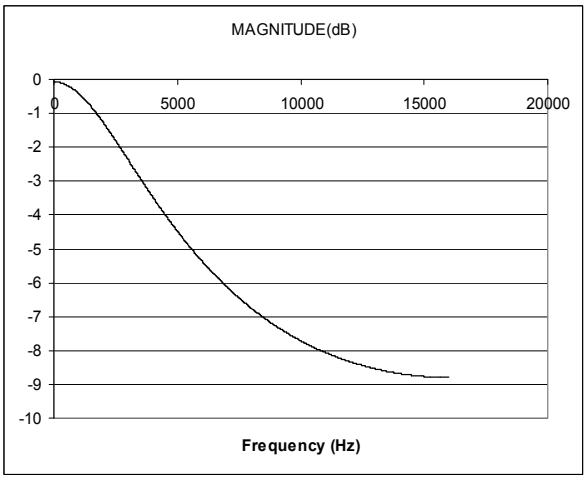


Figure 58 De-Emphasis Digital Filter Response (32kHz)

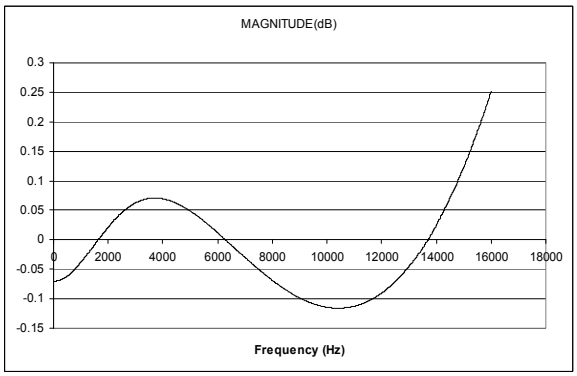


Figure 59 De-Emphasis Error (32kHz)

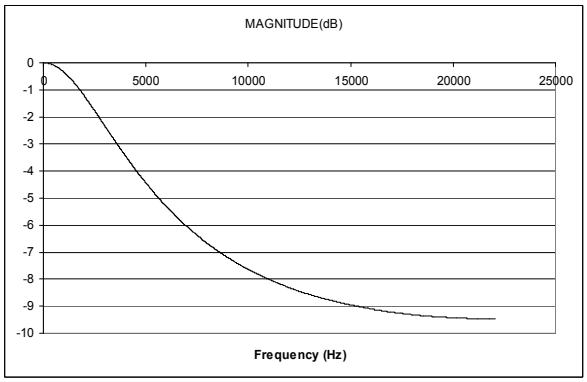


Figure 60 De-Emphasis Digital Filter Response (44.1kHz)

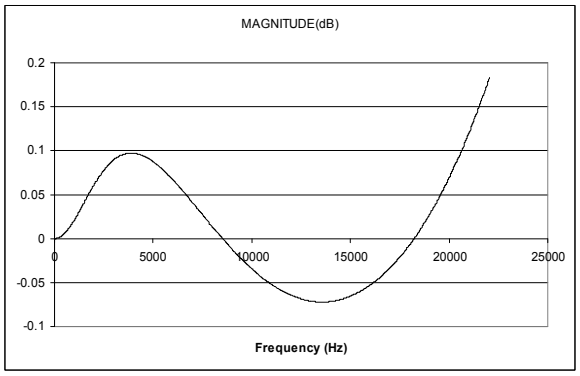


Figure 61 De-Emphasis Error (44.1kHz)

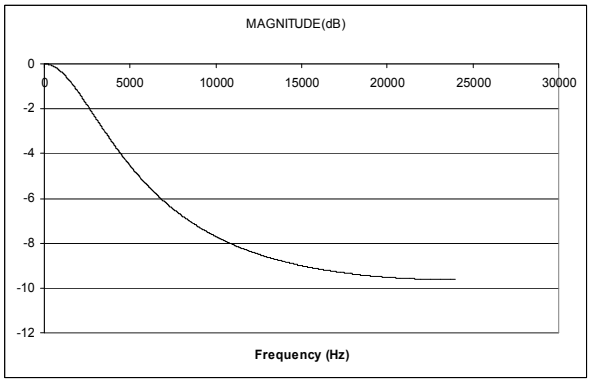


Figure 62 De-Emphasis Digital Filter Response (48kHz)

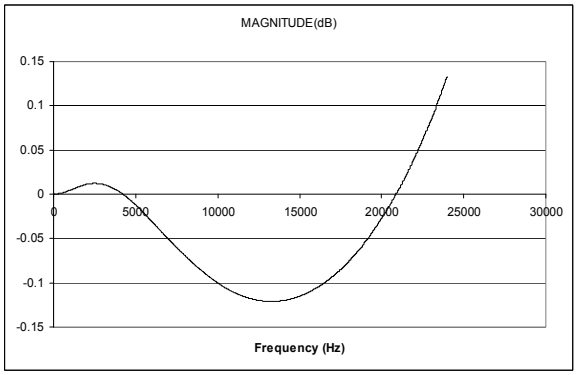


Figure 63 De-Emphasis Error (48kHz)

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

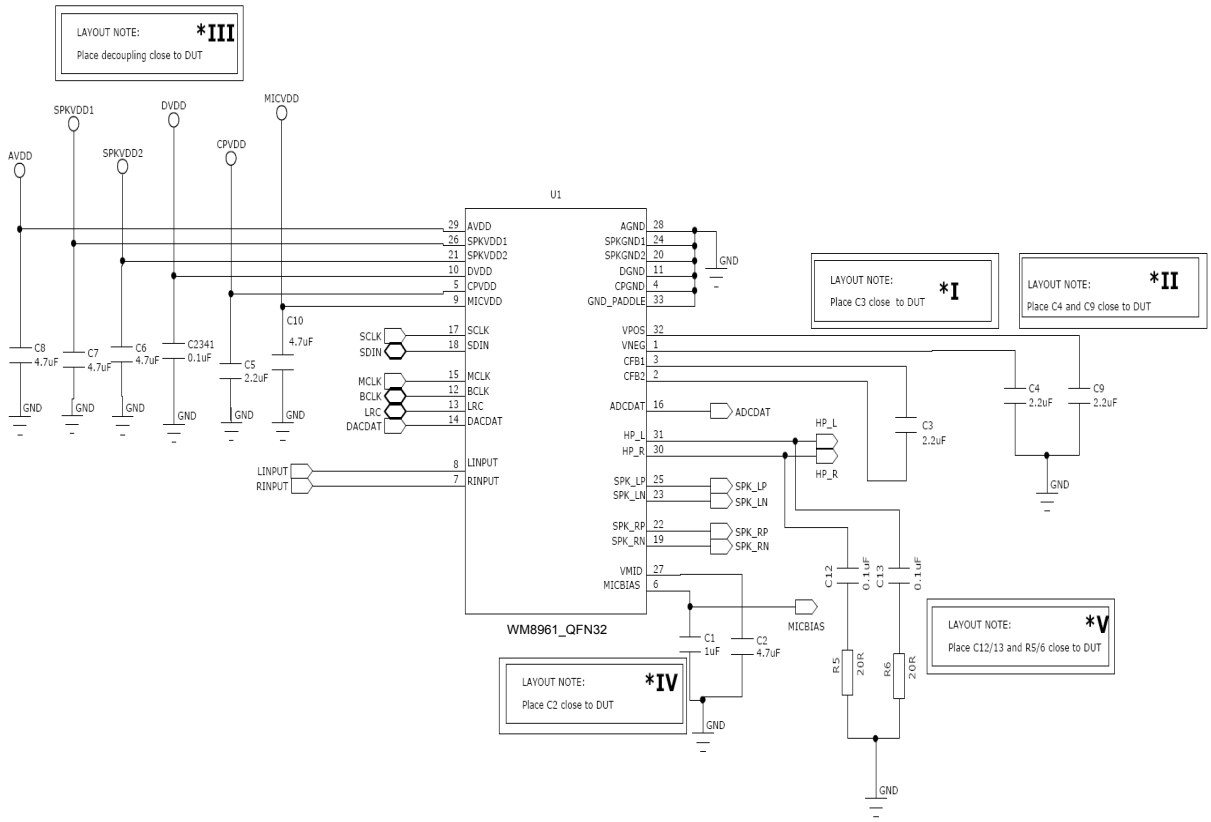


Figure 64 WM8961 Recommended External Components

SPEAKER SELECTION

For filter-less operation, it is important to select a speaker with appropriate internal inductance. The internal inductance and the speaker's load resistance create a low-pass filter with a cut-off frequency of:

$$f_c = R_L / 2\pi L$$

e.g. for an 8Ω speaker and required cut-off frequency of 20kHz, the speaker should be chosen to have an inductance of:

$$L = R_L / 2\pi f_c = 8\Omega / 2\pi * 20kHz = 64\mu H$$

8Ω speakers typically have an inductance in the range 20µH to 100µH. Care should be taken to ensure that the cut-off frequency of the speaker's internal filtering is low enough to prevent speaker damage. The class D outputs of the WM8961 operate at much higher frequencies than is recommended for most speakers, and the cut-off frequency of the filter should be low enough to protect the speaker.

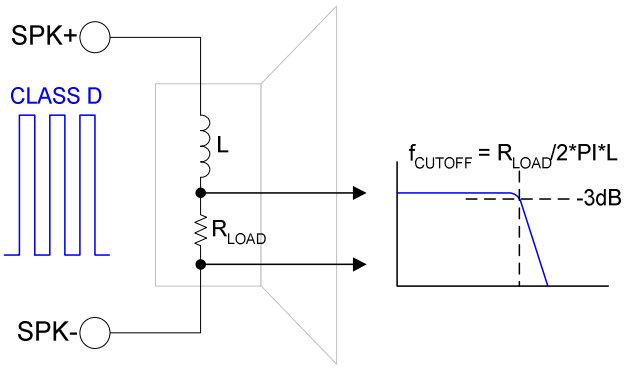


Figure 65 Speaker Equivalent Circuit

PCB LAYOUT CONSIDERATIONS

The efficiency of the speaker drivers is affected by the series resistance between the WM8961 and the speaker (e.g. inductor ESR) as shown in Figure 66. This resistance should be as low as possible to maximize efficiency.

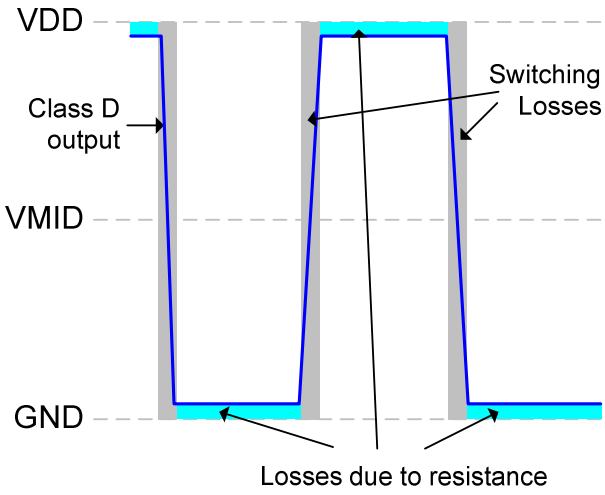


Figure 66 Speaker Connection Losses

The distance between the WM8961 and the speakers should be kept to a minimum to reduce series resistance, and also to reduce EMI. Further reductions in EMI can be achieved by additional passive filtering and/or shielding as shown in Figure 67. When additional passive filtering is used, low ESR components should be chosen to minimize series resistance between the WM8961 and the speaker, maximizing efficiency.

LC passive filtering will usually be effective at reducing EMI at frequencies up to around 30MHz. To reduce emissions at higher frequencies, ferrite beads placed as close to the device as possible will be more effective.

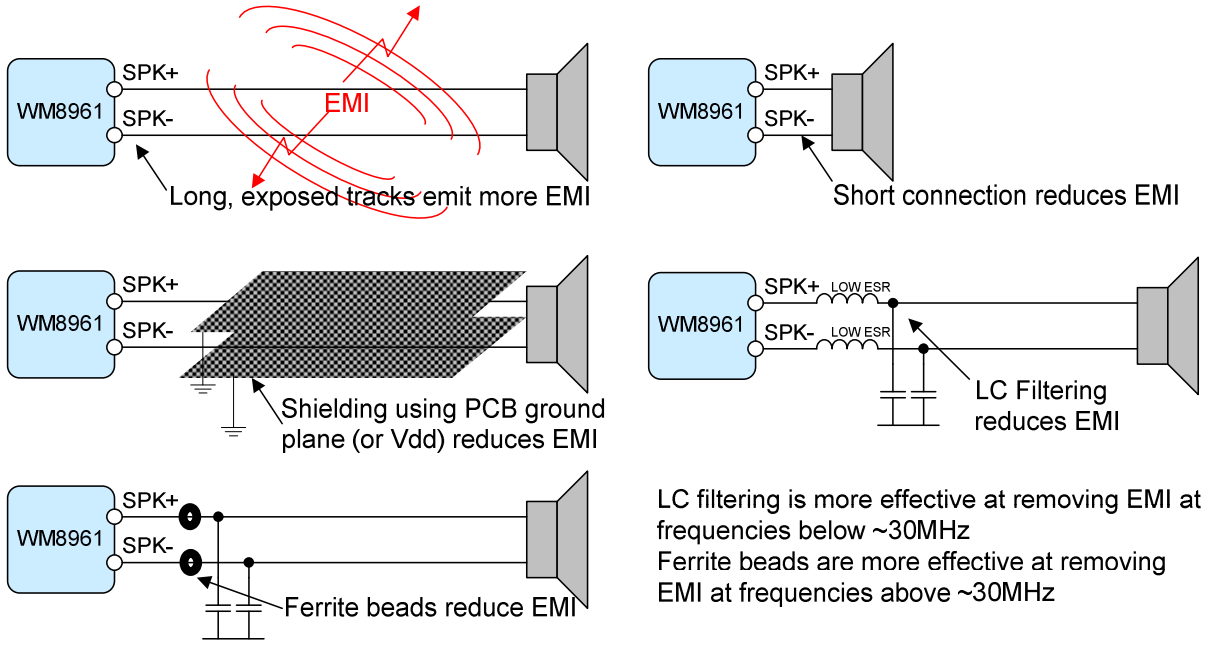


Figure 67 EMI Reduction Techniques

EXAMPLE CONFIGURATIONS

Each of the following example configurations shows a verified register write sequence, which can then be modified to suit the customer requirements.

DAC TO HEADPHONE PLAYBACK

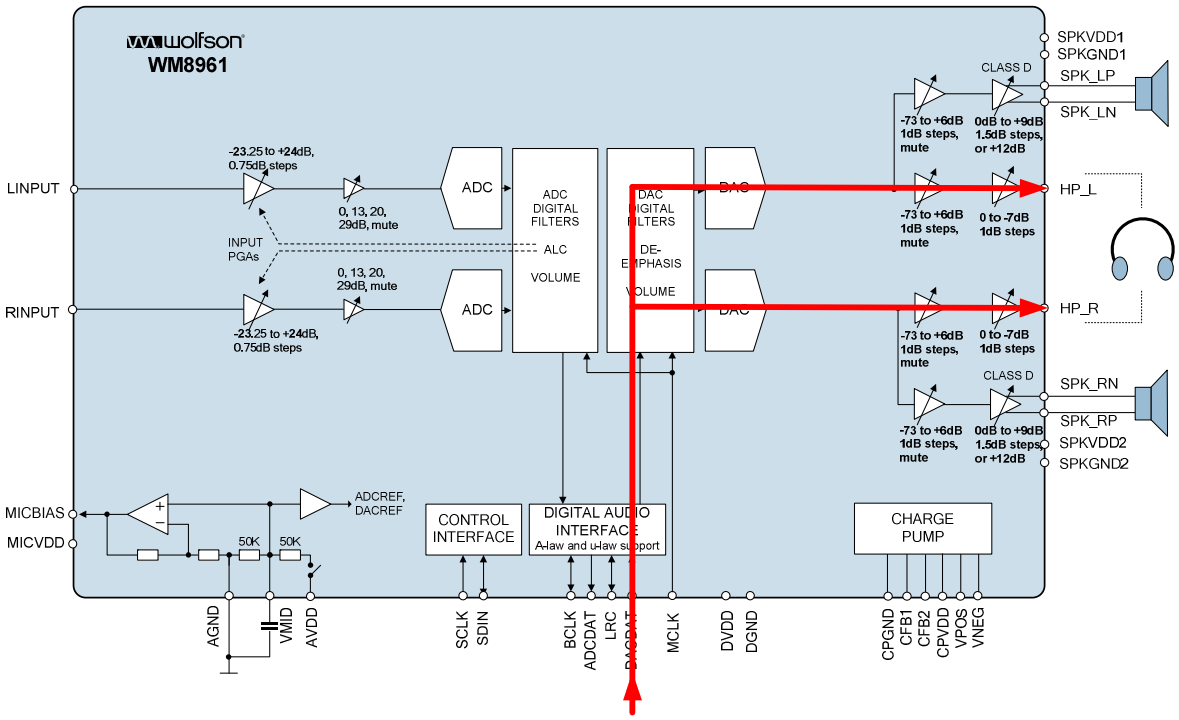


Figure 68 WM8961 Block Diagram for DAC to Headphone Playback

REGISTER	SETTING	COMMENT
0x0F - write	0x0000	Reset device if required
0x0F - read	-	Read Chip ID (=0x1801)
0x08 - write	0x01F4	Enable system clocks
0x52 - write	0x0003	Class W power switching
0x57 - write	0x0020	Enable the write sequencer, DAC to headphone playback with -20dB volume setting
0x5A - write	0x0080	Start the write sequencer to configure pre-programmed enable of the DAC playback (digital input to headphone output) path. Analogue input PGAs still muted.
Allow enough time for the sequencer to finish		
0x5D - read	-	Read status of write sequencer and wait until the WSEQ_BUSY,bit0,=0 which indicates that the DAC playback path has been configured. Then continue.

Table 68 Register Settings for DAC to Headphone playback (-20dB volume setting)

DAC TO SPEAKER AND HEADPHONE PLAYBACK

In order to simplify the configuration of DAC to speaker playback, the headphone output should first be enabled.

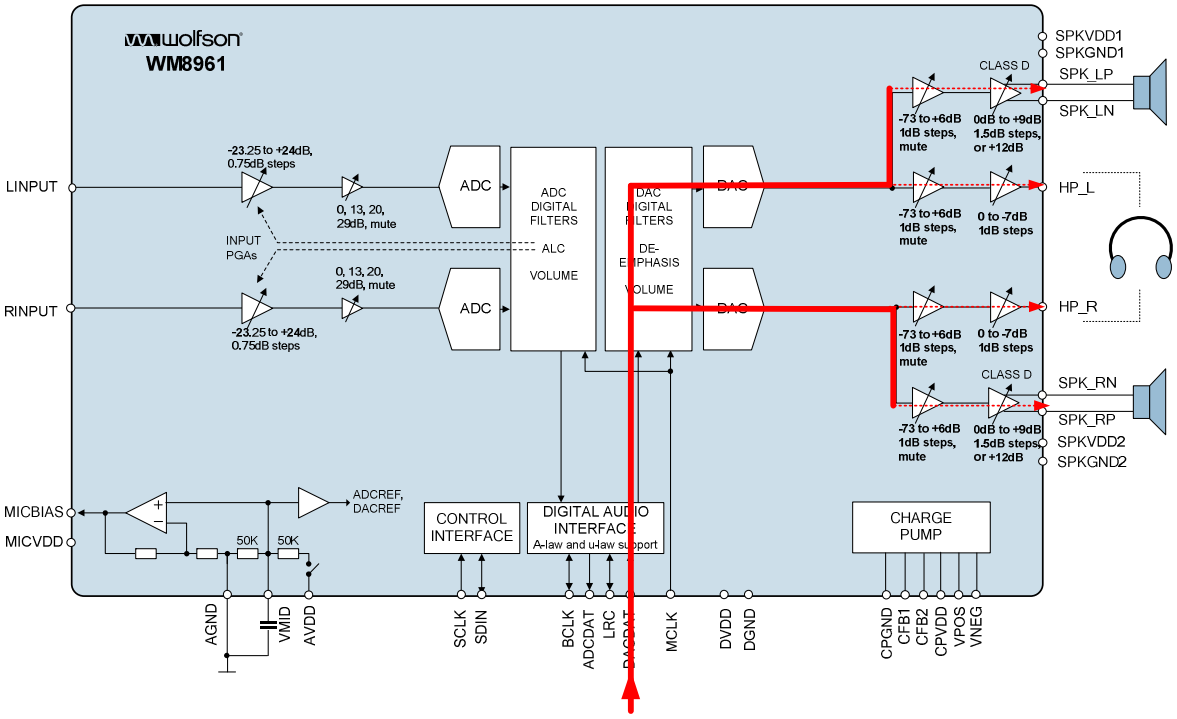


Figure 69 WM8961 Block Diagram for DAC to Speaker and Headphone Playback

REGISTER	SETTING	COMMENT
0x0F - write	0x0000	Reset device if required
0x0F - read	-	Read Chip ID (=0x1801)
0x08 - write	0x01F4	Enable system clocks
0x52 - write	0x0003	Headphone Class W power switching
0x57 - write	0x0020	Enable the write sequencer, DAC to headphone playback with -20dB volume setting.
0x5A - write	0x0080	Start the write sequencer to configure pre-programmed enable of the DAC playback (digital input to headphone output) path. Analogue input PGAs still muted.
Allow enough time for the sequencer to finish		
0x5D - read	-	Read status of write sequencer and wait until the WSEQ_BUSY,bit0,=0 which indicates that the DAC playback path has been configured. Then continue.
0x1A - write	0x01FC	Enable the Speaker PGAs, SPKL_PGA and SPKR_PGA
0x33 - write	0x0001	Program the CLASSD_ACGAIN to x1.5
0x31 - write	0x00C0	Enable the speakers SPKR_ENA and SPKL_ENA
0x28 - write	0x0079	Set the left speaker volume SPKLVOL to 0dB (which defaults to mute), change on zero cross only
0x29 - write	0x0079	Set the right speaker volume SPKRVOL to 0dB (which defaults to mute), change on zero cross only
0x29 - write	0x0179	Update speaker volume SPKVU

Table 69 Register Settings for DAC to Speaker and headphone Outputs

The above configuration enables the speaker and the headphone outputs.

SWITCHING BETWEEN HEADPHONE AND SPEAKERS

With DAC to speaker and headphone playback enabled, switching between headphone and speaker outputs should be done using the PGA and mute bits as shown in Table 70 and Table 71. This achieves best pop-click performance.

To save power, it may also be desirable to apply power management settings in addition to the settings shown, however note that disabled PGAs leave a resistive path hence do not achieve the published mute attenuation specifications.

0x02 - write	0x012F	Headphone L mute
0x03 - write	0x012F	Headphone R mute
0x28 - write	0x0079	Set the left speaker volume SPKRVOL to 0dB
0x29 - write	0x0179	Set the right speaker volume to 0dB and update speaker volume SPKVU

Table 70 Switching from Headphone playback to Speaker Playback

REGISTER	SETTING	COMMENT
0x02 - write	0x0065	Set the left headphone volume to -20dB
0x03 - write	0x0165	Set the right headphone volume to -20dB and update headphone volume OUT1VU
0x28 - write	0x002F	Speaker L mute
0x29 - write	0x012F	Speaker R mute

Table 71 Switching from Speaker Playback to Headphone playback (-20dB volume setting)

LRINPUT TO ADC RECORD

In order to simplify the configuration of LRINPUT to ADC recording, the headphone output should first be enabled

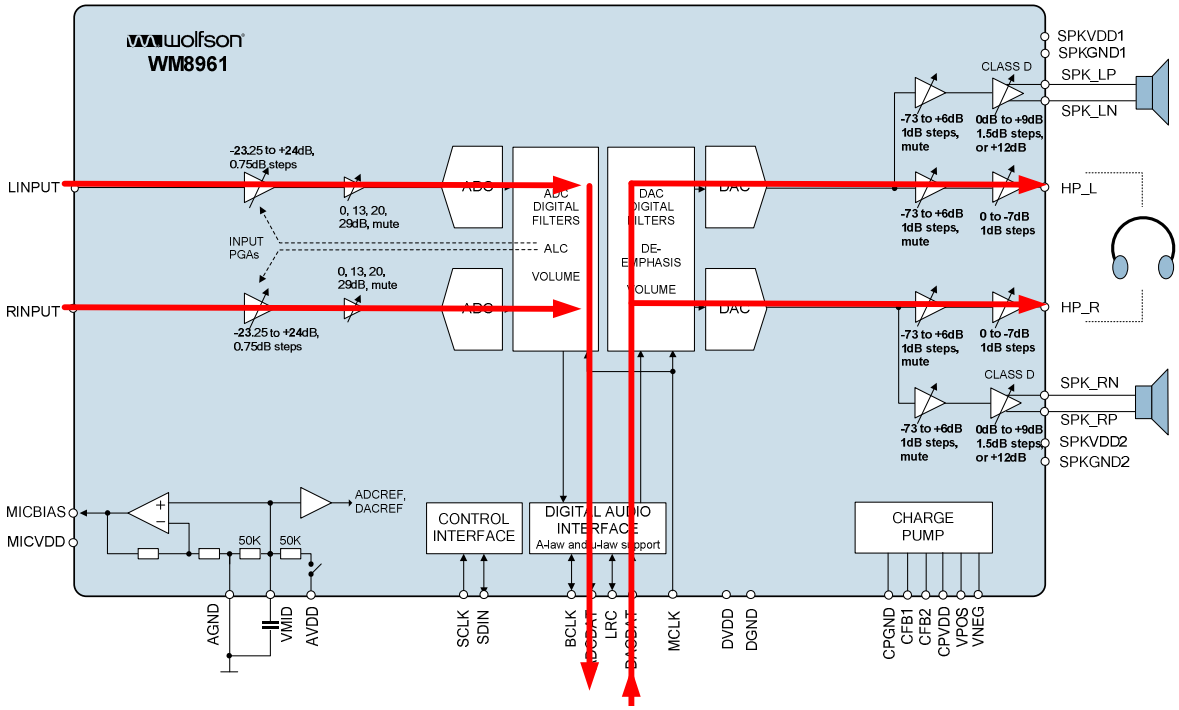


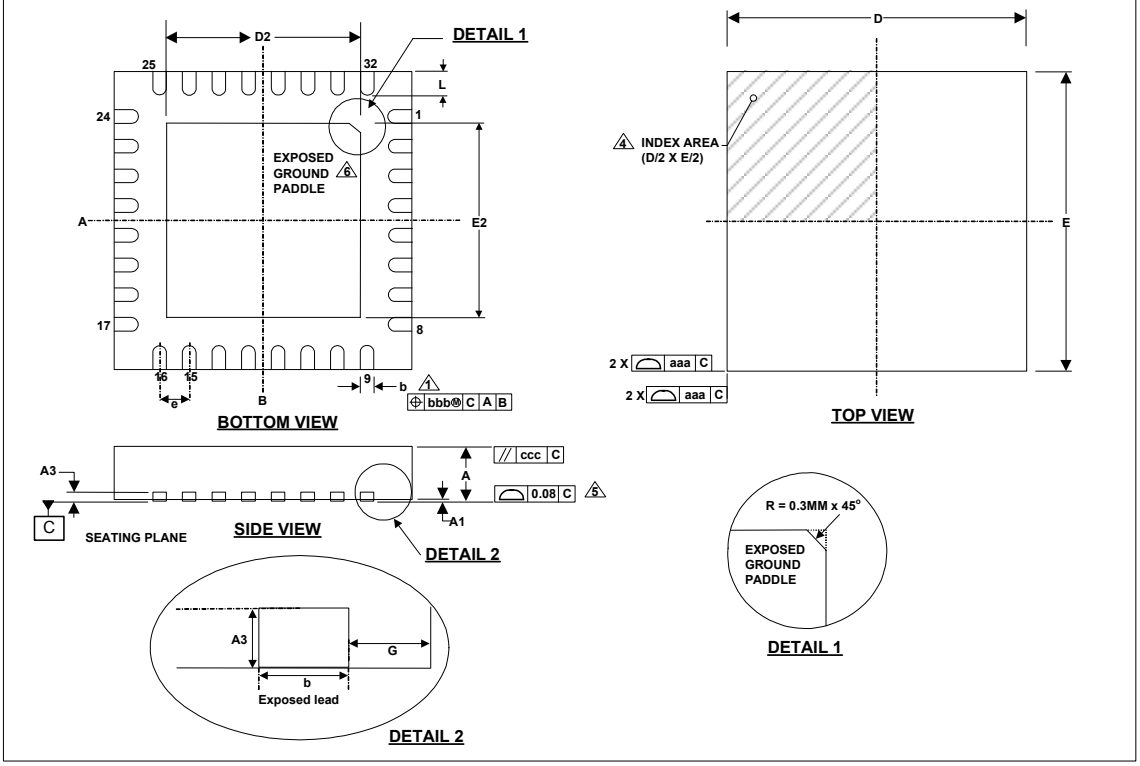
Figure 70 WM8961 Block Diagram for LRINPUT to ADC Record

REGISTER	SETTING	COMMENT
0x0F - write	0x0000	Reset device if required
0x0F - read	-	Read Chip ID (=0x1801)
0x08 - write	0x01F4	Enable system clocks
0x57 - write	0x0020	Enable the write sequencer.
0x5A - write	0x0080	Start the write sequencer to configure pre-programmed enable of the DAC playback (digital input to headphone output) path. Analogue input PGAs still muted.
Allow enough time for the sequencer to finish		
0x5D - read	-	Read status of write sequencer and wait until the WSEQ_BUSY,bit0,=0 which indicates that the DAC playback path has been configured. Then continue.
0x5A - write	0x0092	Start the write sequencer to configure pre-programmed enable of the ADC record (line input to digital output) path
Allow enough time for the sequencer to finish		
0x5D - read	-	Read status of write sequencer and wait until the WSEQ_BUSY,bit0,=0. Then continue.
0x00 - write	0x011F	Unmute left analogue input, leave input PGA volume gain at default 0dB
0x01 - write	0x011F	Unmute right analogue input, leave input PGA volume gain at default 0dB

Table 72 Register Settings for LRINPUT to ADC Record

PACKAGE DIMENSIONS

FL: 32 PIN QFN PLASTIC PACKAGE 5 x 5 x 0.9 mm BODY, 0.50 mm LEAD PITCH **DM044.B**



Symbols		Dimensions (mm)		
	MIN	NOM	MAX	NOTE
A	0.80	0.85	0.90	
A1	0	0.02	0.05	
A3		0.203 REF		
b	0.20	0.25	0.30	1
D		5.00 BSC		
D2	3.05	3.10	3.15	2
E		5.00 BSC		
E2	3.05	3.10	3.15	2
e		0.50 BSC		
G		0.625		
L	0.35	0.40	0.45	
Tolerances of Form and Position				
aaa	0.15			
bbb	0.10			
ccc	0.10			
REF:	JEDEC, MO-220, VARIATION VHHD-5.			

NOTES:
1. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 mm AND 0.30 mm FROM TERMINAL TIP.
2. FALLS WITHIN JEDEC, MO-220, VARIATION VHHD-5.
3. ALL DIMENSIONS ARE IN MILLIMETRES.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-002.
5. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
6. REFER TO APPLICATION NOTE WAN_0118 FOR FURTHER INFORMATION REGARDING PCB FOOTPRINTS AND QFN PACKAGE SOLDERING.
7. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.

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- Подбор аналогов;
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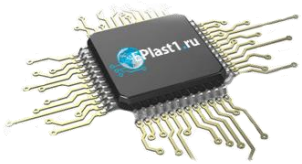

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