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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

September 2015

FAN4800AU / FAN4800CU
PFC/ PWM Controller Combination

Features

- Pin-to-Pin Compatible with ML4800, FAN4800, CM6800, and CM6800A
- PWM Configurable for Current-Mode or Feed-Forward Voltage-Mode Operation
- Internally Synchronized Leading-Edge PFC and Trailing-Edge PWM in One IC
- Low Operating Current
- Innovative Switching-Charge Multiplier Divider
- Average-Current-Mode for Input-Current Shaping
- PFC Over-Voltage and Under-Voltage Protections
- PFC Feedback Open-Loop Protection
- Cycle-by-Cycle Current Limiting for PFC/PWM
- Power-on Sequence Control and Soft-Start
- Line Sagging Protection
- $f_{RTCT}=4 \bullet f_{PFC}=4 \bullet f_{PWM}$ for FAN4800AU
- $f_{RTCT}=4 \bullet f_{PFC}=2 \bullet f_{PWM}$ for FAN4800CU

Applications

- Desktop PC Power Supply
- Internet Server Power Supply
- LCD TV/ Monitor Power Supply
- UPS
- Battery Charger
- DC Motor Power Supply
- Monitor Power Supply
- Telecom System Power Supply
- Distributed Power

Related Resources

- *AN-8027 — FAN480X PFC+PWM Combination Controller Application*

Description

The highly integrated FAN4800AU/CU parts are specially designed for power supplies that consist of boost PFC and PWM. They require very few external components to achieve versatile protections and compensation. They are available in 16-pin DIP and SOP packages.

The PWM can be used in current or Voltage Mode. In Voltage Mode, feed-forward from the PFC output bus can reduce secondary output ripple.

To evaluate FAN4800AU/CU for replacing existing FAN4800A/C, FAN4800AS/CS, old version FAN4800 and ML4800 boards, six things must be completed before the fine-tuning procedure:

1. Change R_{AC} resistor from the old value to a higher resistor value: 6 MΩ to 8 MΩ.
2. Change RT/CT pin from the existing values to R_T=6.8 kΩ and C_T=1000 pF to have f_{PFC}=64 kHz and f_{PWM}=64 kHz.
3. The VRMS pin needs to be 1.224 V at V_{IN}=85 V_{AC} for universal input application with line input from 85 V_{AC} to 270 V_{AC}.
4. Change ISENSE pin filter from the exiting values to R_{Filter}=51 Ω and C_{Filter}=0.01 µF for higher bandwidth.
5. At full load, the average V_{VEA} must be ~4.5 V and ripple on V_{VEA} needs to be less than 400 mV.
6. For the SS pin, the soft-start current has been reduced to half the FAN4800 capacitor.

There are two differences from FAN4800AS/CS to FAN4800AU/CU:

- Add Line Sagging Protection
- Fix Inductance Current Instability during AC Cycle Drop Test

Ordering Information

Part Number	Operating Temperature Range	PFC:PWM Frequency Ratio	Package	Packing Method
FAN4800AUN	-40°C to +105°C	1:1	16-Pin Dual Inline Package (DIP)	Tube
FAN4800CUN		1:2		
FAN4800AUM		1:1	16-Pin Small Outline Package (SOP)	Tape & Reel
FAN4800CUM		1:2		

Block Diagram

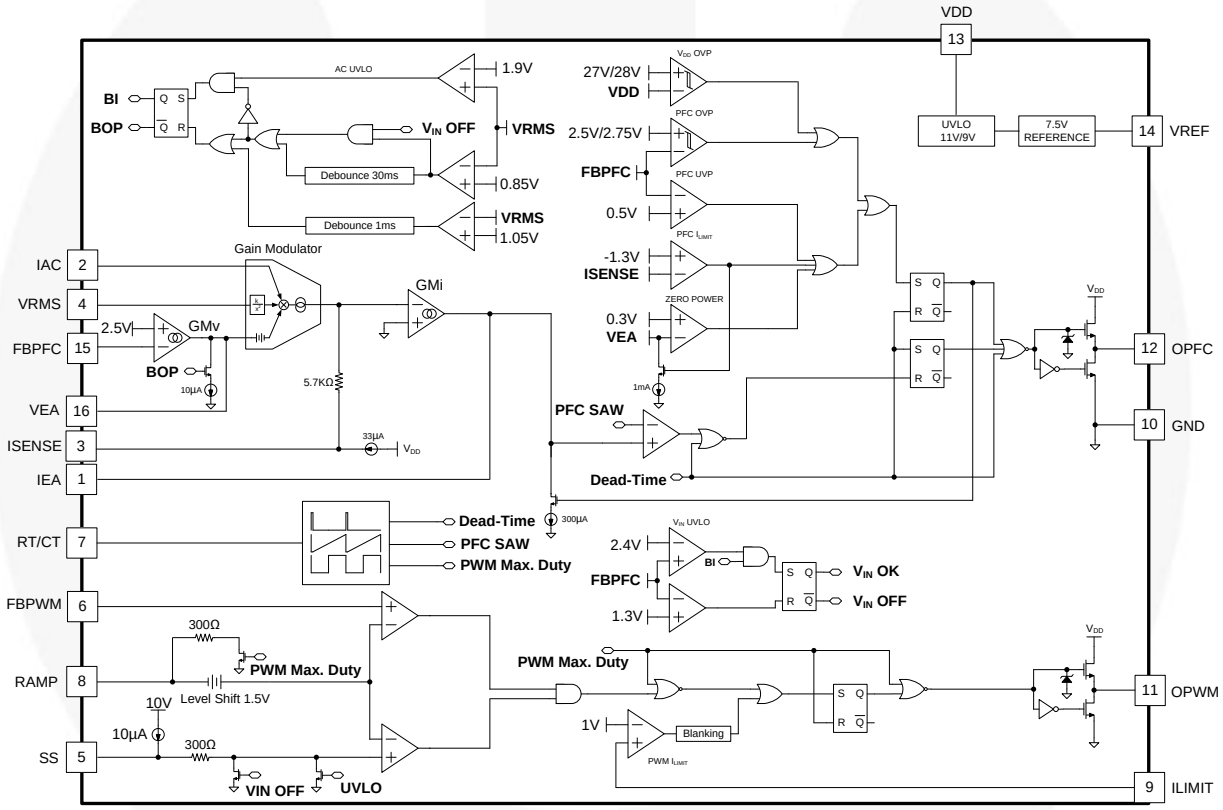


Figure 1. Function Block Diagram

Application Diagrams

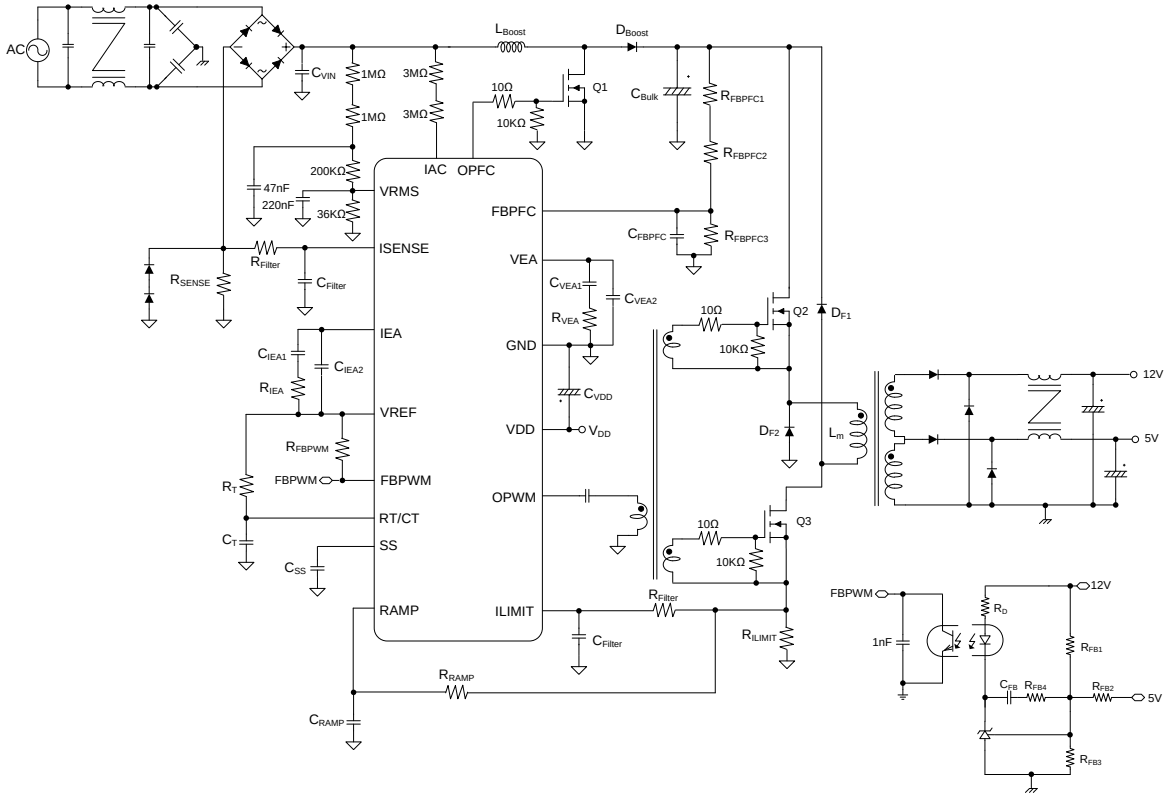


Figure 2. Current Mode

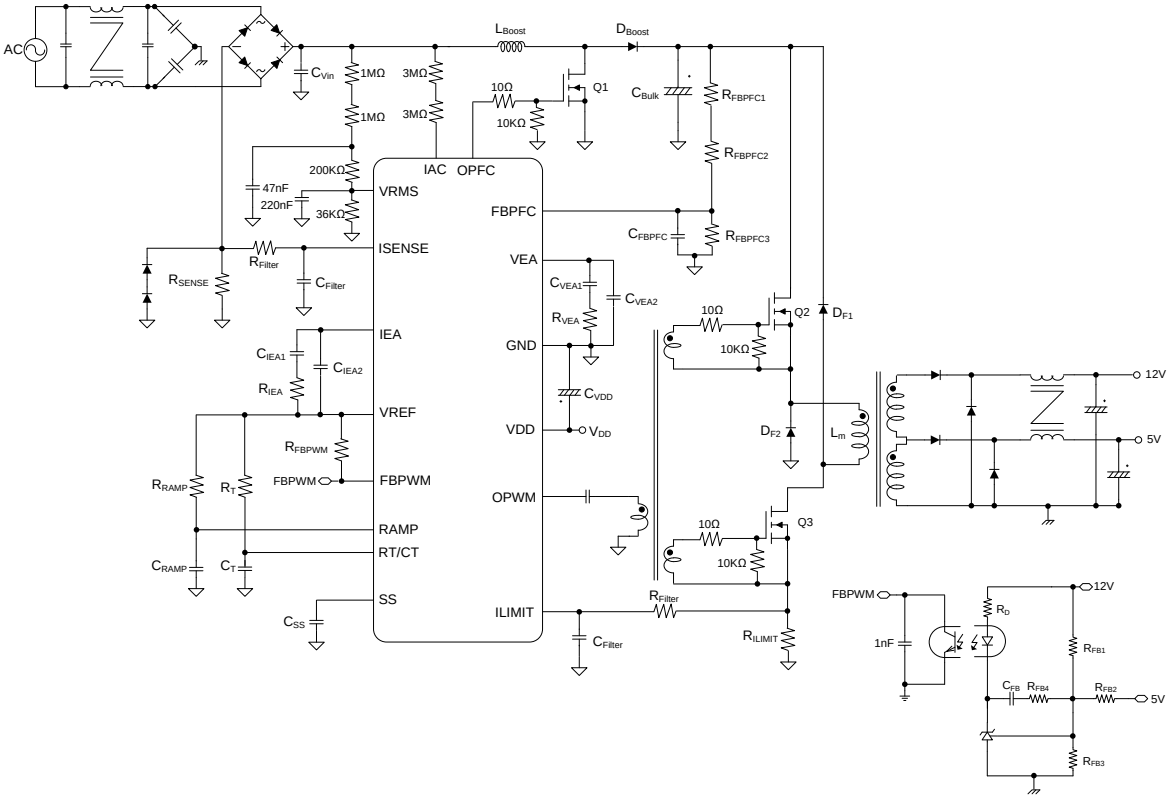
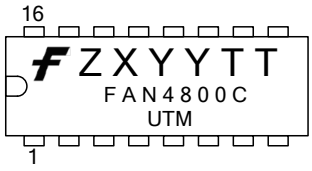
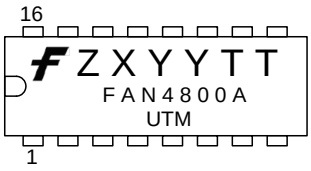


Figure 3. Voltage Mode

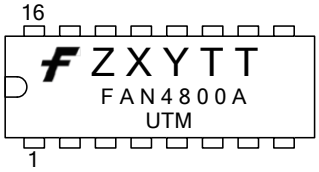
Marking Information

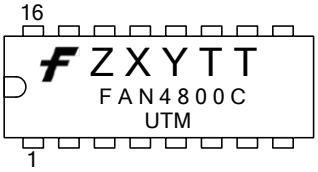




F – Fairchild Logo
Z – Plant Code
X – 1-Digit Year Code
YY – 2-Digit Week Code
TT – 2-Digit Die-Run Code
T – Package Type (N:DIP)
M – Manufacture Flow Code

Figure 4. DIP Top Mark





F – Fairchild Logo
Z – Plant Code
X – 1-Digit Year Code
Y – 1-Digit Week Code
TT – 2-Digit Die-Run Code
T – Package Type (M:SOP)
M – Manufacture Flow Code

Figure 5. SOP Top Mark

Pin Configuration

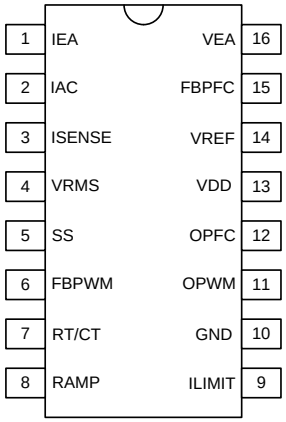


Figure 6. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	IEA	**Output of PFC Current Amplifier**. The signal from this pin is compared with an internal sawtooth to determine the pulse width for the PFC gate drive.
2	IAC	**Input AC Current**. For normal operation, this input provides a current reference for the multiplier. The suggested maximum I_{AC} is 65 µA.
3	ISENSE	**PFC Current Sense**. The inverting input of the PFC current amplifier and the output of multiplier and PFC I_{LIMIT} comparator.
4	VRMS	**Line-Voltage Detection**. The pin is used for the PFC multiplier.
5	SS	**PWM Soft-Start**. During startup, the SS pin charges an external capacitor with a 10 µA constant current source. The voltage on FBPWM is clamped by SS during startup. If a protection condition occurs and/or PWM is disabled, the SS pin is quickly discharged.
6	FBPWM	**PWM Feedback Input**. The control input for voltage-loop feedback of PWM stage.
7	RT/CT	**Oscillator RC Timing Connection**. Oscillator timing node; timing set by R_T and C_T.
8	RAMP	**PWM RAMP Input**. In Current Mode, this pin functions as the current-sense input. In Voltage Mode, it is the feed-forward sense input from PFC output 380 V (feed-forward ramp).
9	ILIMIT	**Peak Current Limit Setting for PWM**. The peak current limit setting for PWM.
10	GND	**Ground**
11	OPWM	**PWM Gate Drive**. The totem-pole output drive for the PWM MOSFET. This pin is internally clamped under 19 V to protect the MOSFET.
12	OPFC	**PFC Gate Drive**. The totem-pole output drive for PFC MOSFET. This pin is internally clamped under 15 V to protect the MOSFET.
13	VDD	**Supply**. The power supply pin. The threshold voltages for startup and turn-off are 11 V and 9.3 V, respectively. The operating current is lower than 10 mA.
14	VREF	**Reference Voltage**. Buffered output for the internal 7.5 V reference.
15	FBPFC	**Voltage Feedback Input for PFC**. The feedback input for PFC voltage loop. The inverting input of PFC error amplifier. This pin is connected to the PFC output through a divider network.
16	VEA	**Output of PFC Voltage Amplifier**. The error amplifier output for PFC voltage feedback loop. A compensation network is connected between this pin and ground.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{DD}	DC Supply Voltage			30	V
V_H	Voltage on SS, FBPWM, RAMP, VREF Pins		-0.3	30.0	V
$V_{PFC-OUT}$	Voltage on OPFC Pin			V_{DD} +0.3V	V
$V_{PWM-OUT}$	Voltage on OPWM Pin			V_{DD} +0.3V	V
V_L	Voltage on IAC, VRMS, RT/CT, ILIMIT, FBPFC, VEA Pins		-0.3	7.0	V
V_{IEA}	Voltage on IEA Pin		0	V_{VREF}+0.3	V
V_N	Voltage on ISENSE Pin		-5.0	0.7	V
I_{AC}	Input AC Current			1	mA
I_{REF}	VREF Output Current			5	mA
$I_{PFC-OUT}$	Peak PFC OUT Current, Source or Sink			0.5	A
$I_{PWM-OUT}$	Peak PWM OUT Current, Source or Sink			0.5	A
P_D	Power Dissipation T_A < 50°C			800	mW
Θ_{JA}	Thermal Resistance (Junction to Air)	DIP		80.80	°C/W
		SOP		104.10	
Θ_{JC}	Thermal Resistance (Junction to Case)	DIP		35.38	°C/W
		SOP		40.41	
T_J	Operating Junction Temperature		-40	+125	°C
T_{STG}	Storage Temperature Range		-55	+150	°C
T_L	Lead Temperature(Soldering)			+260	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114		6.0	kV
		Charged Device Model, JESD22-C101		2.0	

Notes:
1. All voltage values, except differential voltage, are given with respect to GND pin.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
T_A	Operating Ambient Temperature	-40	+105	°C

Electrical Characteristics

Unless otherwise noted, V_{DD}=15 V, T_A= 25°C, T_A=T_J, R_T=6.8 kΩ, and C_T=1000 pF.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD} Section						
I_{DD-ST}	Startup Current	V_{DD}=V_{TH-ON}-0.1V, OPFC OPWM Open		30	80	µA
I_{DD-OP}	Operating Current	V_{DD}=13 V, OPFC OPWM Open	2.0	2.6	5.0	mA
V_{TH-ON}	Turn-on Threshold Voltage		10	11	12	V
△V_{TH}	Hysteresis		1.3		1.9	V
V_{DD-OVP}	V_{DD} OVP		27	28	29	V
△V_{DD-OVP}	V_{DD} OVP Hysteresis			1		V
Oscillator						
$f_{OSC-RT/CT}$	RT/CT Frequency	R_T=6.8 kΩ, C_T=1000 pF	240	256	268	kHz
f_{OSC}	PFC & PWM Frequency		60	64	67	kHz
	FAN4800CU PWM Frequency		120	128	134	
f_{DV}	Voltage Stability(3)	11 V ≦ V_{DD} ≦ 22 V			2	%
f_{DT}	Temperature Stability(3)	-40°C ~ +105°C			2	%
f_{TV}	Total Variation (PFC & PWM)(3)	Line, Temperature	58		70	kHz
f_{RV}	Ramp Voltage	Valley to Peak		2.8		V
$I_{OSC-DIS}$	Discharge Current	V_{RAMP}=0 V, $V_{RT/CT}$=2.5 V	6.5		15.0	mA
f_{RANGE}	Frequency Range		50		75	kHz
$t_{PFC-DEAD}$	PFC Dead Time	R_T=6.8 kΩ, C_T=1000 pF	400	600	800	ns
V_{VREF}						
V_{VREF}	Reference Voltage	I_{VREF}=0 mA, C_{VREF}=0.1 µF	7.4	7.5	7.6	V
△V_{VREF1}	Load Regulation of Reference Voltage	C_{VREF}=0.1 µF, I_{VREF}=0 mA to 3.5 mA V_{DD}=14 V, Rise/Fall Time > 20 µs		30	50	mV
△V_{VREF2}	Line Regulation of Reference Voltage	C_{VREF}=0.1 µF, V_{DD}=11V to 22 V			25	mV
△$V_{VREF-DT}$	Temperature Stability(3)	-40°C ~ +105°C		0.4	0.5	%
△$V_{VREF-TV}$	Total Variation(3)	Line, Load, Temperature	7.35		7.65	V
△$V_{VREF-LS}$	Long-Term Stability(3)	T_J=125°C, 0 ~ 1000 Hours	5		25	mV
$I_{VREF-MAX}$.	Maximum Current	V_{VREF} > 7.35 V	5			mA
PFC OVP Comparator						
$V_{PFC-OVP}$	Over-Voltage Protection		2.70	2.75	2.80	V
△$V_{PFC-OVP}$	PFC OVP Hysteresis		200	250	300	mV
Low-Power Detect Comparator						
V_{VEAOFF}	VEA Voltage OFF OPFC		0.2	0.3	0.4	V
V_{IN} OK Comparator						
$V_{RD-FBPFC}$	Voltage Level on FBPFC to Enable OPWM During Startup		2.3	2.4	2.5	V
△$V_{RD-FBPFC}$	Hysteresis		1.0	1.1	1.2	V

Continued on the following page…

Electrical Characteristics (Continued)

Unless otherwise noted, V_{DD}=15 V, T_A= 25°C, T_A=T_J, R_T=6.8 kΩ, and C_T=1000 pF.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Voltage Error Amplifier						
V_{REF}	Reference Voltage		2.45	2.50	2.55	V
A_V	Open-Loop Gain(3)		35	42		dB
Gm_v	Transconductance	V_{NONINV}=V_{INV}, V_{VEA}=3.75 V	50	70	90	µmho
$I_{FBPFC-L}$	Maximum Source Current	V_{FBPFC}=2 V, V_{VEA}=1.5 V	40	50		µA
$I_{FBPFC-H}$	Maximum Sink Current	V_{FBPFC}=3 V, V_{VEA}=6 V		-50	-40	µA
I_{BS}	Input Bias Current		-1		1	µA
V_{VEA-H}	Output High Voltage on V_{VEA}		5.8	6.0		V
V_{VEA-L}	Output Low Voltage on V_{VEA}			0.1	0.4	V
Current Error Amplifier						
Gm_I	Transconductance	V_{NONINV}=V_{INV}, V_{IEA}=3.75 V	70	88	105	µmho
V_{OFFSET}	Input Offset Voltage	V_{VEA}=0 V, IAC Open	-10		10	mV
V_{IEA-H}	Output High Voltage		6.8	7.4	7.8	V
V_{IEA-L}	Output Low Voltage			0.1	0.4	V
I_L	Source Current	V_{ISENSE}= -0.6 V, V_{IEA}=1.5 V	35	50		µA
I_H	Sink Current	V_{ISENSE}= +0.6 V, V_{IEA}=4.0 V		-50	-35	µA
A_I	Open-Loop Gain(3)		40	50		dB
TriFault Detect™						
$t_{FBPFC-OPEN}$	Time to FBPFC Open	V_{FBPFC}=$V_{PFC-UVP}$ to FBPFC OPEN, 470 pF from FBPFC to GND		2	4	ms
$V_{PFC-UVP}$	PFC Feedback Under-Voltage Protection		0.4	0.5	0.6	V
Gain Modulator						
I_{AC}	Input for AC Current(3)	Multiplier Linear Range	0		65	µA
GAIN	Gain Modulator(4)	I_{AC}=17.67 µA, V_{RMS}=1.080 V V_{FBPFC}=2.25 V		7.94		
		I_{AC}=20 µA, V_{RMS}=1.224 V V_{FBPFC}=2.25 V		7.02		
		I_{AC}=25.69 µA, V_{RMS}=1.585 V V_{FBPFC}=2.25 V		4.18		
		I_{AC}=51.62 µA, V_{RMS}=3.169 V V_{FBPFC}=2.25 V		1.05		
		I_{AC}=62.23 µA, V_{RMS}=3.803 V V_{FBPFC}=2.25 V		0.73		
BW	Bandwidth(3)	I_{AC}=40 µA			2	kHz
V_O(gm)	Output Voltage=5.7 kΩ × (I_{SENSE}-I_{OFFSET})	I_{AC}=50 µA, V_{RMS}=1.224 V V_{FBPFC}=2.25 V	0.76	0.80	0.84	V
PFC I_{LIMIT} Comparator						
$V_{PFC-ILIMIT}$	Peak Current Limit Threshold Voltage, Cycle-by-Cycle Limit		-1.2	-1.3	-1.4	V
$\triangle V_{PK}$	PFC I_{LIMIT}-Gain Modulator Output	I_{AC}=17.67 µA, V_{RMS}=1.08 V V_{FBPFC}=2.25 V	400			mV

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Electrical Characteristics (Continued)

Unless otherwise noted, V_{DD}=15 V, T_A= 25°C, T_A=T_J, R_T=6.8 kΩ, and C_T=1000 pF.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
PFC Output Driver						
$V_{GATE-CLAMP}$	Gate Output Clamping Voltage	V_{DD}=22 V	13	15	17	V
V_{GATE-L}	Gate Low Voltage	V_{DD}=15 V, I_O=100 mA			1.5	V
V_{GATE-H}	Gate High Voltage	V_{DD}=13 V, I_O=100 mA	8			V
t_R	Gate Rising Time	V_{DD}=15 V, C_L=4.7 nF, O/P= 2 V to 9 V	40	70	120	ns
t_F	Gate Falling Time	V_{DD}=15 V, C_L=4.7 nF, O/P=9 V to 2 V	40	60	110	ns
$D_{PFC-MAX}$	Maximum Duty Cycle	V_{IEA}<1.2 V	94	97		%
$D_{PFC-MIN}$	Minimum Duty Cycle	V_{IEA}>4.5 V			0	%
PWM I_{LIMIT} Comparator						
$V_{PWM-ILIMIT}$	Threshold Voltage		0.95	1.00	1.05	V
t_{PD}	Propagation Delay to Output			250		ns
$t_{PWM-BNK}$	Leading-Edge Blanking Time		170	250	350	ns
PWM Output Driver						
$V_{GATE-CLAMP}$	Gate Output Clamping Voltage	V_{DD}=22 V	18	19	20	V
V_{GATE-L}	Gate Low Voltage	V_{DD}=15 V, I_O=100 mA			1.5	V
V_{GATE-H}	Gate High Voltage	V_{DD}=13 V, I_O=100 mA	8			V
t_R	Gate Rising Time	V_{DD}=15 V, C_L=4.7 nF, O/P=2 V to 9 V	30	60	120	ns
t_F	Gate Falling Time	V_{DD}=15 V, C_L=4.7 nF, O/P=9 V to 2 V	30	50	110	ns
$D_{PWM-MAX}$	Maximum Duty Cycle		49.0	49.5	50.0	%
V_{PWM-LS}	PWM Comparator Level Shift		1.3	1.5	1.8	V
Soft-Start						
V_{SS-MAX}	Maximum Voltage	V_{DD}=15 V	9.5	10.0	10.5	V
I_{SS}	Soft-Start Current			10		µA
Brownout						
$V_{RMS-UVL}$	VRMS Threshold LOW		1.00	1.05	1.10	V
$V_{RMS-UVH}$	VRMS Threshold HIGH		1.85	1.90	1.95	V
$\triangle V_{RMS-UVP}$	Hysteresis		750	850	950	mV
t_{UVP}	Under- Voltage Protection Delay		750	1000	1250	ms
Sagging Protection						
$V_{RMS-SAG}$	VRMS Threshold SAG LOW		0.80	0.85	0.90	V
t_{SAG}	SAG Protection Delay		28	33	38	ms

Notes:

3. This parameter, although guaranteed by design, is not 100% production tested.
4. This gain is the maximum gain of modulation with a given V_{RMS} voltage when V_{VEA} is saturated to HIGH.

Typical Characteristics

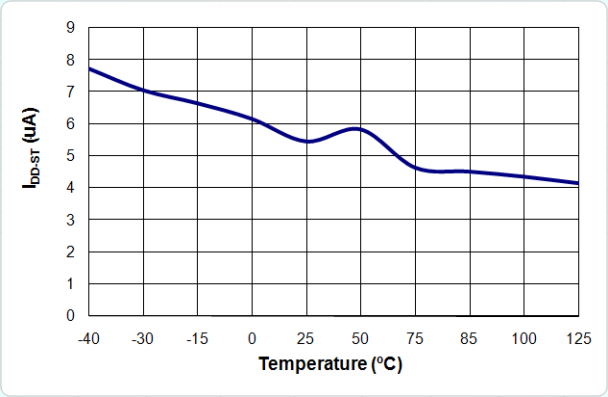


Figure 7. I_{DD-ST} vs. Temperature

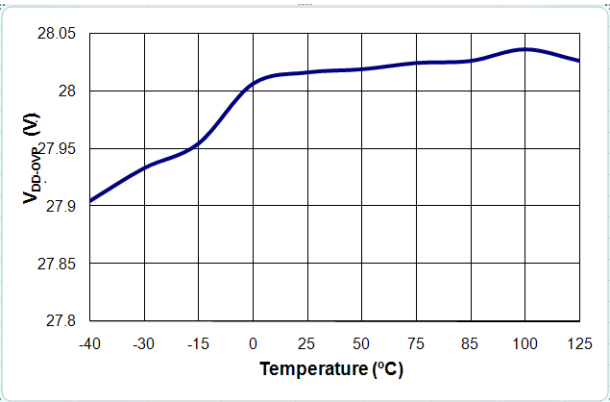


Figure 8. V_{DD-OVP} vs. Temperature

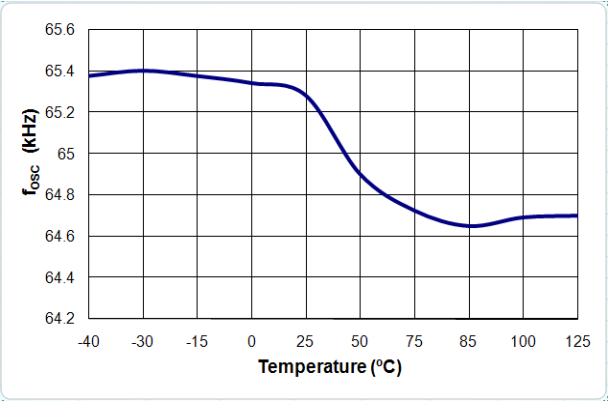


Figure 9. f_{OSC} vs. Temperature

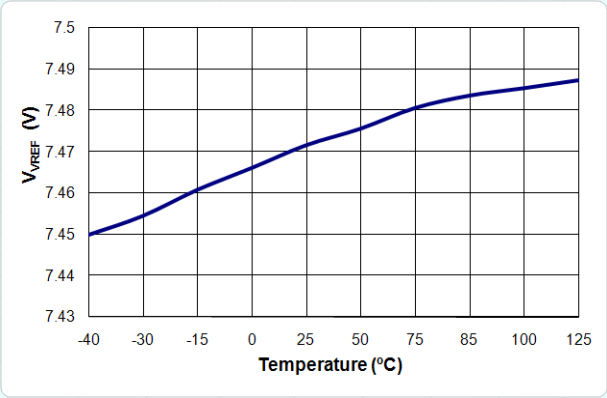


Figure 10. V_{VREF} vs. Temperature

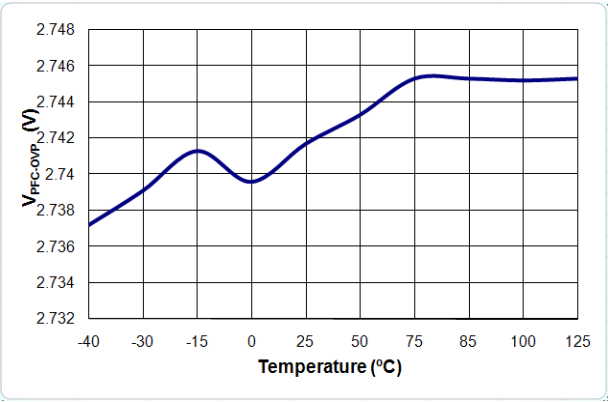


Figure 11. $V_{PFC-OVP}$ vs. Temperature

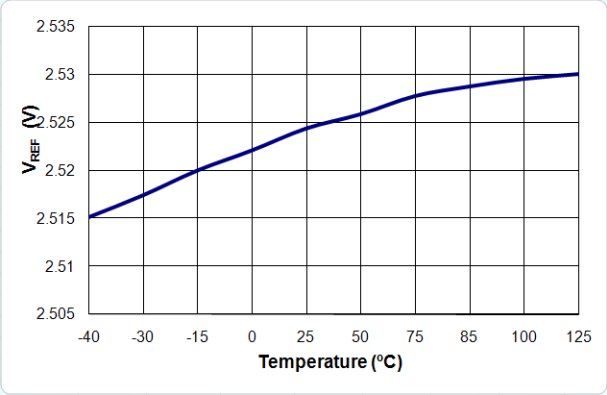


Figure 12. V_{REF} vs. Temperature

Typical Characteristics

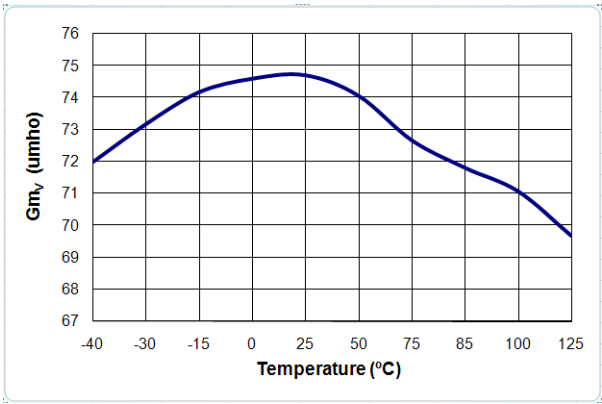


Figure 13. Gm_V vs. Temperature

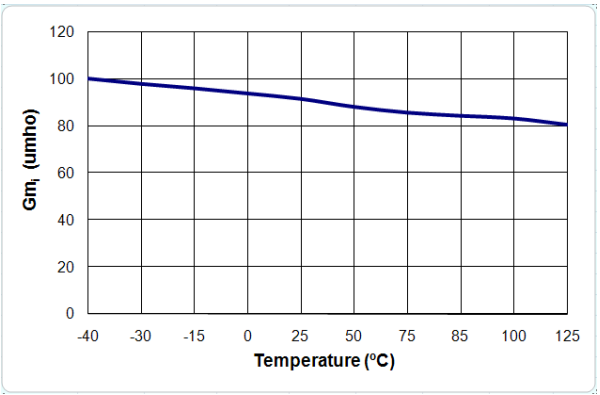


Figure 14. Gm_I vs. Temperature

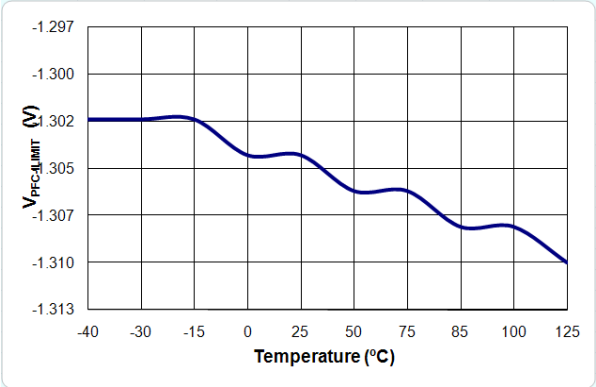


Figure 15. $V_{PFC-ILIMIT}$ vs. Temperature

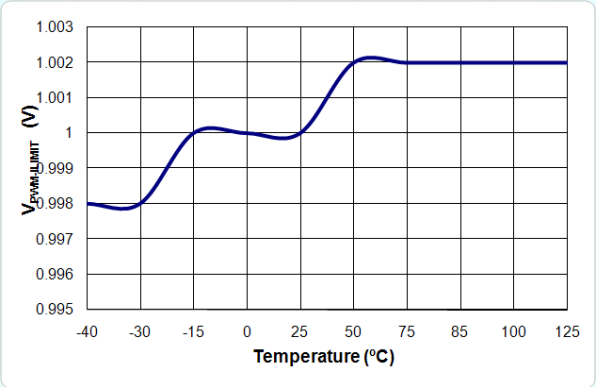


Figure 16. $V_{PWM-ILIMIT}$ vs. Temperature

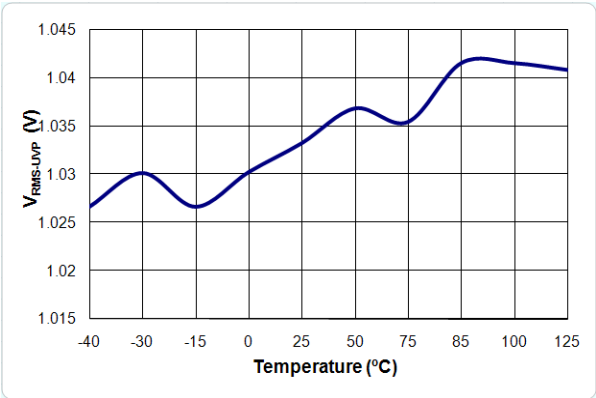


Figure 17. $V_{RMS-UVP}$ vs. Temperature

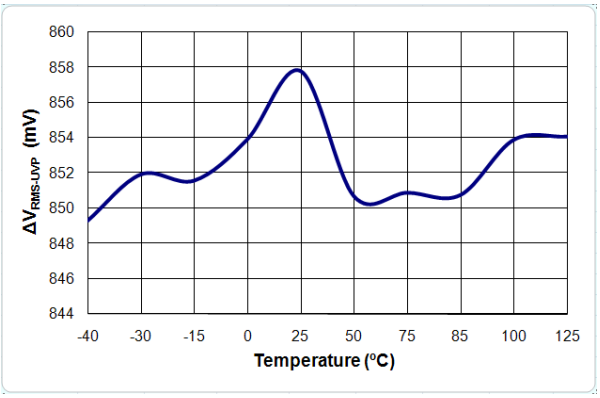


Figure 18. $\Delta V_{RMS-UVP}$ vs. Temperature

Typical Characteristics

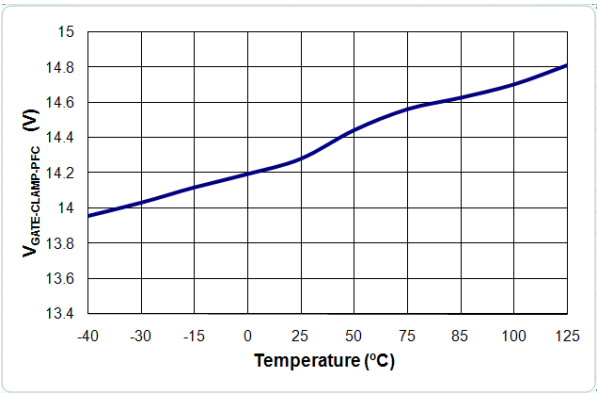


Figure 19. $V_{GATE-CLAMP-PFC}$ vs. Temperature

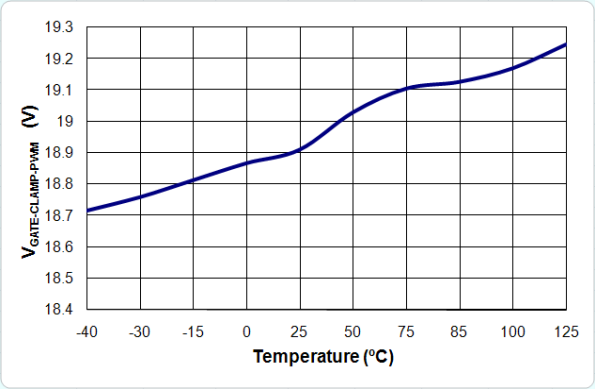


Figure 20. $V_{GATE-CLAMP-PWM}$ vs. Temperature

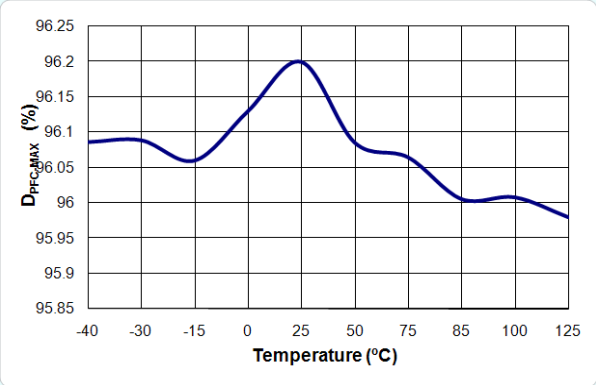


Figure 21. $D_{PFC-MAX}$ vs. Temperature

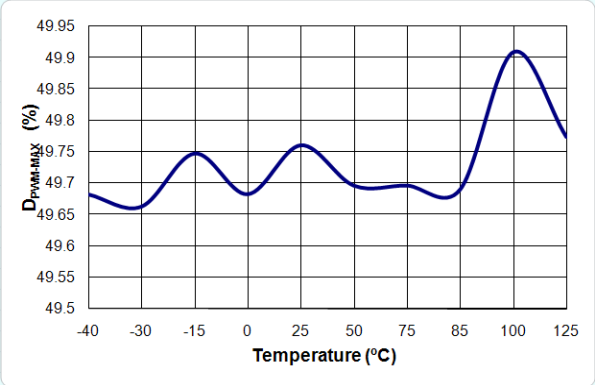


Figure 22. $D_{PWM-MAX}$ vs. Temperature

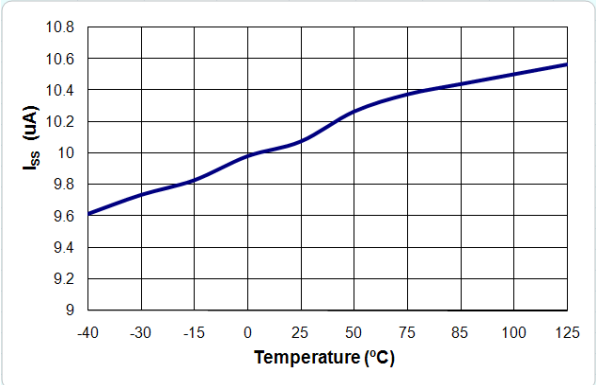


Figure 23. I_{SS} vs. Temperature

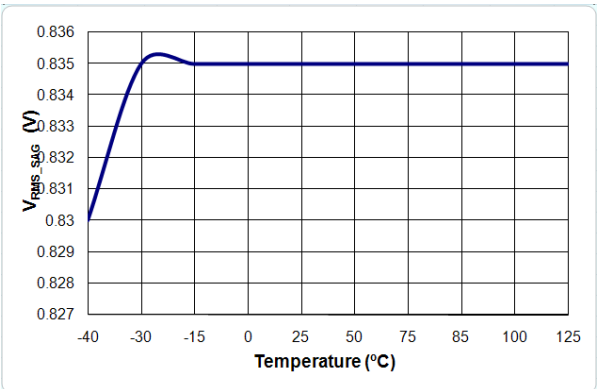


Figure 24. $V_{RMS-SAG}$ vs. Temperature

Functional Description

Oscillator

The internal oscillator frequency is determined by the timing resistor and capacitor on the RT/CT pins as shown in Figure 25. The frequency of the internal oscillator is given:

$$f_{OSC} = \frac{1}{0.56 \cdot R_T \cdot C_T + 360 C_T} \quad (1)$$

Because the PWM stage generally uses a forward converter, it is necessary to limit the maximum duty cycle at 50%. To have a small tolerance of the maximum duty cycle, a frequency divider with toggle flip-flops is used, as illustrated in Figure 25. The operation frequency of PFC and PWM stage is 1/4 of oscillator frequency. (For FAN4800CU, the operation frequencies for PFC and PWM stages are 1/4 and 1/2 of oscillator frequency, respectively).

The dead time for the PFC gate drive signal is determined by:

$$t_{DEAD} = 360 C_T \quad (2)$$

The dead time should be smaller than 2% of the switching period to minimize line current distortion around the line zero crossing.

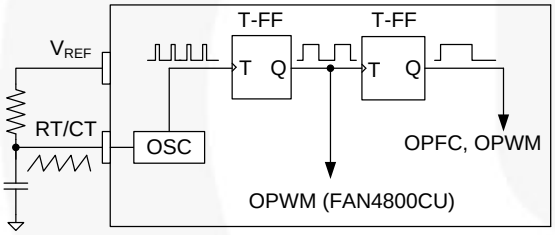


Figure 25. Oscillator Configuration

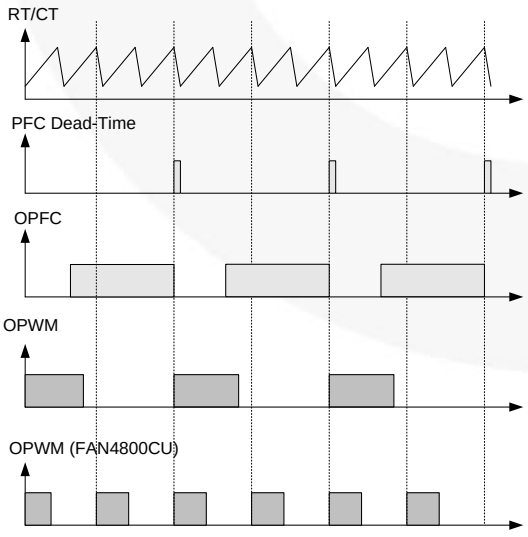


Figure 26. Timing Diagram

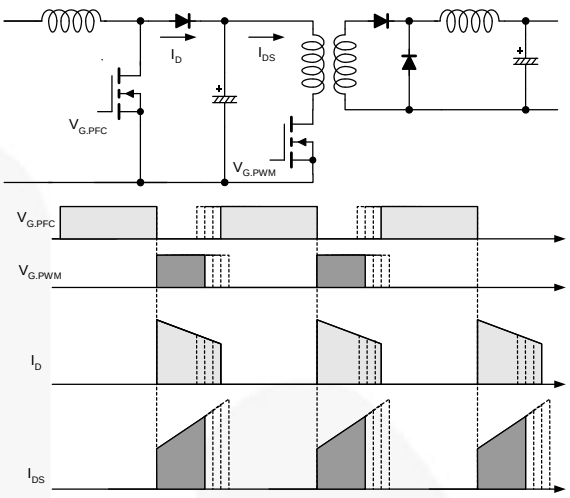


Figure 27. Interleaved Leading / Trailing Edge Modulation

Figure 27 shows the interleaved leading / trailing edge modulation, where the turn-off of the PFC drive signal is synchronized to the turn-on of the PWM drive signal. This technique allows the PFC output diode current to flow directly into the downstream DC/DC converter, minimizing the current ripple of PFC output capacitor.

Gain Modulator

Gain modulator is the key block for the PFC stage because it provides the reference to the current control error amplifier for the input current shaping, as shown in Figure 28. The output current of the gain modulator is a function of V_{EA}, I_{AC}, and V_{RMS}. The gain of the gain modulator is given as a ratio between I_{MO} and I_{AC} with a given V_{RMS} when V_{EA} is saturated to HIGH. The gain is inversely proportional to V_{RMS}^2, as shown in Figure 29, to implement line feed-forward. This automatically adjusts the reference of current control error amplifier according to the line voltage, such that the input power of PFC converter is not changed with line voltage (as shown in Figure 30).

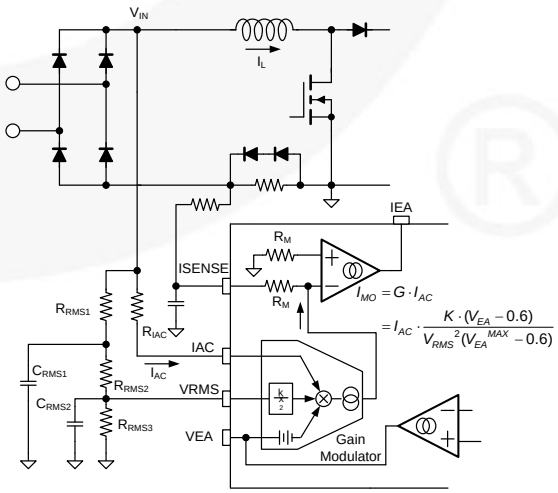


Figure 28. Gain Modulator Block

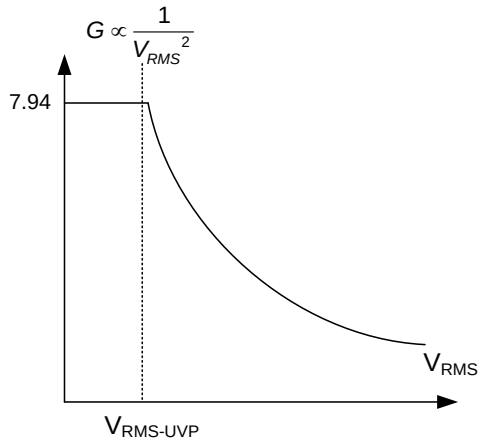


Figure 29. Modulation Gain Characteristics

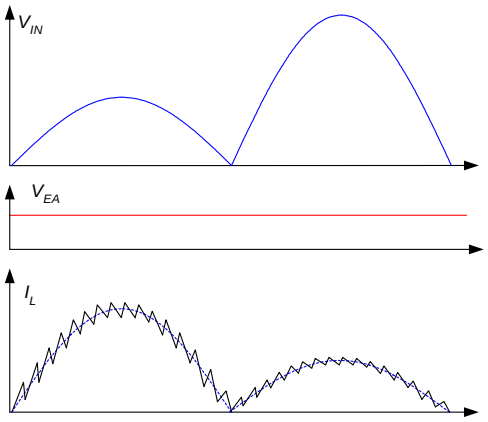


Figure 30. Line Feed-Forward Operation

To sense the RMS value of the line voltage, averaging circuit with two poles is typically employed, as shown in Figure 28. Notice that the input voltage of the PFC is clamped at the peak of the line voltage once the PFC stops switching because the junction capacitance of the bridge diode is not discharged, as shown in Figure 31. Therefore, the voltage divider for VRMS should be designed considering the brownout protection trip-point and minimum operation line voltage.

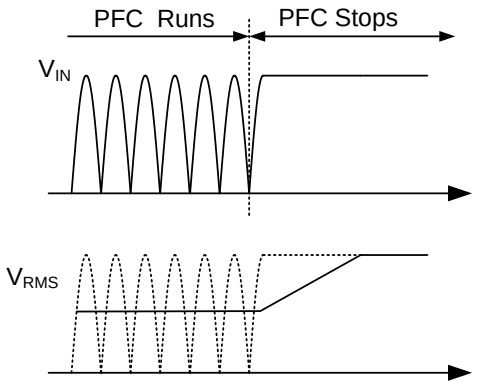


Figure 31. V_{RMS} According to the PFC Operation

The rectified sinusoidal signal is obtained by the current flowing into the IAC pin. The resistor R_{IAC} should be large enough to prevent saturation of the gain modulator, calculating as:

$$\frac{\sqrt{2}V_{LINE}^{MIN}}{R_{IAC}} \cdot G^{MAX} < 140\mu A \quad (3)$$

where $V_{LINEMIN}$ is the line voltage that trips brownout protection, G_{MAX} is the maximum modulator gain when V_{RMS} is 1.08 V (which can be found in the datasheet), and 140 µA is the maximum output current of the gain modulator.

Current Control of Boost Stage

The FAN4800AU/CU employs two control loops for power factor correction, as shown in Figure 32: a current-control loop and a voltage-control loop. The current-control loop shapes inductor current as shown in Figure 33 based on the reference signal obtained at the IAC pin calculated as:

$$I_L \cdot R_{CS1} = I_{MO} \cdot R_M = I_{AC} \cdot G \cdot R_M \quad (4)$$

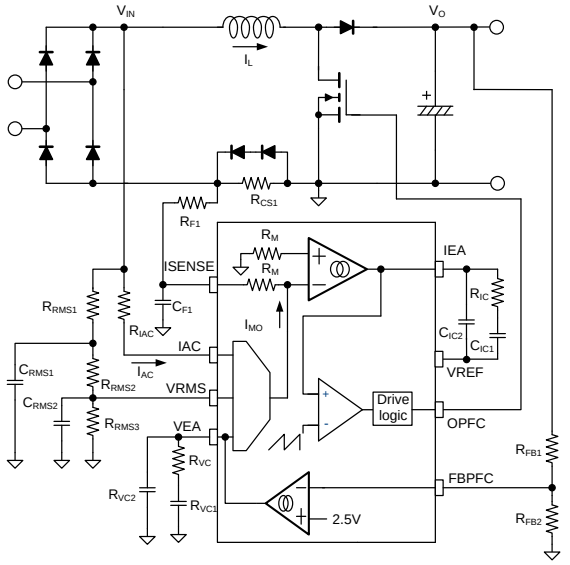


Figure 32. Gain Modulation Block

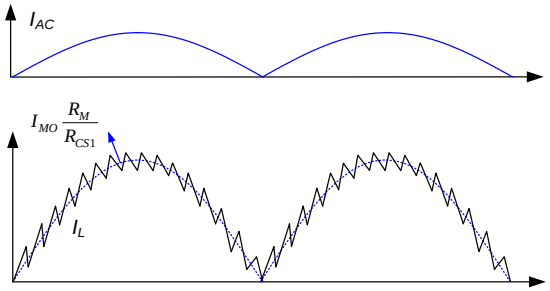


Figure 33. Inductor Current Shaping

The current-control feedback loop also has a pulse-by-pulse current limit comparator that forces the PFC switch to turn off until the next switching cycle if the ISENSE pin voltage drops below -1.3 V.

Voltage Control of Boost Stage

The voltage-control loop regulates PFC output voltage using an internal error amplifier such that the FB voltage is the same as the internal reference of 2.5 V.

Brownout Protection

The built-in internal brownout protection comparator monitors the voltage of the VRMS pin. Once VRMS pin voltage is lower than 1.05 V, the PFC stage is shut down to protect the system from over current. FAN4800AU/CU starts up the boost stage once VRMS voltage increases above 1.9 V.

TriFault Detect™

To improve power supply reliability, reduce system component count, and simplify compliance to UL 1950 safety standards, the FAN4800AU/CU includes Fairchild's TriFault Detect technology.

In a feedback path failure, the output voltage of the PFC can exceed safe operating limits. TriFault Detect protects the power supply from a failure related to the output feedback by monitoring the FBPFC voltage.

TriFault Detect is an entirely internal circuit. It requires no external components to serve its protective function.

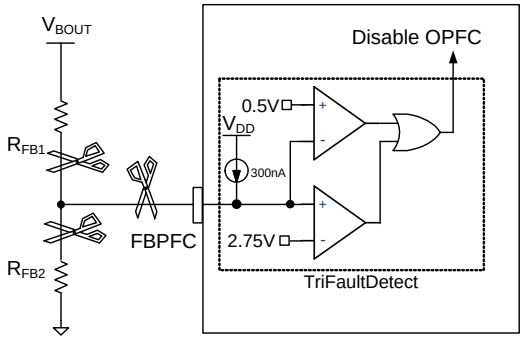


Figure 34. TriFault Detect™

PWM Stage

The PWM stage is capable of Current Mode or Voltage Mode operation. In Current-Mode, the PWM ramp (RAMP) is usually derived directly from a current-sensing resistor or current transformer in the primary side of the output stage, and is thereby representative of the current flowing in the converter's output stage. I_{LIMIT}, which provides cycle-by-cycle current limiting, is typically connected to RAMP in such applications.

For Voltage-Mode operation, RAMP can be connected to a separate RC timing network to generate a voltage ramp against which the FBPWM voltage is compared. Under these conditions, the voltage feed-forward from the PFC bus can be used for better line transient response.

No voltage error amplifier is included in the PWM stage, as this function is generally performed by KA431, in the secondary side. To facilitate the design of opto-coupler feedback circuitry, an offset voltage is built into the inverting input of PWM comparator. This allows FBPWM to command a zero percent duty cycle when its pin voltage is below 1.5 V.

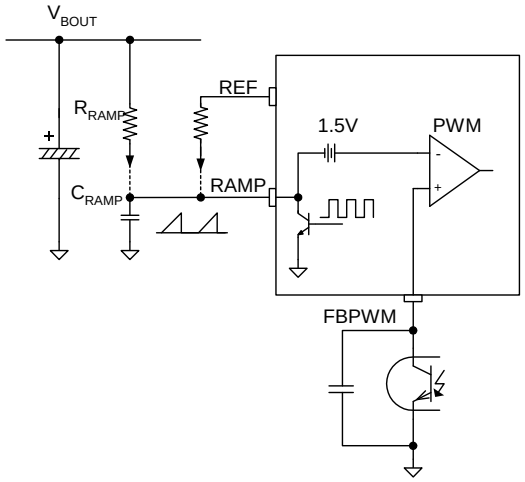


Figure 35. PWM Ramp Generation Circuit

PWM Current Limit

The ILIMIT pin is a direct input to the cycle-by-cycle current limiter for the PWM section. If the input voltage at this pin exceeds 1 V, the output of the PWM is disabled for until the start of the next PWM clock cycle.

V_{IN} OK Comparator

The V_{IN} OK comparator monitors the output of the PFC stage and inhibits the PWM stage if this voltage is less than 2.4 V (96% of its nominal value). Once this voltage goes above 2.4 V, the PWM stage begins soft-start. The PWM stage is shut down when FBPFC voltage drops below 1.3 V.

PWM Soft-Start (SS)

PWM startup is controlled by the soft-start capacitor. A current source of 10 µA supplies the charging current for the soft-start capacitor. PWM startup is prohibited until the soft-start capacitor voltage reaches 1.5 V.

AC Line Drops Out

FAN4800AU/CU is designed such that the operation of PFC part is not perturbed by AC line dropout. Once line voltage disappears, the error amplifier can be saturated, resulting in abnormal current waveforms when the line voltage is recovered if proper preventive measures are not employed.

With a limited gain modulator operation, FAN4800AU /CU guarantees stable PFC operation even when AC line is recovered from dropout, as shown in Figure 36.

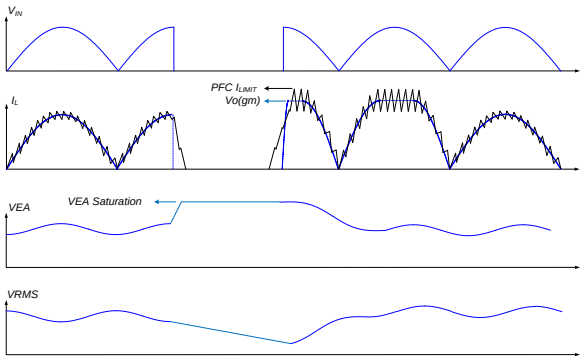


Figure 36. AC Cycle Drop

Line Sag Protection

When the line sags below its normal operational range, the PFC part keeps operating until the brownout protection is triggered, which has 1 s debounce time. Due to the low line voltage, the gain modulator for current loop is saturated and input current of PFC is limited, resulting in a drop of the PFC output voltage at heavy-load condition. Since the PWM part has a V_{IN} OK comparator that shuts down PWM operation when the FBPFC voltage drops below 1.3 V, the downstream DC-DC converter can stop operation while the PFC output voltage drops during line sag. Once the downstream converter stops operation, even the limited PFC input current can charge up the PFC output since the PFC part has no load current. Because this can cause repeated startup and shutdown of downstream converter during line sag, FAN4800AU/CU has line sag protection.

There are two conditions that trigger line sag protection, as shown in Figure 37 and Figure 38. The first condition is when V_{RMS} is lower than $V_{RMS-SAG}$ (0.85 V) for longer than t_{SAG} (33 ms), as shown in Figure 37. The second condition is when V_{RMS} is lower than $V_{RMS-SAG}$ (0.85 V) and VF_{BPFC} is lower than V_{IN-OFF} (1.3 V), as shown in Figure 38. Once line sag protection is triggered, the PWM and the PFC stop operation until V_{RMS} increases above 1.9 V.

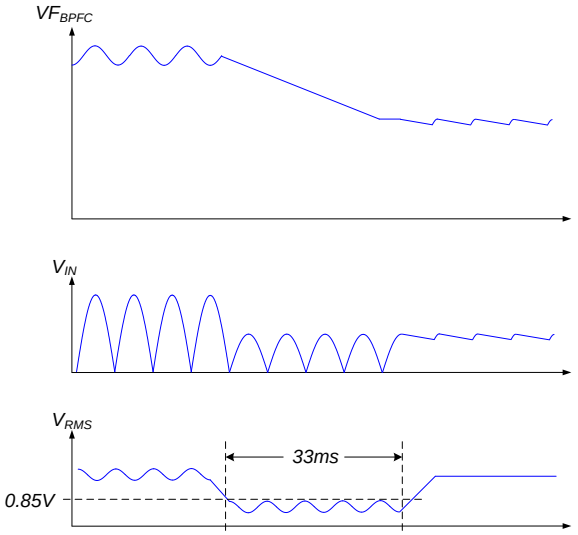


Figure 37. The First Condition of Sag Protection

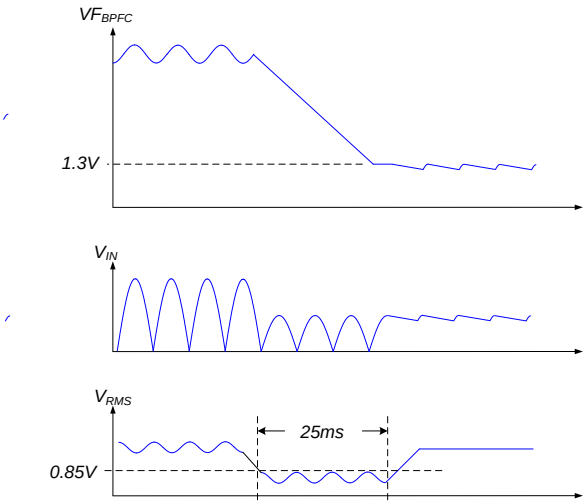
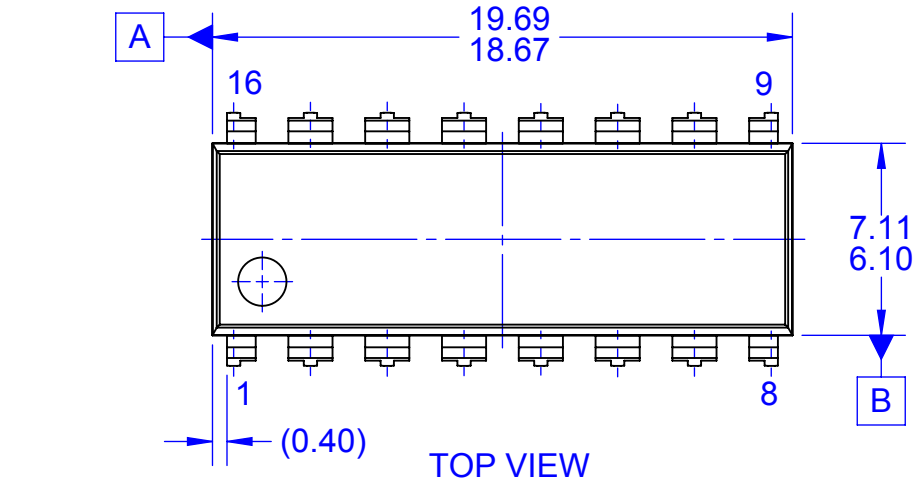
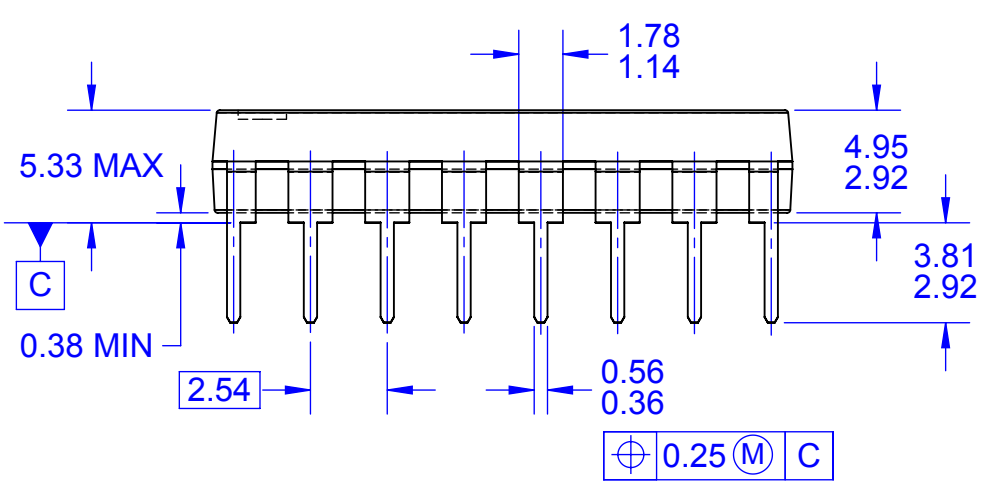


Figure 38. The Second condition of Sag Protection



TOP VIEW



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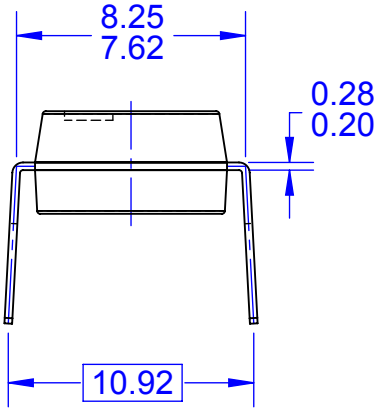

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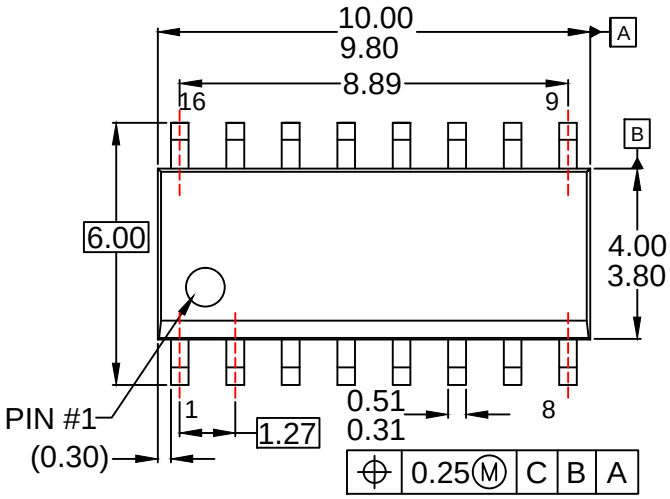

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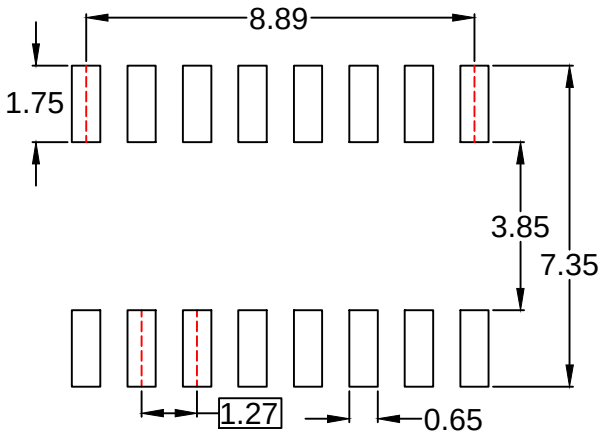

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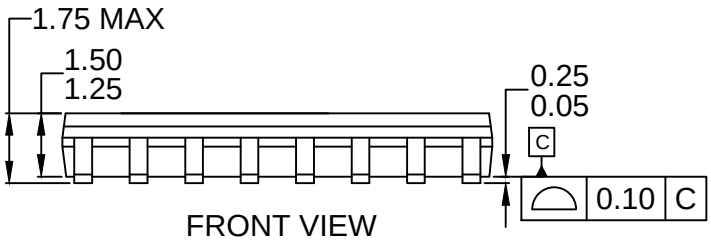

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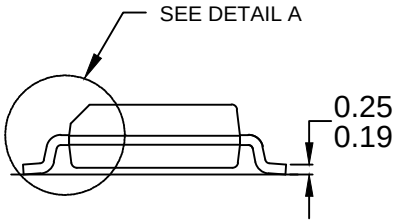

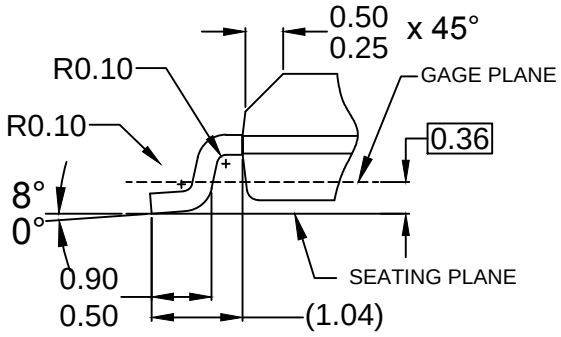

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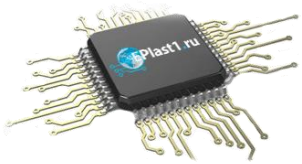

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