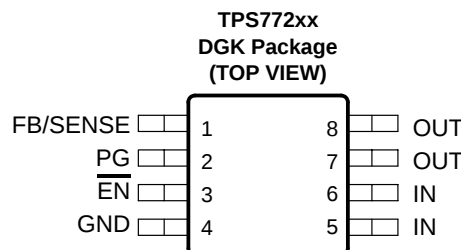
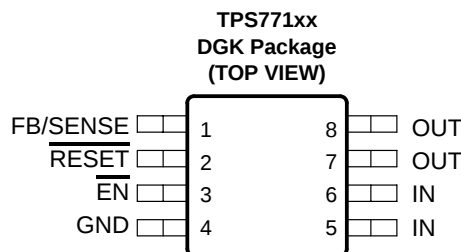


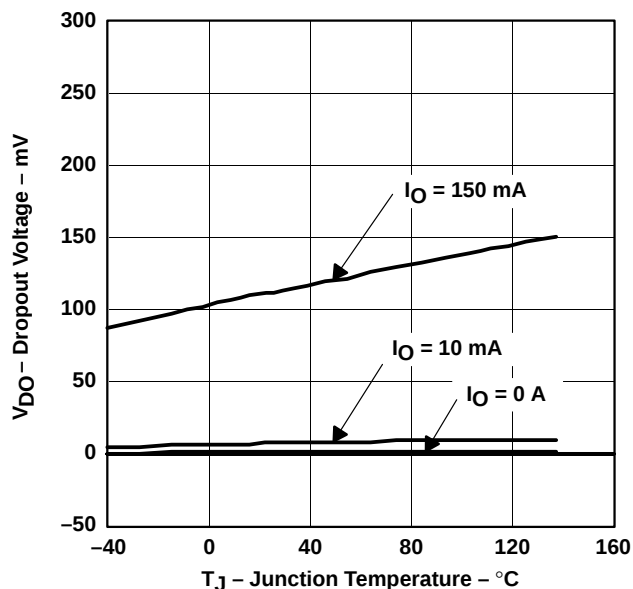
TPS77101/115/118/127/128/133/150 WITH RESET OUTPUT TPS77201/215/218/227/228/233/250 WITH POWER GOOD OUTPUT 150-mA LDO REGULATORS WITH 8-PIN MSOP PACKAGING

SLVS225D – FEBRUARY 2000 – REVISED OCTOBER 2000

- Open Drain Power-On Reset With 220-ms Delay (TPS771xx)
- Open Drain Power-Good (PG) Status Output (TPS772xx)
- 150-mA Low-Dropout Voltage Regulator
- Available in 1.5-V, 1.8-V, 2.7-V, 2.8-V, 3.3-V, 5.0-V Fixed Output and Adjustable Versions
- Dropout Voltage Typically 115 mV at 150 mA (TPS77133, TPS77233)
- Ultralow 92- μ A Quiescent Current (Typ)
- 8-Pin MSOP (DGK) Package
- Low Noise (55 μ V_{rms}) Without External Filter (Bypass) Capacitor (TPS77118, TPS77218)
- 2% Tolerance Over Specified Conditions for Fixed-Output Versions
- Fast Transient Response
- Thermal Shutdown Protection



TPS77x33
DROPOUT VOLTAGE
VS
JUNCTION TEMPERATURE



description

The TPS771xx and TPS772xx are low-dropout regulators with integrated power-on reset and power good (PG) function respectively. These devices are capable of supplying 150 mA of output current with a dropout of 115 mV (TPS77133, TPS77233). Quiescent current is 92 μ A at full load dropping down to 1 μ A when device is disabled. These devices are optimized to be stable with a wide range of output capacitors including low ESR ceramic (10 μ F) or low capacitance (1 μ F) tantalum capacitors. These devices have extremely low noise output performance (55 μ V_{rms}) without using any added filter capacitors. TPS771xx and TPS772xx are designed to have fast transient response for larger load current changes.

The TPS771xx or TPS772xx is offered in 1.5 V, 1.8-V, 2.7-V, 2.8-V, 3.3-V, and 5.0 V fixed-voltage versions and in an adjustable version (programmable over the range of 1.5 V to 5.5 V). Output voltage tolerance is 2% over line, load, and temperature ranges. The TPS771xx and TPS772xx families are available in 8-pin MSOP (DGK) packages.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 115 mV at an output current of 150 mA for 3.3 volt option) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 92 μ A over the full range of output current, 0 mA to 150 mA). These two key specifications yield a significant improvement in operating life for battery-powered systems.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2000, Texas Instruments Incorporated

TPS77101/115/118/127/128/133/150 WITH RESET OUTPUT TPS77201/215/218/227/228/233/250 WITH POWER GOOD OUTPUT 150-mA LDO REGULATORS WITH 8-PIN MSOP PACKAGING

SLVS225D – FEBRUARY 2000 – REVISED OCTOBER 2000

description (continued)

The device is enabled when the $\overline{\text{EN}}$ pin is connected to a low-level input voltage. This LDO family also features a sleep mode; applying a TTL high signal to $\overline{\text{EN}}$ (enable) shuts down the regulator, reducing the quiescent current to less than $1\ \mu\text{A}$ at $T_J = 25^\circ\text{C}$.

The TPS771xx features an integrated power-on reset, commonly used as a supply voltage supervisor (SVS) or reset output voltage. The $\overline{\text{RESET}}$ output of the TPS771xx initiates a reset in DSP, microcomputer or microprocessor systems at power up and in the event of an undervoltage condition. An internal comparator in the TPS771xx monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage. When OUT reaches 95% of its regulated voltage, $\overline{\text{RESET}}$ will go to a high-impedance state after a 220 ms delay. $\overline{\text{RESET}}$ will go to low-impedance state when OUT is pulled below 95% (i.e. over load condition) of its regulated voltage.

For the TPS772xx, the power good terminal (PG) is an active high output, which can be used to implement a power-on reset or a low-battery indicator. An internal comparator in the TPS772xx monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage. When OUT falls below 82% of its regulated voltage, PG will go to a low-impedance state. PG will go to a high-impedance state when OUT is above 82% of its regulated voltage.

AVAILABLE OPTIONS

T_J	OUTPUT VOLTAGE (V)	PACKAGED DEVICES MSOP (DGK)			
	TYP		TPS771xx SYMBOL		TPS772xx SYMBOL
–40°C to 125°C	5.0	TPS77150DGK	AFV	TPS77250DGK	AGE
	3.3	TPS77133DGK	AFU	TPS77233DGK	AGD
	2.8	TPS77128DGK	AFS	TPS77228DGK	AGB
	2.7	TPS77127DGK	AFR	TPS77227DGK	AGA
	1.8	TPS77118DGK	AFP	TPS77218DGK	AFY
	1.5	TPS77115DGK	AFO	TPS77215DGK	AFX
	Adjustable 1.5 V to 5.5 V	TPS77101DGK	AFN	TPS77201DGK	AFW

NOTE: The TPS77101 and TPS77201 are programmable using an external resistor divider (see application information). The DGK package is available taped and reeled. Add an R suffix to the device type (e.g., TPS77101DGKR).

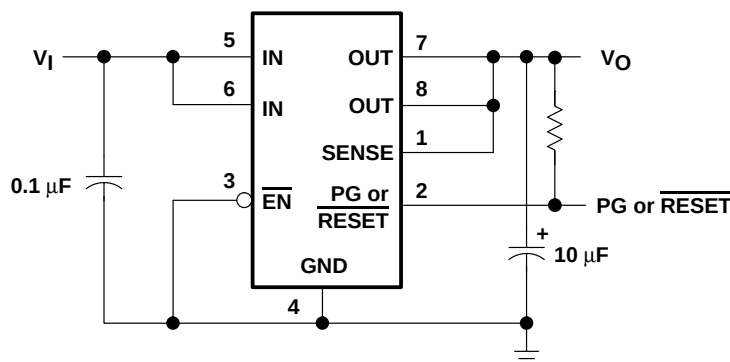


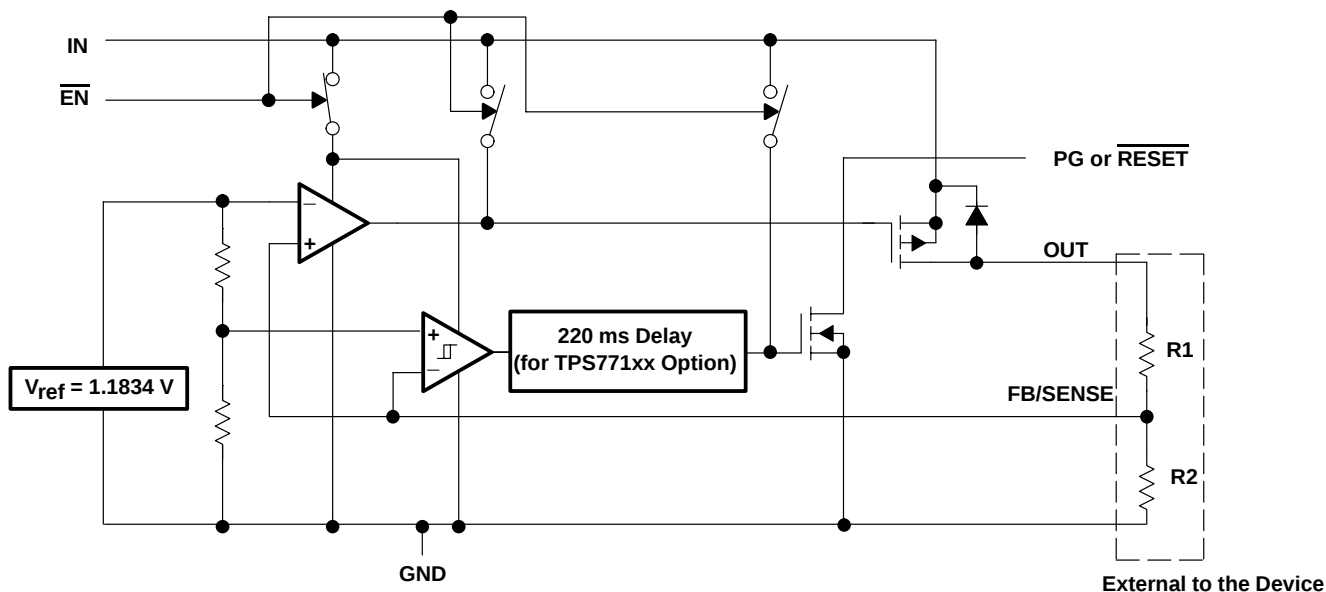
Figure 1. Typical Application Configuration (For Fixed Output Options)

TPS77101/115/118/127/128/133/150 WITH $\overline{\text{RESET}}$ OUTPUT
TPS77201/215/218/227/228/233/250 WITH POWER GOOD OUTPUT
150-mA LDO REGULATORS WITH 8-PIN MSOP PACKAGING

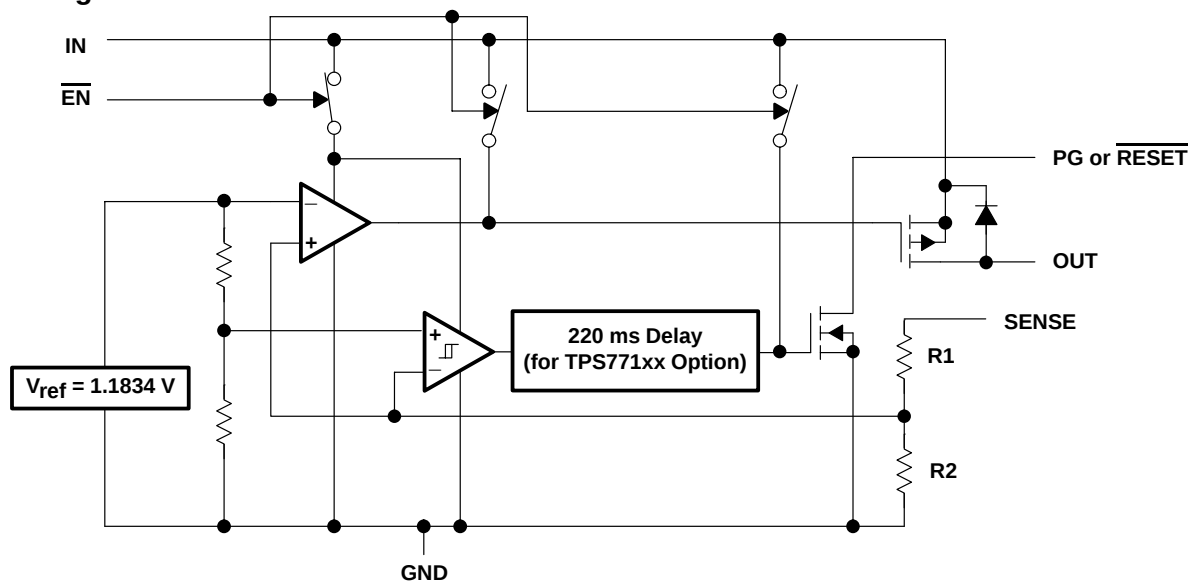
SLVS225D – FEBRUARY 2000 – REVISED OCTOBER 2000

functional block diagrams

adjustable version



fixed-voltage version



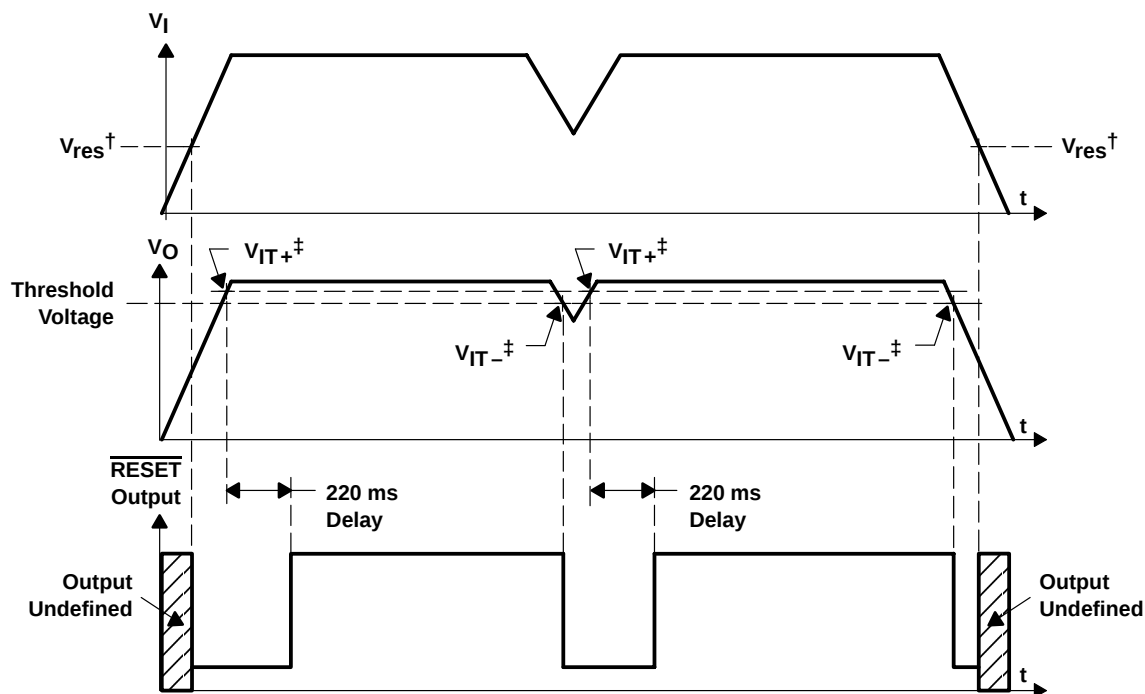
TPS77101/115/118/127/128/133/150 WITH $\overline{\text{RESET}}$ OUTPUT
TPS77201/215/218/227/228/233/250 WITH POWER GOOD OUTPUT
150-mA LDO REGULATORS WITH 8-PIN MSOP PACKAGING

SLVS225D – FEBRUARY 2000 – REVISED OCTOBER 2000

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
TPS771XX			
FB/SENSE	1	I	Feedback input voltage for adjustable device (sense input for fixed options)
$\overline{\text{RESET}}$	2	O	Reset output
$\overline{\text{EN}}$	3	I	Enable input
GND	4		Regulator ground
IN	5, 6	I	Input voltage
OUT	7, 8	O	Regulated output voltage
TPS772XX			
FB/SENSE	1	I	Feedback input voltage for adjustable device (sense input for fixed options)
PG	2	O	Power good
$\overline{\text{EN}}$	3	I	Enable input
GND	4		Regulator ground
IN	5, 6	I	Input voltage
OUT	7, 8	O	Regulated output voltage

TPS771xx $\overline{\text{RESET}}$ timing diagram



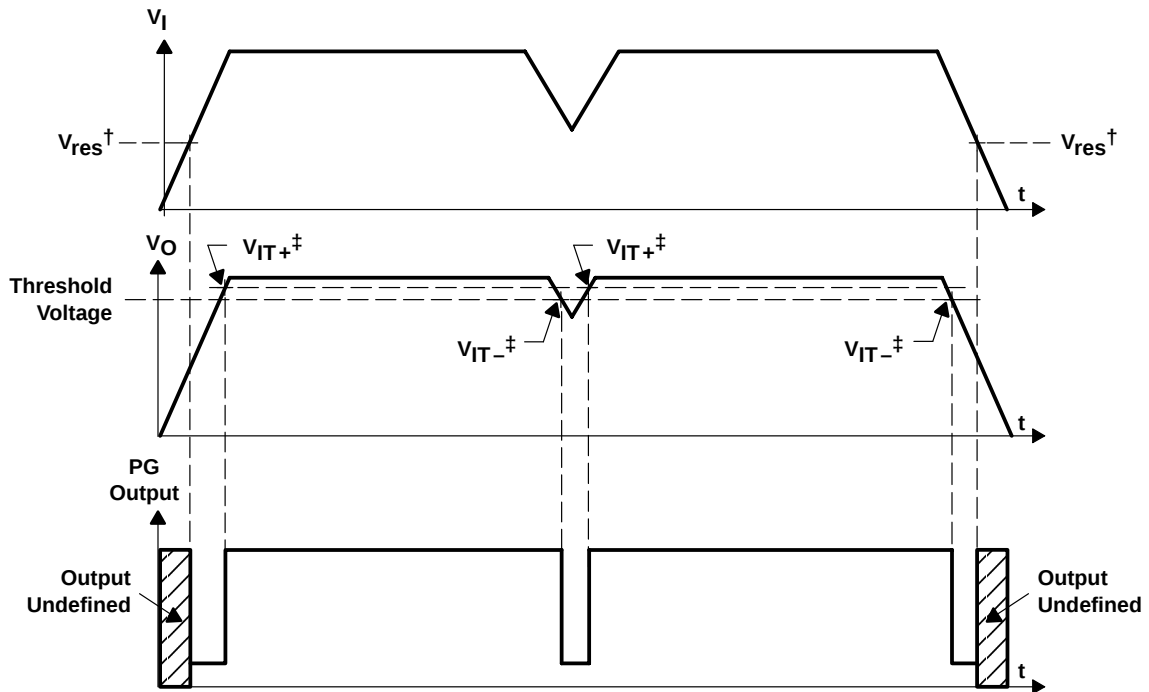
$^\dagger V_{\text{res}}$ is the minimum input voltage for a valid $\overline{\text{RESET}}$. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

$^\ddagger V_{\text{IT}}$ – Trip voltage is typically 5% lower than the output voltage ($95\%V_o$) $V_{\text{IT-}}$ to $V_{\text{IT+}}$ is the hysteresis voltage.

TPS77101/115/118/127/128/133/150 WITH RESET OUTPUT
TPS77201/215/218/227/228/233/250 WITH POWER GOOD OUTPUT
150-mA LDO REGULATORS WITH 8-PIN MSOP PACKAGING

SLVS225D – FEBRUARY 2000 – REVISED OCTOBER 2000

TPS772xx PG timing diagram



[†] V_{res} is the minimum input voltage for a valid PG. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

[‡] V_{IT-} – Trip voltage is typically 18% lower than the output voltage ($82\%V_O$) V_{IT-} to V_{IT+} is the hysteresis voltage.

absolute maximum ratings over operating junction temperature range (unless otherwise noted)[†]

Input voltage range, V_I , (see Note 1)	–0.3 V to 13.5 V
Voltage range at EN	–0.3 V to 16.5 V
Maximum RESET voltage (TPS771xx)	16.5 V
Maximum PG voltage (TPS772xx)	16.5 V
Peak output current	Internally limited
Continuous total power dissipation	See Dissipation Rating Table
Output voltage, V_O (OUT, FB)	5.5 V
Operating virtual junction temperature range, T_J	–40°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
ESD rating, HBM	2 kV

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network terminal ground.

TPS77101/115/118/127/128/133/150 WITH RESET OUTPUT
TPS77201/215/218/227/228/233/250 WITH POWER GOOD OUTPUT
150-mA LDO REGULATORS WITH 8-PIN MSOP PACKAGING

SLVS225D – FEBRUARY 2000 – REVISED OCTOBER 2000

DISSIPATION RATING TABLE – FREE-AIR TEMPERATURES

PACKAGE	AIR FLOW (CFM)	θ_{JA} (°C/W)	θ_{JC} (°C/W)	$T_A < 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
DGK	0	266.2	3.84	376 mW	3.76 mW/°C	207 mW	150 mW
	150	255.2	3.92	392 mW	3.92 mW/°C	216 mW	157 mW
	250	242.8	4.21	412 mW	4.12 mW/°C	227 mW	165 mW

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I [†]	2.7	10	V
Output voltage range, V_O	1.5	5.5	V
Output current, I_O (see Note 2)	0	150	mA
Operating virtual junction temperature, T_J (see Note 2)	–40	125	°C

[†] To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{I(\min)} = V_{O(\max)} + V_{DO(\max \text{ load})}$.
 NOTE 2: Continuous current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.



TPS77101/115/118/127/128/133/150 WITH RESET OUTPUT
TPS77201/215/218/227/228/233/250 WITH POWER GOOD OUTPUT
150-mA LDO REGULATORS WITH 8-PIN MSOP PACKAGING

SLVS225D – FEBRUARY 2000 – REVISED OCTOBER 2000

electrical characteristics over recommended operating junction temperature range (–40°C to 125°C), $V_I = V_{O(typ)} + 1\text{ V}$, $I_O = 1\text{ mA}$, $\overline{\text{EN}} = 0\text{ V}$, $C_O = 10\text{ }\mu\text{F}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage (see Notes 3 and 4)	Adjustable voltage	1.5 V ≤ V _O ≤ 5.5 V, T _J = 25°C	V _O			V
		1.5 V ≤ V _O ≤ 5.5 V	0.98V _O	1.02V _O		
	1.5-V Output	T _J = 25°C, 2.7 V < V _{IN} < 10 V	1.5			V
		2.7 V < V _{IN} < 10 V	1.470	1.530		
	1.8-V Output	T _J = 25°C, 2.8 V < V _{IN} < 10 V	1.8			
		2.8 V < V _{IN} < 10 V	1.764	1.836		
	2.7-V Output	T _J = 25°C, 3.7 V < V _{IN} < 10 V	2.7			
		3.7 V < V _{IN} < 10 V	2.646	2.754		
	2.8-V Output	T _J = 25°C, 3.8 V < V _{IN} < 10 V	2.8			
		3.8 V < V _{IN} < 10 V	2.744	2.856		
	3.3-V Output	T _J = 25°C, 4.3 V < V _{IN} < 10 V	3.3			
		4.3 V < V _{IN} < 10 V	3.234	3.366		
	5.0-V Output	T _J = 25°C, 6 V < V _{IN} < 10 V	5.0			V
		6 V < V _{IN} < 10 V	4.900	5.100		
Quiescent current (GND current) (see Notes 3 and 4)		T _J = 25°C	92			μA
			125			
Output voltage line regulation (ΔV _O /V _O) (see Note 5)		V _O + 1 V < V _I ≤ 10 V, T _J = 25°C	0.005			%/V
		V _O + 1 V < V _I ≤ 10 V	0.05			%/V
Load regulation		T _J = 25°C	1			mV
Output noise voltage		BW = 300 Hz to 100 kHz, T _J = 25°C, TPS77118, TPS77218	55			μVrms
Output current Limit		V _O = 0 V	0.9	1.3		A
Peak output current		2 ms pulse width, 50% duty cycle	400			mA
Thermal shutdown junction temperature			144			°C
Standby current		$\overline{\text{EN}}$ = V _I , T _J = 25°C	1			μA
		$\overline{\text{EN}}$ = V _I	3			μA
FB input current	Adjustable voltage	FB = 1.5 V	1			μA
High level enable input voltage			2			V
Low level enable input voltage			0.7			V
Enable input current			–1	1		μA
Power supply ripple rejection (TPS77118, TPS77218)		f = 1 KHz, T _J = 25°C	55			dB

NOTES: 3. Minimum input operating voltage is 2.7 V or $V_{O(typ)} + 1\text{ V}$, whichever is greater. Maximum input voltage = 10 V, minimum output current 1 mA.

4. If $V_O < 1.8\text{ V}$ then $V_{I(max)} = 10\text{ V}$, $V_{I(min)} = 2.7\text{ V}$:

$$\text{Line regulation (mV)} = (\%/V) \times \frac{V_O(V_{I(max)} - 2.7\text{ V})}{100} \times 1000$$

If $V_O > 2.5\text{ V}$ then $V_{I(max)} = 10\text{ V}$, $V_{I(min)} = V_O + 1\text{ V}$:

$$\text{Line regulation (mV)} = (\%/V) \times \frac{V_O(V_{I(max)} - (V_O + 1))}{100} \times 1000$$

5. $I_O = 1\text{ mA to }150\text{ mA}$



TPS77101/115/118/127/128/133/150 WITH RESET OUTPUT
TPS77201/215/218/227/228/233/250 WITH POWER GOOD OUTPUT
150-mA LDO REGULATORS WITH 8-PIN MSOP PACKAGING

SLVS225D – FEBRUARY 2000 – REVISED OCTOBER 2000

electrical characteristics over recommended operating junction temperature range (–40°C to 125°C), $V_I = V_{O(\text{typ})} + 1\text{ V}$, $I_O = 1\text{ mA}$, $\overline{\text{EN}} = 0\text{ V}$, $C_O = 10\text{ }\mu\text{F}$ (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PG (TPS772xx)	Minimum input voltage for valid PG	$I_{(\text{PG})} = 300\mu\text{A}$ $V_{(\text{PG})} \leq 0.8\text{ V}$		1.1		V
	Trip threshold voltage	V_O decreasing	79		85	% V_O
	Hysteresis voltage	Measured at V_O		0.5		% V_O
	Output low voltage	$V_I = 2.7\text{ V}$, $I_{(\text{PG})} = 1\text{ mA}$		0.15	0.4	V
	Leakage current	$V_{(\text{PG})} = 5\text{ V}$			1	μA
Reset (TPS771xx)	Minimum input voltage for valid $\overline{\text{RESET}}$	$I_{(\text{RESET})} = 300\mu\text{A}$		1.1		V
	Trip threshold voltage	V_O decreasing	92		98	% V_O
	Hysteresis voltage	Measured at V_O		0.5		% V_O
	Output low voltage	$V_I = 2.7\text{ V}$, $I_{(\text{RESET})} = 1\text{ mA}$		0.15	0.4	V
	Leakage current	$V_{(\text{RESET})} = 5\text{ V}$			1	μA
	RESET time-out delay			220		ms
V_{DO}	Dropout voltage (see Note 6)	2.8-V Output	$I_O = 150\text{ mA}$, $T_J = 25^\circ\text{C}$		150	mV
			$I_O = 150\text{ mA}$		265	
	3.3-V Output	$I_O = 150\text{ mA}$, $T_J = 25^\circ\text{C}$		115		
		$I_O = 150\text{ mA}$			200	
	5.0-V Output	$I_O = 150\text{ mA}$, $T_J = 25^\circ\text{C}$		75		
		$I_O = 150\text{ mA}$			115	

NOTE 6: I_N voltage equals $V_{O(\text{typ})} - 100\text{ mV}$; 1.5 V, 1.8 V, and 2.7 V dropout voltage limited by input voltage range limitations (i.e., 3.3 V input voltage needs to drop to 3.2 V for purpose of this test).

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_O	Output voltage	vs Output current	2, 3
		vs Junction temperature	4, 5
	Ground current	vs Junction temperature	6
	Power supply rejection ratio	vs Frequency	7
	Output spectral noise density	vs Frequency	8
Z_O	Output impedance	vs Frequency	9
V_{DO}	Dropout voltage	vs Input voltage	10
		vs Junction temperature	11
	Line transient response		12, 14
	Load transient response		13, 15
	Output voltage and enable pulse	vs Time	16
	Equivalent series resistance (ESR)	vs Output current	18 – 21

TPS77101/115/118/127/128/133/150 WITH $\overline{\text{RESET}}$ OUTPUT
TPS77201/215/218/227/228/233/250 WITH POWER GOOD OUTPUT
150-mA LDO REGULATORS WITH 8-PIN MSOP PACKAGING

SLVS225D – FEBRUARY 2000 – REVISED OCTOBER 2000

TYPICAL CHARACTERISTICS

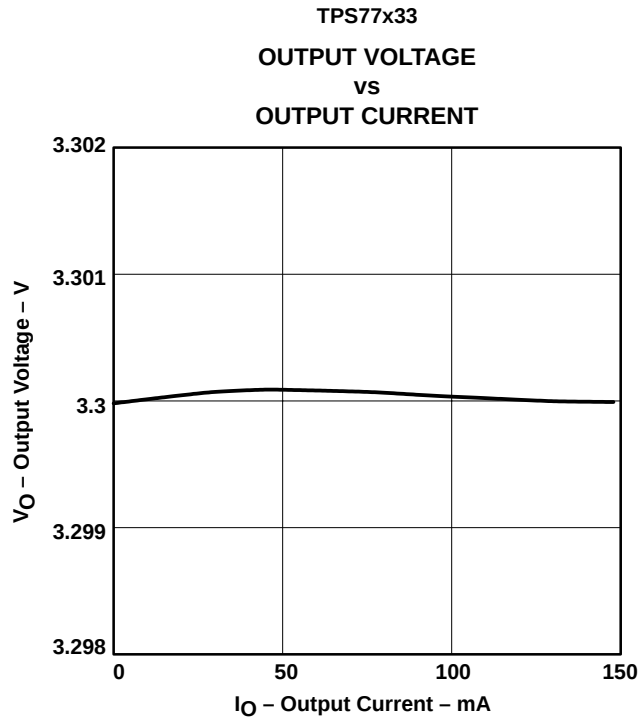


Figure 2

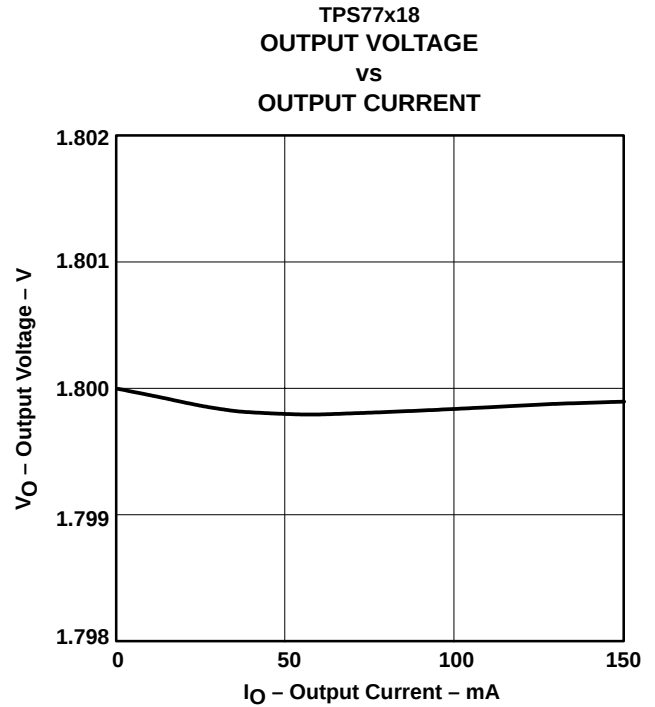


Figure 3

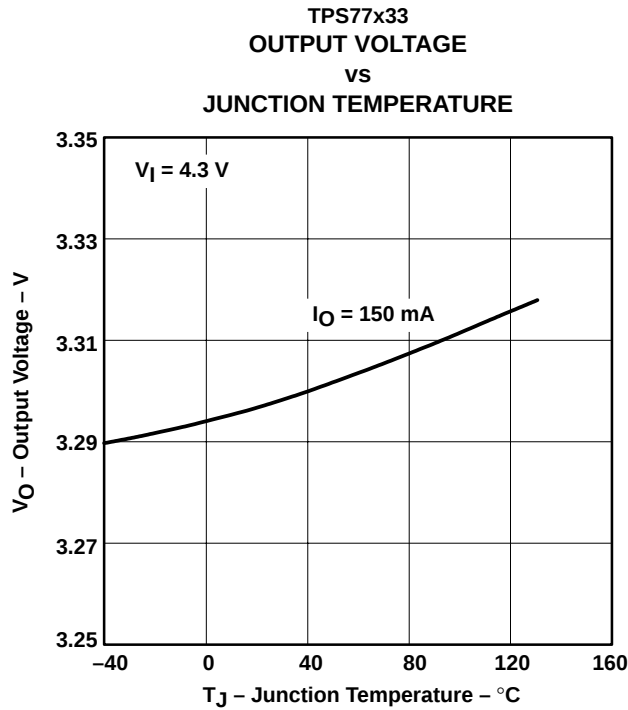


Figure 4

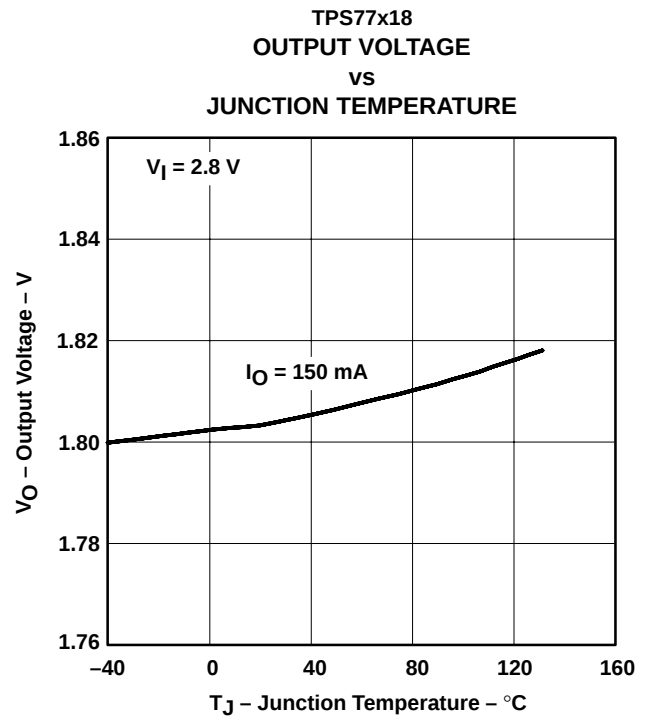


Figure 5

TPS77101/115/118/127/128/133/150 WITH RESET OUTPUT
TPS77201/215/218/227/228/233/250 WITH POWER GOOD OUTPUT
150-mA LDO REGULATORS WITH 8-PIN MSOP PACKAGING

SLVS225D – FEBRUARY 2000 – REVISED OCTOBER 2000

TYPICAL CHARACTERISTICS

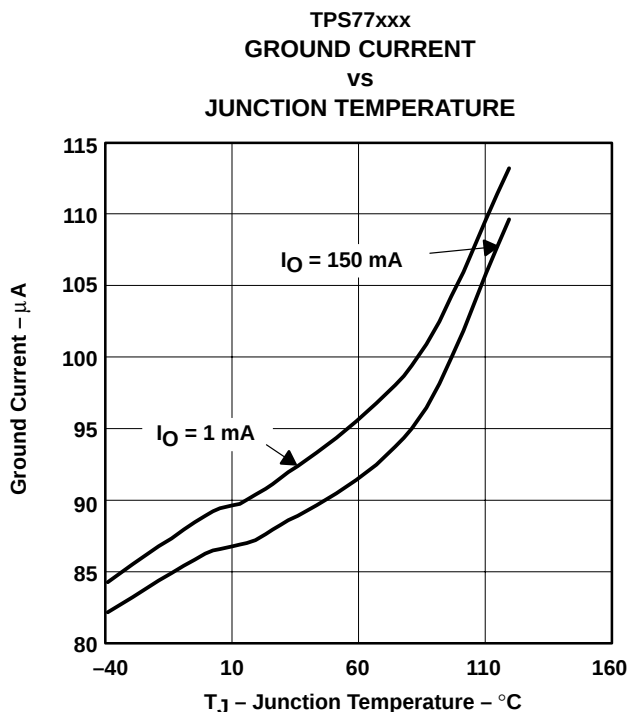


Figure 6

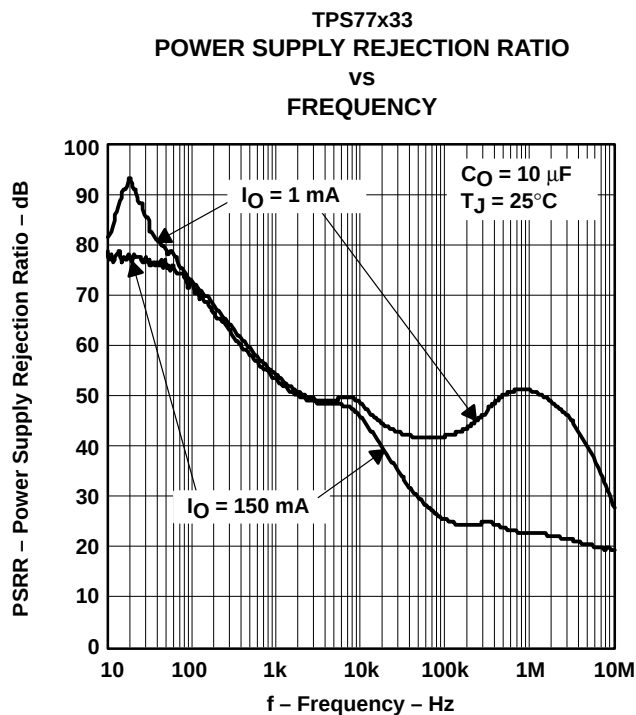


Figure 7

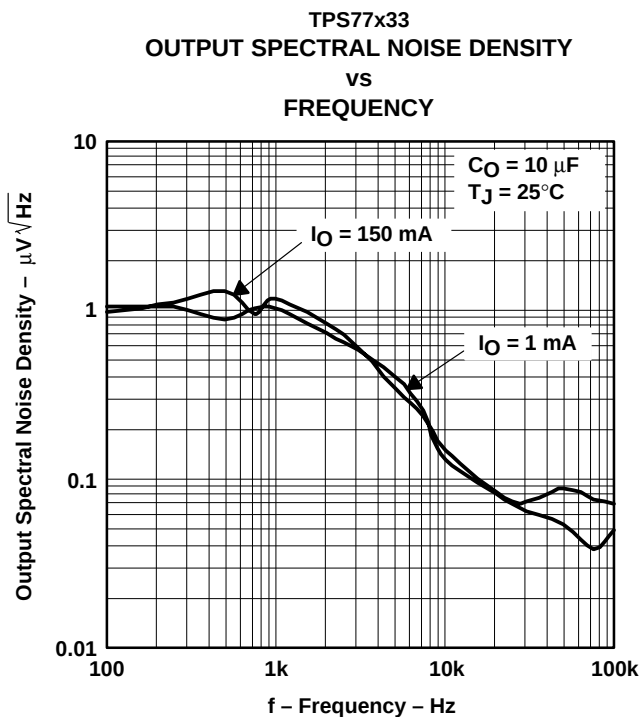


Figure 8

TYPICAL CHARACTERISTICS

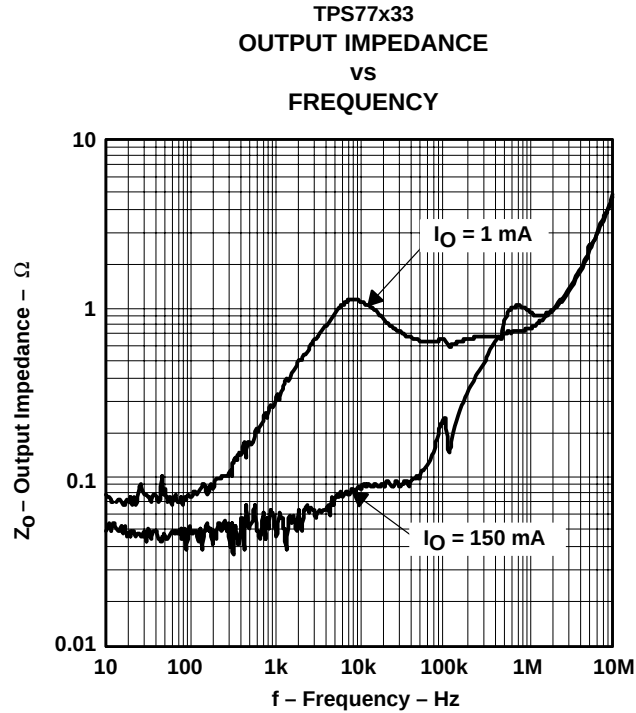


Figure 9

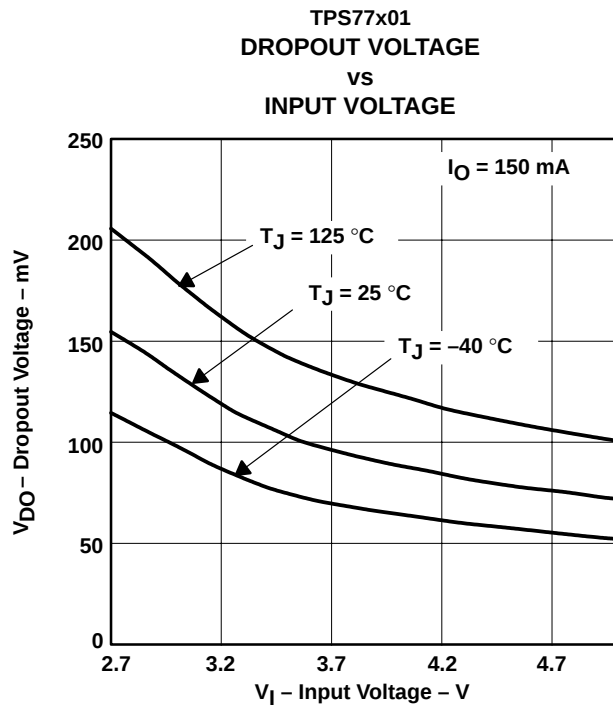


Figure 10

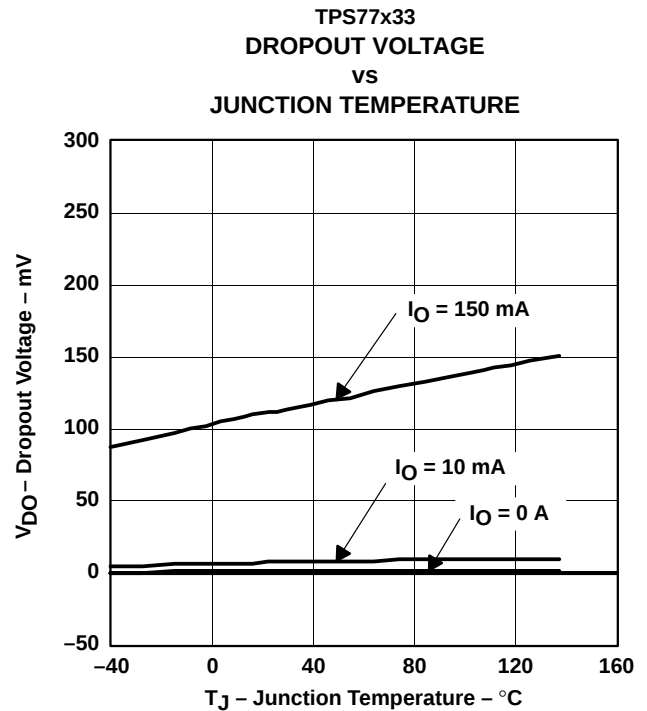


Figure 11

TPS77101/115/118/127/128/133/150 WITH RESET OUTPUT
TPS77201/215/218/227/228/233/250 WITH POWER GOOD OUTPUT
150-mA LDO REGULATORS WITH 8-PIN MSOP PACKAGING

SLVS225D – FEBRUARY 2000 – REVISED OCTOBER 2000

TYPICAL CHARACTERISTICS

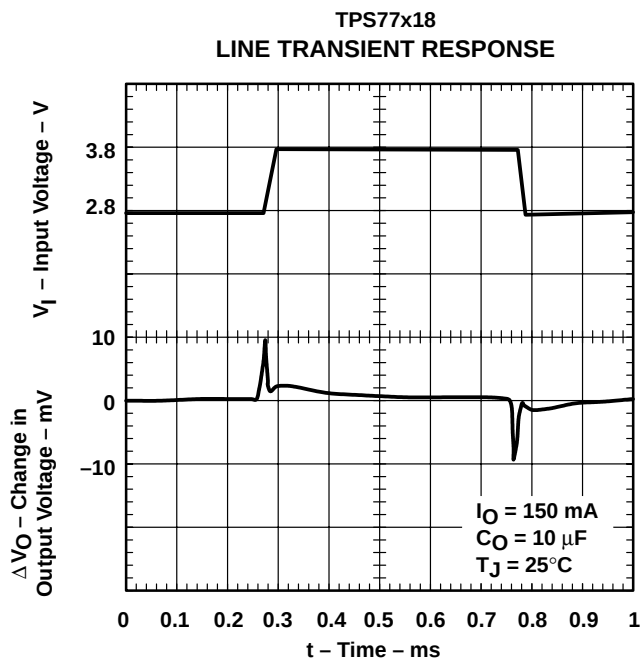


Figure 12

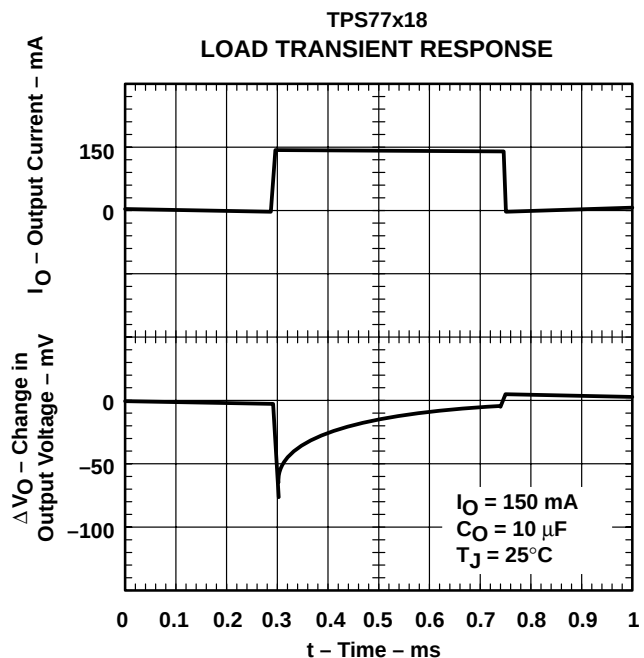


Figure 13

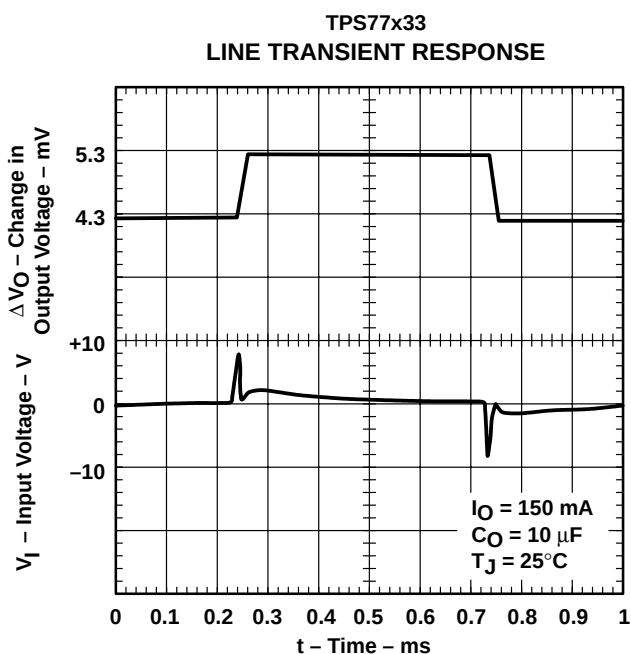


Figure 14

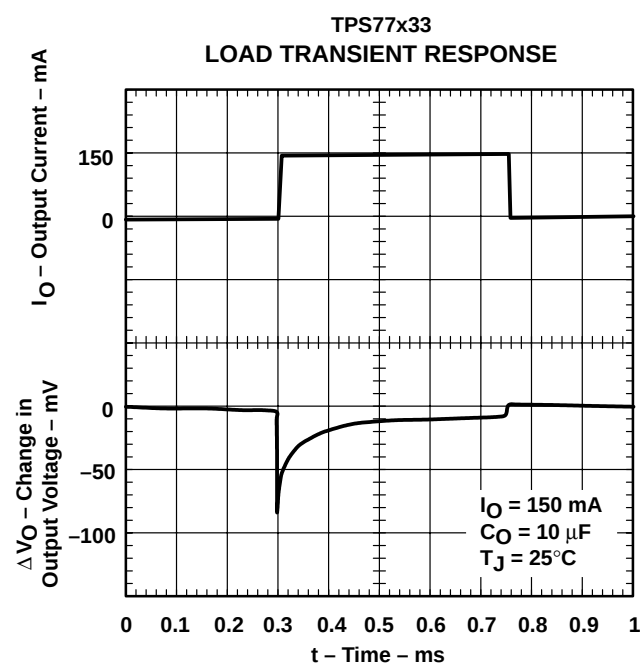


Figure 15

TYPICAL CHARACTERISTICS

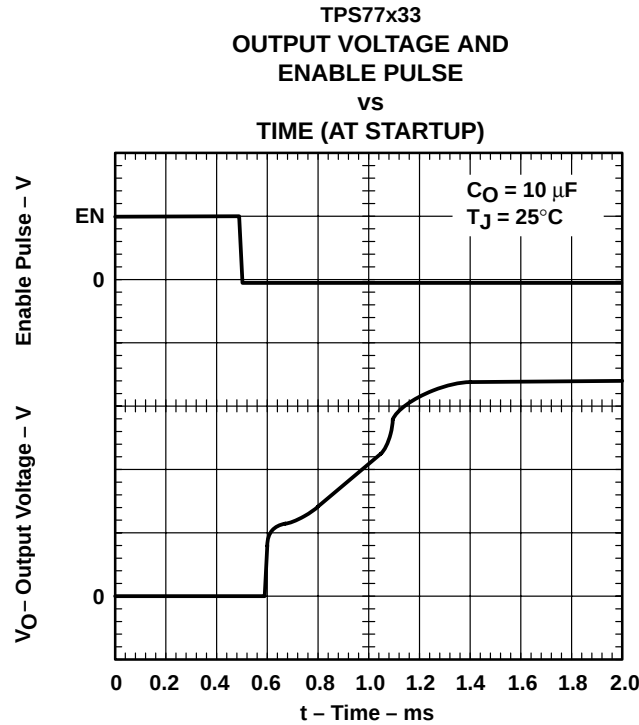


Figure 16

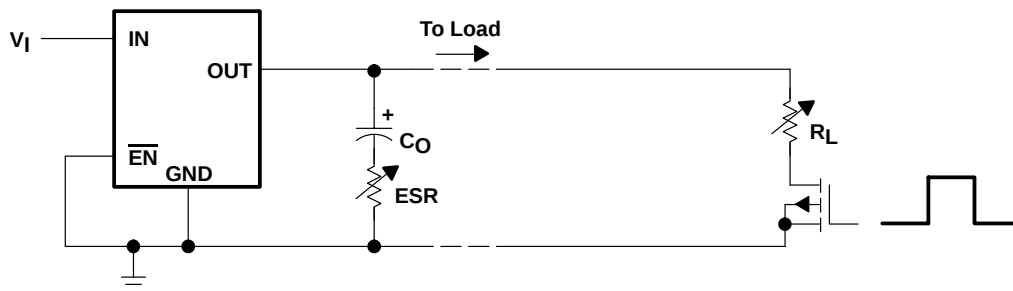


Figure 17. Test Circuit for Typical Regions of Stability (Figures 18 through 21) (Fixed Output Options)

TPS77101/115/118/127/128/133/150 WITH RESET OUTPUT
TPS77201/215/218/227/228/233/250 WITH POWER GOOD OUTPUT
150-mA LDO REGULATORS WITH 8-PIN MSOP PACKAGING

SLVS225D – FEBRUARY 2000 – REVISED OCTOBER 2000

TYPICAL CHARACTERISTICS

**TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE[†]**

**VS
OUTPUT CURRENT**

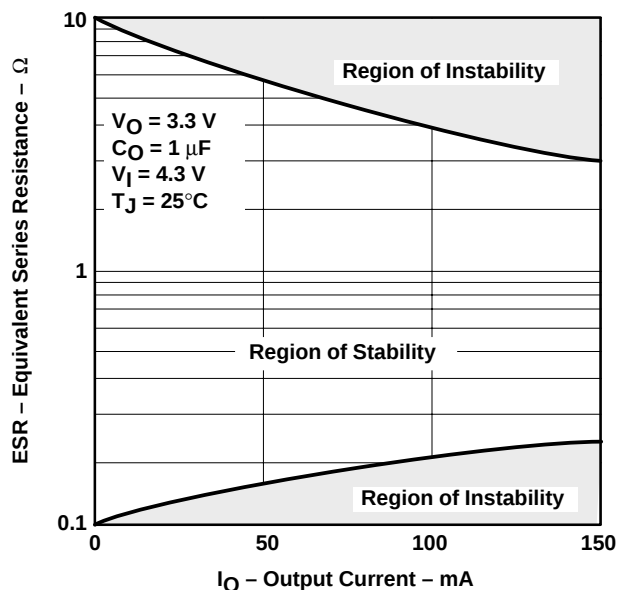


Figure 18

**TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE[†]**

**VS
OUTPUT CURRENT**

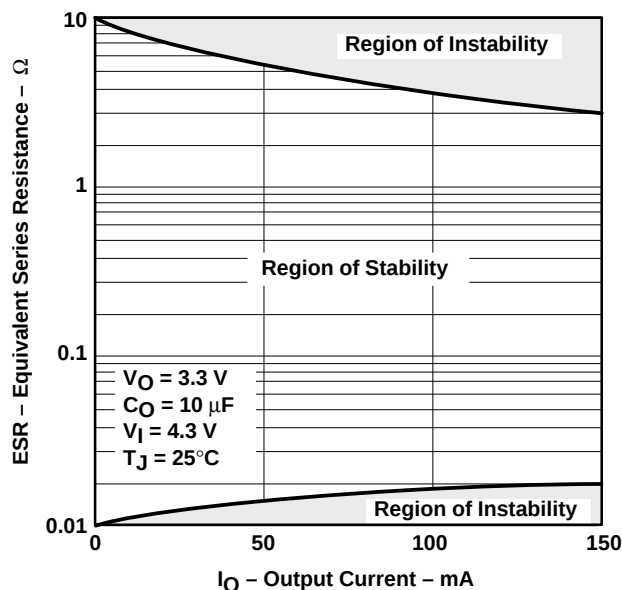


Figure 19

**TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE[†]**

**VS
OUTPUT CURRENT**

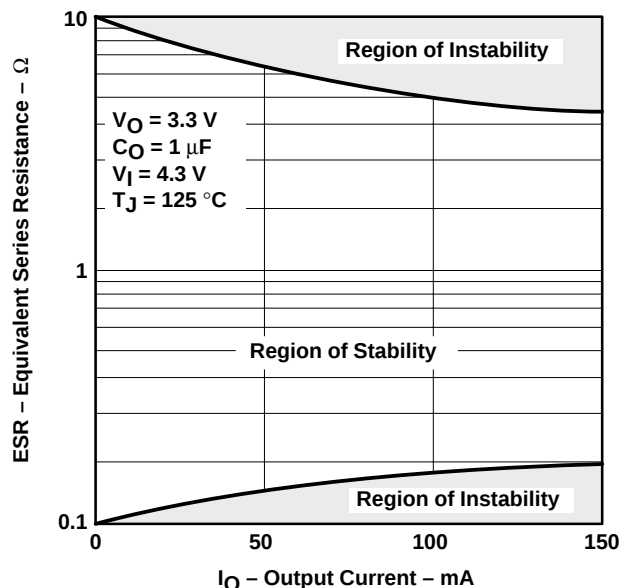


Figure 20

**TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE[†]**

**VS
OUTPUT CURRENT**

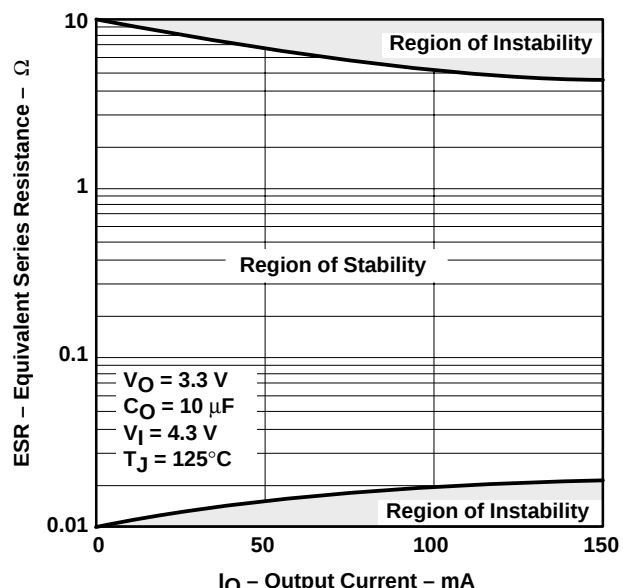


Figure 21

[†] Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

APPLICATION INFORMATION

pin functions

enable ($\overline{\text{EN}}$)

The $\overline{\text{EN}}$ terminal is an input which enables or shuts down the device. If $\overline{\text{EN}}$ is a logic high, the device will be in shutdown mode. When $\overline{\text{EN}}$ goes to logic low, then the device will be enabled.

power good (PG) (TPS772xx)

The PG terminal is an open drain, active high output that indicates the status of V_{out} (output of the LDO). When V_{out} reaches 82% of the regulated voltage, PG will go to a high-impedance state. It will go to a low-impedance state when V_{out} falls below 82% (i.e. over load condition) of the regulated voltage. The open drain output of the PG terminal requires a pullup resistor.

sense (SENSE)

The SENSE terminal of the fixed-output options must be connected to the regulator output, and the connection should be as short as possible. Internally, SENSE connects to a high-impedance wide-bandwidth amplifier through a resistor-divider network and noise pickup feeds through to the regulator output. It is essential to route the SENSE connection in such a way to minimize/avoid noise pickup. Adding RC networks between the SENSE terminal and V_{out} to filter noise is not recommended because it may cause the regulator to oscillate.

feedback (FB)

FB is an input terminal used for the adjustable-output options and must be connected to an external feedback resistor divider. The FB connection should be as short as possible. It is essential to route it in such a way to minimize/avoid noise pickup. Adding RC networks between FB terminal and V_{out} to filter noise is not recommended because it may cause the regulator to oscillate.

reset ($\overline{\text{RESET}}$) (TPS771xx)

The $\overline{\text{RESET}}$ terminal is an open drain, active low output that indicates the status of V_{out} . When V_{out} reaches 95% of the regulated voltage, $\overline{\text{RESET}}$ will go to a high-impedance state after a 220-ms delay. $\overline{\text{RESET}}$ will go to a low-impedance state when V_{out} is below 95% of the regulated voltage. The open-drain output of the $\overline{\text{RESET}}$ terminal requires a pullup resistor.

TPS77101/115/118/127/128/133/150 WITH RESET OUTPUT
TPS77201/215/218/227/228/233/250 WITH POWER GOOD OUTPUT
150-mA LDO REGULATORS WITH 8-PIN MSOP PACKAGING

SLVS225D – FEBRUARY 2000 – REVISED OCTOBER 2000

APPLICATION INFORMATION

external capacitor requirements

An input capacitor is not usually required; however, a bypass capacitor (0.047 μ F or larger) improves load transient response and noise rejection if the TPS771xx or TPS772xx is located more than a few inches from the power supply. A higher-capacitance capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Most low noise LDOs require an external capacitor to further reduce noise. This will impact the cost and board space. The TPS771xx and TPS772xx have very low noise specification requirements without using any external components.

Like all low dropout regulators, the TPS771xx or TPS772xx requires an output capacitor connected between OUT (output of the LDO) and GND (signal ground) to stabilize the internal control loop. The minimum recommended capacitance value is 1 μ F provided the ESR meets the requirement in Figures 19 and 21. In addition, a low-ESR capacitor can be used if the capacitance is at least 10 μ F and the ESR meets the requirements in Figures 18 and 20. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described previously.

Ceramic capacitors have different types of dielectric material with each exhibiting different temperature and voltage variation. The most common types are X5R, X7R, Y5U, Z5U, and NPO. The NPO type ceramic type capacitors are generally the most stable over temperature. However, the X5R and X7R are also relatively stable over temperature (with the X7R being the more stable of the two) and are therefore acceptable to use. The Y5U and Z5U types provide high capacitance in a small geometry, but exhibit large variations over temperature; therefore, the Y5U and Z5U are not generally recommended for use on this LDO. Independent of which type of capacitor is used, one must make certain that at the worst case condition the capacitance/ESR meets the requirement specified in Figures 18 – 21.



APPLICATION INFORMATION

Figure 22 shows the output capacitor and its parasitic impedances in a typical LDO output stage.

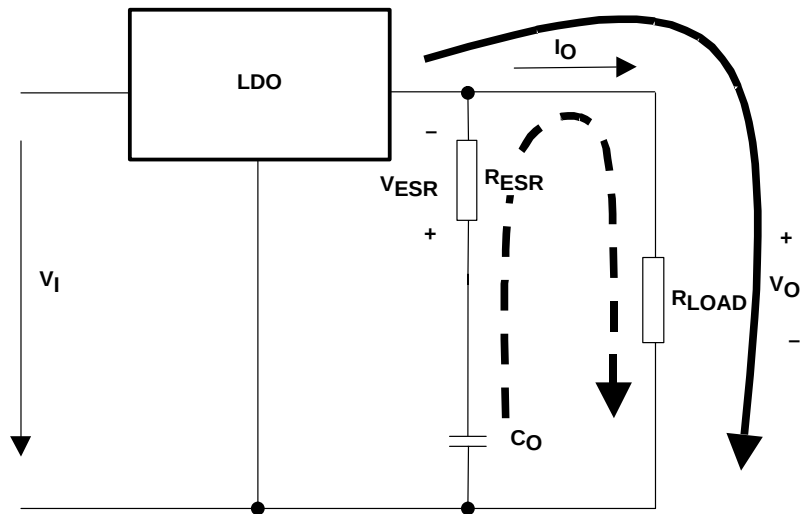


Figure 22. LDO Output Stage With Parasitic Resistances ESR and ESL

In steady state (dc state condition), the load current is supplied by the LDO (solid arrow) and the voltage across the capacitor is the same as the output voltage ($V_{C_{out}} = V_{out}$). This means no current is flowing into the C_{out} branch. If I_{out} suddenly increases (transient condition), the following occurs:

- The LDO is not able to supply the sudden current need due to its response time (t_1 in Figure 23). Therefore, capacitor C_{out} provides the current for the new load condition (dashed arrow). C_{out} now acts like a battery with an internal resistance, ESR. Depending on the current demand at the output, a voltage drop will occur at R_{ESR} . This voltage is shown as V_{ESR} in Figure 22.
- When C_{out} is conducting current to the load, initial voltage at the load will be $V_{out} = V_{C_{out}} - V_{ESR}$. Due to the discharge of C_{out} , the output voltage V_{out} will drop continuously until the response time t_1 of the LDO is reached and the LDO will resume supplying the load. From this point, the output voltage starts rising again until it reaches the regulated voltage. This period is shown as t_2 in Figure 23.

The figure also shows the impact of different ESRs on the output voltage. The left brackets show different levels of ESRs where number 1 displays the lowest and number 3 displays the highest ESR.

From above, the following conclusions can be drawn:

- The higher the ESR, the larger the droop at the beginning of load transient.
- The smaller the output capacitor, the faster the discharge time and the bigger the voltage droop during the LDO response period.

APPLICATION INFORMATION

conclusion

To minimize the transient output droop, capacitors must have a low ESR and be large enough to support the minimum output voltage requirement.

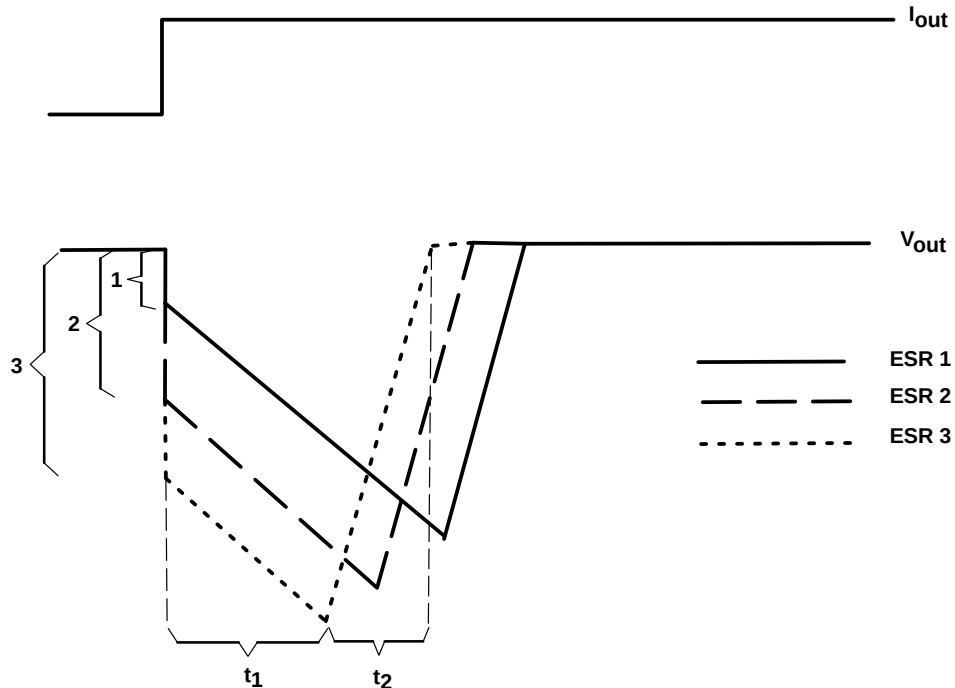


Figure 23. Correlation of Different ESRs and Their Influence to the Regulation of V_{out} at a Load Step From Low-to-High Output Current

TPS77101/115/118/127/128/133/150 WITH $\overline{\text{RESET}}$ OUTPUT
TPS77201/215/218/227/228/233/250 WITH POWER GOOD OUTPUT
150-mA LDO REGULATORS WITH 8-PIN MSOP PACKAGING

SLVS225D – FEBRUARY 2000 – REVISED OCTOBER 2000

APPLICATION INFORMATION

programming the TPS77x01 adjustable LDO regulator

The output voltage of the TPS77x01 adjustable regulator is programmed using an external resistor divider as shown in Figure 24. The output voltage is calculated using:

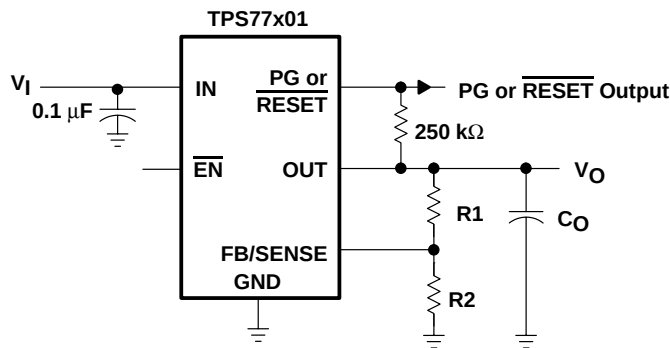
$$V_O = V_{\text{ref}} \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

Where:

$V_{\text{ref}} = 1.1834 \text{ V typ}$ (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 50- μA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided, as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose $R_2 = 30.1 \text{ k}\Omega$ to set the divider current at 50 μA and then calculate R1 using:

$$R_1 = \left(\frac{V_O}{V_{\text{ref}}} - 1\right) \times R_2 \quad (2)$$



**OUTPUT VOLTAGE
PROGRAMMING GUIDE**

OUTPUT VOLTAGE	R1	R2	UNIT
2.5 V	33.5	30.1	k Ω
3.3 V	53.8	30.1	k Ω
3.6 V	61.5	30.1	k Ω

NOTE: To reduce noise and prevent oscillation, R1 and R2 need to be as close as possible to the FB/SENSE terminal.

Figure 24. TPS77x01 Adjustable LDO Regulator Programming

TPS77101/115/118/127/128/133/150 WITH RESET OUTPUT
TPS77201/215/218/227/228/233/250 WITH POWER GOOD OUTPUT
150-mA LDO REGULATORS WITH 8-PIN MSOP PACKAGING

SLVS225D – FEBRUARY 2000 – REVISED OCTOBER 2000

APPLICATION INFORMATION

regulator protection

The TPS771xx or TPS772xx PMOS-pass transistor has a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS771xx or TPS772xx also features internal current limiting and thermal protection. During normal operation, the TPS771xx or TPS772xx limits output current to approximately 0.9 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C(typ), regulator operation resumes.

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D , which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

Where:

T_{Jmax} is the maximum allowable junction temperature.

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 266.2°C/W for the 8-terminal MSOP with no airflow.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

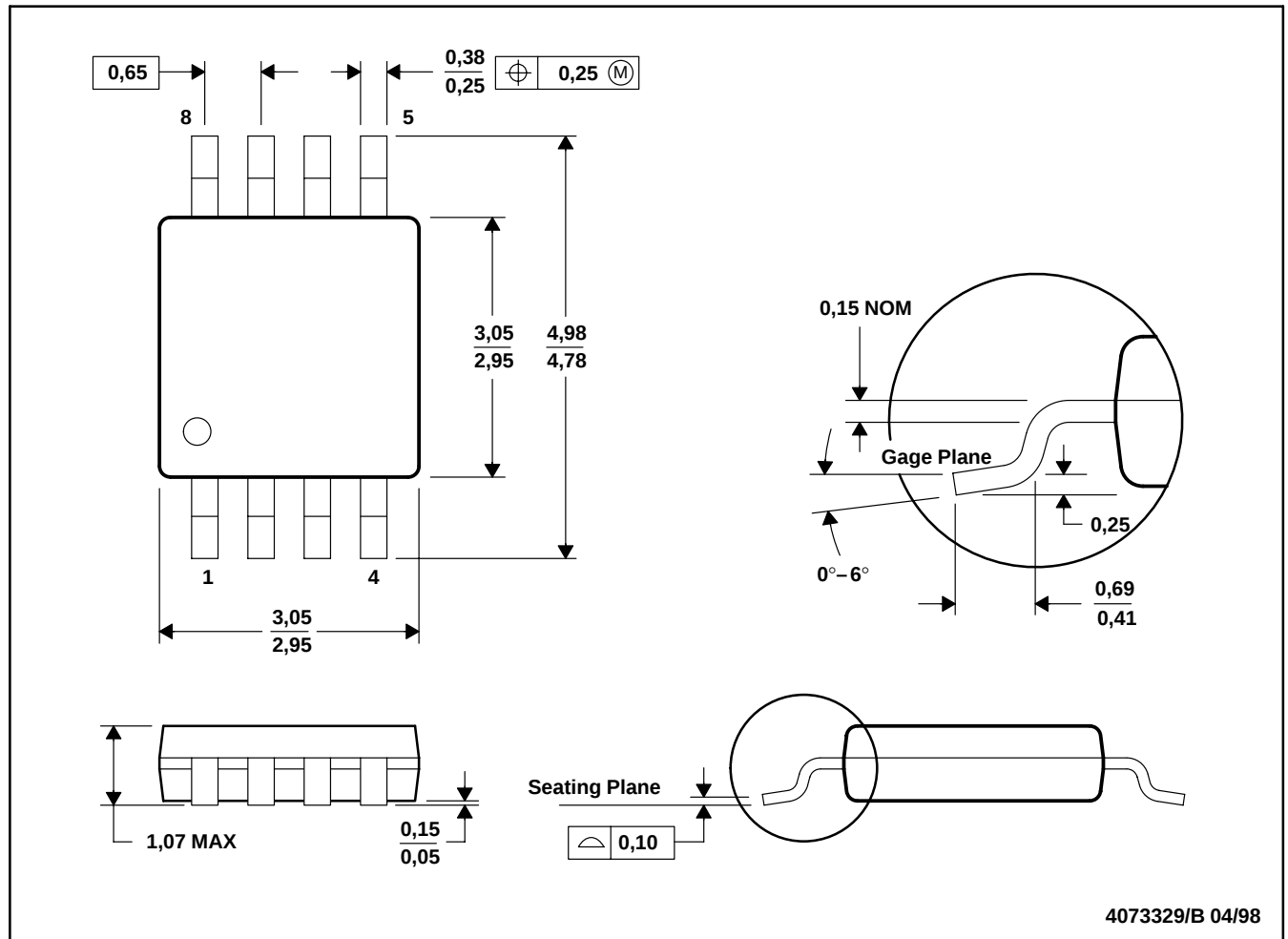
TPS77101/115/118/127/128/133/150 WITH RESET OUTPUT
TPS77201/215/218/227/228/233/250 WITH POWER GOOD OUTPUT
150-mA LDO REGULATORS WITH 8-PIN MSOP PACKAGING

SLVS225D – FEBRUARY 2000 – REVISED OCTOBER 2000

MECHANICAL DATA

DGK (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-187

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS77101DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AFN	Samples
TPS77101DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AFN	Samples
TPS77101DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AFN	Samples
TPS77101DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AFN	Samples
TPS77115DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AFO	Samples
TPS77115DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AFO	Samples
TPS77115DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AFO	Samples
TPS77115DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AFO	Samples
TPS77118DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AFP	Samples
TPS77118DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AFP	Samples
TPS77127DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AFR	Samples
TPS77127DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AFR	Samples
TPS77127DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AFR	Samples
TPS77127DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AFR	Samples
TPS77128DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AFS	Samples
TPS77128DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AFS	Samples
TPS77133DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AFU	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS77133DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AFU	Samples
TPS77133DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AFU	Samples
TPS77133DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AFU	Samples
TPS77150DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AFV	Samples
TPS77150DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AFV	Samples
TPS77150DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AFV	Samples
TPS77150DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AFV	Samples
TPS77201DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AFW	Samples
TPS77201DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AFW	Samples
TPS77201DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AFW	Samples
TPS77201DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AFW	Samples
TPS77215DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AFX	Samples
TPS77215DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AFX	Samples
TPS77218DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AFY	Samples
TPS77218DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AFY	Samples
TPS77227DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AGA	Samples
TPS77227DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AGA	Samples
TPS77233DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AGD	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS77233DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AGD	Samples
TPS77250DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AGE	Samples
TPS77250DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AGE	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Only one of markings shown within the brackets will appear on the physical device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS77101 :

- Automotive: [TPS77101-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS77101DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS77115DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS77127DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS77133DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS77150DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS77201DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS77101DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TPS77115DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TPS77127DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TPS77133DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TPS77150DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TPS77201DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.