

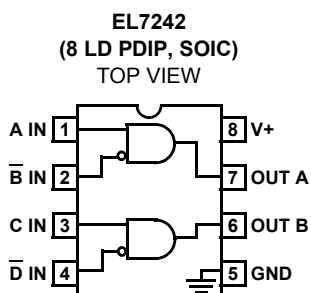
EL7242, EL7252

Dual Input, High Speed, Dual Channel Power MOSFET Driver

FN7285  
Rev 5.00  
September 3, 2015

The EL7242/EL7252 dual input, 2-channel drivers achieve the same excellent switching performance of the EL7212 family while providing added flexibility. The 2-input logic and configuration is applicable to numerous power MOSFET drive circuits. As with other Intersil drivers, the EL7242/EL7252 are excellent for driving large capacitive loads with minimal delay and switching times. "Shoot-thru" protection and latching circuits can be implemented by simply "cross-coupling" the 2-channels.

**Pinouts**



Manufactured under U.S. Patent Nos. 5,334,883, #5,341,047

**Features**

- Logic AND/NAND input
- 3V and 5V Input compatible
- Clocking speeds up to 10MHz
- 20ns Switching/delay time
- 2A Peak drive
- Isolated drains
- Low output impedance
- Low quiescent current
- Wide operating voltage — 4.5V to 16V
- Pb-free available (RoHS compliant)

**Applications**

- Short circuit protected switching
- Undervoltage shut-down circuits
- Switch-mode power supplies
- Motor controls
- Power MOSFET switching
- Switching capacitive loads
- Shoot-thru protection
- Latching drivers

## Ordering Information

PART NUMBER	PART MARKING	PACKAGE	PKG. DWG. #
EL7242CNZ (Note 1)	EL7242CN Z	8 Ld PDIP** (Pb-free)	E8.3
EL7242CSZ (Note 1)	7242CSZ	8 Ld SOIC (Pb-free)	MDP0027
EL7242CSZ-T7* (Note 1)	7242CSZ	8 Ld SOIC (Pb-free)	MDP0027
EL7242CSZ-T13* (Note 1)	7242CSZ	8 Ld SOIC (Pb-free)	MDP0027
EL7252CSZ (Note 1)	7252CSZ	8 Ld SOIC (Pb-free)	MDP0027
EL7252CSZ-T7* (Note 1)	7252CSZ	8 Ld SOIC (Pb-free)	MDP0027
EL7252CSZ-T13* (Note 1)	7252CSZ	8 Ld SOIC (Pb-free)	MDP0027
EL7252CN <b>(No longer available, recommended replacement: EL7252CSZ)</b>	EL7252CN	8 Ld PDIP	E8.3

\*Please refer to TB347 for details on reel specifications.

\*\*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

### NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

**Absolute Maximum Ratings** ( $T_A = +25^\circ\text{C}$ )

Supply (V+ to GND)	16.5V
Input Pins	-0.3V to +0.3V above V+
Combined Peak Output Current	.4A
Storage Temperature Range	-65°C to +150°C

**Operating Conditions**

Ambient Operating Temperature	-40°C to +85°C
Operating Junction Temperature	+125°C

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

**IMPORTANT NOTE:** All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore:  $T_J = T_C = T_A$

**Thermal Information**

Power Dissipation	
8 Ld SOIC	570mW
8 Ld PDIP*	1050mW
Pb-Free Reflow Profile	see link below <a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a>
*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.	

**DC Electrical Specifications**  $T_A = +25^\circ\text{C}$ ,  $V = 15\text{V}$ , unless otherwise specified.

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>INPUT</b>						
$V_{IH}$	Logic '1' Input Voltage		2.4			V
$I_{IH}$	Logic '1' Input Current	@V+		0.1	10	$\mu\text{A}$
$V_{IL}$	Logic '0' Input Voltage				0.8	V
$I_{IL}$	Logic '0' Input Current	@0V		0.1	10	$\mu\text{A}$
$V_{HVS}$	Input Hysteresis			0.3		V
<b>OUTPUT</b>						
$R_{OH}$	Pull-up Resistance	$I_{OUT} = -100\text{mA}$		3	6	$\Omega$
$R_{OL}$	Pull-down Resistance	$I_{OUT} = +100\text{mA}$		4	6	$\Omega$
$I_{PK}$	Peak Output Current	Source		2		A
		Sink		2		A
$I_{DC}$	Continuous Output Current	Source/Sink	100			mA
<b>POWER SUPPLY</b>						
$I_S$	Power Supply Current	Inputs High		1	2.5	mA
$V_S$	Operating Voltage		4.5		16	V

**AC Electrical Specifications**  $T_A = +25^\circ\text{C}$ ,  $V = 15\text{V}$ , unless otherwise specified.

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>SWITCHING CHARACTERISTICS</b>						
$t_R$	Rise Time (Note 2)	$C_L = 500\text{pF}$			10	ns
		$C_L = 1000\text{pF}$			20	ns
$t_F$	Fall Time (Note 2)	$C_L = 500\text{pF}$			10	ns
		$C_L = 1000\text{pF}$			20	ns
$t_{D-ON}$	Turn-On Delay Time (Note 2)			20	25	ns
$t_{D-OFF}$	Turn-Off Delay Time (Note 2)			20	25	ns

NOTE:

2. Limits established by characterization and are not production tested.

**Timing Table**



**Standard Test Configuration**



**Simplified Schematic**



### Typical Performance Curves

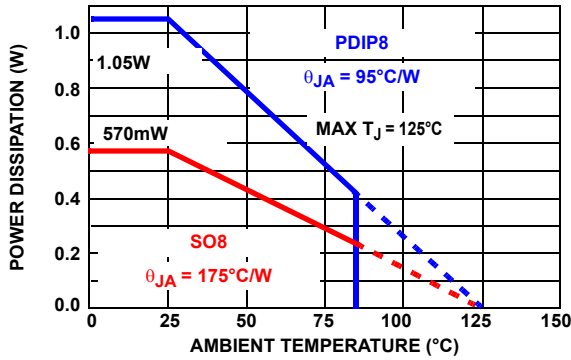


FIGURE 1. MAX POWER/DERATING CURVES



FIGURE 2. SWITCH THRESHOLD vs SUPPLY VOLTAGE



FIGURE 3. INPUT CURRENT vs VOLTAGE



FIGURE 4. PEAK DRIVE vs SUPPLY VOLTAGE



FIGURE 5. QUIESCENT SUPPLY CURRENT

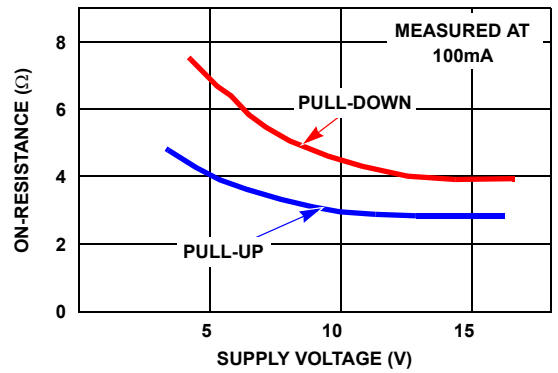


FIGURE 6. ON-RESISTANCE vs SUPPLY VOLTAGE

**Typical Performance Curves** (Continued)



FIGURE 7. AVERAGE SUPPLY CURRENT vs VOLTAGE AND FREQUENCY



FIGURE 8. AVERAGE SUPPLY CURRENT vs CAPACITIVE LOAD

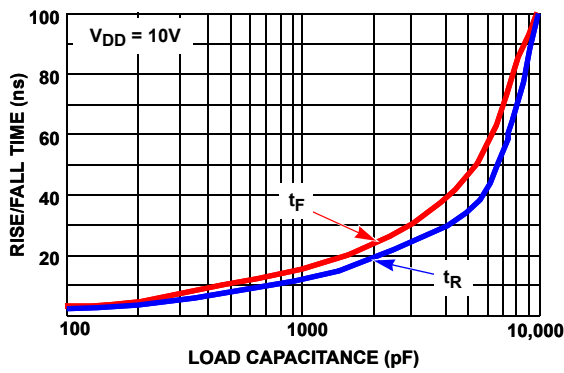


FIGURE 9. RISE/FALL TIME vs LOAD

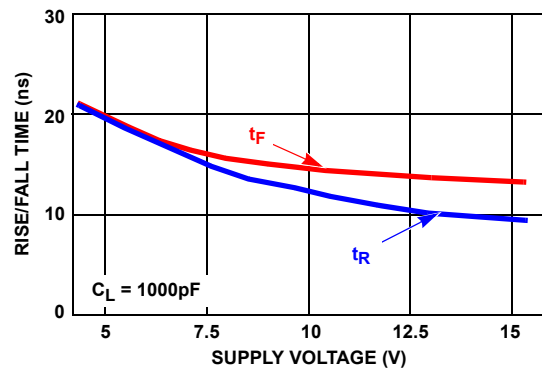


FIGURE 10. RISE/FALL TIME vs SUPPLY VOLTAGE



FIGURE 11. PROPAGATION DELAY vs SUPPLY VOLTAGE

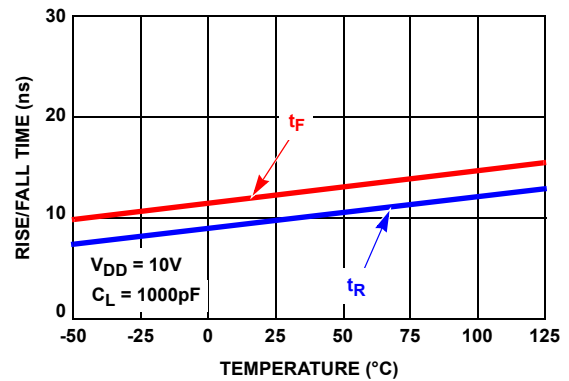


FIGURE 12. RISE/FALL TIME vs TEMPERATURE

**Typical Performance Curves** (Continued)



FIGURE 13. DELAY vs TEMPERATURE

**Revision History**

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
September 3, 2015	FN7285.5	Updated Ordering Information Table on page 2. Added Revision History and About Intersil sections.

**About Intersil**

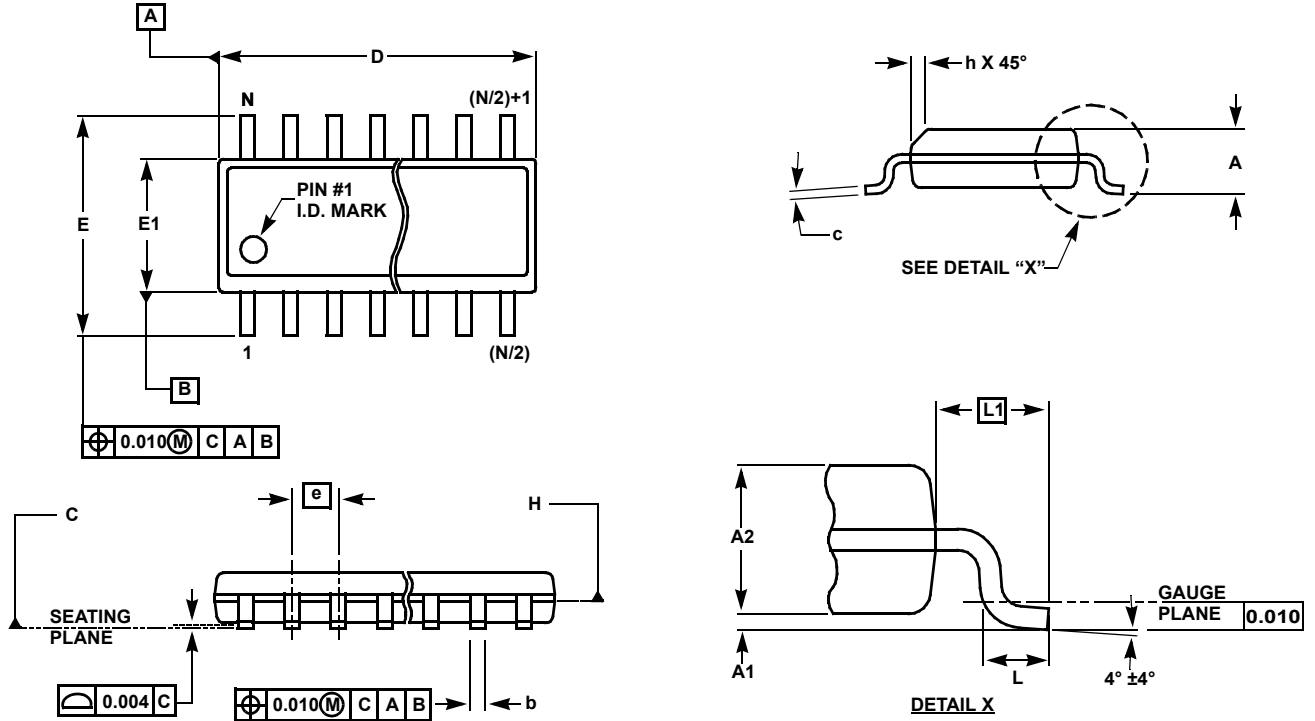
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For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at [www.intersil.com](http://www.intersil.com).

You may report errors or suggestions for improving this datasheet by visiting [www.intersil.com/ask](http://www.intersil.com/ask).

Reliability reports are also available from our website at [www.intersil.com/support](http://www.intersil.com/support)

**Small Outline Package Family (SO)**



**MDP0027**

**SMALL OUTLINE PACKAGE FAMILY (SO)**

SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. M 2/07

**NOTES:**

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994



## Dual-In-Line Plastic Packages (PDIP)



**NOTES:**

- Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
- Dimensioning and tolerancing per ANSI Y14.5M-1982.
- Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
- Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
- D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
- E and  $e_A$  are measured with the leads constrained to be perpendicular to datum  $-C-$ .
- $e_B$  and  $e_C$  are measured at the lead tips with the leads unconstrained.  $e_C$  must be zero or greater.
- B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
- N is the maximum number of terminal positions.
- Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

### E8.3 (JEDEC MS-001-BA ISSUE D) 8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
$e_A$	0.300 BSC		7.62 BSC		6
$e_B$	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

Rev. 0 12/93

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- Поставка образцов и прототипов;
- Техническая поддержка проекта;
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