



Rev. 1.0

# AS7C38096B

## 1024K X 8 BIT HIGH SPEED CMOS SRAM

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### REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	June.2014

### FEATURES

- Fast access time : 10ns
- **Low power consumption:**  
 Operating current:  
   90/80mA (TYP.)  
 Standby current:  
   3mA (TYP.)
- Single 3.3V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage: 1.5V (MIN.)
- **All parts are ROHS Compliant**
- Package : 48-ball 6mm x 8mm TFBGA

### GENERAL DESCRIPTION

The AS7C38096B is a 16M-bit high speed CMOS static random access memory organized as 1,024K words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The AS7C38096B operates from a single power supply of 3.3V and all inputs and outputs are fully TTL compatible

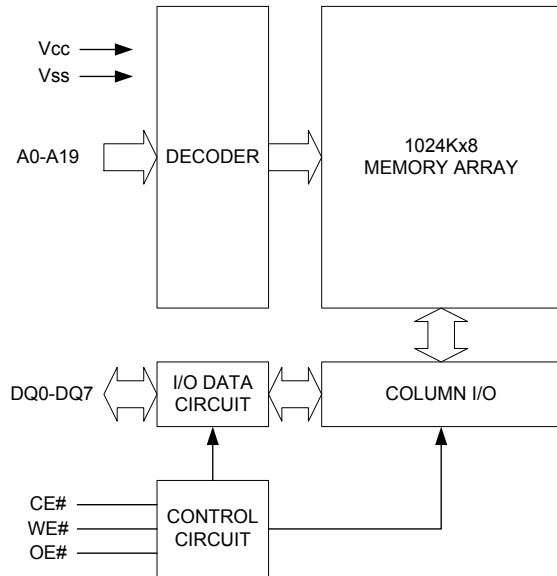
**Table 1. Speed Grade Information**

Product Family	V <sub>CC</sub> Range	Speed	Power Dissipation	
			Standby(I <sub>SB1</sub> , TYP.)	Operating(I <sub>CC</sub> , TYP.)
AS7C38096B	2.7 ~ 3.6V	10ns	3mA	80mA

**Table 2. Ordering Information**

Product part No	Org	Temperature	Package
AS7C38096B-10BIN	1024K x 8	Industrial -40°C to 85°C	48-ball 6mm x 8mm TFBGA

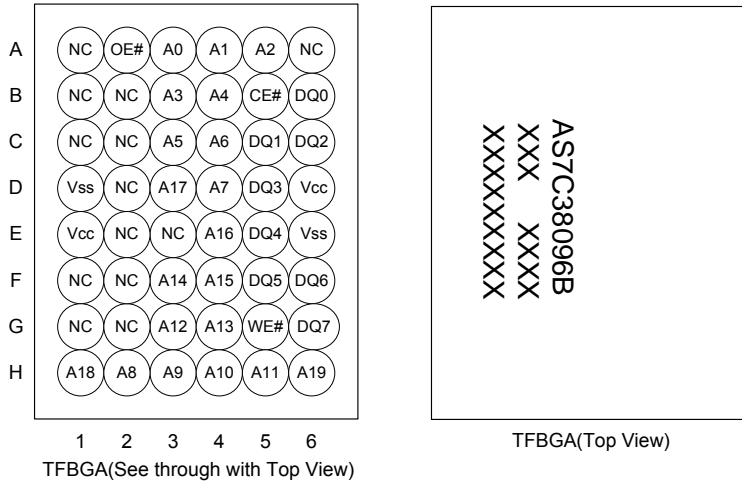
### FUNCTIONAL BLOCK DIAGRAM



### PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 – A19	Address Inputs
DQ0 – DQ7	Data Inputs/Outputs
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
V <sub>CC</sub>	Power Supply
V <sub>SS</sub>	Ground

### PIN CONFIGURATION



### ABSOLUTE MAXIMUM RATINGS\*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on $V_{CC}$ relative to $V_{SS}$	$V_{T1}$	-0.5 to 4.6	V
Voltage on any other pin relative to $V_{SS}$	$V_{T2}$	-0.5 to $V_{CC}+0.5$	V
Operating Temperature	$T_A$	-40 to 85(I grade)	°C
Storage Temperature	$T_{STG}$	-65 to 150	°C
Power Dissipation	$P_D$	1	W
DC Output Current	$I_{OUT}$	50	mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

### TRUTH TABLE

MODE	CE#	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High-Z	$I_{SB1}$
Output Disable	L	H	H	High-Z	$I_{CC}$
Read	L	L	H	$D_{OUT}$	$I_{CC}$
Write	L	X	L	$D_{IN}$	$I_{CC}$

Note: H =  $V_{IH}$ , L =  $V_{IL}$ , X = Don't care.

### DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. <sup>4</sup>	MAX.	UNIT	
Supply Voltage	$V_{CC}$	-10	2.7	3.3	3.6	V	
Input High Voltage	$V_{IH}^{*1}$		2.2	-	$V_{CC}+0.3$	V	
Input Low Voltage	$V_{IL}^{*2}$		- 0.3	-	0.8	V	
Input Leakage Current	$I_{LI}$	$V_{CC} \cong V_{IN} \cong V_{SS}$	- 1	-	1	$\mu A$	
Output Leakage Current	$I_{LO}$	$V_{CC} \cong V_{OUT} \cong V_{SS}$ , Output Disabled	- 1	-	1	$\mu A$	
Output High Voltage	$V_{OH}$	$I_{OH} = -4mA$	2.4	-	-	V	
Output Low Voltage	$V_{OL}$	$I_{OL} = 8mA$	-	-	0.4	V	
Average Operating Power Supply Current	$I_{CC}$	CE# $\leq 0.2$ , Others at 0.2V or $V_{CC}-0.2V$ $I_{I/O} = 0mA; f = max$	-10	-	80	110	mA
Standby Power Supply Current	$I_{SB1}$	CE# $\cong V_{CC} - 0.2V$ , Others at 0.2V or $V_{CC} - 0.2V$	-	4	40	mA	

Notes:

- $V_{IH}(max) = V_{CC} + 2.0V$  for pulse width less than 6ns.
- $V_{IL}(min) = V_{SS} - 2.0V$  for pulse width less than 6ns.
- Over/Undershoot specifications are characterized on engineering evaluation stage, not for mass production test.
- Typical values are included for reference only and are not guaranteed or tested.  
Typical values are measured at  $V_{CC} = V_{CC}(TYP.)$  and  $T_A = 25^\circ C$

### CAPACITANCE ( $T_A = 25^\circ C$ , $f = 1.0MHz$ )

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	$C_{IN}$	-	8	pF
Input/Output Capacitance	$C_{I/O}$	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

### AC TEST CONDITIONS

Speed	10ns
Input Pulse Levels	0.2V to $V_{CC} - 0.2V$
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	$V_{CC}/2$
Output Load	$C_L = 30pF + 1TTL$ , $I_{OH}/I_{OL} = -4mA/8mA$

### AC ELECTRICAL CHARACTERISTICS

#### (1) READ CYCLE

PARAMETER	SYM.	AS7C38096B-10		UNIT
		MIN.	MAX.	
Read Cycle Time	$t_{RC}$	10	-	ns
Address Access Time	$t_{AA}$	-	10	ns
Chip Enable Access Time	$t_{ACE}$	-	10	ns
Output Enable Access Time	$t_{OE}$	-	4.5	ns
Chip Enable to Output in Low-Z	$t_{CLZ}^*$	2	-	ns
Output Enable to Output in Low-Z	$t_{OLZ}^*$	0	-	ns
Chip Disable to Output in High-Z	$t_{CHZ}^*$	-	4	ns
Output Disable to Output in High-Z	$t_{OHZ}^*$	-	4	ns
Output Hold from Address Change	$t_{OH}$	2	-	ns

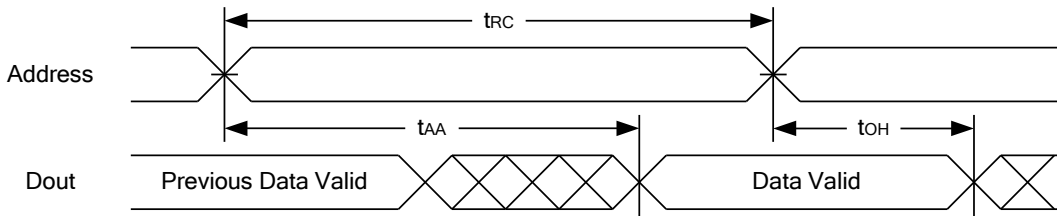
#### (2) WRITE CYCLE

PARAMETER	SYM.	AS7C38096B-10		UNIT
		MIN.	MAX.	
Write Cycle Time	$t_{WC}$	10	-	ns
Address Valid to End of Write	$t_{AW}$	8	-	ns
Chip Enable to End of Write	$t_{CW}$	8	-	ns
Address Set-up Time	$t_{AS}$	0	-	ns
Write Pulse Width	$t_{WP}$	8	-	ns
Write Recovery Time	$t_{WR}$	0	-	ns
Data to Write Time Overlap	$t_{DW}$	6	-	ns
Data Hold from End of Write Time	$t_{DH}$	0	-	ns
Output Active from End of Write	$t_{OW}^*$	2	-	ns
Write to Output in High-Z	$t_{WHZ}^*$	-	4	ns

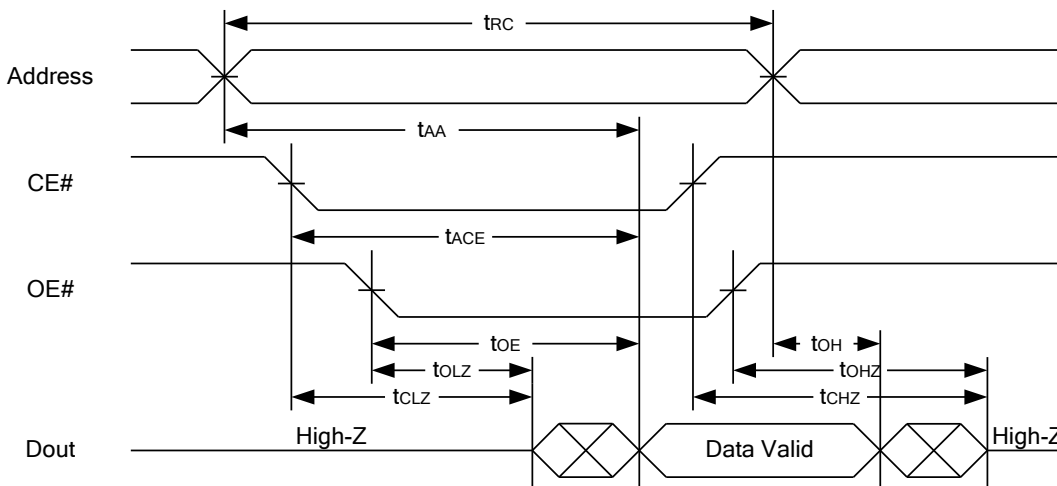
\*These parameters are guaranteed by device characterization, but not production tested.

### TIMING WAVEFORMS

#### READ CYCLE 1 (Address Controlled) (1,2)

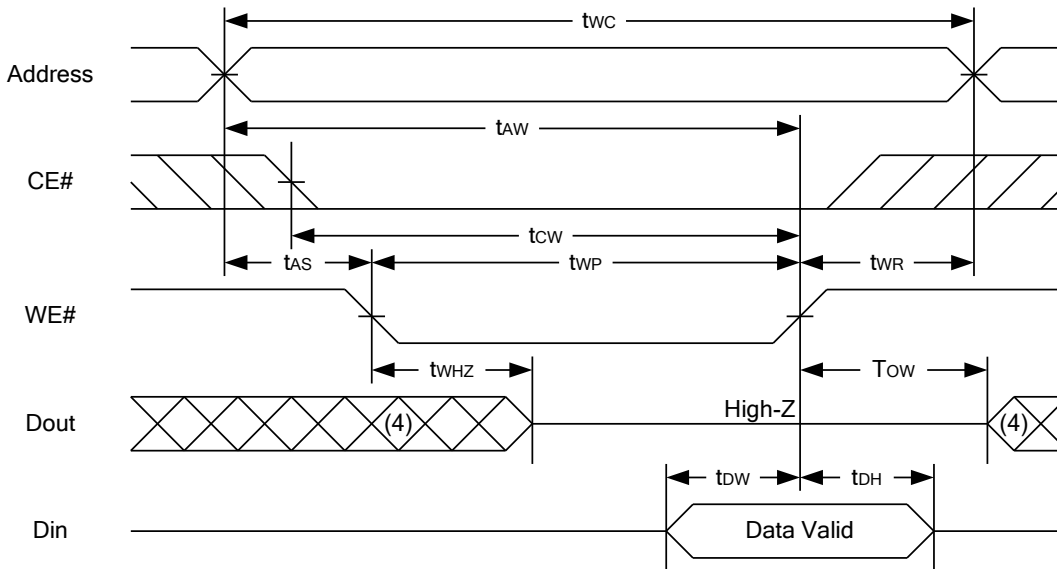
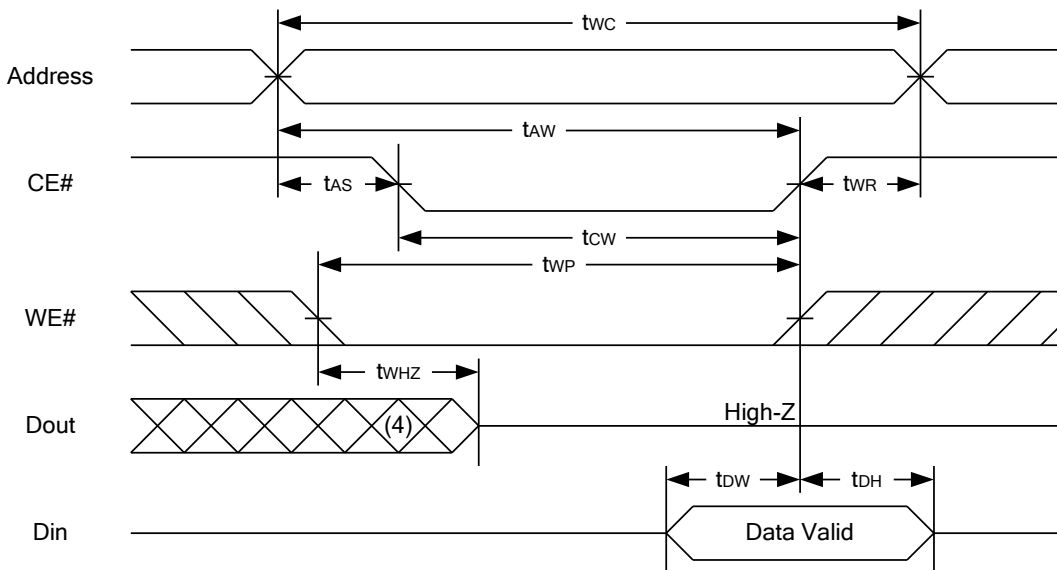


#### READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)



#### Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low.
3. Address must be valid prior to or coincident with CE# = low; otherwise  $t_{AA}$  is the limiting parameter.
4.  $t_{CLZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ}$  and  $t_{OHZ}$  are specified with  $C_L = 5\text{pF}$ . Transition is measured  $\pm 500\text{mV}$  from steady state.
5. At any given temperature and voltage condition,  $t_{CHZ}$  is less than  $t_{CLZ}$ ,  $t_{OHZ}$  is less than  $t_{OLZ}$ .

**WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)**

**WRITE CYCLE 2 (CE# Controlled) (1,2,5,6)**

**Notes :**

1. WE#, CE#, LB#, UB# must be high during all address transitions.
2. A write occurs during the overlap of a low CE#, low WE#, LB# or UB# = low.
3. During a WE# controlled write cycle with OE# low, t<sub>WP</sub> must be greater than t<sub>WHZ</sub> + t<sub>DW</sub> to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE#, LB#, UB# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. t<sub>OW</sub> and t<sub>WHZ</sub> are specified with C<sub>L</sub> = 5pF. Transition is measured ±500mV from steady state.

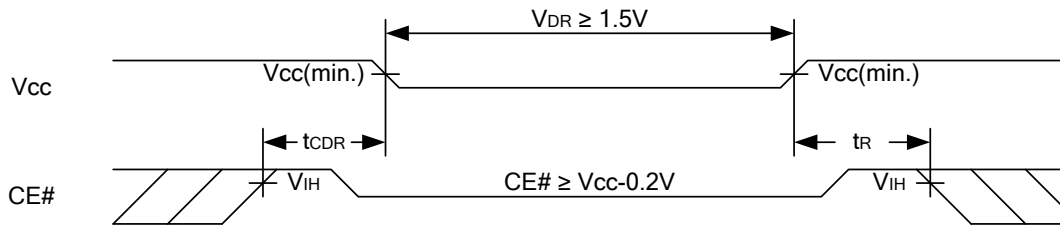


### DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
VCC for Data Retention	$V_{DR}$	$CE\# \geq V_{CC} - 0.2V$	1.5	-	3.6	V
Data Retention Current	$I_{DR}$	$V_{CC} = 1.5V$ $CE\# \geq V_{CC} - 0.2V$ Others at 0.2V or $V_{CC} - 0.2V$	-	3	25	mA
Chip Disable to Data Retention Time	$t_{CDR}$	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	$t_R$		$t_{RC}^*$	-	-	ns

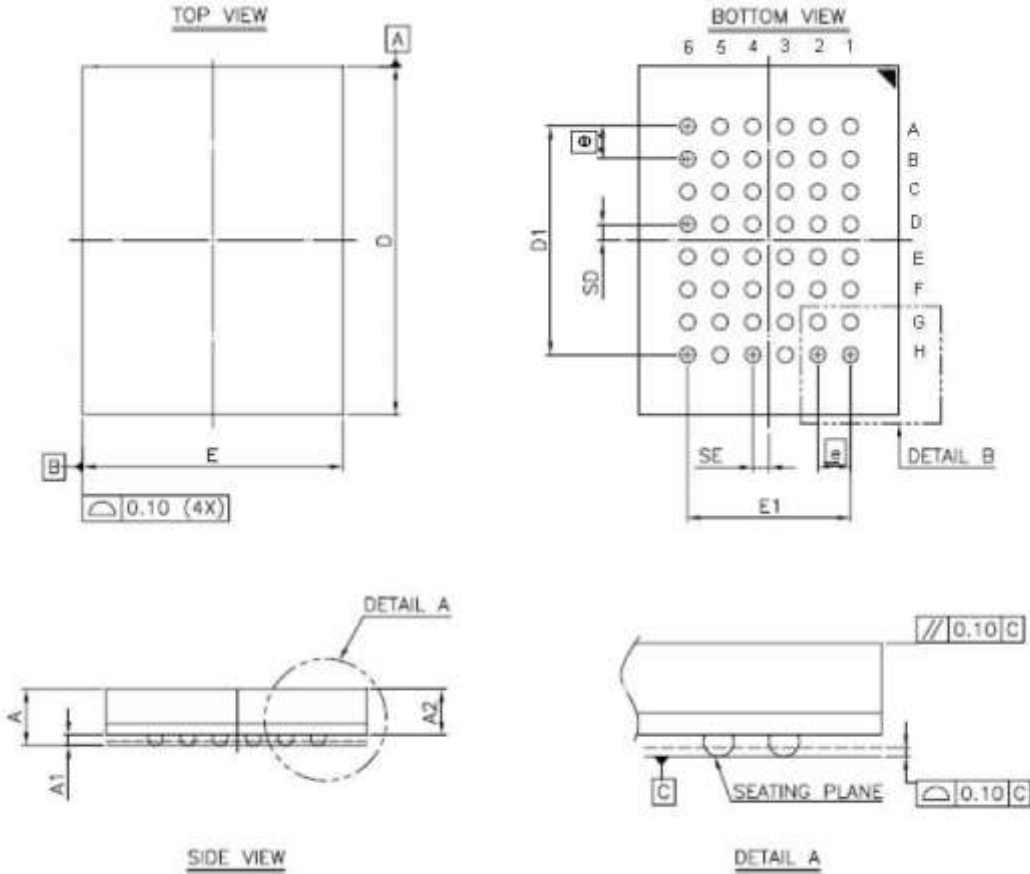
$t_{RC}^*$  = Read Cycle Time

### DATA RETENTION WAVEFORM

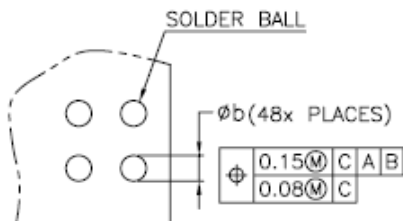


### PACKAGE OUTLINE DIMENSION

#### 48-ball 6mm × 8mm TFBGA Package Outline Dimension



SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.40	—	—	0.055
A1	0.20	0.25	0.30	0.008	0.010	0.012
A2	—	—	1.05	—	—	0.041
b	0.30	0.35	0.40	0.012	0.014	0.016
D	7.95	8.00	8.05	0.313	0.315	0.317
D1	5.25 BSC			0.207 BSC		
E	5.95	6.00	6.05	0.234	0.236	0.238
E1	3.75 BSC			0.148 BSC		
SE	0.375 TYP			0.015 TYP		
SD	0.375 TYP			0.015 TYP		
Ⓢ	0.75 BSC			0.030 BSC		



DETAIL B

## NOTE:

1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.



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## 1024K X 8 BIT HIGH SPEED CMOS SRAM

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