



FEATURES

- Standard 7.0mm x 5.0mm 4-Pad Surface Mount Package
- HCMOS/TTL Compatible Output
- Fundamental and 3rd Overtone Crystal Designs
- Frequency Range 1 – 200 MHz
- Frequency Stability ±50 ppm Standard, ±25 ppm and ±20 ppm Available
- Operating Voltages +5.0Vdc or +3.3Vdc
- Operating Temperature to -40°C to +85°C
- Output Enable Standard
- Tape & Reel Packaging
- **RoHS/Green Compliant (6/6)**



APPLICATIONS

Applications for Model CB3 and CB3LV include digital video, networking equipment, wireless communications, broadband access, Ethernet/Gigabit Ethernet, microprocessors/DSP/FPGA, storage area networks, fiber channel, computers and peripherals, test and measurement, SONET/SDH/DWDM, base stations and Pico cells.

ORDERING INFORMATION



- 1] 6I Stability/Temperature combination is not available.
- 2] These stabilities are not recommended for new designs.
- 3] Frequency is recorded with only leading significant digits before the 'M' and 4 - 6 significant digits after the 'M' (including zeros).
[Ex. 3.579545 MHz, code as 3M579545; 14.31818 MHz, code as 14M31818; 125 MHz, code as 125M0000]
- 4] CTS Distributors may add a -T or -1 at the end of the part number to indicate Tape and Reel packaging.

Not all performance combinations and frequencies may be available.
Contact your local CTS Representative or CTS Customer Service for availability.

PACKAGING INFORMATION [reference]

Device quantity is 1,000 pieces maximum per reel.



ELECTRICAL CHARACTERISTICS

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT | |
|------------------------|---------------------------------|---|----------------------------------|-----|--------------------|-------|-----------------------|
| Maximum Supply Voltage | V _{CC} | - | -0.5 | - | +7.0 | V | |
| Storage Temperature | T _{STG} | - | -40 | - | +100 | °C | |
| Frequency Range | f ₀ | - | 1.5 | - | 107 | MHz | |
| CB3LV | | - | 1.5 | - | 200 | | |
| Frequency Stability | Δf/f ₀ | See Note 1 and Ordering Information | - | - | 20,25,50 or 100 | ± ppm | |
| Aging | Δf | First year | - | 3 | 5 | ± ppm | |
| Operating Temperature | T _A | - | -20 | 25 | +70 | °C | |
| Commercial | | - | -40 | | +85 | | |
| Supply Voltage | V _{CC} | ±10% | 4.5 | 5.0 | 5.5 | V | |
| CB3LV | | | 3.0 | 3.3 | 3.6 | | |
| Supply Current | I _{CC} | Frequency Range | | | | mA | |
| CB3 | | Tested load condition noted for typical values. | | | | | |
| | | 1.5MHz to 20MHz | C _L =50pF | - | 10 | | 25 |
| | | 20.001MHz to 80MHz | C _L =50pF | - | 30 | | 50 |
| CB3LV | | 80.001MHz to 107MHz | C _L =15pF | - | 40 | | 80 |
| | | 1.5MHz to 20MHz | C _L =15pF | - | 7 | | 12 |
| | 20.001MHz to 80MHz | C _L =15pF | - | 20 | 40 | | |
| Output Load | C _L | 80.001MHz to 200MHz | C _L =15pF | - | 30 | pF | |
| | | 1.5MHz to 50MHz | - | - | 50 | | |
| | | 50.001MHz to 80MHz | - | - | 30 | | |
| Output Voltage Levels | V _{OH} | CMOS Load | 90%V _{CC} | - | - | V | |
| | | 10 TTL LOAD | | | | | V _{CC} -0.6V |
| Logic '0' Level | V _{OL} | CMOS | - | - | 10%V _{CC} | 0.4 | |
| | | TTL Load | | | | | |
| Output Current | I _{OH} | V _{OH} = 3.9V/2.2V | - | - | -16/-8 | mA | |
| Logic '1' Level | | V _{CC} = 4.5V/3.0V | | | | | |
| Logic '0' Level | I _{OL} | V _{OL} = 0.4V | - | - | +16/+8 | | |
| Output Duty Cycle | SYM | @ 50% Level | 45 | - | 55 | % | |
| Rise and Fall Time | T _R , T _F | @ 10% - 90% Levels | | | | ns | |
| CB3 | | Tested load condition noted for typical values. | | | | | |
| | | 1.5MHz to 20MHz | C _L =50pF | - | 8 | | 10 |
| | | 20.001MHz to 80MHz | C _L =50pF | - | 5 | | 8 |
| CB3LV | | 80.001MHz to 200MHz | C _L =15pF | - | 2.5 | | 5 |
| | | 1.5MHz to 20MHz | C _L =15pF | - | 6 | | 8 |
| | 20.001MHz to 80MHz | C _L =15pF | - | 3 | 5 | | |
| 80.001MHz to 200MHz | C _L =15pF | - | 1.5 | 3 | | | |
| Start Up Time | T _S | Application of V _{CC} | - | - | 10 | ms | |
| Enable Function | V _{IH} | Pin 1 Logic '1', Output Enabled | 2.0 | - | - | V | |
| Disable Input Voltage | | V _{IL} | Pin 1 Logic '0', Output Disabled | - | - | 0.8 | |
| Enable Time | T _{PLZ} | Pin 1 Logic '1' | - | - | 200 | ns | |
| Standby Current | I _{ST} | Pin 1 Logic '0', Output Disabled | - | - | 10 | μA | |
| Period Jitter, Pk-Pk | - | - | - | - | 50 | | |
| Period Jitter, RMS | - | - | - | - | 5 | ps | |
| Phase Jitter, RMS | - | Bandwidth 12kHz - 20MHz | - | - | 1 | | |

- Notes:
- Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 1st year aging.

ELECTRICAL CHARACTERISTICS

LVC MOS OUTPUT WAVEFORM



TEST CIRCUIT, CMOS LOAD



ENABLE TRUTH TABLE

| PIN 1 | PIN 3 |
|-----------|-----------|
| Logic '1' | Output |
| Open | Output |
| Logic '0' | High Imp. |

D.U.T. PIN ASSIGNMENTS

| PIN | SYMBOL | DESCRIPTION |
|-----|-----------------|--------------------------|
| 1 | EOH | Enable |
| 2 | GND | Circuit & Package Ground |
| 3 | Output | RF Output |
| 4 | V _{CC} | Supply Voltage |

MECHANICAL SPECIFICATIONS

PACKAGE DRAWING



MARKING INFORMATION

- ** – Manufacturing Site Code.
[Note a dash may follow the site code and is acceptable.]
- XXXMXXXXXX – Frequency is marked with only leading significant digits before the 'M' and 4 – 6 digits after the 'M' (including zeros).
Ex. XMXXXXXX [3M579545]
XXMXXXXXX [14M31818]
XXXMXXXXXX [125M0000]
- YYWW – Date code, YY – year, WW – week.
- ST – Frequency stability/temperature code.
[Refer to Ordering Information.]
- V – Voltage code. 3 = 3.3V, 5 = 5.0V.

NOTES

- Termination pads [e4]. Barrier-plating is nickel [Ni] with gold [Au] flash plate.
- Reflow conditions per JEDEC J-STD-020, 260°C maximum.
- Moisture Sensitivity Level 1 per JEDEC J-STD-020.

SUGGESTED SOLDER PAD GEOMETRY

C_{BYPASS} should be ≥ 0.01 uF.





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- Поставка более 17-ти миллионов наименований электронных компонентов;
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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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