

# USB 2.0 Hi-Speed Hub Controller

## PRODUCT FEATURES

Datasheet

### General Description

The SMSC USB251xB/xBi hub is a family of low-power, configurable, MTT (multi transaction translator) hub controller IC products for embedded USB solutions. The *x* in the part number indicates the number of downstream ports available, while the *B* indicates battery charging support. The SMSC hub supports low-speed, full-speed, and hi-speed (if operating as a hi-speed hub) downstream devices on all of the enabled downstream ports.

### Highlights

- High performance, low-power, small footprint hub controller IC with 2, 3, or 4 downstream ports
- Fully compliant with the *USB 2.0 Specification* [1]
- Enhanced OEM configuration options available through either a single serial I<sup>2</sup>C<sup>®</sup> EEPROM, or SMBus slave port
- **MultiTRAK™**
  - High-performance multiple transaction translator which provides one transaction translator per port
- **PortMap**
  - Flexible port mapping and disable sequencing
- **PortSwap**
  - Programmable USB differential-pair pin locations ease PCB design by aligning USB signal lines directly to connectors
- **PHYBoost**
  - Programmable USB signal drive strength for recovering signal integrity using 4-level driving strength resolution

### Features

- USB251xB/xBi products are fully footprint compatible with USB251x/xi/xA/xAi products as direct drop-in replacements
  - Cost savings include using the same PCB components and application of USB-IF Compliance by Similarity
- Full power management with individual or ganged power control of each downstream port
- Fully integrated USB termination and pull-up/pull-down resistors
- Supports a single external 3.3 V supply source; internal regulators provide 1.2 V internal core voltage
- Onboard 24 MHz crystal driver or external 24 MHz clock input
- Customizable vendor ID, product ID, and device ID
- 4 kilovolts of HBM JESD22-A114F ESD protection (powered and unpowered)
- Supports self- or bus-powered operation
- Supports the USB Battery Charging specification Rev. 1.1 for Charging Downstream Ports (CDP)
- The USB251xB/xBi offers the following package:
  - 36-pin QFN (6x6 mm) lead-free RoHS compliant package
- USB251xBi products support the industrial temperature range of -40°C to +85°C
- USB251xB products support the extended commercial temperature range of 0°C to +85°C

### Applications

- LCD monitors and TVs
- Multi-function USB peripherals
- PC motherboards
- Set-top boxes, DVD players, DVR/PVR
- Printers and scanners
- PC media drive bay
- Portable hub boxes
- Mobile PC docking
- Embedded systems

**Order Numbers:**

ORDER NUMBERS*	LEAD-FREE ROHS COMPLIANT PACKAGE	PACKAGE SIZE (MM)	TEMPERATURE RANGE
USB2512B-AEZG USB2513B-AEZC USB2514B-AEZC	36-QFN	6x6x0.5	0°C to 85°C
USB2512Bi-AEZG USB2513Bi-AEZG USB2514Bi-AEZG			-40°C to 85°C

\* Add -TR to the end of any QFN order number to order tape and reel (36-pin packages only). Reel size is 3,000 pieces.

**This product meets the halogen maximum concentration values per IEC61249-2-21**

**For RoHS compliance and environmental information, please visit [www.smSC.com/rohs](http://www.smSC.com/rohs)**

*Please contact your SMSC sales representative for additional documentation related to this product such as application notes, anomaly sheets, and design guidelines.*

## Conventions

Within this manual, the following abbreviations and symbols are used to improve readability.

Example	Description
<b>BIT</b>	Name of a single bit within a field
<b>FIELD.BIT</b>	Name of a single bit (BIT) in FIELD
x...y	Range from x to y, inclusive
<b>BITS[m:n]</b>	Groups of bits from m to n, inclusive
<b>PIN</b>	Pin Name
zzzzb	Binary number (value zzzz)
0xzzz	Hexadecimal number (value zzz)
zzh	Hexadecimal number (value zz)
rsvd	Reserved memory location. Must write 0, read value indeterminate
code	Instruction code, or API function or parameter
<i>Section Name</i>	Section or Document name
x	Don't care
<Parameter>	<> indicate a Parameter is optional or is only used under some conditions
{,Parameter}	Braces indicate Parameter(s) that repeat one or more times
[Parameter]	Brackets indicate a nested Parameter. This Parameter is not real and actually decodes into one or more real parameters.

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## Chapter 1 Overview

The SMSC USB251xB/xBi hub family is a group of low-power, configurable, MTT (multi transaction translator) hub controller ICs. The hub provides downstream ports for embedded USB solutions and is fully compliant with the *USB 2.0 Specification* [1]. Each of the SMSC hub controllers can attach to an upstream port as a full-speed or full-/hi-speed hub. The hub can support low-speed, full-speed, and hi-speed downstream devices when operating as a hi-speed hub.

All required resistors on the USB ports are integrated into the hub. This includes all series termination resistors and all required pull-down and pull-up resistors on D+ and D- pins. The over-current sense inputs for the downstream facing ports have internal pull-up resistors.

The USB251xB/xBi hub family includes programmable features, such as:

- **MultiTRAK™ Technology:** implements a dedicated Transaction Translator (TT) for each port. Dedicated TTs help maintain consistent full-speed data throughput regardless of the number of active downstream connections.
- **PortMap:** provides flexible port mapping and disable sequences. The downstream ports of a USB251xB/xBi hub can be reordered or disabled in any sequence to support multiple platform designs with minimum effort. For any port that is disabled, the USB251xB/xBi hub controller automatically reorders the remaining ports to match the USB host controller's port numbering scheme.
- **PortSwap:** allows direct alignment of USB signals (D+/D-) to connectors to avoid uneven trace length or crossing of the USB differential signals on the PCB.
- **PHYBoost:** enables 4 programmable levels of USB signal drive strength in downstream port transceivers. PHYBoost will also attempt to restore USB signal integrity.

### 1.1 Configurable Features

The SMSC USB251xB/xBi hub controller provides a default configuration that may be sufficient for most applications. Strapping option pins (see [Section 3.3.1 on page 22](#)) provide additional features to enhance the default configuration. When the hub is initialized in the default configuration, the following features may be configured using the strapping options:

- Downstream non-removable ports, where the hub will automatically report as a compound device
- Downstream disabled ports
- Enabling of battery charging option on individual ports

The USB251xB/xBi hub controllers can alternatively be configured by an external I<sup>2</sup>C EEPROM or a microcontroller as an SMBus slave device. When the hub is configured by an I<sup>2</sup>C EEPROM or over SMBus, the following configurable features are provided:

- Support for compound devices on a port-by-port basis
- Selectable over-current sensing and port power control on an individual or ganged basis to match the circuit board component selection
- Customizable vendor ID, product ID, and device ID
- Configurable USB signal drive strength
- Configurable USB differential pair pin location
- Configurable delay time for filtering the over-current sense inputs
- Configurable downstream port power-on time reported to the host
- Indication of the maximum current that the hub consumes from the USB upstream port

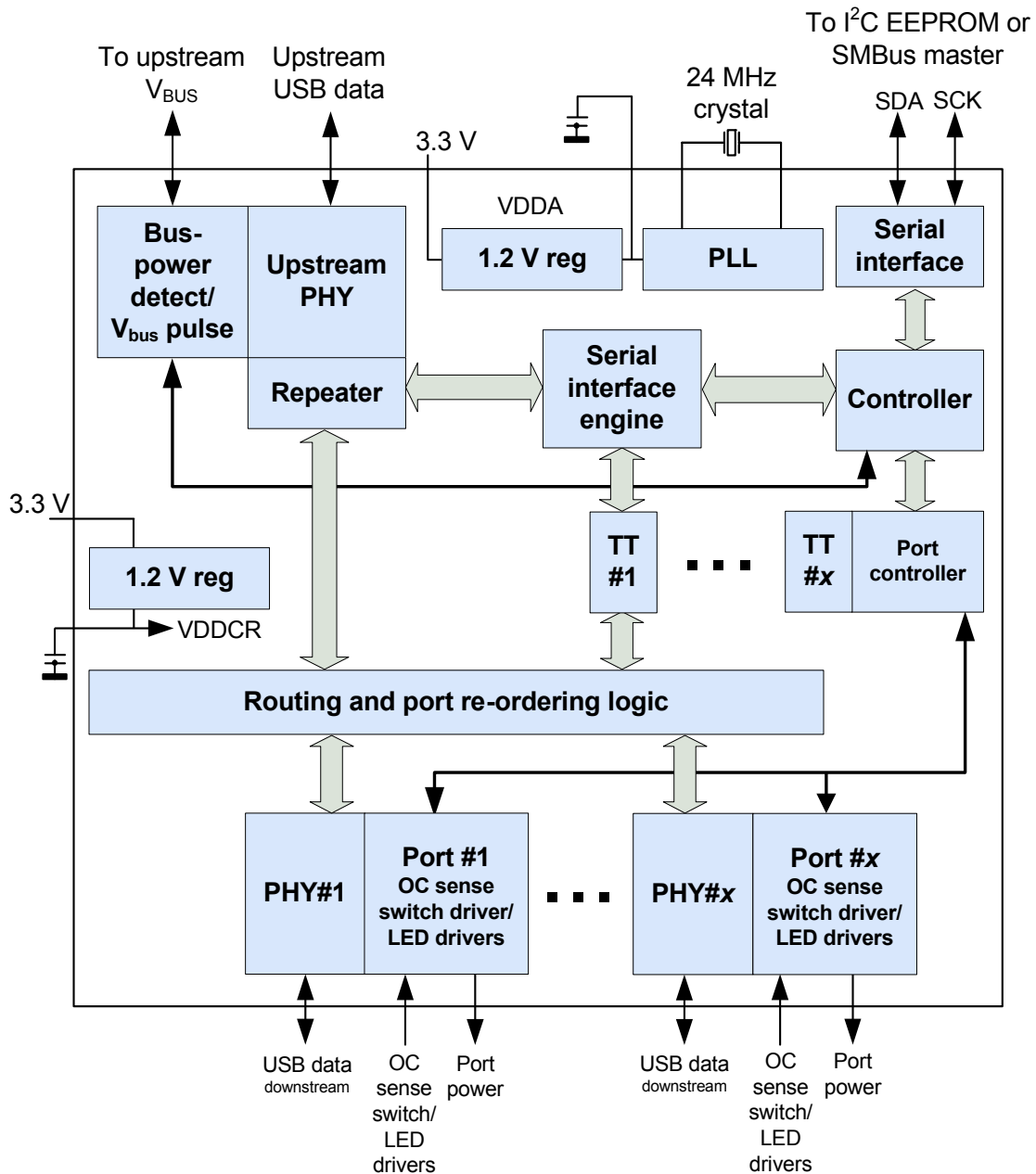


- Indication of the maximum current required for the hub controller
- Custom string descriptors (up to 31 characters):
  - Product
  - Manufacturer
  - Serial number
- Battery charging USB251xB/xBi products are fully footprint compatible with USB251x/xi/xA/xAi products:
  - Pin-compatible
  - Direct drop-in replacement
  - Use the same PCB components
  - USB-IF Compliance by Similarity for ease of use and a complete cost reduction solution
  - Product IDs, device IDs, and other register defaults may differ. See [Section 5.1 on page 27](#) for details.

**Table 1.1 Summary of Compatibilities between USB251xB/xBi and USB251x/xi/xA/xAi Products**

<b>Part Number</b>	<b>Drop-in Replacement</b>
USB2512	USB2512B
USB2512i	USB2512Bi
USB2512A	USB2512B
USB2512Ai	USB2512Bi
USB2513	USB2513B
USB2513i	USB2513Bi
USB2514	USB2514B
USB2514i	USB2514Bi

## Chapter 2 Block Diagram



**x indicates the number of available downstream ports: 2, 3, or 4**

Figure 2.1 USB251xB/xBi Hub Family Block Diagram

## Chapter 3 Pin Information

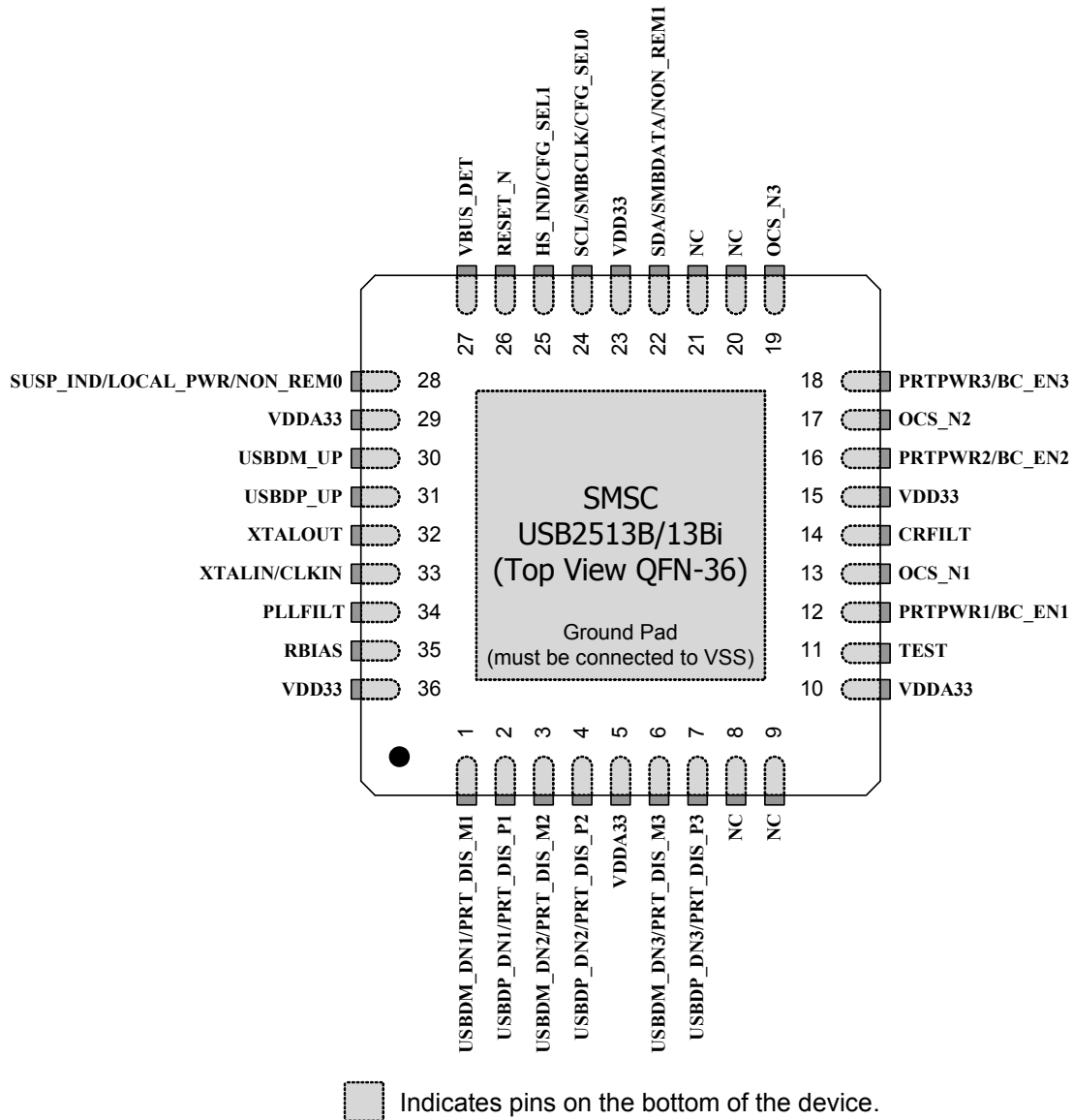
This chapter outlines the pinning configurations for each package type available, followed by a corresponding pin list organized alphabetically. The detailed pin descriptions are listed then outlined by function in [Section 3.3: Pin Descriptions \(Grouped by Function\)](#) on page 19.

### 3.1 Pin Configurations

The following figures detail the pinouts of the various USB251xB/xBi versions.



Figure 3.1 2-Port 36-Pin QFN


**Figure 3.2 3-Port 36-Pin QFN**



 Indicates pins on the bottom of the device.

**Figure 3.3 4-Port 36-Pin QFN**

## 3.2 Pin List (Alphabetical)

**Table 3.1 USB251xB/xBi Pin List (Alphabetical)**

SYMBOL	NAME	PIN NUMBERS		
		36 QFN		
		USB2512B USB2512Bi	USB2513B USB2513Bi	USB2514B USB2514Bi
BC_EN1	Battery Charging Strap Option	12		
BC_EN2		16		
BC_EN3		-	18	
BC_EN4		-		20
CFG_SEL0	Configuration Programming Selection	24		
CFG_SEL1		25		
CLKIN	External Clock Input	33		
CRFILT	Core Regulator Filter Capacitor	14		
Ground Pad	Exposed Pad Tied to Ground (VSS)	ePad		
HS_IND	Hi-Speed Upstream Port Indicator	25		
LOCAL_PWR	Local Power Detection	28		
NC	No Connect	6	-	
NC		7	-	
NC		18	-	
NC		19	-	
NC		8		-
NC		9		-
NC		20		-
NC		21		-
NON_REM0		Non-Removable Port Strap Option	28	
NON_REM1	22			
OCS_N1	Over-Current Sense	13		
OCS_N2		17		
OCS_N3		-	19	
OCS_N4		-		21
PLLFILT		PLL Regulator Filter Capacitor	34	

Table 3.1 USB251xB/xBi Pin List (Alphabetical) (continued)

SYMBOL	NAME	PIN NUMBERS		
		36 QFN		
		USB2512B USB2512Bi	USB2513B USB2513Bi	USB2514B USB2514Bi
PRT_DIS_M1	Downstream Port Disable Strap Option	-	1	
PRT_DIS_M2		3		
PRT_DIS_M3		-	6	
PRT_DIS_M4		-	8	
PRT_DIS_P1	Port Disable	-	2	
PRT_DIS_P2		4		
PRT_DIS_P3		-	7	
PRT_DIS_P4		-	9	
P RTPWR1	USB Port Power Enable	12		
P RTPWR2		16		
P RTPWR3		-	18	
P RTPWR4		-	20	
RBIAS	USB Transceiver Bias	35		
RESET_N	Reset Input	26		
SCL	Serial Clock	24		
SDA	Serial Data Signal	22		
SMBCLK	System Management Bus Clock	24		
SMBDATA	Server Message Block Data Signal	22		
SUSP_IND	Active/Suspend Status Indicator	28		
TEST	Test Pin	11		
USBDM_UP	USB Bus Data	30		
USBDP_UP		31		
USBDM_DN1	Hi-Speed USB Data	1		
USBDM_DN2		3		
USBDM_DN3		-	6	
USBDM_DN4		-	8	
USBDP_DN1		2		
USBDP_DN2		4		
USBDP_DN3		-	7	
USBDP_DN4		-	9	

**Table 3.1 USB251xB/xBi Pin List (Alphabetical) (continued)**

SYMBOL	NAME	PIN NUMBERS		
		36 QFN		
		USB2512B USB2512Bi	USB2513B USB2513Bi	USB2514B USB2514Bi
VBUS_DET	Upstream VBUS Power Detection	27		
VDD33	3.3 V Power	5		
VDD33		10		
VDD33		15		
VDD33		23		
VDD33		29		
VDD33		36		
XTALIN	Crystal Input	33		
XTALOUT	Crystal Output	32		

**Table 3.2 USB251xB/xBi Pin List (Alphabetical)**

SYMBOL	NAME	PIN NUMBERS		
		36 QFN		
		USB2512B USB2512Bi	USB2513B USB2513Bi	USB2514B USB2514Bi
BC_EN1	Battery Charging Strap Option	12		
BC_EN2		16		
BC_EN3		-	18	
BC_EN4		-		20
CFG_SEL0	Configuration Programming Selection	24		
CFG_SEL1		25		
CLKIN	External Clock Input	33		
CRFILT	Core Regulator Filter Capacitor	14		
Ground Pad (VSS)	Exposed Pad Tied to Ground (VSS)	ePad		
HS_IND	Hi-Speed Upstream Port Indicator	25		
LOCAL_PWR	Local Power Detection	28		



Table 3.2 USB251xB/xBi Pin List (Alphabetical) (continued)

SYMBOL	NAME	PIN NUMBERS		
		36 QFN		
		USB2512B USB2512Bi	USB2513B USB2513Bi	USB2514B USB2514Bi
NC	No Connect	6	-	
NC		7	-	
NC		18	-	
NC		19	-	
NC		8		-
NC		9		-
NC		20		-
NC		21		-
NON_REM0	Non-Removable Port Strap Option	28		
NON_REM1		22		
OCS_N1	Over-Current Sense	13		
OCS_N2		17		
OCS_N3		-	19	
OCS_N4		-	21	
PLLFLT	PLL Regulator Filter Capacitor	34		
PRT_DIS_M1	Downstream Port Disable Strap Option	-	1	
PRT_DIS_M2		3		
PRT_DIS_M3		-	6	
PRT_DIS_M4		-	8	
PRT_DIS_P1	Port Disable	-	2	
PRT_DIS_P2		4		
PRT_DIS_P3		-	7	
PRT_DIS_P4		-	9	
PRTPWR1	USB Port Power Enable	12		
PRTPWR2		16		
PRTPWR3		-	18	
PRTPWR4		-	20	
RBIAS	USB Transceiver Bias	35		
RESET_N	Reset Input	26		
SCL	Serial Clock	24		
SDA	Serial Data Signal	22		

**Table 3.2 USB251xB/xBi Pin List (Alphabetical) (continued)**

SYMBOL	NAME	PIN NUMBERS			
		36 QFN			
		USB2512B USB2512Bi	USB2513B USB2513Bi	USB2514B USB2514Bi	
SMBCLK	System Management Bus Clock	24			
SMBDATA	Server Message Block Data Signal	22			
SUSP_IND	Active/Suspend Status Indicator	28			
TEST	Test Pin	11			
USBDM_UP	USB Bus Data	30			
USBDP_UP		31			
USBDM_DN1	Hi-Speed USB Data	1			
USBDM_DN2		3			
USBDM_DN3		-	6		
USBDM_DN4		-	8		
USBDP_DN1		2			
USBDP_DN2		4			
USBDP_DN3		-	7		
USBDP_DN4		-	9		
VBUS_DET		Upstream VBUS Power Detection	27		
VDD33		3.3 V Digital Power	15		
VDD33	23				
VDD33	36				
VDDA33	3.3 V Analog Power	5			
VDDA33		10			
VDDA33		29			
VDDA33		-			
XTALIN	Crystal Input	33			
XTALOUT	Crystal Output	32			

### 3.3 Pin Descriptions (Grouped by Function)

An *N* at the end of a signal name indicates that the active (asserted) state occurs when the signal is at a low voltage level. When the *N* is not present, the signal is asserted when it is at a high voltage level. The terms assertion and negation are used exclusively in order to avoid confusion when working with a mixture of active low and active high signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

**Table 3.3 USB251xB/xBi Pin Descriptions**

SYMBOL	BUFFER TYPE	DESCRIPTION
<b>UPSTREAM USB 2.0 INTERFACES</b>		
<b>USBDM_UP</b> <b>USBDP_UP</b>	IO-U	USB Data: connect to the upstream USB bus data signals (host, port, or upstream hub).
<b>VBUS_DET</b>	I	Detect Upstream VBUS Power: detects the state of the upstream VBUS power. The SMSC hub monitors <b>VBUS_DET</b> to determine when to assert the internal D+ pull-up resistor: (signaling a connect event).  When designing a detachable hub, this pin should be connected to VBUS on the upstream port via a 2:1 voltage divider. Two 100 kΩ resistors are suggested.  For self-powered applications with a permanently attached host, this pin must be connected to a dedicated host control output, or connected to the 3.3 V domain that powers the host (typically <b>VDD33</b> ).
<b>DOWNSTREAM USB 2.0 INTERFACES</b>		
<b>USBDP_DN[x:1]/</b> <b>PRT_DIS_P[x:1]</b>	IO-U	Hi-Speed USB Data: connect to the downstream USB peripheral devices attached to the hub's port. To disable, use a 10 kΩ pull-up resistor to 3.3 V.
<b>USBDM_DN[x:1]/</b> <b>PRT_DIS_M[x:1]</b>		Downstream Port Disable Strap Option: when enabled by package and configuration settings (see <a href="#">Table 5.1 on page 26</a> ), this pin is sampled at <b>RESET_N</b> negation to determine if the port is disabled.  To disable a port, pull up both <b>PRT_DIS_M[x:1]</b> and <b>PRT_DIS_P[x:1]</b> pins for the corresponding port number(s). See <a href="#">Section 3.3.1, on page 22</a> for pull up details.
<b>P RTPWR[x:1]/</b> <b>BC_EN[x:1]</b>	O12	USB Power Enable: enables power to USB peripheral devices downstream.
	IPD	Battery Charging Strap Option: when enabled by package and configuration settings (see <a href="#">Table 5.1</a> ), the pin will be sampled at <b>RESET_N</b> negation to determine if ports [x:1] support the battery charging protocol. When supporting the battery charging protocol, the hub also supports external port power controllers. The battery charging protocol enables a device to draw the currents per the USB battery charging specification. See <a href="#">Section 3.3.1, on page 22</a> for strap pin details.  1 : Battery charging feature is supported for port x 0 : Battery charging feature is not supported for port x
<b>OCS_N[x:1]</b>	IPU	Over-Current Sense: input from external current monitor indicating an over-current condition.
<b>RBIAS</b>	I-R	USB Transceiver Bias: a 12.0 kΩ (+/- 1%) resistor is attached from ground to this pin to set the transceiver's internal bias settings.

**Table 3.3 USB251xB/xBi Pin Descriptions (continued)**

SYMBOL	BUFFER TYPE	DESCRIPTION
<b>SERIAL PORT INTERFACES</b>		
SDA/ SMBDATA/ NON_REM1	I/OSD12	Serial Data Signal
		System Management Bus Signal
		<p>Non-Removable Port 1 Strap Option: when enabled by package and configuration options (see <a href="#">Table 5.1 on page 26</a>), this pin will be sampled (in conjunction with LOCAL_PWR/SUSP_IND/NON_REM0) at RESET_N negation to determine if ports [x:1] contain permanently attached (non-removable) devices:</p> <p>NON_REM[1:0] = 00 : all ports are removable            NON_REM[1:0] = 01 : port 1 is non-removable            NON_REM[1:0] = 10 : ports 1 and 2 are non-removable            NON_REM[1:0] = 11 : when available, ports 1, 2, and 3 are non-removable</p> <p>When NON_REM[1:0] is chosen such that there is a non-removable device, the hub will automatically report itself as a compound device (using the proper descriptors).</p>
RESET_N	IS	RESET Input: the system can reset the chip by driving this input low. The minimum active low pulse is 1 $\mu$ s.
SCL/ SMBCLK/ CFG_SEL0	I/OSD12	Serial Clock (SCL)
		System Management Bus Clock
		Configuration Select: the logic state of this multifunction pin is internally latched on the rising edge of RESET_N (RESET_N negation), and will determine the hub configuration method as described in <a href="#">Table 5.1</a> .
HS_IND/ CFG_SEL1	I/O12	<p>Hi-Speed Upstream Port Indicator: upstream port connection speed.</p> <p>Asserted = the hub is connected at HS            Negated = the hub is connected at FS</p> <p><b>Note:</b> When implementing an external LED on this pin, the active state is indicated above and outlined in <a href="#">Section 3.3.1.3, on page 23</a>.</p>
		Configuration Programming Select 1: the logic state of this pin is internally latched on the rising edge of RESET_N (RESET_N negation), and will determine the hub configuration method as described in <a href="#">Table 5.1</a> .
<b>MISC</b>		
XTALIN	ICLKx	<p>Crystal Input: 24 MHz crystal.</p> <p>This pin connects to either one terminal of the crystal or to an external 24 MHz clock when a crystal is not used.</p>
CLKIN		External Clock Input: this pin connects to either one terminal of the crystal or to an external 24 MHz clock when a crystal is not used.
XTALOUT	OCLKx	Crystal Output: this is the other terminal of the crystal circuit with 1.2 V p-p output and a weak (< 1mA) driving strength. When an external clock source is used to drive XTALIN/CLKIN, leave this pin unconnected, or use with appropriate caution.

Table 3.3 USB251xB/xBi Pin Descriptions (continued)

SYMBOL	BUFFER TYPE	DESCRIPTION
SUSP_IND/  LOCAL_PWR/  NON_REM0	I/O	<p>Active/Suspend Status LED: indicates USB state of the hub. Negated = unconfigured; or configured and in USB suspend Asserted = hub is configured and is active (i.e., not in suspend)</p> <p>Local Power: detects availability of local self-power source. Low = self/local power source is NOT available (i.e., the hub gets all power from the upstream USB VBus) High = self/local power source is available</p> <p>Non-Removable 0 Strap Option: when enabled by package and configuration settings (see <a href="#">Table 5.1 on page 26</a>), this pin will be sampled (in conjunction with NON_REM[1]) at RESET_N negation to determine if ports [x:1] contain permanently attached (non-removable) devices:</p> <p><b>Note:</b> When implementing an external LED on this pin, the active state is outlined below and detailed in <a href="#">Section 3.3.1.3, on page 23</a>.</p> <p>NON_REM[1:0] = 00 : all ports are removable; LED is active high NON_REM[1:0] = 01 : port 1 is non-removable; LED is active low NON_REM[1:0] = 10 : ports 1 and 2 are non-removable; LED is active high NON_REM[1:0] = 11 : (when available) ports 1, 2, and 3 are non-removable; LED is active low</p>
TEST	IPD	Test Pin: treat as a no connect pin or connect to ground. No trace or signal should be routed or attached to this pin.
<b>POWER, GROUND, and NO CONNECTS</b>		
CRFILT		VDD Core Regulator Filter Capacitor: this pin can have up to a 0.1 $\mu$ F low-ESR capacitor to VSS, or be left unconnected.
VDD33		3.3 V Power
PLLFILT		PLL Regulator Filter Capacitor: this pin can have up to a 0.1 $\mu$ F low-ESR capacitor to VSS, or be left unconnected.
VSS		Ground Pad/ePad: the package slug is the only VSS for the device and must be tied to ground with multiple vias.
NC		No Connect: no signal or trace should be routed or attached to all NC pins.

### 3.3.1 Configuring the Strap Pins

If a pin's strap function is enabled through the hub configuration selection, ([Table 5.1: Initial Interface/Configuration Options on page 26](#)) the strap pins must be pulled either high or low using the values provided in [Table 3.4](#). Each strap option is dependent on the pin's buffer type, as outlined in the sections that follow.

**Table 3.4 Strap Option Summary**

STRAP OPTION	RESISTOR VALUE	BUFFER TYPE	NOTES
Non-Removable	47 - 100 k $\Omega$	I/O	
Internal Pull-Down	10 k $\Omega$	IPD	<ul style="list-style-type: none"> <li>■ Only applicable to port power pins</li> <li>■ Contains a built-in resistor</li> </ul>
LED	47 - 100 k $\Omega$	I/O	

#### 3.3.1.1 Non-Removable

If a strap pin's buffer type is I/O, an external pull-up or pull-down must be implemented as shown in [Figure 3.4](#). Use Strap High to set the strap option to 1 and Strap Low to set the strap option to 0. When implementing the Strap Low option, no additional components are needed (i.e., the internal pull-down provides the resistor)



**Figure 3.4 Non-Removable Pin Strap Example**

#### 3.3.1.2 Internal Pull-Down (IPD)

If a strap pin's buffer type is IPD (pins `BC_EN[x:1]`), one of the two hardware configurations outlined below must be implemented. Use the Strap High configuration to set the strap option value to 1 and Strap Low to set the strap option value to 0.



**Figure 3.5 Pin Strap Option with IPD Pin Example**

### 3.3.1.3 LED

If a strap pin's buffer type is I/O and shares functionality with an LED, the hardware configuration outlined below must be implemented. The internal logic will drive the LED appropriately (active high or low) depending on the sampled strap option. Use the Strap High configuration to set the strap option value to 1 and Strap Low to set the strap option to 0.

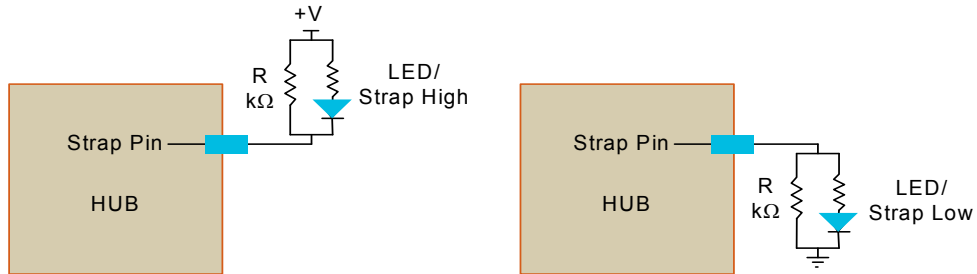


Figure 3.6 LED Pin Strap Example

## 3.4 Buffer Type Descriptions

Table 3.5 Buffer Type Descriptions

BUFFER TYPE	DESCRIPTION
I	Input
I/O	Input/output
IPD	Input with internal weak pull-down resistor
IPU	Input with internal weak pull-up resistor
IS	Input with Schmitt trigger
O12	Output 12 mA
I/O12	Input/output buffer with 12 mA sink and 12 mA source
I/OSD12	Open drain with Schmitt trigger and 12 mA sink. Meets the I <sup>2</sup> C-Bus Specification [2] requirements.
ICLKx	XTAL clock input
OCLKx	XTAL clock output
I-R	RBIAS
I/O-U	Analog input/output defined in USB specification

## Chapter 4 Battery Charging Support

The USB251xB/xBi SMSC hub provides support for battery charging devices on a per port basis in compliance with the *USB Battery Charging Specification, Revision 1.1*. The hub can be configured to individually enable each downstream port for battery charging support either via pin strapping as illustrated in Figure 4.1 or by setting the corresponding configuration bits via I<sup>2</sup>C EEPROM or SMBus (Section 5.1 on page 27).



**Figure 4.1 Battery Charging via External Power Supply**

**Note:** R<sub>STRAP</sub> enables battery charging.

### 4.1 USB Battery Charging

A downstream port enabled for battery charging turns on port power as soon as the power on reset and hardware configuration process has completed. The hub does not need to be enumerated nor does VBUS\_DET need to be asserted for the port power to be enabled. These conditions allow battery charging in S3, S4, and S5 system power states as well as in the fully operational state. The *USB Battery Charging Specification* does not interfere with standard USB operation, which allows a device to perform battery charging at any time.

A port that supports battery charging must be able to support 1.5 amps of current on VBUS. Standard USB port power controllers typically only allow for 0.8 amps of current before detecting an over-current condition. Therefore, the 5 volt power supply, port power controller, or over-current protection devices must be chosen to handle the larger current demand compared to standard USB hub designs.

#### 4.1.1 Special Behavior of PRT PWR Pins

The USB251xB/xBi enables VBUS by asserting the port power (PRT PWR) as soon as the hardware configuration process has completed. If the port detects an over-current condition, PRT PWR will be turned off to protect the circuitry from overloading. If an over-current condition is detected when the hub is not enumerated, PRT PWR can only be turned on from the host or if RESET\_N is toggled. These



behaviors provide battery charging even when the hub is not enumerated and protect the hub from sustained short circuit conditions. If the short circuit condition persists when the hub is plugged into a host system the user is notified that a port has an over-current condition. Otherwise **PRT\_PWR** turned on by the host system and the ports operate normally.

## 4.2 Battery Charging Configuration

The battery charging option can be configured in one of two ways:

- When the hub is brought up in the default configuration with strapping options enabled, with the **PRT\_PWR[x:1]/BC\_EN[x:1]** pins configured. See the following sections for details:
  - [Section 3.3: Pin Descriptions \(Grouped by Function\) on page 19](#)
  - [Section 3.3.1.2: Internal Pull-Down \(IPD\) on page 22](#)
- When the hub is initialized for configuration over I<sup>2</sup>C EEPROM or SMBus. Either of these interfaces can be used to configure the battery charging option.

### 4.2.1 Battery Charging enabled via I<sup>2</sup>C EEPROM or SMBus

Register memory map location 0xD0 is allocated for battery charging support. The Battery Charging register at location 0xD0 starting from bit 1 enables battery charging for each downstream port when asserted. Bit 1 represents port 1, bit 2 represents port 2, etc. Each port with battery charging enabled asserts the corresponding **PRT\_PWR[x:1]** pin.

## Chapter 5 Initial Interface/Configuration Options

The hub must be configured in order to correctly function when attached to a USB host controller. The hub can be configured either internally or externally by setting the **CFG\_SEL[1:0]** pins (immediately after **RESET\_N** negation) as outlined in the table below.

**Note:** See Chapter 11 (Hub Specification) of the USB specification for general details regarding hub operation and functionality.

To configure the hub externally, there are two principal ways to interface to the hub: over SMBus or I<sup>2</sup>C EEPROM. The hub can be configured internally, where several default configurations are available as described in the table below. When configured internally, additional configuration is available using the strap options (listed in [Section 3.3.1 on page 22](#)).

**Note:** Strap options are not available when configuring the hub over I<sup>2</sup>C or SMBus.

**Table 5.1 Initial Interface/Configuration Options**

CFG_SEL[1]	CFG_SEL[0]	DESCRIPTION
0	0	Default configuration: <ul style="list-style-type: none"> <li>■ Strap options enabled</li> <li>■ Self-powered operation enabled</li> <li>■ Individual power switching</li> <li>■ Individual over-current sensing</li> </ul>
0	1	The hub is configured externally over SMBus (as an SMBus slave device): <ul style="list-style-type: none"> <li>■ Strap options disabled</li> <li>■ All registers configured over SMBus</li> </ul>
1	0	Default configuration with the following overrides: <ul style="list-style-type: none"> <li>■ Bus-powered operation</li> </ul>
1	1	The hub is configured over 2-wire I <sup>2</sup> C EEPROM: <ul style="list-style-type: none"> <li>■ Strap options disabled</li> <li>■ All registers configured by I<sup>2</sup>C EEPROM</li> </ul>

## 5.1 Internal Register Set (Common to I<sup>2</sup>C EEPROM and SMBus)

The register set available when configuring the hub to interface over I<sup>2</sup>C or SMBus is outlined in the table below. Each register has R/W capability, where EEPROM reset values are 0x00. Reserved registers should be written to 0 unless otherwise specified. Contents read from unavailable registers should be ignored.

ADDRESS	REGISTER NAME	DEFAULT ROM VALUES (HEXIDECIMAL)		
		USB2512B/12Bi	USB2513B/13Bi	USB2514B/14Bi
00h	Vendor ID LSB	24		
01h	Vendor ID MSB	04		
02h	Product ID LSB	12	13	14
03h	Product ID MSB	25		
04h	Device ID LSB	B3		
05h	Device ID MSB	0B		
06h	Configuration Data Byte 1	9B		
07h	Configuration Data Byte 2	20		
08h	Configuration Data Byte 3	02		
09h	Non-Removable Devices	00		
0Ah	Port Disable (Self)	00		
0Bh	Port Disable (Bus)	00		
0Ch	Max Power (Self)	01		
0Dh	Max Power (Bus)	32		
0Eh	Hub Controller Max Current (Self)	01		
0Fh	Hub Controller Max Current (Bus)	32		
10h	Power-on Time	32		
11h	Language ID High	00		
12h	Language ID Low	00		
13h	Manufacturer String Length	00		
14h	Product String Length	00		
15h	Serial String Length	00		
16h-53h	Manufacturer String	00		

ADDRESS	REGISTER NAME	DEFAULT ROM VALUES (HEXIDECIMAL)		
		USB2512B/12Bi	USB2513B/13Bi	USB2514B/14Bi
54h-91h	Product String	00		
92h-CFh	Serial String	00		
D0h	Battery Charging Enable	00		
E0h	rsvd	00		
F5h	rsvd	00		
F6h	Boost_Up	00		
F7h	rsvd	00		
F8h	Boost_x:0	00		
F9h	rsvd	00		
FAh	Port Swap	00		
FBh	Port Map 12	00		
FCh	Port Map 34	-	00	
FD-FEh	rsvd	00		
FFh	Status/Command Note: SMBus register only	00		

### 5.1.1 Register 00h: Vendor ID (LSB)

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	VID_LSB	Least Significant Byte of the Vendor ID: a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB-Interface Forum). Set this field using either the SMBus or I <sup>2</sup> C EEPROM interface options.

### 5.1.2 Register 01h: Vendor ID (MSB)

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	VID_MSB	Most Significant Byte of the Vendor ID: a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB-Interface Forum). Set this field using either the SMBus or I <sup>2</sup> C EEPROM interface options.

### 5.1.3 Register 02h: Product ID (LSB)

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	PID_LSB	Least Significant Byte of the Product ID: a 16-bit value that uniquely identifies the Product ID of the user device. Set this field using either the SMBus or I <sup>2</sup> C EEPROM interface options.

### 5.1.4 Register 03h: Product ID (MSB)

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	PID_MSB	Most Significant Byte of the Product ID: a 16-bit value that uniquely identifies the Product ID of the user device. Set this field using either the SMBus or I <sup>2</sup> C EEPROM interface options.

### 5.1.5 Register 04h: Device ID (LSB)

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	DID_LSB	Least Significant Byte of the Device ID: a 16-bit device release number in BCD format (assigned by OEM). Set this field using either the SMBus or I <sup>2</sup> C EEPROM interface options.

### 5.1.6 Register 05h: Device ID (MSB)

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	DID_MSB	Most Significant Byte of the Device ID: a 16-bit device release number in BCD format (assigned by OEM). Set this field using either the SMBus or I <sup>2</sup> C EEPROM interface options.

### 5.1.7 Register 06h: CONFIG\_BYTE\_1

BIT NUMBER	BIT NAME	DESCRIPTION
7	SELF_BUS_PWR	<p>Self or Bus Power: selects between self- and bus-powered operation.</p> <p>The hub is either self-powered (draws less than 2 mA of upstream bus power) or bus-powered (limited to a 100 mA maximum of upstream power prior to being configured by the host controller).</p> <p>When configured as a bus-powered device, the SMSC hub consumes less than 100 mA of current prior to being configured. After configuration, the bus-powered SMSC hub, along with all associated hub circuitry, any embedded devices (if part of a compound device), and all externally available downstream ports (max 100 mA) must consume no more than 500 mA of upstream VBUS current. The current consumption is system dependent and must not violate the <i>USB 2.0 Specification</i> [1].</p> <p>When configured as a self-powered device, &lt; 1 mA of upstream VBUS current is consumed and all ports are available. Each port is capable of sourcing 500 mA of current.</p> <p>This field is set over either the SMBus or I<sup>2</sup>C EEPROM interface options.</p> <p>0 : bus-powered operation 1 : self-powered operation</p> <p>If dynamic power switching is enabled (<a href="#">Section 5.1.8</a>), this bit is ignored and LOCAL_PWR is used to determine if the hub is operating from self or bus power.</p>
6	rsvd	
5	HS_DISABLE	<p>Hi-Speed Disable: disables the capability to attach as either a hi- or full-speed device, forcing full-speed attachment only (i.e., no hi-speed support).</p> <p>0 : hi-/full-speed 1 : full-speed only (hi-speed disabled)</p>
4	MTT_ENABLE	<p>Multi-TT Enable: enables one transaction translator per port operation.</p> <p>Selects between a mode where only one transaction translator is available for all ports (single-TT), or each port gets a dedicated transaction translator (multi-TT).</p> <p>0 : single TT for all ports 1 : multi-TT (one TT per port)</p>
3	EOP_DISABLE	<p>EOP Disable: disables End Of Packet (EOP) generation at End Of Frame Time #1 (EOF1) when in full-speed mode.</p> <p>During full-speed operation only, the hub can send EOP when no downstream traffic is detected at EOF1. See the <i>USB 2.0 Specification, Section 11.3.1</i> for details.</p> <p>0 : EOP generation is normal 1 : EOP generation is disabled</p>
2:1	CURRENT_SNS	<p>Over-Current Sense: selects current sensing on all ports (ganged); a port-by-port basis (individual); or none (for bus-powered hubs only). The ability to support current sensing on a ganged or port-by-port basis is hardware implementation dependent.</p> <p>00 : ganged sensing 01 : individual sensing 1x : over-current sensing not supported (use with bus-powered configurations)</p>

BIT NUMBER	BIT NAME	DESCRIPTION
0	PORT_PWR	<p>Port Power Switching: enables power switching on all ports (ganged) or a port-by-port basis (individual). The ability to support power enabling on a ganged or port-by-port basis is hardware implementation dependent.</p> <p>0 : ganged switching 1 : individual switching</p>

### 5.1.8 Register 07h: Configuration Data Byte 2

BIT NUMBER	BIT NAME	DESCRIPTION
7	DYNAMIC	<p>Dynamic Power Enable: controls the ability of the hub to automatically change from self-powered to bus-powered operation if the local power source is removed or unavailable. It can also go from bus-powered to self-powered operation if the local power source is restored.</p> <p>When dynamic power switching is enabled, the hub detects the availability of a local power source by monitoring <b>LOCAL_PWR</b>. If the hub detects a change in power source availability, the hub immediately disconnects and removes power from all downstream devices. It also disconnects the upstream port. The hub will then re-attach to the upstream port as either a bus-powered hub (if local power is unavailable) or a self-powered hub (if local power is available).</p> <p>0 : no dynamic auto-switching 1 : dynamic auto-switching capable</p>
6	rsvd	
5:4	OC_TIMER	<p>Over Current Timer Delay:</p> <p>00 : 0.1 ms 01 : 4.0 ms 10 : 8.0 ms 11 : 16.0 ms</p>
3	COMPOUND	<p>Compound Device: indicates the hub is part of a compound device (see the <i>USB Specification</i> for definition). The applicable port(s) must also be defined as having a non-removable device.</p> <p><b>Note:</b> When configured via strapping options, declaring a port as non-removable automatically causes the hub controller to report that it is part of a compound device.</p> <p>0 : no 1 : yes, the hub is part of a compound device</p>
2:0	rsvd	

### 5.1.9 Register 08h: Configuration Data Byte 3

BIT NUMBER	BIT NAME	DESCRIPTION
7:4	rsvd	
3	PRTMAP_EN	Port Mapping Enable: selects the method used by the hub to assign port numbers and disable ports. 0 : standard mode 1 : port mapping mode
2:1	rsvd	
0	STRING_EN	Enables String Descriptor Support 0 : string support disabled 1 : string support enabled

### 5.1.10 Register 09h: Non-Removable Device

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	NR_DEVICE	Non-Removable Device: indicates which port has a non-removable device. 0 : port is removable 1 : port is non-removable  Bit 7 : rsvd Bit 6 : rsvd Bit 5 : rsvd Bit 4 : controls port 4 Bit 3 : controls port 3 Bit 2 : controls port 2 Bit 1 : controls port 1 Bit 0 : rsvd  <b>Note:</b> The device must provide its own descriptor data. When using the default configuration, the <b>NON_REM[1:0]</b> pins will designate the appropriate ports as being non-removable.



### 5.1.11 Register 0Ah: Port Disable For Self-Powered Operation

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	PORT_DIS_SP	<p>Port Disable Self-Powered: disables one or more ports.</p> <p>0 = port is available 1 = port is disabled</p> <p>Bit 7 : rsvd Bit 6 : rsvd Bit 5 : rsvd Bit 4 : controls port 4 Bit 3 : controls port 3 Bit 2 : controls port 2 Bit 1 : controls port 1 Bit 0 : rsvd</p> <p>During self-powered operation when mapping mode is disabled (<b>PRTMAP_EN</b> = 0), this register selects the ports that will be permanently disabled. These ports are then unavailable and cannot be enabled or enumerated by a host controller. The ports can be disabled in any order, where the internal logic will automatically report the correct number of enabled ports to the USB host. The active ports will be reordered in order to ensure proper function.</p> <p>When using the default configuration, <b>PRT_DIS_P[x:1]</b> and <b>PRT_DIS_M[x:1]</b> pins disable the appropriate ports.</p>

### 5.1.12 Register 0Bh: Port Disable For Bus-Powered Operation

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	PORT_DIS_BP	<p>Port Disable Bus-Powered: disables one or more ports.</p> <p>0 = port is available 1 = port is disabled</p> <p>Bit 7 : rsvd Bit 6 : rsvd Bit 5 : rsvd Bit 4 : controls port 4 Bit 3 : controls port 3 Bit 2 : controls port 2 Bit 1 : controls port 1 Bit 0 : rsvd</p> <p>During self-powered operation when mapping mode is disabled (<b>PRTMAP_EN</b> = 0), this selects the ports which will be permanently disabled. These ports are then unavailable and cannot be enabled or enumerated by a host controller. The ports can be disabled in any order, where the internal logic will automatically report the correct number of enabled ports to the USB host. The active ports will be reordered in order to ensure proper function.</p> <p>When using the internal default option, the <b>PRT_DIS_P[x:1]</b> and <b>PRT_DIS_M[x:1]</b> pins disable the appropriate ports.</p>

### 5.1.13 Register 0Ch: Max Power For Self-Powered Operation

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	MAX_PWR_SP	<p>Max Power Self-Powered: the value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device. The embedded peripheral reports 0 mA in its descriptors.</p> <p><b>Note:</b> The <i>USB 2.0 Specification</i> does not permit this value to exceed 100 mA</p>

### 5.1.14 Register 0Dh: Max Power For Bus-Powered Operation

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	MAX_PWR_BP	<p>Max Power Bus-Powered: the value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a bus-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device. The embedded peripheral reports 0 mA in its descriptors.</p>

### 5.1.15 Register 0Eh: Hub Controller Max Current For Self-Powered Operation

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	HC_MAX_C_SP	<p>Hub Controller Max Current Self-Powered: the value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value does NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device.</p> <p><b>Note:</b> The <i>USB 2.0 Specification</i> does not permit this value to exceed 100 mA</p> <p>A value of 50 (decimal) indicates 100 mA, which is the default value.</p>

### 5.1.16 Register 0Fh: Hub Controller Max Current For Bus-Powered Operation

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	HC_MAX_C_BP	<p>Hub Controller Max Current Bus-Powered: the value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a bus-powered hub. This value will include the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board.</p> <p><b>Note:</b> This value will not include the power consumption of a permanently attached peripheral if the hub is configured as a compound device. A value of 50 (decimal) would indicate 100 mA, which is the default value.</p>

### 5.1.17 Register 10h: Power-On Time

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	POWER_ON_TIME	Power-On Time: the length of time that it takes (in 2 ms intervals) from the time the host initiated the power-on sequence on a port until the port has adequate power.

### 5.1.18 Register 11h: Language ID High

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	LANG_ID_H	USB Language ID: upper 8 bits of a 16-bit ID field

### 5.1.19 Register 12h: Language ID Low

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	LANG_ID_L	USB Language ID: lower 8 bits of a 16-bit ID field

### 5.1.20 Register 13h: Manufacturer String Length

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	MFR_STR_LEN	Manufacturer String Length: with a maximum string length of 31 characters (when supported).

### 5.1.21 Register 14h: Product String Length

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	PRD_STR_LEN	Product String Length: with a maximum string length of 31 characters (when supported).

### 5.1.22 Register 15h: Serial String Length

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	SER_STR_LEN	Serial String Length: with a maximum string length of 31 characters (when supported).

### 5.1.23 Register 16h-53h: Manufacturer String

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	MFR_STR	<p>Manufacturer String: UNICODE UTF-16LE per <i>USB 2.0 Specification</i>: with a maximum string length of 31 characters (when supported).</p> <p><b>Note:</b> The string consists of individual 16-bit UNICODE UTF-16LE characters. The characters will be stored starting with the LSB at the least significant address and the MSB at the next 8-bit location. (Subsequent characters must be stored in sequential contiguous addresses in the same LSB, MSB manner.)</p> <p><b>Warning:</b> Close attention to the byte order of the selected programming tool should be monitored.</p>

### 5.1.24 Register 54h-91h: Product String

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	PRD_STR	<p>Product String: UNICODE UTF-16LE per <i>USB 2.0 Specification</i></p> <p>When supported, the maximum string length is 31 characters (62 bytes).</p> <p><b>Note:</b> The string consists of individual 16-bit UNICODE UTF-16LE characters. The characters will be stored starting with the LSB at the least significant address and the MSB at the next 8-bit location. (Subsequent characters must be stored in sequential contiguous address in the same LSB, MSB manner.)</p> <p><b>Warning:</b> Close attention to the byte order of the selected programming tool should be monitored.</p>

### 5.1.25 Register 92h-CFh: Serial String

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	SER_STR	<p>Serial String: UNICODE UTF-16LE per USB 2.0 specification</p> <p>When supported, the maximum string length is 31 characters (62 bytes).</p> <p><b>Note:</b> The string consists of individual 16-bit UNICODE UTF-16LE characters. The characters will be stored starting with the LSB at the least significant address and the MSB at the next 8-bit location. (Subsequent characters must be stored in sequential contiguous address in the same LSB, MSB manner.)</p> <p><b>Warning:</b> Close attention to the byte order of the selected programming tool should be monitored.</p>

### 5.1.26 Register D0h: Battery Charging Enable

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	BC_EN	<p>Battery Charging Enable: enables the battery charging feature for the corresponding port.</p> <p>0 : battery charging support is not enabled 1 : battery charging support is enabled</p> <p>Bit 7 : rsvd Bit 6 : rsvd Bit 5 : rsvd Bit 4 : controls port 4 Bit 3 : controls port 3 Bit 2 : controls port 2 Bit 1 : controls port 1 Bit 0 : rsvd</p>

### 5.1.27 Register F6h: Boost\_Up

BIT NUMBER	BIT NAME	DESCRIPTION
7:2	rsvd	
1:0	BOOST_IOUT	<p>USB electrical signaling drive strength boost bit for the upstream port.</p> <p>00 : normal electrical drive strength - no boost 01 : elevated electrical drive strength - low (~ 4% boost) 10 : elevated electrical drive strength - medium (~ 8% boost) 11 : elevated electrical drive strength - high (~12% boost)</p> <p><b>Note:</b> Boost could result in non-USB compliant parameters. Therefore, a value of 00 should be implemented unless specific implementation issues require additional signal boosting to correct for degraded USB signalling levels.</p>

### 5.1.28 Register F8h: Boost\_4:0

BIT NUMBER	BIT NAME	DESCRIPTION
7:6	BOOST_IOUT_4	USB electrical signaling drive strength boost bit for downstream port 4. 00 : normal electrical drive strength - no boost 01 : elevated electrical drive strength - low (~4% boost) 10 : elevated electrical drive strength - medium (~ 8% boost) 11 : elevated electrical drive strength - high (~12% boost)
5:4	BOOST_IOUT_3	USB electrical signaling drive strength boost bit for downstream port 3. 00 : normal electrical drive strength - no boost 01 : elevated electrical drive strength - low (~4% boost) 10 : elevated electrical drive strength - medium (~ 8% boost) 11 : elevated electrical drive strength - high (~12% boost)
3:2	BOOST_IOUT_2	USB electrical signaling drive strength boost bit for downstream port 2. 00 : normal electrical drive strength - no boost 01 : elevated electrical drive strength - low (~4% boost) 10 : elevated electrical drive strength - medium (~ 8% boost) 11 : elevated electrical drive strength - high (~12% boost)
1:0	BOOST_IOUT_1	USB electrical signaling drive strength boost bit for downstream port 1. 00 : normal electrical drive strength - no boost 01 : elevated electrical drive strength - low (~4% boost) 10 : elevated electrical drive strength - medium (~ 8% boost) 11 : elevated electrical drive strength - high (~12% boost)

**Note:** Boost could result in non-USB compliant parameters. Therefore, a value of 00 should be implemented unless specific implementation issues require additional signal boosting to correct for degraded USB signalling levels.

### 5.1.29 Register FAh: Port Swap

BIT NUMBER	BIT NAME	DESCRIPTION
7:0	PRTSP	Port Swap: swaps the upstream USBDP/USBDM pins ( <b>USBDP_UP</b> and <b>USBDM_UP</b> ) and the downstream USBDP/USBDM pins ( <b>USBDP_DN[x:1]</b> and <b>USBDM_DN[x:1]</b> ) for ease of board routing to devices and connectors. 0 : USB D+ functionality is associated with the DP pin and D- functionality is associated with the DM pin. 1 : USB D+ functionality is associated with the DM pin and D- functionality is associated with the DP pin. Bit 7 : rsvd Bit 6 : rsvd Bit 5 : rsvd Bit 4 : controls port 4 Bit 3 : controls port 3 Bit 2 : controls port 2 Bit 1 : controls port 1 Bit 0 : when set to 1, the upstream port DP/DM is swapped.



### 5.1.30 Register FBh: PortMap 12

BIT NUMBER	BIT NAME	DESCRIPTION																										
7:0	PRTR12	<p>PortMap Register for Ports 1 and 2: When a hub is enumerated by a USB host controller, the hub is only permitted to report how many ports it has; the hub is not permitted to select a numerical range or assignment. The host controller will number the downstream ports of the hub starting with the number 1, up to the number of ports that the hub reports having.</p> <p>The host's port number is called the Logical Port Number and the physical port on the hub is the Physical Port Number. When mapping mode is enabled (see <b>PRTMAP_EN</b>, Section 5.1.9 on page 32) the hub's downstream port numbers can be mapped to different logical port numbers (assigned by the host).</p> <p><b>Note:</b> Contiguous logical port numbers must be implemented, starting from number 1 up to the maximum number of enabled ports. This ensures that the hub's ports are numbered in accordance with the way a host will communicate with the ports.</p> <table border="1" data-bbox="602 831 1421 1541"> <tbody> <tr> <td data-bbox="602 831 813 1184" rowspan="6">Bit [7:4]</td> <td data-bbox="813 831 935 877">0000</td> <td data-bbox="935 831 1421 877">Physical port 2 is disabled</td> </tr> <tr> <td data-bbox="813 877 935 924">0001</td> <td data-bbox="935 877 1421 924">Physical port 2 is mapped to logical port 1</td> </tr> <tr> <td data-bbox="813 924 935 970">0010</td> <td data-bbox="935 924 1421 970">Physical port 2 is mapped to logical port 2</td> </tr> <tr> <td data-bbox="813 970 935 1016">0011</td> <td data-bbox="935 970 1421 1016">Physical port 2 is mapped to logical port 3</td> </tr> <tr> <td data-bbox="813 1016 935 1062">0100</td> <td data-bbox="935 1016 1421 1062">Physical port 2 is mapped to logical port 4</td> </tr> <tr> <td data-bbox="813 1062 935 1184">1000 to 1111</td> <td data-bbox="935 1062 1421 1184">rsvd, will default to 0000 value</td> </tr> <tr> <td data-bbox="602 1184 813 1541" rowspan="6">Bit [3:0]</td> <td data-bbox="813 1184 935 1230">0000</td> <td data-bbox="935 1184 1421 1230">Physical port 1 is disabled</td> </tr> <tr> <td data-bbox="813 1230 935 1276">0001</td> <td data-bbox="935 1230 1421 1276">Physical port 1 is mapped to logical port 1</td> </tr> <tr> <td data-bbox="813 1276 935 1323">0010</td> <td data-bbox="935 1276 1421 1323">Physical port 1 is mapped to logical port 2</td> </tr> <tr> <td data-bbox="813 1323 935 1369">0011</td> <td data-bbox="935 1323 1421 1369">Physical port 1 is mapped to logical port 3</td> </tr> <tr> <td data-bbox="813 1369 935 1415">0100</td> <td data-bbox="935 1369 1421 1415">Physical port 1 is mapped to logical port 4</td> </tr> <tr> <td data-bbox="813 1415 935 1541">1000 to 1111</td> <td data-bbox="935 1415 1421 1541">rsvd, will default to 0000 value</td> </tr> </tbody> </table>	Bit [7:4]	0000	Physical port 2 is disabled	0001	Physical port 2 is mapped to logical port 1	0010	Physical port 2 is mapped to logical port 2	0011	Physical port 2 is mapped to logical port 3	0100	Physical port 2 is mapped to logical port 4	1000 to 1111	rsvd, will default to 0000 value	Bit [3:0]	0000	Physical port 1 is disabled	0001	Physical port 1 is mapped to logical port 1	0010	Physical port 1 is mapped to logical port 2	0011	Physical port 1 is mapped to logical port 3	0100	Physical port 1 is mapped to logical port 4	1000 to 1111	rsvd, will default to 0000 value
Bit [7:4]	0000	Physical port 2 is disabled																										
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	0010	Physical port 2 is mapped to logical port 2																										
	0011	Physical port 2 is mapped to logical port 3																										
	0100	Physical port 2 is mapped to logical port 4																										
	1000 to 1111	rsvd, will default to 0000 value																										
Bit [3:0]	0000	Physical port 1 is disabled																										
	0001	Physical port 1 is mapped to logical port 1																										
	0010	Physical port 1 is mapped to logical port 2																										
	0011	Physical port 1 is mapped to logical port 3																										
	0100	Physical port 1 is mapped to logical port 4																										
	1000 to 1111	rsvd, will default to 0000 value																										

**5.1.31 Register FCh: PortMap 34**

BIT NUMBER	BIT NAME	DESCRIPTION																																				
7:0	PRTR34	<p>PortMap Register for Ports 3 and 4: When a hub is enumerated by a USB host controller, the hub is only permitted to report how many ports it has; the hub is not permitted to select a numerical range or assignment. The host controller will number the downstream ports of the hub starting with the number 1, up to the number of ports that the hub reports having.</p> <p>The host's port number is called the Logical Port Number and the physical port on the hub is the Physical Port Number. When mapping mode is enabled (see <b>PRTMAP_EN</b>, Section 5.1.9 on page 32) the hub's downstream port numbers can be mapped to different logical port numbers (assigned by the host).</p> <p><b>Note:</b> Contiguous logical port numbers must be implemented, starting from number 1 up to the maximum number of enabled ports. This ensures that the hub's ports are numbered in accordance with the way a host will communicate with the ports.</p> <table border="1" data-bbox="599 829 1421 1539"> <tbody> <tr> <td data-bbox="599 829 816 877">Bit [7:4]</td> <td data-bbox="816 829 935 877">0000</td> <td data-bbox="935 829 1421 877">Physical port 4 is disabled</td> </tr> <tr> <td></td> <td data-bbox="816 877 935 926">0001</td> <td data-bbox="935 877 1421 926">Physical port 4 is mapped to logical port 1</td> </tr> <tr> <td></td> <td data-bbox="816 926 935 974">0010</td> <td data-bbox="935 926 1421 974">Physical port 4 is mapped to logical port 2</td> </tr> <tr> <td></td> <td data-bbox="816 974 935 1022">0011</td> <td data-bbox="935 974 1421 1022">Physical port 4 is mapped to logical port 3</td> </tr> <tr> <td></td> <td data-bbox="816 1022 935 1071">0100</td> <td data-bbox="935 1022 1421 1071">Physical port 4 is mapped to logical port 4</td> </tr> <tr> <td></td> <td data-bbox="816 1071 935 1184">1000 to 1111</td> <td data-bbox="935 1071 1421 1184">rsvd, will default to 0000 value</td> </tr> <tr> <td data-bbox="599 1184 816 1232">Bit [3:0]</td> <td data-bbox="816 1184 935 1232">0000</td> <td data-bbox="935 1184 1421 1232">Physical port 3 is disabled</td> </tr> <tr> <td></td> <td data-bbox="816 1232 935 1281">0001</td> <td data-bbox="935 1232 1421 1281">Physical port 3 is mapped to logical port 1</td> </tr> <tr> <td></td> <td data-bbox="816 1281 935 1329">0010</td> <td data-bbox="935 1281 1421 1329">Physical port 3 is mapped to logical port 2</td> </tr> <tr> <td></td> <td data-bbox="816 1329 935 1377">0011</td> <td data-bbox="935 1329 1421 1377">Physical port 3 is mapped to logical port 3</td> </tr> <tr> <td></td> <td data-bbox="816 1377 935 1425">0100</td> <td data-bbox="935 1377 1421 1425">Physical port 3 is mapped to logical port 4</td> </tr> <tr> <td></td> <td data-bbox="816 1425 935 1539">1000 to 1111</td> <td data-bbox="935 1425 1421 1539">rsvd, will default to 0000 value</td> </tr> </tbody> </table>	Bit [7:4]	0000	Physical port 4 is disabled		0001	Physical port 4 is mapped to logical port 1		0010	Physical port 4 is mapped to logical port 2		0011	Physical port 4 is mapped to logical port 3		0100	Physical port 4 is mapped to logical port 4		1000 to 1111	rsvd, will default to 0000 value	Bit [3:0]	0000	Physical port 3 is disabled		0001	Physical port 3 is mapped to logical port 1		0010	Physical port 3 is mapped to logical port 2		0011	Physical port 3 is mapped to logical port 3		0100	Physical port 3 is mapped to logical port 4		1000 to 1111	rsvd, will default to 0000 value
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Bit [3:0]	0000	Physical port 3 is disabled																																				
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	0011	Physical port 3 is mapped to logical port 3																																				
	0100	Physical port 3 is mapped to logical port 4																																				
	1000 to 1111	rsvd, will default to 0000 value																																				



### 5.1.32 Register FFh: Status/Command

BIT NUMBER	BIT NAME	DESCRIPTION
7:3	rsvd	
2	INTF_PW_DN	SMBus Interface Power Down: 0 : interface is active 1 : interface power down after ACK has completed
1	RESET	Reset the SMBus interface and internal memory back to <b>RESET_N</b> assertion default settings. 0 : normal run/idle state 1 : force a reset of registers to their default state
0	USB_ATTACH	USB Attach (and write protect) 0 : SMBus slave interface is active 1 : the hub will signal a USB attach event to an upstream device, and the internal memory (address range 0x00-0xFE) is write-protected to prevent unintentional data corruption.

## 5.2 I<sup>2</sup>C EEPROM

The SMSC hub can be configured via a 2-wire (I<sup>2</sup>C) EEPROM (256x8). See [Table 5.1](#) for details on enabling the I<sup>2</sup>C EEPROM interface. The I<sup>2</sup>C EEPROM interface implements a subset of the *I<sup>2</sup>C Master Specification* (refer to the Philips Semiconductor Standard I<sup>2</sup>C-Bus Specification I<sup>2</sup>C protocol for details). The hub's interface is designed to attach to a single dedicated I<sup>2</sup>C EEPROM which conforms to the Standard-mode I<sup>2</sup>C specification (100 kbit/s transfer rate and 7-bit addressing) for protocol and electrical compatibility. The I<sup>2</sup>C EEPROM shares the same pins as the SMBus interface, therefore the SMBus interface is not available when the I<sup>2</sup>C EEPROM interface has been enabled (and vice versa).

The hub acts as the master and generates the serial clock SCL, controls the bus access (determines which device acts as the transmitter and which device acts as the receiver), and generates the START and STOP conditions. The hub will read the external EEPROM for configuration data and then attach to the upstream USB host.

**Note:** If no external EEPROM is present, the hub will write 0 to all configuration registers.

The hub does not have the capacity to write to the external EEPROM. The hub only has the capability to read from an external EEPROM. The external EEPROM will be read (even if it is blank), and the hub will be configured with the values that are read. Any values read for unsupported registers will not be retained (i.e., they will remain as the default values). Reserved registers should be set to 0 unless otherwise specified. EEPROM reset values are 0x00. Contents read from unavailable registers should be ignored.

**Note:** Go to [www.smsc.com](http://www.smsc.com), search for *USB251xB* and select *e2prommap.msi* from the documents section to download the EEPROM data configuration utility tool.

### 5.2.1 I<sup>2</sup>C Slave Address

The 7-bit slave address is 0101100b.

**Note:** 10-bit addressing is not supported.

### 5.2.2 Protocol Implementation

The hub will only access an EEPROM using the sequential read protocol as outlined in Chapter 8 of *MicroChip 24AA02/24LC02B* [4].

### 5.2.3 Pull-Up Resistor

The circuit board designer is required to place external pull-up resistors (10 k $\Omega$  recommended) on the SDA/SMBDATA and SCL/SMBCLK/CFG\_SEL[0] lines (per *SMBus 1.0 Specification* [3], and EEPROM manufacturer guidelines) to VDD33 in order to assure proper operation.

### 5.2.4 In-Circuit EEPROM Programming

The EEPROM can be programmed via automatic test equipment (ATE) by pulling RESET\_N low (which tri-states the hub's EEPROM interface and allows an external source to program the EEPROM).

## 5.3 SMBus

The SMSC hub can be configured by an external processor via an SMBus interface (see [Table 5.1](#) for details on enabling the SMBus interface). The SMBus interface shares the same pins as the EEPROM interface, and therefore the hub no longer supports the I<sup>2</sup>C EEPROM interface when the SMBus interface has been enabled. The SMSC hub waits indefinitely for the SMBus code load to complete and only appears as a newly connected device on USB after the code load is complete.

The hub's SMBus acts as a slave-only SMBus device. The implementation only supports block write ([Section 5.3.2.1](#)) and block read ([Section 5.3.2.2](#)) protocols, where the available registers are outlined in [Section 5.1 on page 27](#). Reference the *System Management Bus Specification* [3] for additional information.

### 5.3.1 SMBus Slave Address

The 7-bit slave address is 0101100b. The hub will not respond to the general call address of 0000000b.

### 5.3.2 Protocol Implementation

Typical block write and block read protocols are shown in figures [5.1](#) and [5.2](#). Register accesses are performed using 7-bit slave addressing, an 8-bit register address field, and an 8-bit data field. The shading shown in the figures during a read or write indicates the hub is driving data on the SMBDATA line; otherwise, host data is on the SDA/SMBDATA line.

The SMBus slave address assigned to the hub (0101100b) allows it to be identified on the SMBus. The register address field is the internal address of the register to be accessed. The register data field is the data that the host is attempting to write to the register or the contents of the register that the host is attempting to read.

**Note:** Data bytes are transferred MSB first.

### 5.3.2.1 Block Write/Read

The block write begins with a slave address and a write condition. After the command code, the host issues a byte count which describes how many more bytes will follow in the message. If a slave had 20 bytes to send, the first byte would be the number 20 (14h), followed by the 20 bytes of data. The byte count may not be zero. A block write or read allows a transfer maximum of 32 data bytes.

**Note:** For the following SMBus tables:

Denotes Master-to-Slave       Denotes Slave-to-Master

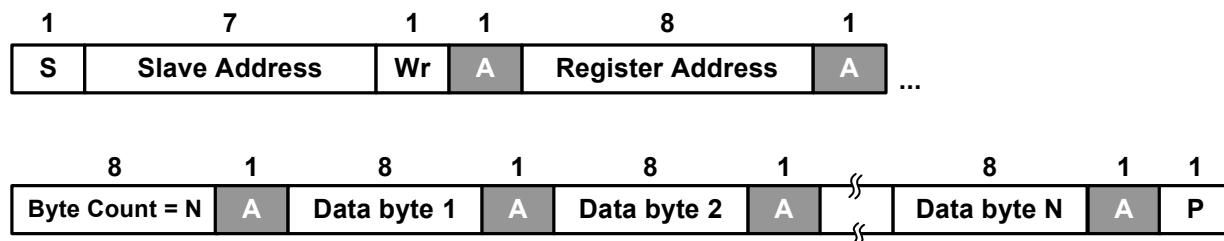


Figure 5.1 Block Write

### 5.3.2.2 Block Read

A block read differs from a block write in that the repeated start condition exists to satisfy the I<sup>2</sup>C specification's requirement for a change in the transfer direction.

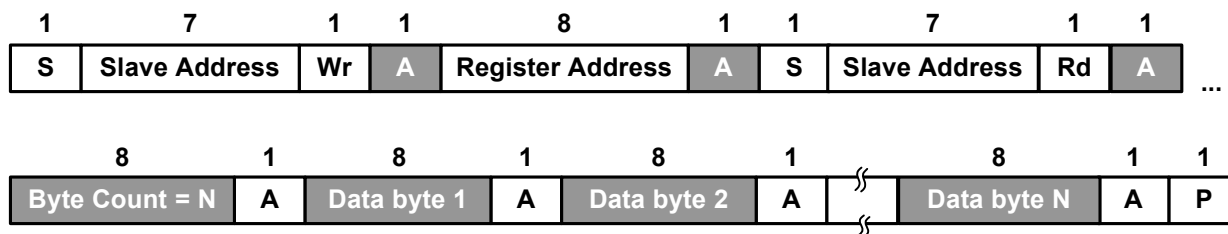


Figure 5.2 Block Read

### 5.3.2.3 Invalid Protocol Response Behavior

Note that any attempt to update registers with an invalid protocol will not be updated. The only valid protocols are write block and read block (described above), where the hub only responds to the 7-bit hardware selected slave address (0101100b). Also, the only valid registers for the hub are outlined in [Section 5.1 on page 27](#). Attempts to access any other registers will return no response.

### 5.3.3 Slave Device Timeout

Devices in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds 25 ms ( $T_{TIMEOUT, MIN}$ ). The master must detect this condition and generate a stop condition within or after the transfer of the interrupted data byte. Slave devices must reset their communication and be able to receive a new START condition no later than 35 ms ( $T_{TIMEOUT, MAX}$ ).

**Note:** Some simple devices do not contain a clock low drive circuit; this simple kind of device typically resets its communications port after a start or stop condition. The slave device timeout must be implemented.

### 5.3.4 Stretching the SCLK Signal

The hub supports stretching of the SCLK by other devices on the SMBus. However, the hub does not stretch the SCLK.

### 5.3.5 SMBus Timing

The SMBus slave interface complies with the *SMBus Specification Revision 1.0* [3]. See Section 2.1, *AC Specifications* on page 3 for more information.

### 5.3.6 Bus Reset Sequence

The SMBus slave interface resets and returns to the idle state upon a START condition followed immediately by a STOP condition.

### 5.3.7 SMBus Alert Response Address

The SMBALERT# signal is not supported by the hub.

## 5.4 Default Configuration

To put the SMSC hub in the default configuration, strap CFG\_SEL[1:0] to 00b. This procedure configures the hub to the internal defaults and enables the strapping options. To place the hub in default configuration with overrides, see [Table 5.1 on page 26](#) for the list of the options.

The internal default values are used for the registers that are not controlled by strapping option pins. Refer to [Section 5.1 on page 27](#) for the internal default values that are loaded when this option is selected. For a list of strapping option pins, see [Chapter 5 on page 26](#), and to configure the strapping pins, see [Section 3.3.1 on page 22](#).

## 5.5 Reset

The hub experiences the following two resets:

- Hardware reset via the RESET\_N pin
- USB bus reset

### 5.5.1 External Hardware RESET\_N

A valid hardware reset is defined as assertion of RESET\_N for a minimum of 1  $\mu$ s after all power supplies are within operating range. While reset is asserted, the hub (and its associated external circuitry) consumes less than 500  $\mu$ A of current from the upstream USB power source.

Assertion of RESET\_N causes the following:

1. All downstream ports are disabled, and PRTPOWER[x:1] to downstream devices is removed (unless BC\_EN[x:1] is enabled).
2. The PHYs are disabled, and the differential pairs will be in a high-impedance state.
3. All transactions immediately terminate; no states are saved.
4. All internal registers return to the default state (in most cases, 00h).
5. The external crystal oscillator is halted.
6. The PLL is halted.

The hub is operational 500  $\mu$ s after RESET\_N is negated. Once operational, the hub will do one of the following, depending on configuration:

- Read the strapping pins (default configuration with strapping options enabled)
- Read configuration information from the external I<sup>2</sup>C EEPROM
- Wait for configuration over SMBus.

### 5.5.1.1 RESET\_N for Strapping Option Configuration

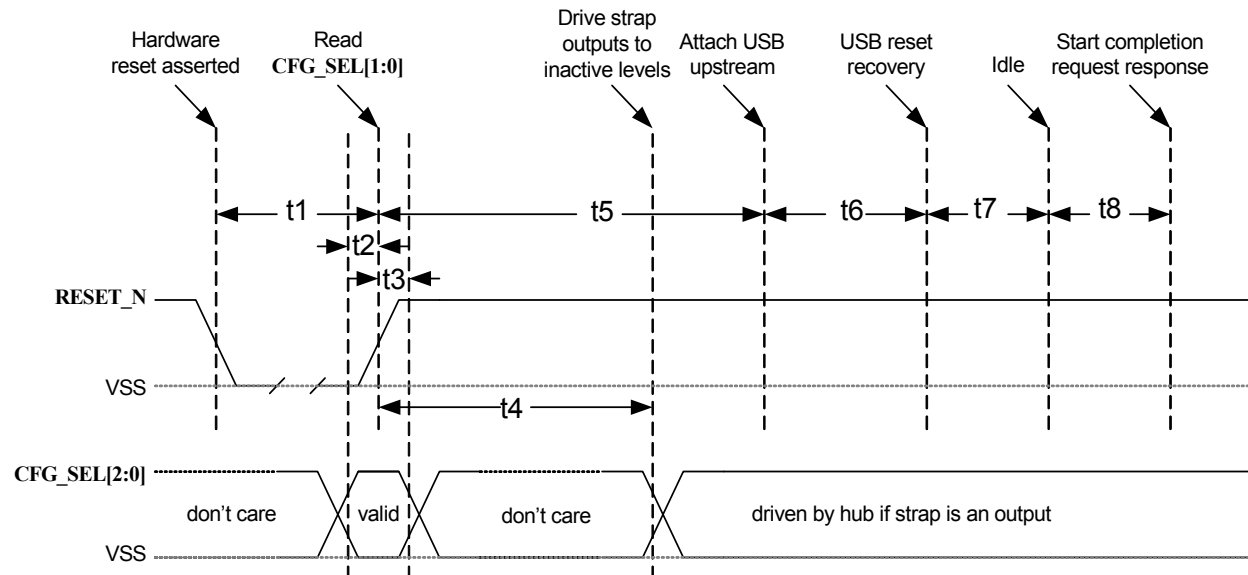


Figure 5.3 Reset\_N Timing for Default Configuration

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	RESET_N asserted	1			μs
t2	CFG_SEL[1:0] setup time	16.7			ns
t3	CFG_SEL[1:0] hold time	16.7		1400	ns
t4	Hub outputs driven to inactive logic states		1.5	2	μs
t5	USB attach (see notes)			100	ms
t6	Host acknowledges attach and signals USB reset	100			ms
t7	USB idle		undefined		ms
t8	Completion time for requests (with or without data stage)			5	msec

**Notes:**

- When in bus-powered mode, the hub and its associated circuitry must not consume more than 100 mA from the upstream USB power source during t1+t5.
- All power supplies must have reached the operating levels mandated in [Chapter 6: DC Parameters](#), prior to (or coincident with) the assertion of RESET\_N.

### 5.5.1.2 RESET\_N for EEPROM Configuration

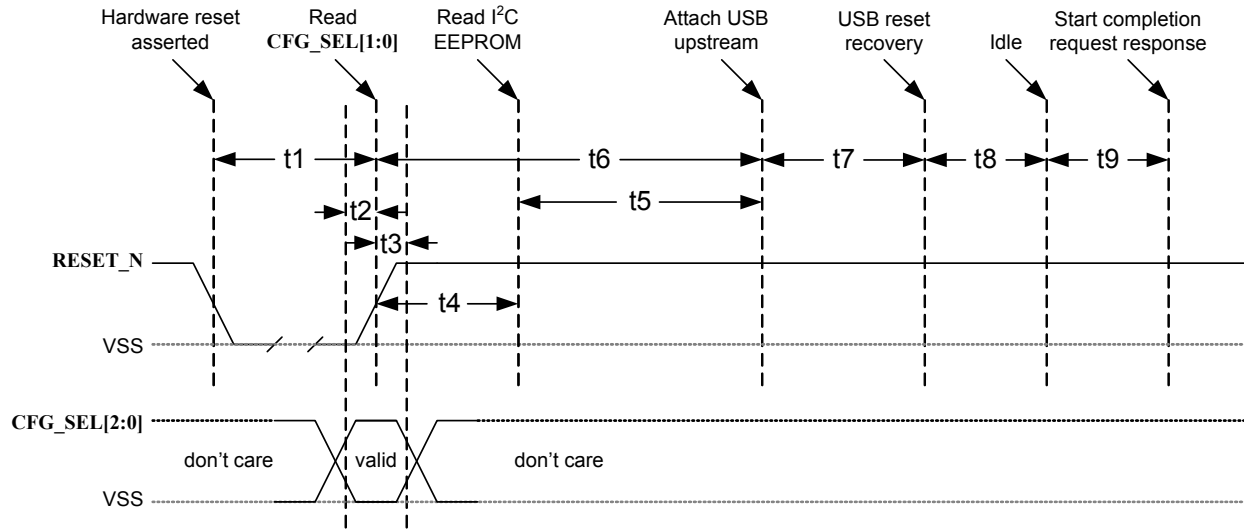


Figure 5.4 Reset\_N Timing for EEPROM Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	RESET_N asserted	1			μs
t2	CFG_SEL[1:0] setup time	16.7			ns
t3	CFG_SEL[1:0] hold time	16.7		1400	ns
t4	Hub recovery/stabilization			500	μs
t5	EEPROM read (hub configuration)		2.0	99.5	ms
t6	USB attach (see notes)			100	ms
t7	Host acknowledges attach and signals USB reset	100			ms
t8	USB idle		undefined		ms
t9	Completion time for requests (with or without data stage)			5	ms

**Notes:**

- When in bus-powered mode, the hub and its associated circuitry must not consume more than 100 mA from the upstream USB power source during t6+t7+t8+t9.
- All power supplies must have reached the operating levels mandated in [Chapter 6: DC Parameters](#), prior to (or coincident with) the assertion of **RESET\_N**.

### 5.5.1.3 RESET\_N for SMBus Slave Configuration

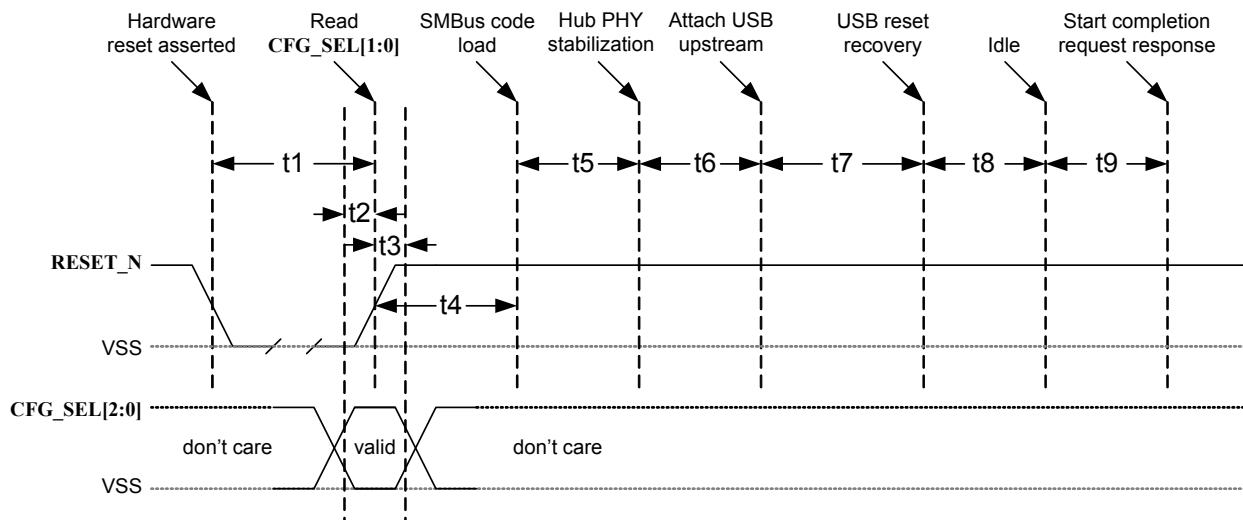


Figure 5.5 Reset\_N Timing for SMBus Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	RESET_N Asserted	1			μs
t2	CFG_SEL[1:0] setup time	16.7			ns
t3	CFG_SEL[1:0] hold time	16.7		1400	ns
t4	Hub recovery/stabilization			500	μs
t5 <sub>BUS</sub>	SMBus code load (Note 5.1)			99.5	ms
t5 <sub>SELF</sub>	SMBus Code Load (Note 5.1)			undefined	ms
t6	Hub configuration and USB attach			100	ms
t7	Host acknowledges attach and signals USB reset	100			ms
t8	USB idle		undefined		ms
t9	Completion time for requests (with or without data stage)			5	ms

**Note 5.1** For bus-powered configurations, there is a 99.5 ms MAX, and the hub and its associated circuitry must not consume more than 100 mA from the upstream USB power source during t4+t5+t6+t7+t8+t9. For self-powered configurations, t5 MAX is not applicable and the time to load the configuration is determined by the external SMBus host.

**Note 5.2** All power supplies must have reached the operating levels mandated in [Chapter 6: DC Parameters](#), prior to (or coincident with) the assertion of RESET\_N.

## 5.5.2 USB Bus Reset

In response to the upstream port signaling a reset to the hub, the hub does the following:

1. Sets default internal USB address to 0
2. Sets configuration to: unconfigured
3. Negates **PRTPOWER[x:1]** to all downstream ports unless battery charging (**BC\_EN[x:1]**) is enabled
4. Clears all TT buffers
5. Moves device from suspended to active (if suspended)
6. Complies with Section 11.10 of the *USB 2.0 Specification* [1] for behavior after completion of the reset sequence. The host then configures the hub and the hub's downstream port devices in accordance with the *USB Specification*.

**Note:** The hub does not propagate the upstream USB reset to downstream devices.



## Chapter 6 DC Parameters

### 6.1 Maximum Guaranteed Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS	COMMENTS
Storage Temperature	$T_{STOR}$	-55	150	°C	
Lead Temperature					Refer to <i>JEDEC Specification J-STD-020D</i> [5]
3.3 V supply voltage	VDD33 VDDA33		4.6	V	Applies to all packages
Voltage on any I/O pin		-0.5	5.5	V	
Voltage on XTALIN		-0.5	4.0	V	
Voltage on XTALOUT		-0.5	2.5	V	

**Notes:**

- Stresses above the specified parameters could cause permanent damage to the device. This is a stress rating only. Therefore, functional operation of the device at any condition above those indicated in the operation sections of this specification are not implied.
- When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. When this possibility exists, it is suggested that a clamp circuit be used.

### 6.2 Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS	COMMENTS
Extended Commercial Operating Temperature	$T_{AE}$	0	85	°C	Ambient temperature in still air
Industrial Operating Temperature	$T_{AI}$	-40	85	°C	Ambient temperature in still air Only applies to USB251xBi products
3.3 V supply voltage	VDD33 VDDA33	3.0	3.6	V	Applies to all parts
3.3 V supply rise time	$t_{RT33}$	0	400	μs	See <a href="#">Figure 6.1</a>

PARAMETER	SYMBOL	MIN	MAX	UNITS	COMMENTS
Voltage on any I/O pin		-0.3	5.5	V	If any 3.3 V supply voltage drops below 3.0 V, then the MAX becomes: (3.3 V supply voltage) + 0.5
Voltage on XTALIN		-0.3	VDD33	V	

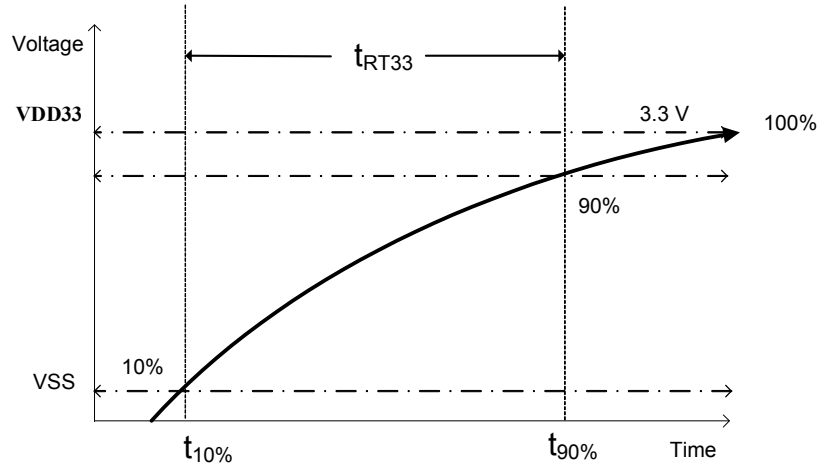


Figure 6.1 Supply Rise Time Model

Table 6.1 DC Electrical Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
<b>I, IS Type Input Buffer</b>						
Low Input Level	$V_{ILI}$			0.8	V	TTL Levels
High Input Level	$V_{IHI}$	2.0			V	
Input Leakage	$I_{IL}$	-10		+10	$\mu$ A	$V_{IN} = 0$ to VDD33
Hysteresis (IS only)	$V_{HYSI}$	250		350	mV	
<b>Input Buffer with Pull-Up (IPU)</b>						
Low Input Level	$V_{ILI}$			0.8	V	TTL Levels
High Input Level	$V_{IHI}$	2.0			V	
Low Input Leakage	$I_{ILL}$	+35		+90	$\mu$ A	$V_{IN} = 0$
High Input Leakage	$I_{IHL}$	-10		+10	$\mu$ A	$V_{IN} = VDD33$

**Table 6.1 DC Electrical Characteristics (continued)**

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
<b>Input Buffer with Pull-Down (IPD)</b>						
Low Input Level	$V_{ILI}$			0.8	V	TTL Levels
High Input Level	$V_{IHI}$	2.0			V	
Low Input Leakage	$I_{ILL}$	+10		-10	$\mu$ A	$V_{IN} = 0$
High Input Leakage	$I_{IHL}$	-35		-90	$\mu$ A	$V_{IN} = VDD33$
<b>USB251xB/xBi ICLK Input Buffer</b>						
Low Input Level	$V_{ILCK}$			0.3	V	
High Input Level	$V_{IHCK}$	0.9			V	
Input Leakage	$I_{IL}$	-10		+10	$\mu$ A	$V_{IN} = 0$ to <b>VDD33</b>
<b>O12, I/O12 &amp; I/OSD12 Type Buffer</b>						
Low Output Level	$V_{OL}$			0.4	V	$I_{OL} = 12$ mA @ <b>VDD33 = 3.3 V</b>
High Output Level	$V_{OH}$	2.4			V	$I_{OH} = -12$ mA @ <b>VDD33 = 3.3 V</b>
Output Leakage	$I_{OL}$	-10		+10	$\mu$ A	
Hysteresis (SD pad only)	$I_{HYSC}$	250		350	mV	$V_{IN} = VDD33$ (Notes:)

**Note 6.1** Output leakage is measured with the current pins in high impedance.

**Note 6.2** See *USB 2.0 Specification [1]* for USB DC electrical characteristics.

**Table 6.2 Supply Current Unconfigured: Hi-Speed Host ( $I_{CCINTHS}$ )**

PART	MIN	TYP	MAX	UNITS	COMMENTS
USB2512B/12Bi		40	45	mA	
USB2513B/13Bi		40	45	mA	
USB2514B/14Bi		45	50	mA	

**Table 6.3 Supply Current Unconfigured: Full-Speed Host ( $I_{CCINTFS}$ )**

PART	MIN	TYP	MAX	UNITS	COMMENTS
USB2512B/12Bi		35	40	mA	
USB2513B/13Bi		35	40	mA	
USB2514B/14Bi		35	40	mA	

**Table 6.4 Supply Current Configured: Hi-Speed Host ( $I_{HCH1}$ )**

PART	MIN	TYP	MAX	UNITS	COMMENTS
USB2512B		60	65	mA	This is the base current of one downstream port.
USB2512Bi		60	70	mA	
USB2513B		65	70	mA	
USB2513Bi		65	75	mA	
USB2514B		70	80	mA	
USB2514Bi		70	85	mA	
<b>USB251xB/xBi</b> <b>Supply Current Configured</b> <i>Hi-Speed Host</i> , each additional downstream port		1 port base + 25 mA	1 port base + 25 mA	mA	

**Table 6.5 Supply Current Configured: Full-Speed Host ( $I_{FCC1}$ )**

PART	MIN	TYP	MAX	UNITS	COMMENTS
USB2512B		45	50	mA	Base current of one downstream port
USB2512Bi		45	55	mA	
USB2513B		50	55	mA	
USB2513Bi		50	60	mA	
USB2514B		50	60	mA	
USB2514Bi		50	65	mA	
<b>USB251xB/xBi</b> <b>Supply Current Configured</b> <i>Full-Speed Host</i> , each additional downstream port		1 port base + 8 mA	1 port base + 8 mA	mA	

Table 6.6 Supply Current Suspend ( $I_{CSBY}$ )

PART	MIN	TYP	MAX	UNITS	COMMENTS
USB2512B		475	1000	$\mu$ A	All supplies combined
USB2512Bi		475	1200	$\mu$ A	
USB2513B		500	1100	$\mu$ A	
USB2513Bi		500	1300	$\mu$ A	
USB2514B		550	1200	$\mu$ A	
USB2514Bi		550	1500	$\mu$ A	

Table 6.7 Supply Current Reset ( $I_{CRST}$ )

PART	MIN	TYP	MAX	UNITS	COMMENTS
USB2512B		550	1100	$\mu$ A	All supplies combined
USB2512Bi		550	1250	$\mu$ A	
USB2513B		650	1200	$\mu$ A	
USB2513Bi		650	1400	$\mu$ A	
USB2514B		750	1400	$\mu$ A	
USB2514Bi		750	1600	$\mu$ A	

Table 6.8 Pin Capacitance

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	$C_{XTAL}$			6	pF	All pins except USB pins and the pins under the test tied to AC ground
Input Capacitance	$C_{IN}$			6	pF	(Note 6.3)
Output Capacitance	$C_{OUT}$			6	pF	

**Note 6.3** Capacitance  $T_A = 25^\circ\text{C}$ ;  $f_c = 1\text{ MHz}$ ;  $V_{DD33} = 3.3\text{ V}$

## 6.2.1 Package Thermal Specifications

Thermal parameters are measured or estimated for devices with the exposed pad soldered to thermal vias in a multilayer 2S2P PCB per JESD51. Thermal resistance is measured from the die to the ambient air. The values provided are based on the package body, die size, maximum power consumption, 85°C ambient temperature, and 125°C junction temperature of the die.

SYMBOL	USB2512B/12Bi USB2513B/13Bi USB2514B/14Bi (°C/W)	VELOCITY (meters/s)
$\Theta_{JA}$	40.1	0
	35.0	1
$\Psi_{JT}$	0.5	0
	0.7	1
$\Theta_{JC}$	6.3	0
	6.3	1

**Table 6.9 Package Thermal Resistance Parameters**

**Table 6.10 Package Thermal Resistance Parameters**

SYMBOL	USB2512B/12Bi USB2513B/13Bi USB2514B/14Bi (°C/W)	VELOCITY (meters/s)
$\Theta_{JA}$	40.1	0
	35.0	1
$\Psi_{JT}$	0.5	0
	0.7	1
$\Theta_{JC}$	6.3	0
	6.3	1

Use the following formulas to calculate the junction temperature:

$$T_J = P \times \Theta_{JA} + T_A$$

$$T_J = P \times \Psi_{JT} + T_T$$

$$T_J = P \times \Theta_{JC} + T_C$$

$$\text{Max Power Supported} = (T_J \text{ Max. Spec.} \times T_{\text{Amb.}}) / \Theta_{JA}$$

Table 6.11 Legend

SYMBOL	DESCRIPTION
$T_J$	Junction temperature
$P$	Power dissipated
$\Theta_{JA}$	Junction-to-ambient-temperature
$\Theta_{JC}$	Junction-to-top-of-package
$\Psi_{JT}$	Junction-to-bottom-of-case
$T_A$	Ambient temperature
$T_C$	Temperature of the bottom of the case
$T_T$	Temperature of the top of the case

## Chapter 7 AC Specifications

### 7.1 Oscillator/Crystal

Crystal: Parallel resonant, fundamental mode, 24 MHz  $\pm 350$  ppm



Figure 7.1 Typical Crystal Circuit

Table 7.1 Crystal Circuit Legend

SYMBOL	DESCRIPTION	IN ACCORDANCE WITH
$C_0$	Crystal shunt capacitance	Crystal manufacturer's specification (Note 7.1)
$C_L$	Crystal load capacitance	
$C_B$	Total board or trace capacitance	OEM board design
$C_S$	Stray capacitance	SMSC IC and OEM board design
$C_{XTAL}$	XTAL pin input capacitance	SMSC IC
$C_1$	Load capacitors installed on OEM board	Calculated values based on Figure 7.2 (Note 7.2)
$C_2$		

$$C_1 = 2 \times (C_L - C_0) - C_{S1}$$

$$C_2 = 2 \times (C_L - C_0) - C_{S2}$$

Figure 7.2 Formula to Find the Value of  $C_1$  and  $C_2$

**Note 7.1**  $C_0$  is usually included (subtracted by the crystal manufacturer) in the specification for  $C_L$  and should be set to 0 for use in the calculation of the capacitance formulas in Figure 7.2. However, the PCB itself may present a parasitic capacitance between XTALIN and XTALOUT. For an accurate calculation of  $C_1$  and  $C_2$ , take the parasitic capacitance between traces XTALIN and XTALOUT into account.

**Note 7.2** Each of these capacitance values is typically around 18 pF.





## 7.2 External Clock

50% duty cycle  $\pm 10\%$ , 24 MHz  $\pm 350$  ppm, jitter  $< 100$  ps rms.

The external clock is recommended to conform to the signaling level designated in the *JESD76-2 Specification* [5] on 1.2 V CMOS Logic. XTALOUT should be treated as a weak ( $< 1$ mA) buffer output.

### 7.2.1 SMBus Interface

The SMSC hub conforms to all voltage, power, and timing characteristics and specifications as set forth in the *SMBus 1.0 Specification* [3] for slave-only devices (except as noted in [Section 5.3: SMBus on page 42](#)).

### 7.2.2 I<sup>2</sup>C EEPROM

Clock frequency is fixed at 60 kHz  $\pm 20\%$ .

### 7.2.3 USB 2.0

The SMSC hub conforms to all voltage, power, and timing characteristics and specifications as set forth in the *USB 2.0 Specification* [1].

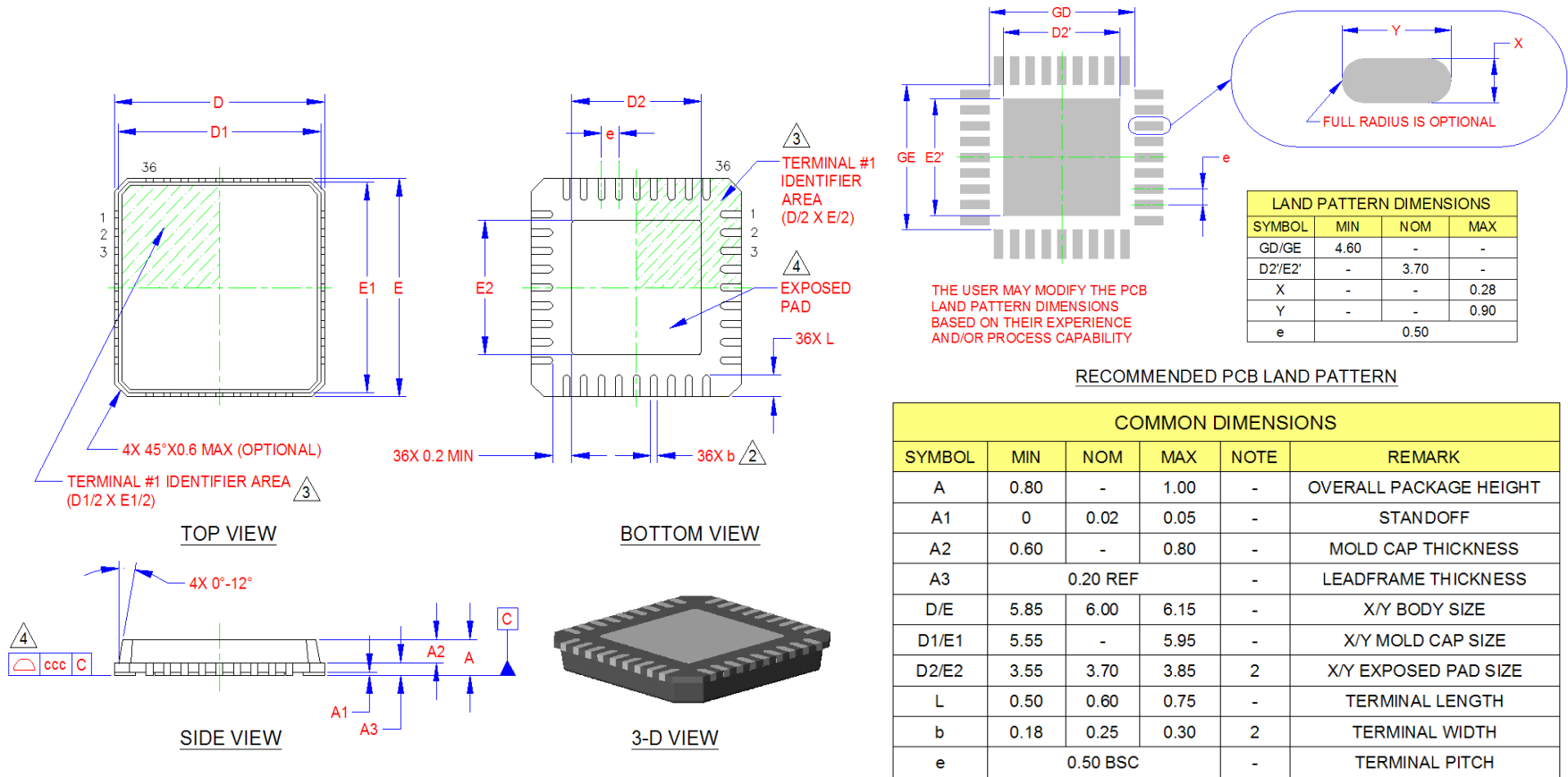
# Chapter 8 Package Outlines

Revision 2.2 (02-17-12)

DATASHEET

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SMSC USB251xB/xBI



- NOTES:**
1. ALL DIMENSIONS ARE IN MILLIMETERS.
  2. POSITION TOLERANCE OF EACH TERMINAL AND EXPOSED PAD IS  $\pm 0.05\text{mm}$  AT MAXIMUM MATERIAL CONDITION. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
  3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.
  4. COPLANARITY ZONE APPLIES TO EXPOSED PAD AND TERMINALS.

Figure 8.1 36-Pin QFN, 6x6 mm Body, 0.5 mm Pitch

## 8.1 Tape and Reel Specifications



### TAPE LENGTH & PART QUANTITY



TAPE SECTIONS		
SECTION	SYM	SIZE
TRAILER	T	14 pockets (MIN)
COMPONENT	C	3000 components
LEADER	L	34 pockets (MIN)

Figure 8.2 36-Pin Package Tape Specifications

### REEL PHYSICAL DIMENSIONS



Figure 8.3 36-Pin Package Reel Specifications

## Appendix A (Acronyms)

**I<sup>2</sup>C<sup>®</sup>**: Inter-Integrated Circuit<sup>1</sup>

**OCS**: Over-Current Sense

**PCB**: Printed Circuit Board

**PHY**: Physical Layer

**PLL**: Phase-Locked Loop

**QFN**: Quad Flat No Leads

**RoHS**: Restriction of Hazardous Substances Directive

**SCL**: Serial Clock

**SIE**: Serial Interface Engine

**SMBus**: System Management Bus

**TT**: Transaction Translator

---

<sup>1</sup>.I<sup>2</sup>C is a registered trademark of Philips Corporation.

## Appendix B (References)

- [1] Universal Serial Bus Specification, Version 2.0, April 27, 2000 (12/7/2000 and 5/28/2002 Errata)  
USB Implementers Forum, Inc. <http://www.usb.org>
- [2] I<sup>2</sup>C-Bus Specification Version 1.1  
NXP (formerly a division of Philips). <http://www.nxp.com>
- [3] System Management Bus Specification, version 1.0  
SMBus. <http://smbus.org/specs/>
- [4] MicroChip 24AA02/24LC02B (Revision C)  
Microchip Technology Inc. <http://www.microchip.com/>
- [5] JEDEC Specifications: JESD76-2 (June 2001) and J-STD-020D.1 (March 2008)  
JEDEC Global Standards for the Microelectronics Industry. <http://www.jedec.org/standards-documents>

## Datasheet Revision History

### Customer Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 2.2 (02-17-12)	Cover	Updated clock bullet to remove reference to 48MHz clock support.
	<a href="#">Section 1.1: Configurable Features on page 8</a>	Updated bulleted lists. USB signal drive strength, USB differential pair pin location and downstream port power control / over-current detection items moved from first (strap-configurable) bulleted list to the second (EEPROM-configurable) bulleted list. Added enabling of battery charging to the first bulleted list.
	<a href="#">Section 3.1: Pin Configurations on page 11</a>	Clarified introductory sentence.
	<a href="#">Table 3.3: USB251xB/xBi Pin Descriptions on page 19</a>	Updated VBUS_DET buffer type to "I" and changed description to: "For self-powered applications with a permanently attached host, this pin must be connected to a dedicated host control output, or connected to the 3.3 V domain that powers the host (typically VDD33)."
	<a href="#">Table 3.3: USB251xB/xBi Pin Descriptions on page 19</a>	Updated CRFILT and PLLFILT pin descriptions.
	<a href="#">Section 7.1: Oscillator/Crystal on page 56</a>	Removed redundant sentence: "External Clock: 50% duty cycle $\pm$ 10%, 24/48 MHz $\pm$ 350 ppm, jitter < 100 ps rms". This information is provided in <a href="#">Section 7.2: External Clock on page 57</a> .
	<a href="#">Chapter 7: AC Specifications</a>	Removed ceramic resonator information.
	<a href="#">Section 7.2: External Clock</a>	Replaced "1.8 V CMOS Logic" with "1.2 V CMOS Logic". Updated XTALOUT description.
	<a href="#">Section 3.3: Pin Descriptions (Grouped by Function)</a>	Updated CRFILT and PLLFILT pin descriptions.
	Cover, Package, All	Removed the 49-BGA option.
	Order Code Page	Changed ordering codes for non-industrial USB2513B and USB2514B. Last character was changed from "G" to "C".
	Front page	Removed support for ceramic resonator.
Rev. 2.1 (02/24/11)	Section 6.1 and 6.2, DC Parameters	The 1.2V supply information was added and the graph that includes both 3.3 and 1.2 V rise time was added for 49-BGA.
Rev. 2.1 (02/24/11)	All	Added the 49-BGA option.
Rev. 2.1 (02/22/11)	Section 6.2.1, <i>Package Thermal Specifications</i>	Added Max Power Supported = $(T_J, \text{max.spec.} - T_{\text{amb}}) / \theta_{JA}$
Rev. 2.0 (10/01/10)	All	General refresh, corrected grammatical errors and unified tone.



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