LM2940-N/LM2940C 1A Low Dropout Regulator

Check for Samples: LM2940-N, LM2940C

FEATURES

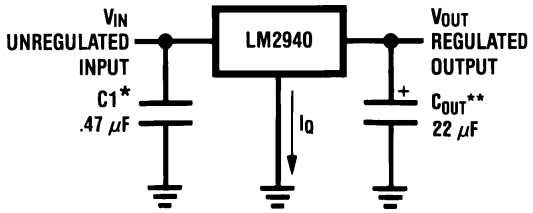
- **Dropout Voltage Typically 0.5V @I_O = 1A**
- **Output Current in Excess of 1A**
- **Output Voltage Trimmed Before Assembly**
- **Reverse Battery Protection**
- **Internal Short Circuit Current Limit**
- **Mirror Image Insertion Protection**
- **P^+ Product Enhancement Tested**

DESCRIPTION

The LM2940-N/LM2940C positive voltage regulator features the ability to source 1A of output current with a dropout voltage of typically 0.5V and a maximum of 1V over the entire temperature range. Furthermore, a quiescent current reduction circuit has been included which reduces the ground current when the differential between the input voltage and the output voltage exceeds approximately 3V. The quiescent current with 1A of output current and an input-output differential of 5V is therefore only 30 mA. Higher quiescent currents only exist when the regulator is in the dropout mode ($V_{IN} - V_{OUT} \leq 3V$).

Designed also for vehicular applications, the LM2940-N/LM2940C and all regulated circuitry are protected from reverse battery installations or 2-battery jumps. During line transients, such as load dump when the input voltage can momentarily exceed the specified maximum operating voltage, the regulator will automatically shut down to protect both the internal circuits and the load. The LM2940/LM2940C cannot be harmed by temporary mirror-image insertion. Familiar regulator features such as short circuit and thermal overload protection are also provided.

Typical Application



*Required if regulator is located far from power supply filter.

**C_{OUT} must be at least 22 µF to maintain stability. May be increased without bound to maintain regulation during transients. Locate as close as possible to the regulator. This capacitor must be rated over the same operating temperature range as the regulator and the ESR is critical; see curve.

Connection Diagrams

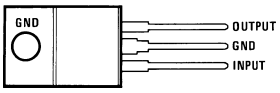


Figure 1. TO-220 (NDE) Plastic Package
Front View
See Package Number NDE0003B

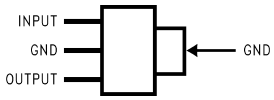


Figure 2. SOT-223 (DCY) 3-Lead
Front View
See Package Number DCY0004A

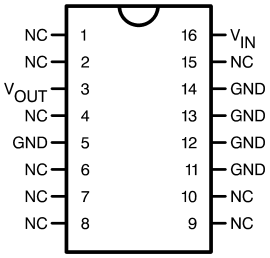


Figure 3. 16-Lead CDIP (NFE)
Top View
See Package Number NFE0016A

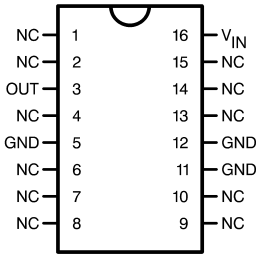


Figure 4. 16-Lead CLGA (NAC)
Top View
See Package Number NAC0016A

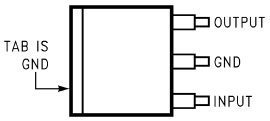


Figure 5. DDPAK/ TO-263 (KTT)
Top View

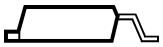
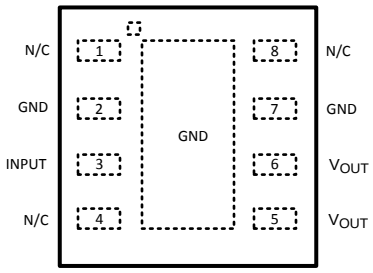


Figure 6. Side View
See Package Number KTT0003B



Pin 2 and pin 7 are fused to center DAP
Pin 5 and 6 need to be tied together on PCB board

Figure 7. WSON (NGN) 8-Lead
Top View
See Package Number NGN0008A

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

LM2940-N KTT, NFE, NAC, NDE, DCY ≤ 100 ms		60V
LM2940C KTT, NDE ≤ 1 ms		45V
Internal Power Dissipation(3)		Internally Limited
Maximum Junction Temperature		150°C
Storage Temperature Range		−65°C ≤ T_J ≤ +150°C
Soldering Temperature (4)	TO-220 (NDE), Wave	260°C, 10s
	DDPAK/ TO-263 (KTT)	235°C, 30s
	SOT-223 (DCY)	260°C, 30s
	WSON-8 (NGN)	235°C, 30s
ESD Susceptibility (5)		2 kV

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Conditions are conditions under which the device functions but the specifications might not be ensured. For ensured specifications and test conditions see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. The value of θ_{JA} (for devices in still air with no heatsink) is 60°C/W for the TO-220 package, 80°C/W for the DDPAK/TO-263 package, and 174°C/W for the SOT-223 package. The effective value of θ_{JA} can be reduced by using a heatsink (see Application Hints for specific information on heatsinking). The value of θ_{JA} for the WSON package is specifically dependent on PCB trace area, trace material, and the number of layers and thermal vias. For improved thermal resistance and power dissipation for the WSON package, refer to Application Note AN-1187 (SNOA401). It is recommended that 6 vias be placed under the center pad to improve thermal performance.
(4) Refer to JEDEC J-STD-020C for surface mount device (SMD) package reflow profiles and conditions. Unless otherwise stated, the temperature and time are for Sn-Pb (STD) only.
(5) ESD rating is based on the human body model, 100 pF discharged through 1.5 kΩ.

Operating Conditions (1)

Input Voltage		26V
Temperature Range	LM2940-N NDE, LM2940-N KTT	−40°C ≤ T_J ≤ 125°C
	LM2940C NDE, LM2940C KTT	0°C ≤ T_J ≤ 125°C
	LM2940-N DCY	−40°C ≤ T_A ≤ 85°C
	LM2940-N NFE, LM2940-N NAC	−55°C ≤ T_J ≤ 125°C
	LM2940-N NGN	−40°C ≤ T_J ≤ 125°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Conditions are conditions under which the device functions but the specifications might not be ensured. For ensured specifications and test conditions see the Electrical Characteristics.

Electrical Characteristics

$V_{IN} = V_O + 5V$, $I_O = 1A$, $C_O = 22\ \mu F$, unless otherwise specified. **Boldface limits apply over the entire operating temperature range of the indicated device.** All other specifications apply for $T_A = T_J = 25°C$.

Output Voltage (V_O)		5V			8V			Units
Parameter	**Conditions**	**Typ**	**LM2940-N Limit (1)**	**LM2940-N/883 Limit (2)**	**Typ**	**LM2940-N Limit (1)**	**LM2940-N/883 Limit (2)**	
Output Voltage	5 mA ≤ I_O ≤ 1A		**6.25V ≤ V_{IN} ≤ 26V**			**9.4V ≤ V_{IN} ≤ 26V**		
		5.00	4.85/**4.75**	4.85/**4.75**	8.00	7.76/**7.60**	7.76/**7.60**	V_{MIN}
			5.15/**5.25**	5.15/**5.25**		8.24/**8.40**	8.24/**8.40**	V_{MAX}
Line Regulation	V_O + 2V ≤ V_{IN} ≤ 26V, I_O = 5 mA	20	50	40/**50**	20	80	50/**80**	mV_{MAX}
Load Regulation	50 mA ≤ I_O ≤ 1A							
	LM2940-N, LM2940-N/883	35	50/**80**	50/**100**	55	80/**130**	80/**130**	mV_{MAX}
	LM2940C	35	50		55	80		
Output Impedance	100 mADC and 20 mArms, f_O = 120 Hz	35		1000/**1000**	55		1000/**1000**	mΩ
Quiescent Current	V_O +2V ≤ V_{IN} ≤ 26V, I_O = 5 mA							
	LM2940-N, LM2940-N/883	10	15/**20**	15/**20**	10	15/**20**	15/**20**	mA_{MAX}
	LM2940C	10	15					
	$V_{IN} = V_O + 5V$, I_O = 1A	30	45/**60**	50/**60**	30	45/**60**	50/**60**	mA_{MAX}
Output Noise Voltage	10 Hz − 100 kHz, I_O = 5 mA	150		700/**700**	240		1000/**1000**	μV_{rms}
Ripple Rejection	f_O = 120 Hz, 1 V_{rms}, I_O = 100 mA							
	LM2940-N	72	60/**54**		66	54/**48**		dB_{MIN}
	LM2940C	72	60		66	54		
	f_O = 1 kHz, 1 V_{rms}, I_O = 5 mA			60/**50**			54/**48**	dB_{MIN}
Long Term Stability		20			32			mV/ 1000 Hr
Dropout Voltage	I_O = 1A	0.5	0.8/**1.0**	0.7/**1.0**	0.5	0.8/**1.0**	0.7/**1.0**	V_{MAX}
	I_O = 100 mA	110	150/**200**	150/**200**	110	150/**200**	150/**200**	mV_{MAX}
Short Circuit Current	See (3)	1.9	1.6	1.5/**1.3**	1.9	1.6	1.6/**1.3**	A_{MIN}
Maximum Line Transient	R_O = 100Ω							
	LM2940-N, T ≤ 100 ms	75	60/**60**		75	60/**60**		V_{MIN}
	LM2940-N/883, T ≤ 20 ms			40/**40**			40/**40**	
	LM2940C, T ≤ 1 ms	55	45		55	45		
Reverse Polarity DC Input Voltage	R_O = 100Ω							
	LM2940-N, LM2940-N/883	−30	−15/**−15**	−15/**−15**	−30	−15/**−15**	−15/**−15**	V_{MIN}
	LM2940C	−30	−15		−30	−15		

(1) All limits are specified at $T_A = T_J = 25°C$ only (standard typeface) or over the entire operating temperature range of the indicated device (boldface type). All limits at $T_A = T_J = 25°C$ are 100% production tested. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control methods.

(2) All limits are specified at $T_A = T_J = 25°C$ only (standard typeface) or over the entire operating temperature range of the indicated device (boldface type). All limits are 100% production tested and are used to calculate Outgoing Quality Levels.

(3) Output current will decrease with increasing temperature but will not drop below 1A at the maximum specified temperature.

Electrical Characteristics (continued)

V_{IN} = V_O + 5V, I_O = 1A, C_O = 22 µF, unless otherwise specified. **Boldface limits apply over the entire operating temperature range of the indicated device.** All other specifications apply for T_A = T_J = 25°C.

Output Voltage (V_O)		5V			8V			Units
Parameter	Conditions	Typ	LM2940-N Limit(1)	LM2940-N/883 Limit(2)	Typ	LM2940-N Limit(1)	LM2940-N/883 Limit(2)	
Reverse Polarity Transient Input Voltage	R_O = 100Ω							V_{MIN}
	LM2940-N, T ≤ 100 ms	−75	−50/**−50**		−75	−50/**−50**		
	LM2940-N/883, T ≤ 20 ms			−45/**−45**			−45/**−45**	
	LM2940C, T ≤ 1 ms	−55	−45/**−45**					

Electrical Characteristics

V_{IN} = V_O + 5V, I_O = 1A, C_O = 22 µF, unless otherwise specified. **Boldface limits apply over the entire operating temperature range of the indicated device.** All other specifications apply for T_A = T_J = 25°C.

Output Voltage (V_O)		9V		10V		Units
Parameter	Conditions	Typ	LM2940-N Limit (1)	Typ	LM2940-N Limit (1)	
Output Voltage		**10.5V ≤ V_{IN} ≤ 26V**		**11.5V ≤ V_{IN} ≤ 26V**		
	5 mA ≤ I_O ≤1A	9.00	8.73/**8.55**	10.00	9.70/**9.50**	V_{MIN}
			9.27/**9.45**		10.30/**10.50**	V_{MAX}
Line Regulation	V_O + 2V ≤ V_{IN} ≤ 26V, I_O = 5 mA	20	90	20	100	mV_{MAX}
Load Regulation	50 mA ≤ I_O ≤ 1A					
	LM2940-N	60	90/**150**	65	100/**165**	mV_{MAX}
	LM2940C	60	90			
Output Impedance	100 mADC and 20 mArms, f_O = 120 Hz	60		65		mΩ
Quiescent Current	V_O +2V ≤ V_{IN} < 26V, I_O = 5 mA					
	LM2940-N	10	15/**20**	10	15/**20**	mA_{MAX}
	LM2940C	10	15			
	V_{IN} = V_O + 5V, I_O = 1A	30	45/**60**	30	45/**60**	mA_{MAX}
Output Noise Voltage	10 Hz − 100 kHz, I_O = 5 mA	270		300		$µV_{rms}$
Ripple Rejection	f_O = 120 Hz, 1 V_{rms}, I_O = 100 mA					
	LM2940-N	64	52/**46**	63	51/**45**	dB_{MIN}
	LM2940C	64	52			
Long Term Stability		34		36		mV/ 1000 Hr
Dropout Voltage	I_O = 1A	0.5	0.8/**1.0**	0.5	0.8/**1.0**	V_{MAX}
	I_O = 100 mA	110	150/**200**	110	150/**200**	mV_{MAX}
Short Circuit Current	See (2)	1.9	1.6	1.9	1.6	A_{MIN}

(1) All limits are specified at T_A = T_J = 25°C only (standard typeface) or over the entire operating temperature range of the indicated device (boldface type). All limits at T_A = T_J = 25°C are 100% production tested. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control methods.
(2) Output current will decrease with increasing temperature but will not drop below 1A at the maximum specified temperature.

Electrical Characteristics (continued)

V_{IN} = V_O + 5V, I_O = 1A, C_O = 22 µF, unless otherwise specified. **Boldface limits apply over the entire operating temperature range of the indicated device.** All other specifications apply for T_A = T_J = 25°C.

Output Voltage (V_O)		9V		10V		Units
Parameter	Conditions	Typ	LM2940-N Limit (1)	Typ	LM2940-N Limit (1)	
Maximum Line Transient	R_O = 100Ω T ≤ 100 ms					
	LM2940-N	75	60/**60**	75	60/**60**	V_{MIN}
	LM2940C	55	45			
Reverse Polarity DC Input Voltage	R_O = 100Ω					
	LM2940-N	−30	−15/**−15**	−30	−15/**−15**	V_{MIN}
	LM2940C	−30	−15			
Reverse Polarity Transient Input Voltage	R_O = 100Ω T ≤ 100 ms					
	LM2940-N	−75	−50/**−50**	−75	−50/**−50**	V_{MIN}
	LM2940C	−55	−45/**−45**			

Electrical Characteristics

V_{IN} = V_O + 5V, I_O = 1A, C_O = 22 µF, unless otherwise specified. **Boldface limits apply over the entire operating temperature range of the indicated device.** All other specifications apply for T_A = T_J = 25°C.

Output Voltage (V_O)		12V			15V			Units
Parameter	Conditions	Typ	LM2940-N Limit (1)	LM2940-N/833 Limit (2)	Typ	LM2940-N Limit (1)	LM2940-N/833 Limit (2)	
Output Voltage		**13.6V ≤ V_{IN} ≤ 26V**			**16.75V ≤ V_{IN} ≤ 26V**			
	5 mA ≤ I_O ≤1A	12.00	11.64/**11.40**	11.64/**11.40**	15.00	14.55/**14.25**	14.55/**14.25**	V_{MIN}
			12.36/**12.60**	12.36/**12.60**		15.45/**15.75**	15.45/**15.75**	V_{MAX}
Line Regulation	V_O + 2V ≤ V_{IN} ≤ 26V, I_O = 5 mA	20	120	75/**120**	20	150	95/**150**	mV_{MAX}
Load Regulation	50 mA ≤ I_O ≤ 1A							
	LM2940-N, LM2940-N/883	55	120/**200**	120/**190**			150/**240**	mV_{MAX}
	LM2940C	55	120		70	150		
Output Impedance	100 mADC and 20 mArms, f_O = 120 Hz	80		1000/**1000**	100		1000/**1000**	mΩ
Quiescent Current	V_O +2V ≤ V_{IN} ≤ 26V, I_O = 5 mA							
	LM2940-N, LM2940-N/883	10	15/**20**	15/**20**			15/**20**	mA_{MAX}
	LM2940C	10	15		10	15		
	V_{IN} = V_O + 5V, I_O = 1A	30	45/**60**	50/**60**	30	45/**60**	50/**60**	mA_{MAX}
Output Noise Voltage	10 Hz − 100 kHz, I_O = 5 mA	360		1000/**1000**	450		1000/**1000**	$µV_{rms}$

(1) All limits are specified at T_A = T_J = 25°C only (standard typeface) or over the entire operating temperature range of the indicated device (boldface type). All limits at T_A = T_J = 25°C are 100% production tested. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control methods.

(2) All limits are specified at T_A = T_J = 25°C only (standard typeface) or over the entire operating temperature range of the indicated device (boldface type). All limits are 100% production tested and are used to calculate Outgoing Quality Levels.

Electrical Characteristics (continued)

V_{IN} = V_O + 5V, I_O = 1A, C_O = 22 µF, unless otherwise specified. **Boldface limits apply over the entire operating temperature range of the indicated device.** All other specifications apply for T_A = T_J = 25°C.

Output Voltage (V_O)		12V			15V			Units
Parameter	**Conditions**	**Typ**	**LM2940-N Limit (1)**	**LM2940-N/833 Limit (2)**	**Typ**	**LM2940-N Limit (1)**	**LM2940-N/833 Limit (2)**	
Ripple Rejection	f_O = 120 Hz, 1 V_{rms}, I_O = 100 mA							
	LM2940-N	66	54/**48**					dB_{MIN}
	LM2940C	66	54		64	52		
	f_O = 1 kHz, 1 V_{rms}, I_O = 5 mA			52/**46**			48/**42**	dB_{MIN}
Long Term Stability		48			60			mV/ 1000 Hr
Dropout Voltage	I_O = 1A	0.5	0.8/**1.0**	0.7/**1.0**	0.5	0.8/**1.0**	0.7/**1.0**	V_{MAX}
	I_O = 100 mA	110	150/**200**	150/**200**	110	150/**200**	150/**200**	mV_{MAX}
Short Circuit Current	See (3)	1.9	1.6	1.6/**1.3**	1.9	1.6	1.6/**1.3**	A_{MIN}
Maximum Line Transient	R_O = 100Ω							
	LM2940-N, T ≤ 100 ms	75	60/**60**					
	LM2940-N/883, T ≤ 20 ms			40/**40**			40/**40**	V_{MIN}
	LM2940C, T ≤ 1 ms	55	45		55	45		
Reverse Polarity DC Input Voltage	R_O = 100Ω							
	LM2940-N, LM2940-N/883	−30	−15/**−15**	−15/**−15**			−15/**−15**	V_{MIN}
	LM2940C	−30	−15		−30	−15		
Reverse Polarity Transient Input Voltage	R_O = 100Ω							
	LM2940-N, T ≤ 100 ms	−75	−50/**−50**					
	LM2940-N/883, T ≤ 20 ms			−45/**−45**			−45/**−45**	V_{MIN}
	LM2940C, T ≤ 1 ms	−55	−45/**−45**		−55	−45/**−45**		

(3) Output current will decrease with increasing temperature but will not drop below 1A at the maximum specified temperature.

Thermal Performance

Thermal Resistance Junction-to-Case, $\theta_{(JC)}$	3-Lead TO-220	4	°C/W
	3-Lead DDPAK/TO-263	4	
Thermal Resistance Junction-to-Ambient, $\theta_{(JA)}$	3-Lead TO-220 (1)	60	°C/W
	3-Lead DDPAK/TO-263 (1)	80	
	SOT-223 (1)	174	
	8-Lead WSON (1)	35	

(1) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. The value of θ_{JA} (for devices in still air with no heatsink) is 60°C/W for the TO-220 package, 80°C/W for the DDPAK/TO-263 package, and 174°C/W for the SOT-223 package. The effective value of θ_{JA} can be reduced by using a heatsink (see Application Hints for specific information on heatsinking). The value of θ_{JA} for the WSON package is specifically dependent on PCB trace area, trace material, and the number of layers and thermal vias. For improved thermal resistance and power dissipation for the WSON package, refer to Application Note AN-1187 (SNOA401). It is recommended that 6 vias be placed under the center pad to improve thermal performance.

Typical Performance Characteristics

Dropout Voltage

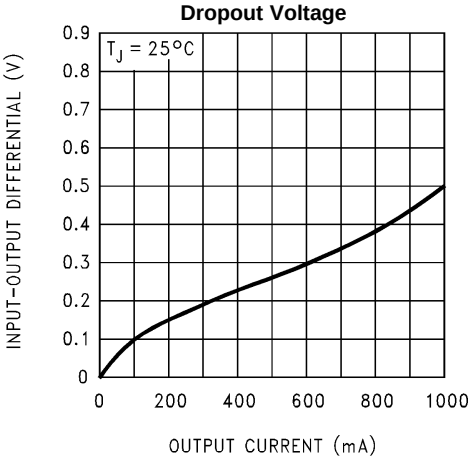


Figure 8.

Dropout Voltage vs. Temperature

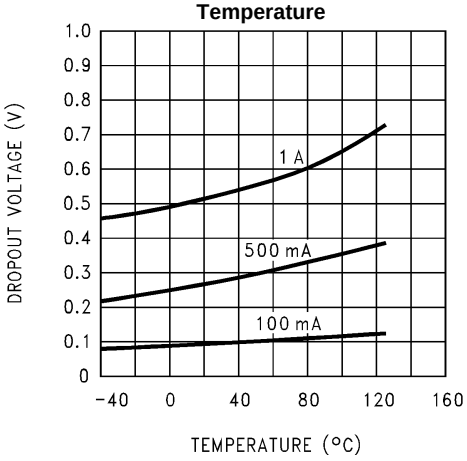


Figure 9.

Output Voltage vs. Temperature

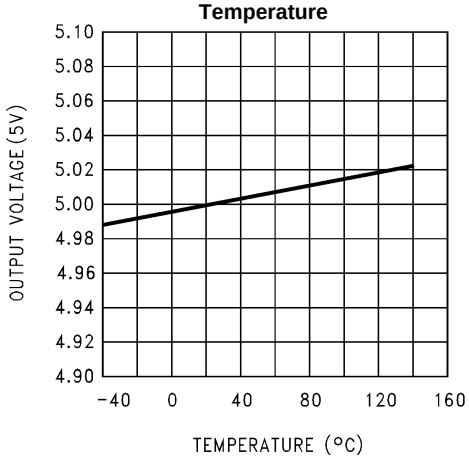


Figure 10.

Quiescent Current vs. Temperature

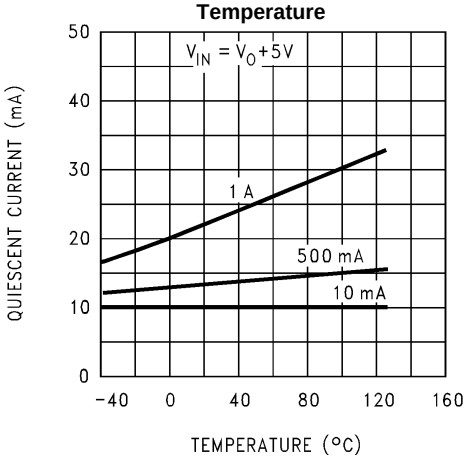


Figure 11.

Quiescent Current

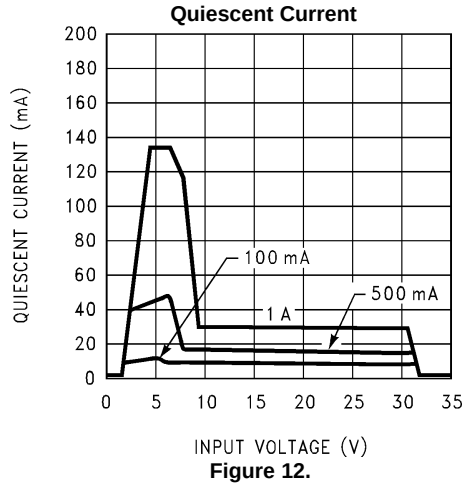


Figure 12.

Quiescent Current

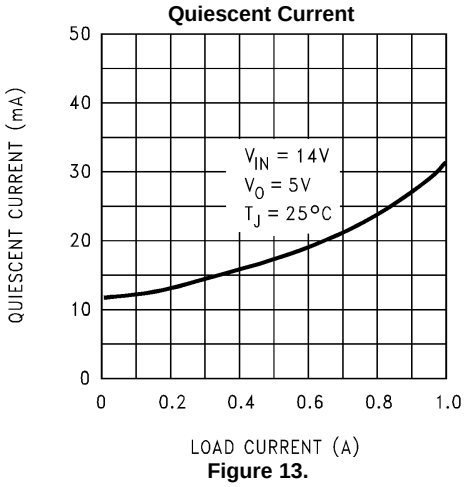


Figure 13.

Typical Performance Characteristics (continued)

Line Transient Response

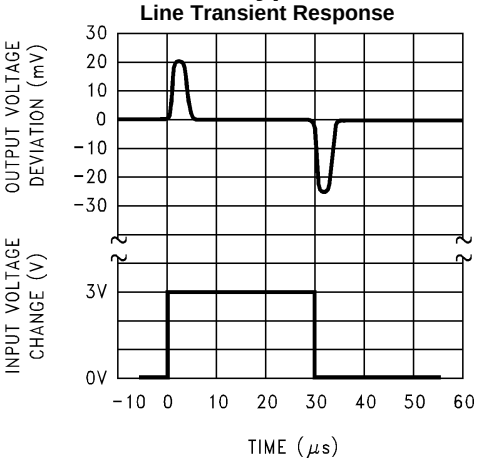


Figure 14.

Load Transient Response

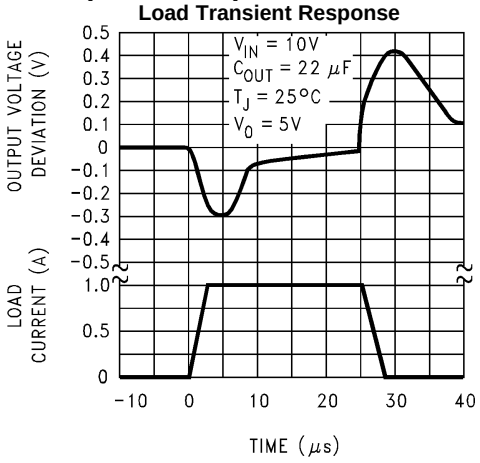


Figure 15.

Ripple Rejection

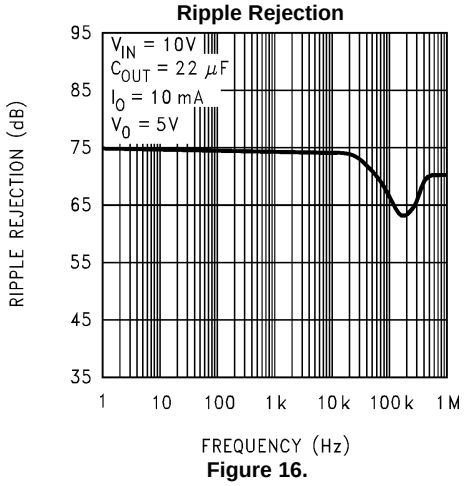


Figure 16.

Low Voltage Behavior

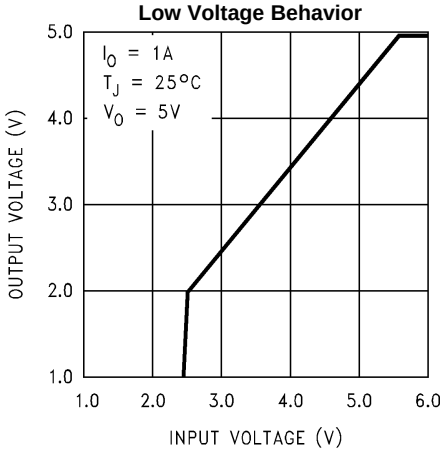


Figure 17.

Low Voltage Behavior

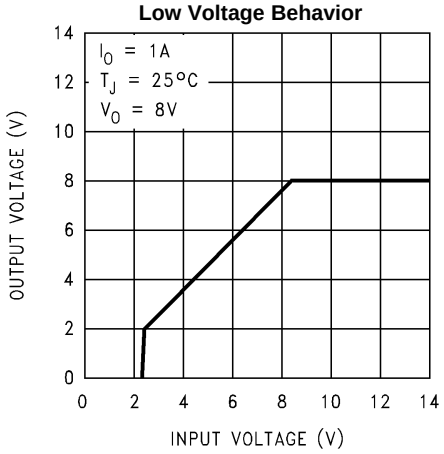


Figure 18.

Low Voltage Behavior

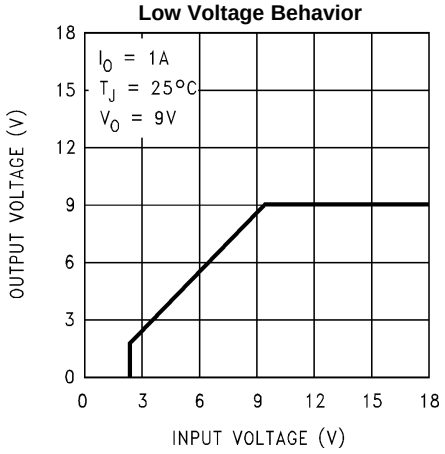


Figure 19.

Typical Performance Characteristics (continued)

Low Voltage Behavior

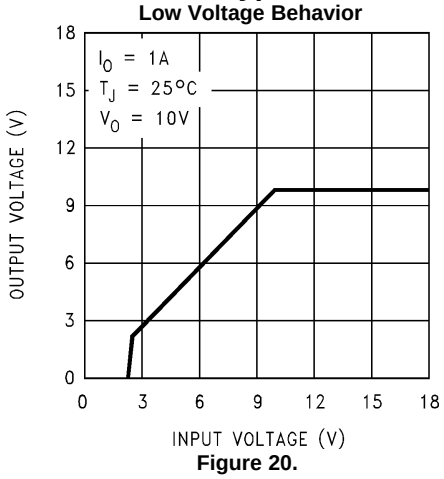


Figure 20.

Low Voltage Behavior

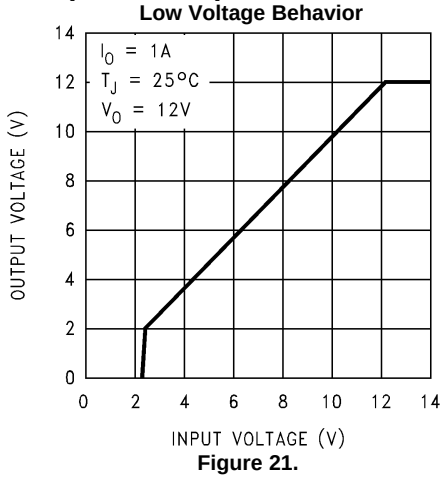


Figure 21.

Low Voltage Behavior

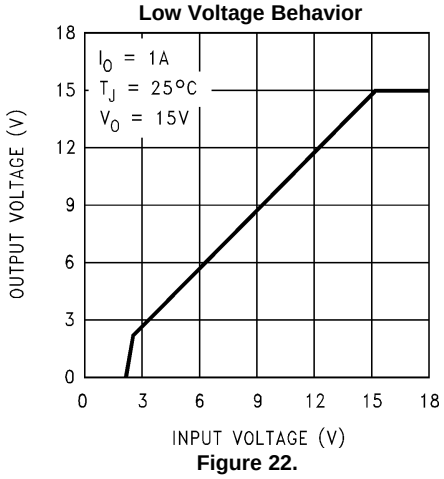


Figure 22.

Output at Voltage Extremes

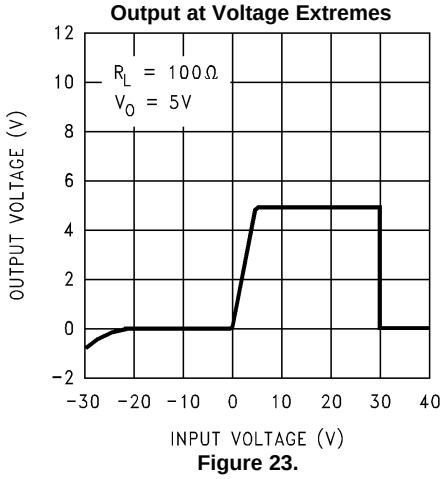


Figure 23.

Output at Voltage Extremes

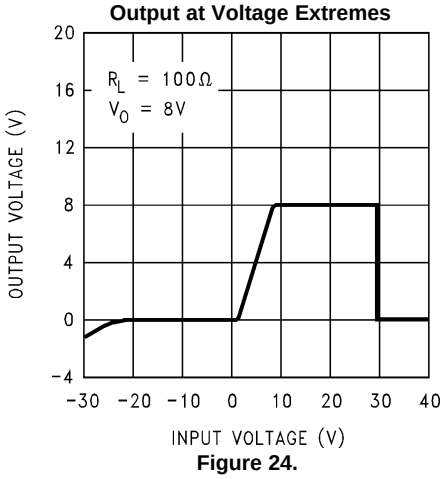


Figure 24.

Output at Voltage Extremes

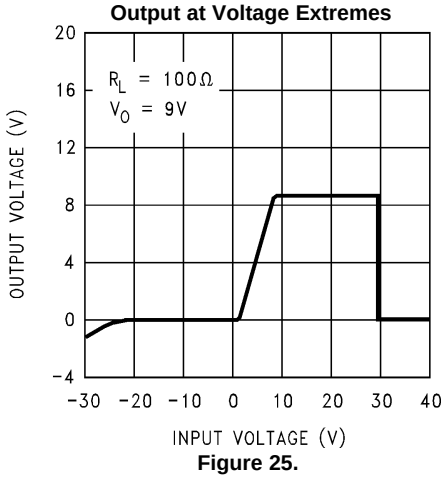


Figure 25.

Typical Performance Characteristics (continued)

Output at Voltage Extremes

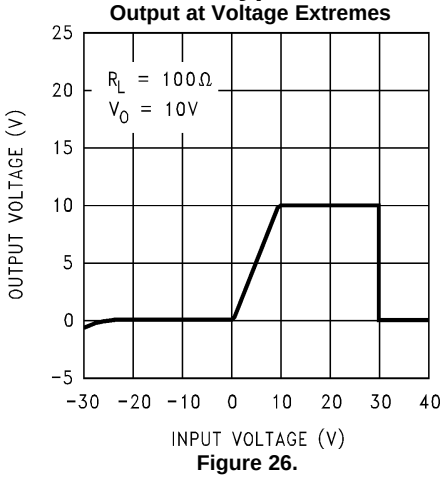


Figure 26.

Output at Voltage Extremes

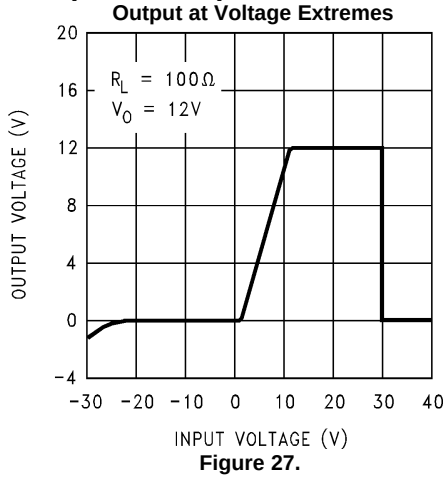


Figure 27.

Output at Voltage Extremes

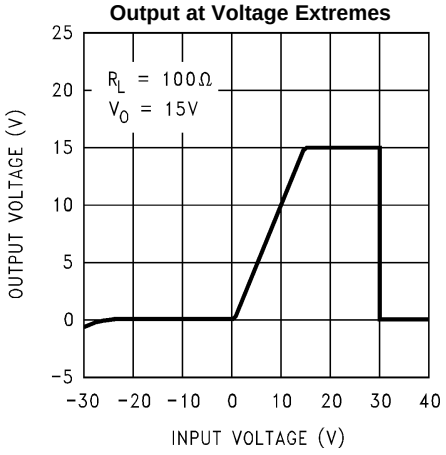


Figure 28.

Output Capacitor ESR

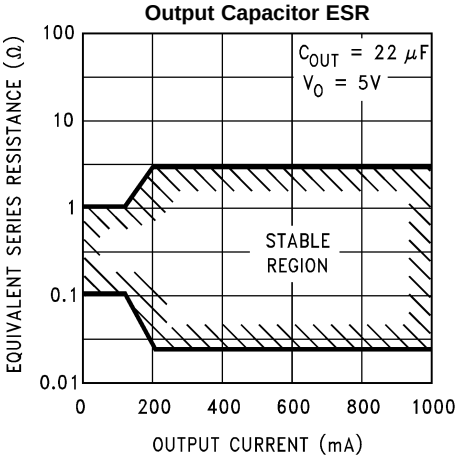


Figure 29.

Peak Output Current

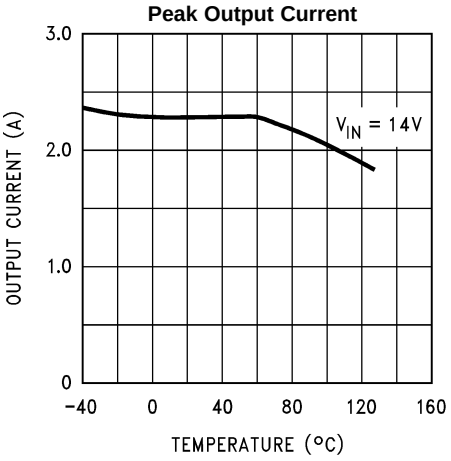


Figure 30.

Output Impedance

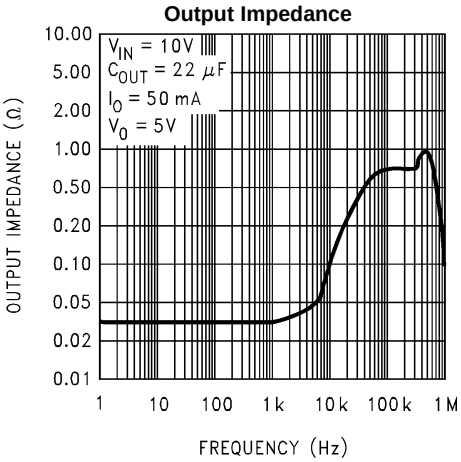


Figure 31.

Typical Performance Characteristics (continued)

Maximum Power Dissipation (TO-220)

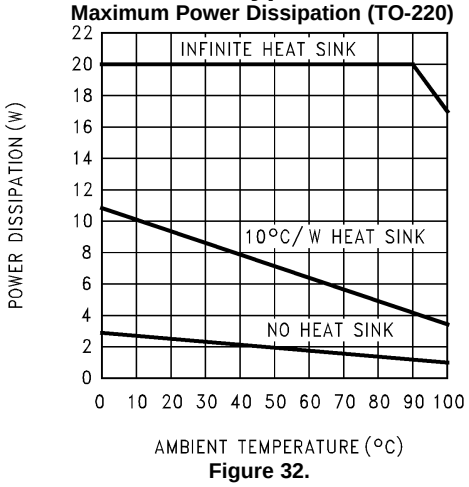


Figure 32.

Maximum Power Dissipation (SOT-223)

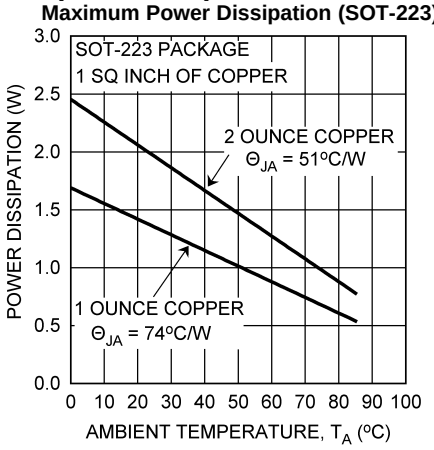


Figure 33.

Maximum Power Dissipation (DDPAK/TO-263)

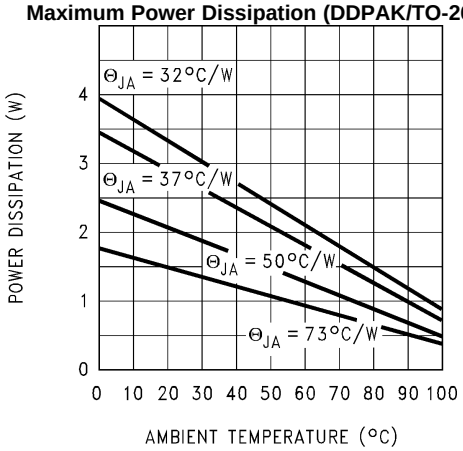
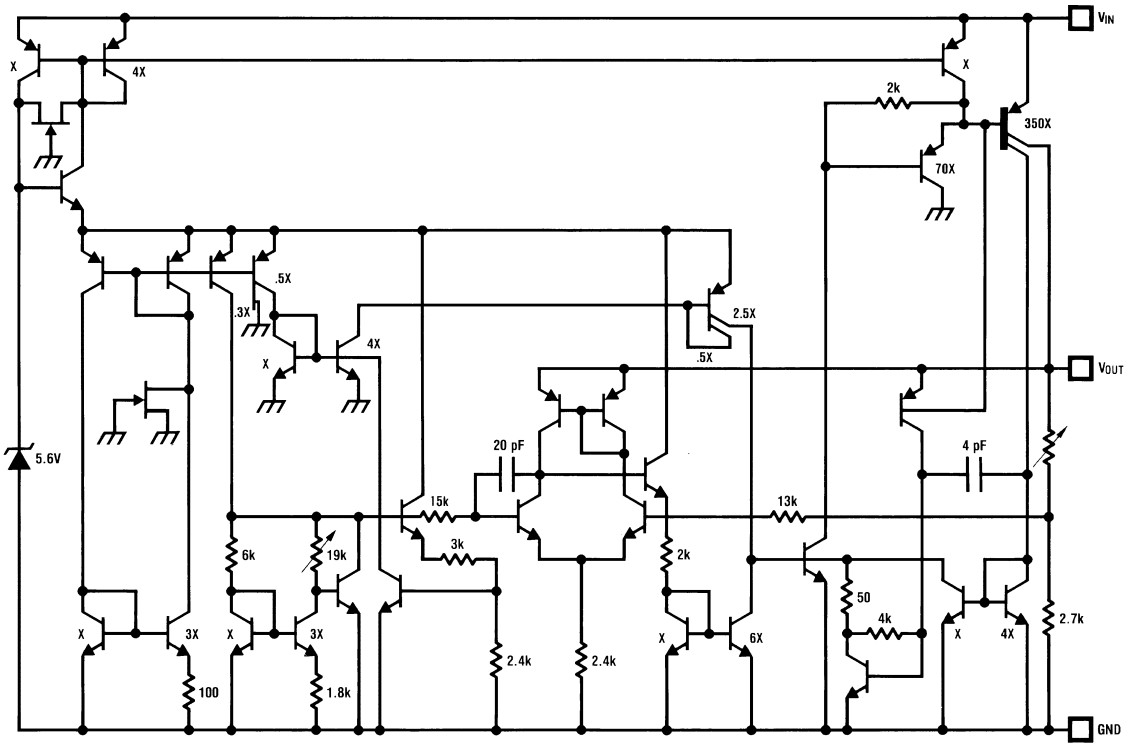


Figure 34.

Equivalent Schematic Diagram



APPLICATION INFORMATION

EXTERNAL CAPACITORS

The output capacitor is critical to maintaining regulator stability, and must meet the required conditions for both ESR (Equivalent Series Resistance) and minimum amount of capacitance.

MINIMUM CAPACITANCE:

The minimum output capacitance required to maintain stability is 22 µF (this value may be increased without limit). Larger values of output capacitance will give improved transient response.

ESR LIMITS:

The ESR of the output capacitor will cause loop instability if it is too high or too low. The acceptable range of ESR plotted versus load current is shown in the graph below. ***It is essential that the output capacitor meet these requirements, or oscillations can result.***

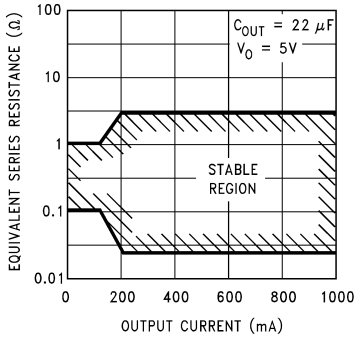


Figure 35. Output Capacitor ESR Limits

It is important to note that for most capacitors, ESR is specified only at room temperature. However, the designer must ensure that the ESR will stay inside the limits shown over the entire operating temperature range for the design.

For aluminum electrolytic capacitors, ESR will increase by about 30X as the temperature is reduced from 25°C to −40°C. This type of capacitor is not well-suited for low temperature operation.

Solid tantalum capacitors have a more stable ESR over temperature, but are more expensive than aluminum electrolytics. A cost-effective approach sometimes used is to parallel an aluminum electrolytic with a solid Tantalum, with the total capacitance split about 75/25% with the Aluminum being the larger value.

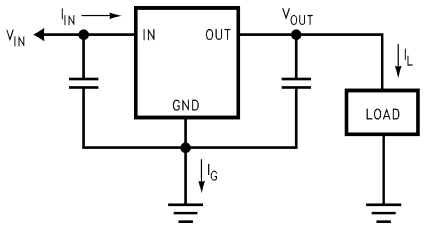
If two capacitors are paralleled, the effective ESR is the parallel of the two individual values. The “flatter” ESR of the Tantalum will keep the effective ESR from rising as quickly at low temperatures.

HEATSINKING

A heatsink may be required depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible operating conditions, the junction temperature must be within the range specified under Absolute Maximum Ratings.

To determine if a heatsink is required, the power dissipated by the regulator, P_D, must be calculated.

The figure below shows the voltages and currents which are present in the circuit, as well as the formula for calculating the power dissipated in the regulator:



$I_{IN} = I_L + I_G$
$P_D = (V_{IN} - V_{OUT})\ I_L + (V_{IN})\ I_G$

Figure 36. Power Dissipation Diagram

The next parameter which must be calculated is the maximum allowable temperature rise, $T_{R(MAX)}$. This is calculated by using the formula:

$$T_{R(MAX)} = T_{J(MAX)} - T_{A(MAX)}$$

where

- $T_{J(MAX)}$ is the maximum allowable junction temperature, which is 125°C for commercial grade parts.
- $T_{A(MAX)}$is the maximum ambient temperature which will be encountered in the application. (1)

Using the calculated values for $T_{R(MAX)}$ and P_D, the maximum allowable value for the junction-to-ambient thermal resistance, $\theta_{(JA)}$, can now be found:

$$\theta_{(JA)} = T_{R(MAX)} / P_D \quad (2)$$

NOTE

If the maximum allowable value for $\theta_{(JA)}$ is found to be ≥ 53°C/W for the TO-220 package, ≥ 80°C/W for the DDPAK/TO-263 package, or ≥ 174°C/W for the SOT-223 package, no heatsink is needed since the package alone will dissipate enough heat to satisfy these requirements.

If the calculated value for $\theta_{(JA)}$falls below these limits, a heatsink is required.

HEATSINKING TO-220 PACKAGE PARTS

The TO-220 can be attached to a typical heatsink, or secured to a copper plane on a PC board. If a copper plane is to be used, the values of $\theta_{(JA)}$ will be the same as shown in the next section for the DDPAK/TO-263.

If a manufactured heatsink is to be selected, the value of heatsink-to-ambient thermal resistance, $\theta_{(H-A)}$, must first be calculated:

$$\theta_{(H-A)} = \theta_{(JA)} - \theta_{(C-H)} - \theta_{(J-C)}$$

where

- $\theta_{(J-C)}$ is defined as the thermal resistance from the junction to the surface of the case. A value of 3°C/W can be assumed for $\theta_{(J-C)}$ for this calculation.
- $\theta_{(C-H)}$ is defined as the thermal resistance between the case and the surface of the heatsink. The value of $\theta_{(C-H)}$ will vary from about 1.5°C/W to about 2.5°C/W (depending on method of attachment, insulator, etc.). If the exact value is unknown, 2°C/W should be assumed for $\theta_{(C-H)}$. (3)

When a value for $\theta_{(H-A)}$ is found using the equation shown, *a heatsink must be selected that has a value that is less than or equal to this number.*

$\theta_{(H-A)}$ is specified numerically by the heatsink manufacturer in the catalog, or shown in a curve that plots temperature rise vs power dissipation for the heatsink.

HEATSINKING DDPAK/TO-263 PACKAGE PARTS

The DDPAK/TO-263 (KTT) package uses a copper plane on the PCB and the PCB itself as a heatsink. To optimize the heat sinking ability of the plane and PCB, solder the tab of the package to the plane.

Figure 37 shows for the DDPAK/TO-263 the measured values of $\theta_{(JA)}$ for different copper area sizes using a typical PCB with 1 ounce copper *and no solder mask over the copper area used for heatsinking.*

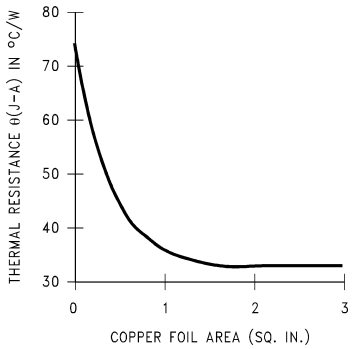


Figure 37. $\theta_{(JA)}$ vs. Copper (1 ounce) Area for the DDPAK/TO-263 Package

As shown in the figure, increasing the copper area beyond 1 square inch produces very little improvement. It should also be observed that the minimum value of $\theta_{(JA)}$ for the DDPAK/TO-263 package mounted to a PCB is 32°C/W.

As a design aid, Figure 38 shows the maximum allowable power dissipation compared to ambient temperature for the DDPAK/TO-263 device. This assumes a $\theta_{(JA)}$ of 35°C/W for 1 square inch of 1 ounce copper and a maximum junction temperature (T_J) of 125°C.

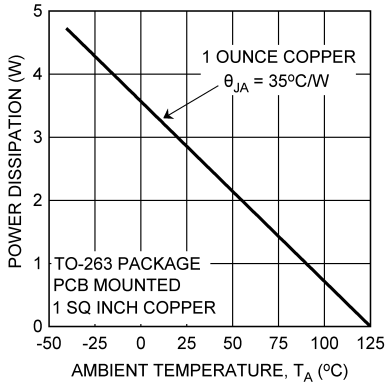


Figure 38. Maximum Power Dissipation vs. T_A for the DDPAK/TO-263 Package

HEATSINKING SOT-223 PACKAGE PARTS

The SOT-223 (DCY) packages use a copper plane on the PCB and the PCB itself as a heatsink. To optimize the heat sinking ability of the plane and PCB, solder the tab of the package to the plane.

Figure 39 and Figure 40 show the information for the SOT-223 package. Figure 40 assumes a $\theta_{(JA)}$ of 74°C/W for 1 square inch of 1 ounce copper and 51°C/W for 1 square inch of 2 ounce copper, with a maximum ambient temperature (T_A) of 85°C and a maximum junction temperature (T_J) of 125°C.

For techniques for improving the thermal resistance and power dissipation for the SOT-223 package, please refer to Application Note AN-1028 (SNVA036).

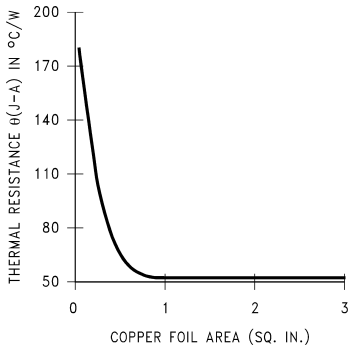


Figure 39. $\theta_{(JA)}$ vs. Copper (2 ounce) Area for the SOT-223 Package

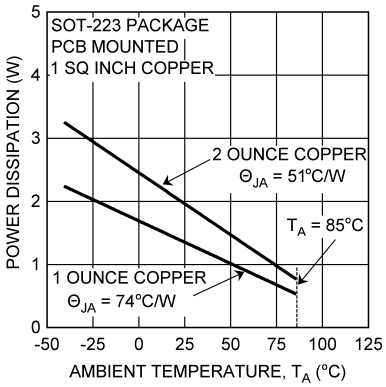


Figure 40. Maximum Power Dissipation vs. T_A for the SOT-223 Package

HEATSINKING WSON PACKAGE PARTS

The value of θ_{JA} for the WSON package is specifically dependent on PCB trace area, trace material, and the number of layers and thermal vias. It is recommended that a minimum of 6 thermal vias be placed under the center pad to improve thermal performance.

For techniques for improving the thermal resistance and power dissipation for the WSON package, please refer to Application Note AN-1187 (SNOA401).

REVISION HISTORY

Changes from Revision H (April 2013) to Revision I	Page
• Changed layout of National Data Sheet to TI format	17

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM2940CS-12	ACTIVE	DDPAK/ TO-263	KTT	3	45	TBD	Call TI	Call TI	0 to 125	LM2940CS -12 P+	Samples
LM2940CS-12/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	0 to 125	LM2940CS -12 P+	Samples
LM2940CS-15	ACTIVE	DDPAK/ TO-263	KTT	3	45	TBD	Call TI	Call TI	0 to 125	LM2940CS -15 P+	Samples
LM2940CS-15/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	0 to 125	LM2940CS -15 P+	Samples
LM2940CS-5.0	ACTIVE	DDPAK/ TO-263	KTT	3	45	TBD	Call TI	Call TI	0 to 125	LM2940CS -5.0 P+	Samples
LM2940CS-5.0/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	0 to 125	LM2940CS -5.0 P+	Samples
LM2940CS-9.0	ACTIVE	DDPAK/ TO-263	KTT	3	45	TBD	Call TI	Call TI	0 to 125	LM2940CS -9.0 P+	Samples
LM2940CS-9.0/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	0 to 125	LM2940CS -9.0 P+	Samples
LM2940CSX-12	ACTIVE	DDPAK/ TO-263	KTT	3	500	TBD	Call TI	Call TI	0 to 125	LM2940CS -12 P+	Samples
LM2940CSX-12/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	0 to 125	LM2940CS -12 P+	Samples
LM2940CSX-15	ACTIVE	DDPAK/ TO-263	KTT	3	500	TBD	Call TI	Call TI	0 to 125	LM2940CS -15 P+	Samples
LM2940CSX-15/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	0 to 125	LM2940CS -15 P+	Samples
LM2940CSX-5.0	ACTIVE	DDPAK/ TO-263	KTT	3	500	TBD	Call TI	Call TI	0 to 125	LM2940CS -5.0 P+	Samples
LM2940CSX-5.0/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	0 to 125	LM2940CS -5.0 P+	Samples
LM2940CSX-9.0	ACTIVE	DDPAK/ TO-263	KTT	3	500	TBD	Call TI	Call TI	0 to 125	LM2940CS -9.0 P+	Samples
LM2940CSX-9.0/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	0 to 125	LM2940CS -9.0 P+	Samples
LM2940CT-12	ACTIVE	TO-220	NDE	3	45	TBD	Call TI	Call TI	0 to 125	LM2940CT -12 P+	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM2940CT-12/NOPB	ACTIVE	TO-220	NDE	3	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	0 to 125	LM2940CT -12 P+	Samples
LM2940CT-15	ACTIVE	TO-220	NDE	3	45	TBD	Call TI	Call TI	0 to 125	LM2940CT -15 P+	Samples
LM2940CT-15/NOPB	ACTIVE	TO-220	NDE	3	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	0 to 125	LM2940CT -15 P+	Samples
LM2940CT-5.0	ACTIVE	TO-220	NDE	3	45	TBD	Call TI	Call TI	0 to 125	LM2940CT -5.0 P+	Samples
LM2940CT-5.0/LF01	ACTIVE	TO-220	NDG	3	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR		LM2940CT -5.0 P+	Samples
LM2940CT-5.0/NOPB	ACTIVE	TO-220	NDE	3	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	0 to 125	LM2940CT -5.0 P+	Samples
LM2940CT-9.0	ACTIVE	TO-220	NDE	3	45	TBD	Call TI	Call TI	0 to 125	LM2940CT -9.0 P+	Samples
LM2940CT-9.0/NOPB	ACTIVE	TO-220	NDE	3	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	0 to 125	LM2940CT -9.0 P+	Samples
LM2940IMP-10	ACTIVE	SOT-223	DCY	4	1000	TBD	Call TI	Call TI	-40 to 85	L55B	Samples
LM2940IMP-10/NOPB	ACTIVE	SOT-223	DCY	4	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L55B	Samples
LM2940IMP-12	ACTIVE	SOT-223	DCY	4	1000	TBD	Call TI	Call TI	-40 to 85	L56B	Samples
LM2940IMP-12/NOPB	ACTIVE	SOT-223	DCY	4	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L56B	Samples
LM2940IMP-15	ACTIVE	SOT-223	DCY	4	1000	TBD	Call TI	Call TI	-40 to 85	L70B	Samples
LM2940IMP-15/NOPB	ACTIVE	SOT-223	DCY	4	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L70B	Samples
LM2940IMP-5.0	ACTIVE	SOT-223	DCY	4	1000	TBD	Call TI	Call TI	-40 to 85	L53B	Samples
LM2940IMP-5.0/NOPB	ACTIVE	SOT-223	DCY	4	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L53B	Samples
LM2940IMP-9.0	ACTIVE	SOT-223	DCY	4	1000	TBD	Call TI	Call TI	-40 to 85	L0EB	Samples
LM2940IMP-9.0/NOPB	ACTIVE	SOT-223	DCY	4	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L0EB	Samples
LM2940IMPX-10	ACTIVE	SOT-223	DCY	4	2000	TBD	Call TI	Call TI	-40 to 85	L55B	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM2940IMPX-10/NOPB	ACTIVE	SOT-223	DCY	4	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L55B	Samples
LM2940IMPX-12	ACTIVE	SOT-223	DCY	4	2000	TBD	Call TI	Call TI	-40 to 85	L56B	Samples
LM2940IMPX-12/NOPB	ACTIVE	SOT-223	DCY	4	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L56B	Samples
LM2940IMPX-5.0	ACTIVE	SOT-223	DCY	4	2000	TBD	Call TI	Call TI	-40 to 85	L53B	Samples
LM2940IMPX-5.0/NOPB	ACTIVE	SOT-223	DCY	4	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L53B	Samples
LM2940IMPX-8.0	ACTIVE	SOT-223	DCY	4	2000	TBD	Call TI	Call TI	-40 to 85	L54B	Samples
LM2940IMPX-8.0/NOPB	ACTIVE	SOT-223	DCY	4	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L54B	Samples
LM2940LD-12	ACTIVE	WSON	NGN	8	1000	TBD	Call TI	Call TI	-40 to 125	L00018B	Samples
LM2940LD-12/NOPB	ACTIVE	WSON	NGN	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L00018B	Samples
LM2940LD-5.0	ACTIVE	WSON	NGN	8	1000	TBD	Call TI	Call TI	-40 to 125	L00014B	Samples
LM2940LD-5.0/NOPB	ACTIVE	WSON	NGN	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L00014B	Samples
LM2940S-10	ACTIVE	DDPAK/ TO-263	KTT	3	45	TBD	Call TI	Call TI	-40 to 125	LM2940S -10 P+	Samples
LM2940S-10/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM2940S -10 P+	Samples
LM2940S-12	ACTIVE	DDPAK/ TO-263	KTT	3	45	TBD	Call TI	Call TI	-40 to 125	LM2940S -12 P+	Samples
LM2940S-12/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM2940S -12 P+	Samples
LM2940S-5.0	ACTIVE	DDPAK/ TO-263	KTT	3	45	TBD	Call TI	Call TI	-40 to 125	LM2940S -5.0 P+	Samples
LM2940S-5.0/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM2940S -5.0 P+	Samples
LM2940S-8.0	ACTIVE	DDPAK/ TO-263	KTT	3	45	TBD	Call TI	Call TI	-40 to 125	LM2940S -8.0 P+	Samples
LM2940S-8.0/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM2940S -8.0 P+	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM2940S-9.0	ACTIVE	DDPAK/ TO-263	KTT	3	45	TBD	Call TI	Call TI	-40 to 125	LM2940S -9.0 P+	Samples
LM2940S-9.0/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM2940S -9.0 P+	Samples
LM2940SX-10	ACTIVE	DDPAK/ TO-263	KTT	3	500	TBD	Call TI	Call TI	-40 to 125	LM2940S -10 P+	Samples
LM2940SX-10/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM2940S -10 P+	Samples
LM2940SX-12	ACTIVE	DDPAK/ TO-263	KTT	3	500	TBD	Call TI	Call TI	-40 to 125	LM2940S -12 P+	Samples
LM2940SX-12/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM2940S -12 P+	Samples
LM2940SX-5.0	ACTIVE	DDPAK/ TO-263	KTT	3	500	TBD	Call TI	Call TI	-40 to 125	LM2940S -5.0 P+	Samples
LM2940SX-5.0/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM2940S -5.0 P+	Samples
LM2940SX-8.0	ACTIVE	DDPAK/ TO-263	KTT	3	500	TBD	Call TI	Call TI	-40 to 125	LM2940S -8.0 P+	Samples
LM2940SX-8.0/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM2940S -8.0 P+	Samples
LM2940SX-9.0	ACTIVE	DDPAK/ TO-263	KTT	3	500	TBD	Call TI	Call TI	-40 to 125	LM2940S -9.0 P+	Samples
LM2940SX-9.0/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM2940S -9.0 P+	Samples
LM2940T-10.0	ACTIVE	TO-220	NDE	3	45	TBD	Call TI	Call TI	-40 to 125	LM2940T 10.0 P+	Samples
LM2940T-10.0/NOPB	ACTIVE	TO-220	NDE	3	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LM2940T 10.0 P+	Samples
LM2940T-12.0	ACTIVE	TO-220	NDE	3	45	TBD	Call TI	Call TI	-40 to 125	LM2940T 12.0 P+	Samples
LM2940T-12.0/NOPB	ACTIVE	TO-220	NDE	3	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LM2940T 12.0 P+	Samples
LM2940T-5.0	ACTIVE	TO-220	NDE	3	45	TBD	Call TI	Call TI	-40 to 125	LM2940T -5.0 P+	Samples
LM2940T-5.0/LF08	ACTIVE	TO-220	NEB	3	45	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR		LM2940T -5.0 P+	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM2940T-5.0/NOPB	ACTIVE	TO-220	NDE	3	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LM2940T -5.0 P+	Samples
LM2940T-8.0	ACTIVE	TO-220	NDE	3	45	TBD	Call TI	Call TI	-40 to 125	LM2940T -8.0 P+	Samples
LM2940T-8.0/NOPB	ACTIVE	TO-220	NDE	3	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LM2940T -8.0 P+	Samples
LM2940T-9.0	ACTIVE	TO-220	NDE	3	45	TBD	Call TI	Call TI	-40 to 125	LM2940T -9.0 P+	Samples
LM2940T-9.0/NOPB	ACTIVE	TO-220	NDE	3	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LM2940T -9.0 P+	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

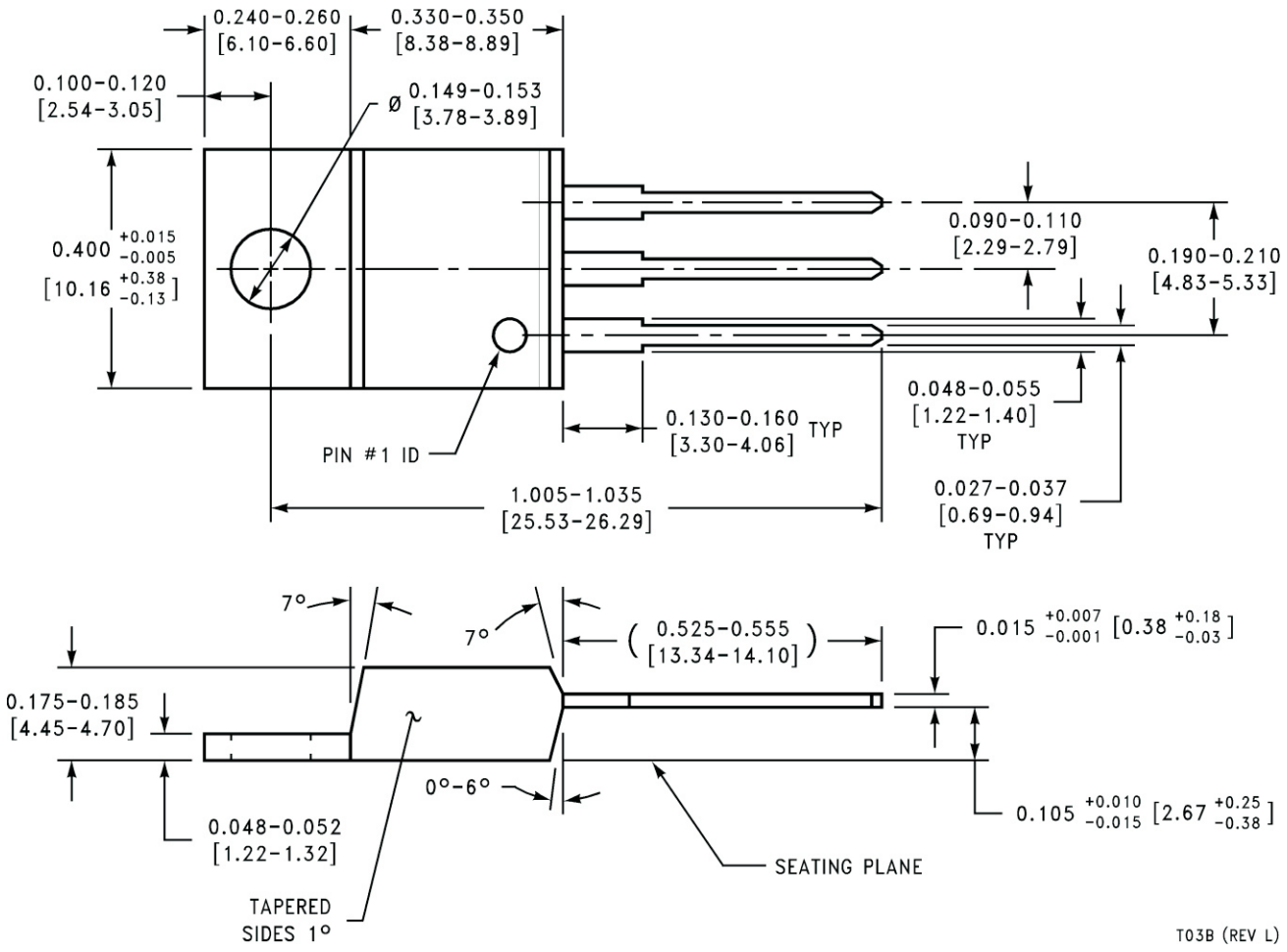
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

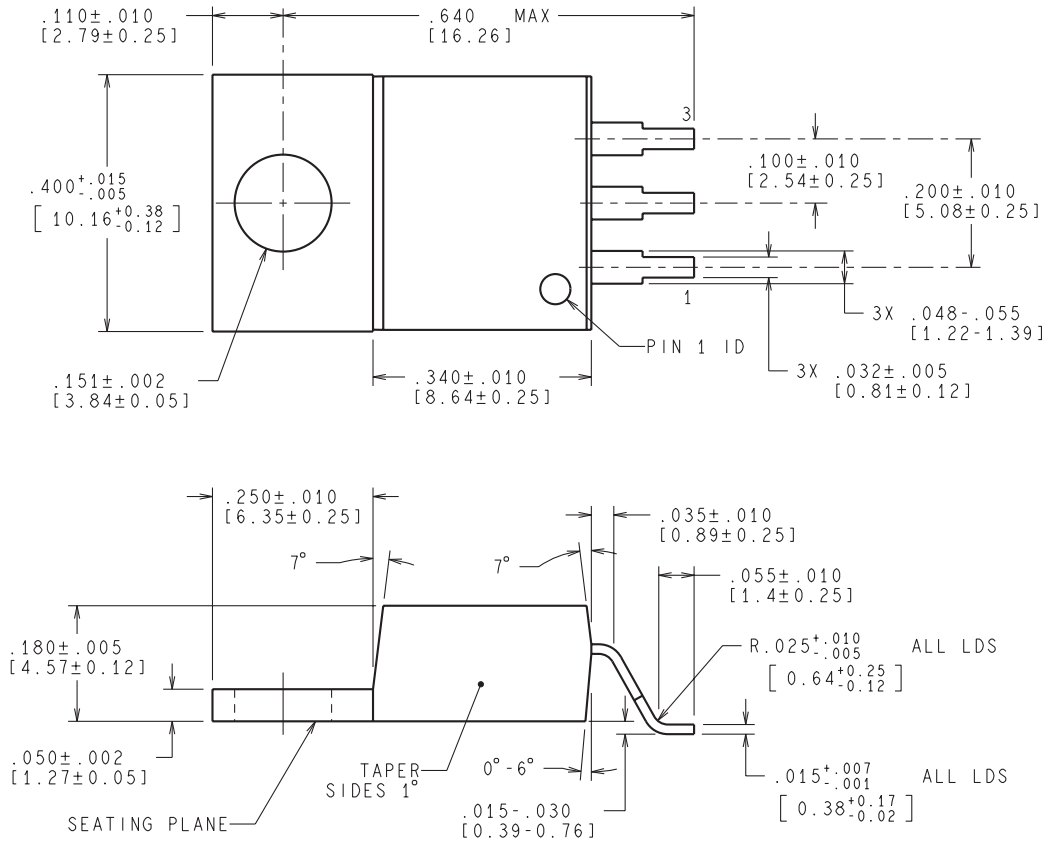
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

NDE0003B


0.240-0.260
[6.10-6.60]
0.330-0.350
[8.38-8.89]
0.100-0.120
[2.54-3.05]
Ø 0.149-0.153
[3.78-3.89]
0.400 +0.015 -0.005
[10.16 +0.38 -0.13]
0.090-0.110
[2.29-2.79]
0.190-0.210
[4.83-5.33]
PIN #1 ID
0.130-0.160 TYP
[3.30-4.06]
0.048-0.055
[1.22-1.40]
TYP
1.005-1.035
[25.53-26.29]
0.027-0.037
[0.69-0.94]
TYP
7°
7°
(0.525-0.555
[13.34-14.10])
0.015 +0.007 -0.001 [0.38 +0.18 -0.03]
0.175-0.185
[4.45-4.70]
0°-6°
0.105 +0.010 -0.015 [2.67 +0.25 -0.38]
0.048-0.052
[1.22-1.32]
SEATING PLANE
TAPERED
SIDES 1°
T03B (REV L)

NDG0003F



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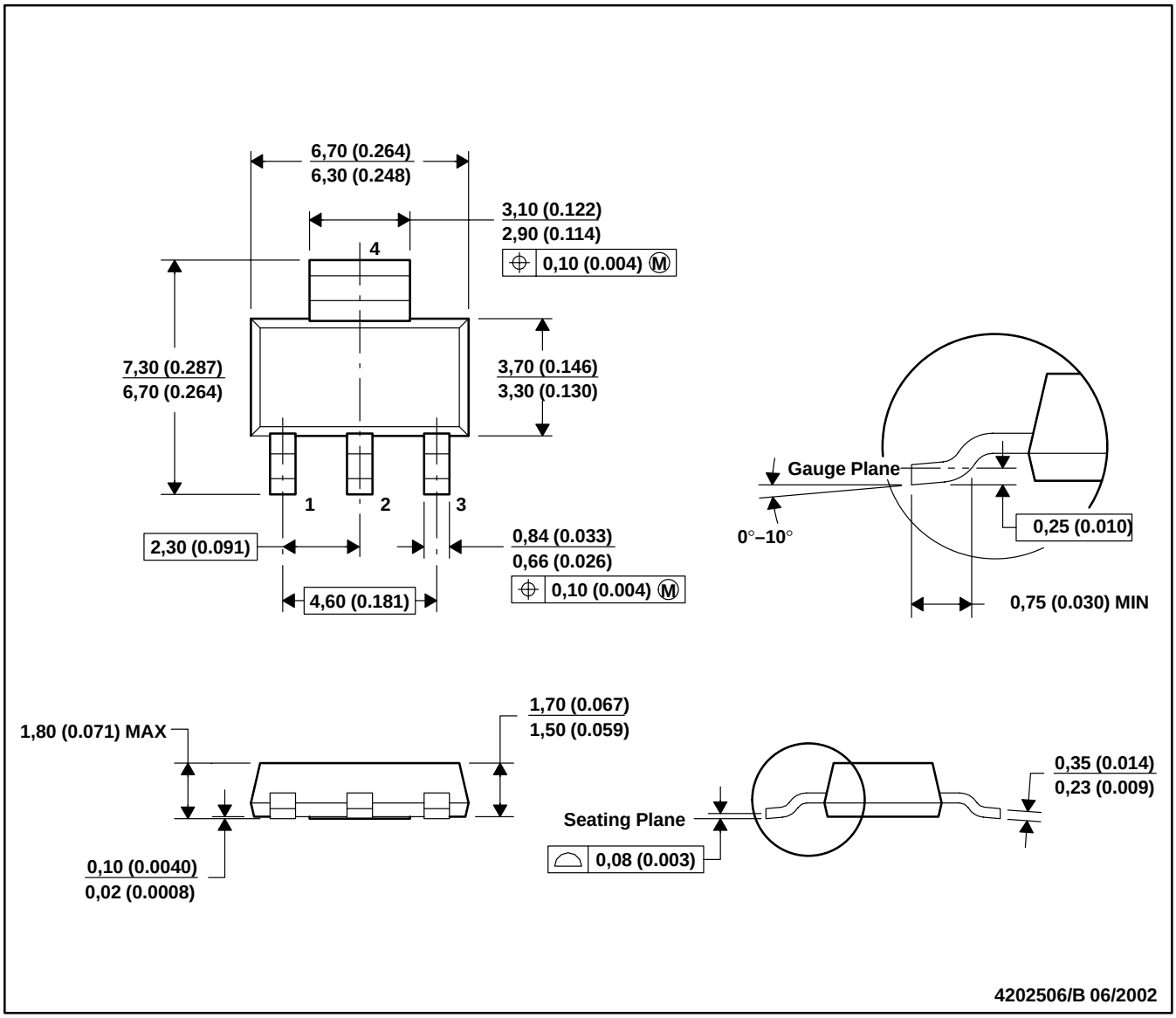
T03F (Rev B)

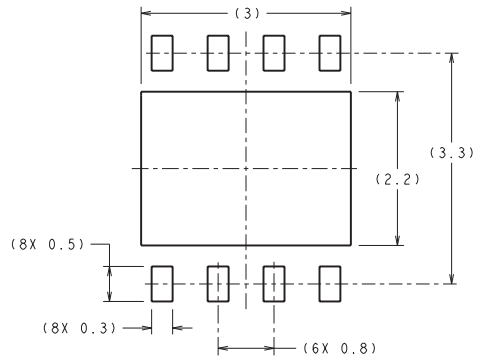
MPDS094A – APRIL 2001 – REVISED JUNE 2002

DCY (R-PDSO-G4) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters (inches).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC TO-261 Variation AA.

NGN0008A



RECOMMENDED LAND PATTERN
1:1 RATION WITH PKG SOLDER PADS

DIMENSIONS ARE IN MILLIMETERS
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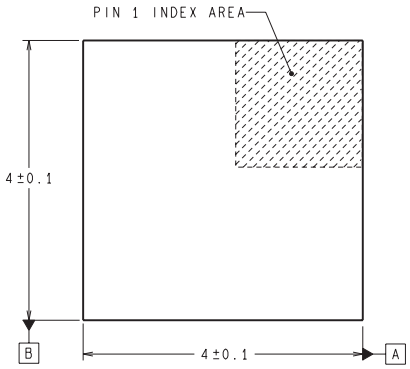
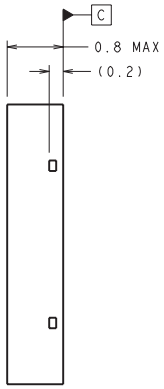
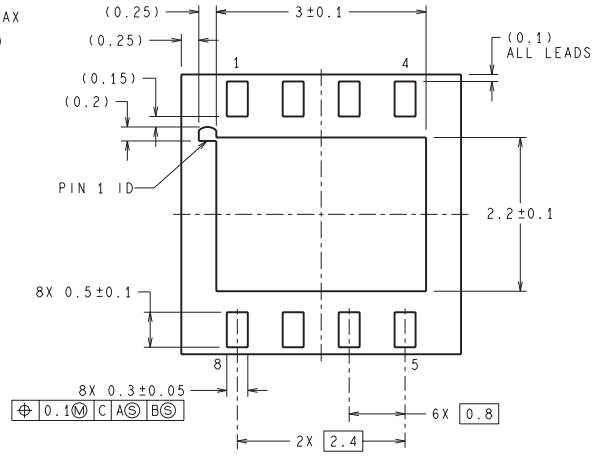
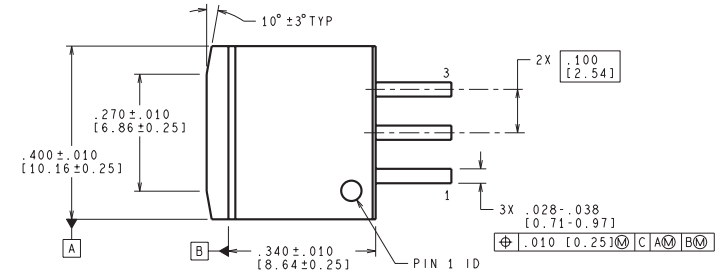


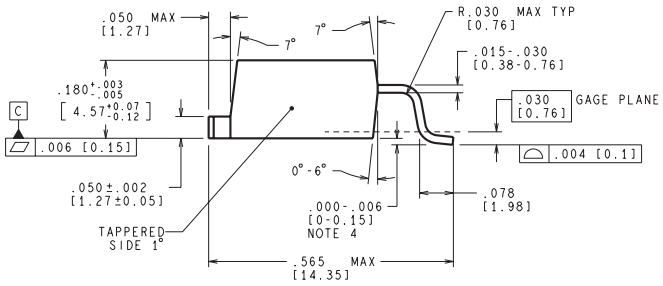


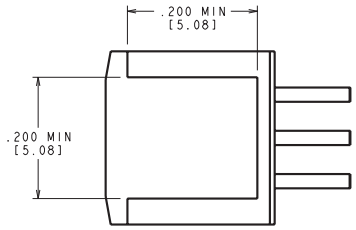


LDC08A (Rev B)

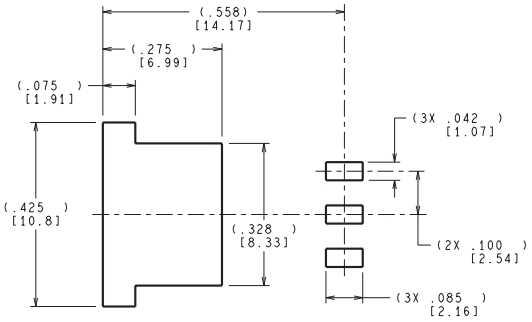
KTT0003B







BOTTOM SIDE OF PACKAGE



LAND PATTERN RECOMMENDATION

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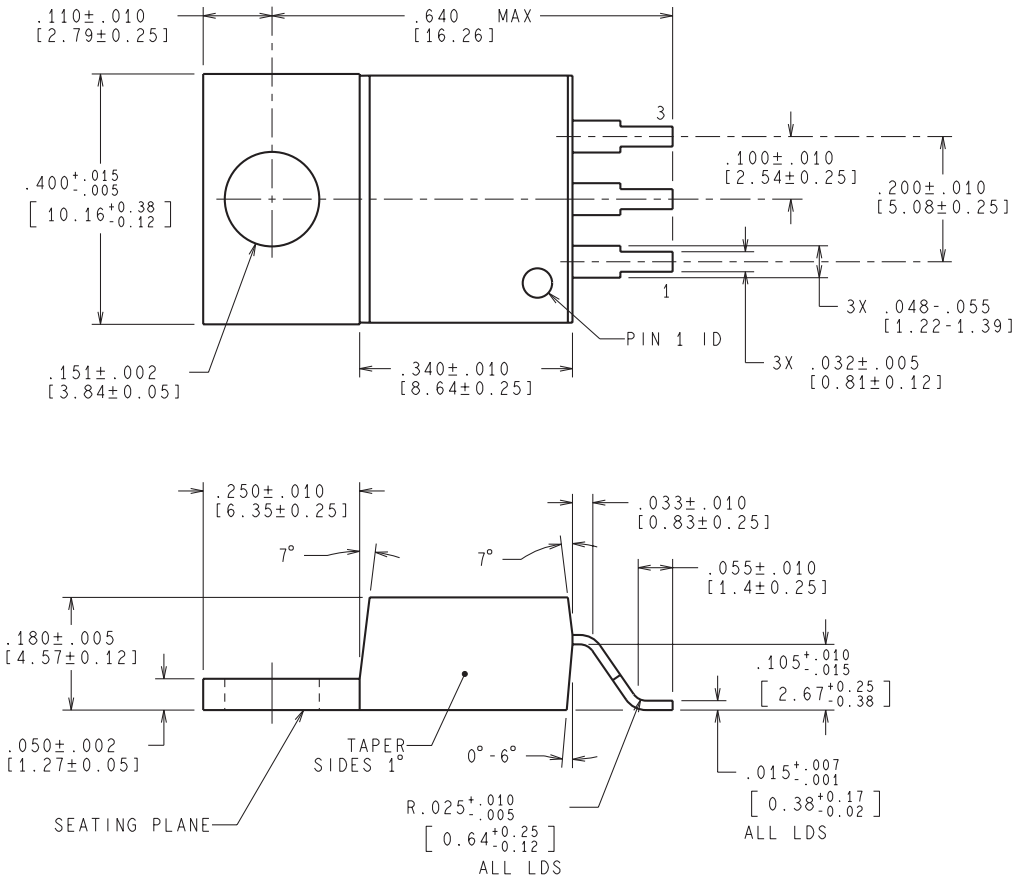
TS3B (Rev F)

NEB0003G



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TA03G (Rev A)

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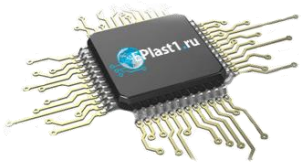
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.