bq24750/50A/51/51A/51B/52/53 EVM (HPA207) For Multi Cell Synchronous Notebook Charger and System Power Selector

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1.1 EVM Features

- Evaluation Module For the bq24750/50A/51/51A/51B/52/53
- High Efficiency NMOS-NMOS Synchronous Buck Charger With 300 kHz Frequency
- Battery/Adapter to System Power Selector Function
- User-Selectable 2-cell, 3-cell or 4-cell Li-ion Battery Voltage
- User-Programmable Battery Regulation Voltage with External Voltage Source (4.2/cell by Default)
- User-Programmable Charge Current with External Voltage Source (3 A by Default)
- User-Programmable Input Current Limit with External Voltage Source (4.5 A by Default)
- Pin Programmable Interface for Control and Status Communications with Host
- AC Adapter Operating Range 18 V to 22 V
- Adapter Overcurrent Protection
- ACFET Overpower Protection
- LED Indication for Control and Status Signals.

- Test Points for Key Signals Available for Testing Purpose. Easy Probe Hook-up
- Jumpers Available, Easy to Change Connections

1.2 General Description

The bq24750/50A/51/51A/51B/52/53 evaluation module is a complete charger module for evaluating a multi cell synchronous notebook charge and path selection solution using the bq24750/50A/51/51A/51B/52/53 devices. It is designed to deliver up to 6A of charge current to Li-Ion or Li-Pol applications. The charge current is programmable by external voltage input.

The bq24750/50A/51/51A/51B/52/53 has a highly integrated battery charge controller designed to work with external host commands. The battery voltage, charge current, input current limit and other system parameters are pin-programmable.

The dynamic power management (DPM) function modifies the charge current depending on system load conditions, avoiding ac adapter overload.

High accuracy current sense amplifiers enable accurate measurement of the ac adapter current, allowing monitoring of overall system power.

For details, see the bq24750 data sheet (SLUS735) , the bq24750A data sheet (SLUS834), the bq24751 data sheet (SLUS734), the bq24751A data sheet (SLUS756), the bq24751B data sheet (SLUS835) and the bq24753 data sheet (SLUS885).

1.3 I/O Description

Jack		Description
J1–ACPWR		AC adapter, positive output
J1–PGND		AC adapter, negative output
J2–VADJ		VADJ pin (12)
J2–ACSET		ACSET pin (6)
J2–SRSET		SRSET pin (16)
J3–$\overline{\text{CHGEN}}$		$\overline{\text{CHGEN}}$ pin (1)
J3–CELLS		CELLS pin (20)
J4–VEXT		External power supply, positive output
J4–GND		External power supply, negative output
J5–VREF		IC reference voltage VREF
J5–VDAC		VDAC pin (11)
J5–VDACEXT		External VDAC voltage
J5–GND		Ground
J6–TS		TS pin (8) output for bq24750/50A/52, OVPSET pin (8) output for bq24751/51A/51B/53
J6–PGND		Ground
J6–BAT		Connected to battery pack
J6–SYS		Connected to system
J7–ACGOOD		$\overline{\text{ACGOOD}}$ pin (13)
J7–IOUTF		R21 terminal connected to C23
J7–VREF		IC reference voltage VREF
J7–$\overline{\text{DPMDET}}$		pin number 21, $\overline{\text{DPMDET}}$ for bq24750/50A/52, LEARN for bq24751/51A/51B/53
JP1–1	bq24751/51A/51B/53	OVPSET resistor divider for bq24751/51A/51B/53
JP1–2		Pin 8
JP1–3	bq24750/50A/52	TS resistor divider for bq24750/50A/52
JP2–1	LEARN DISA	Pin 21, LEARN for bq24751/51A/51B/53
JP2–2		Ground
JP3–1	ACDRV	$\overline{\text{ACDRV}}$ pin (4) output
JP3–2		LED drive

Jack		Description
JP4–1	LEDPWR	Pull-up voltage source
JP4–2		LED Pull-up power line
JP5–VEXT		External power supply
JP5–HI		Pull-up voltage source
JP5–VREF		IC reference voltage VREF
JP6–1	4.2V REG	REGN pin (24)
JP6–2		VADJ pin (12)
JP7–VREF		IC reference voltage VREF
JP7–VDAC		VDAC pin (11)
JP7–EXT		External VDAC voltage
JP8–1	BATDRV	BATDRV pin (14) output
JP8–2		LED drive
JP9–1	CHGDISA	Pull-up voltage source
JP9–2		$\overline{\text{CHGEN}}$ pin (1)
JP10–HI		Pull-up voltage source
JP10–CELLS		CELLS pin (20) output
JP10–LO		Ground

1.4 Control and Key Parameters Setting

Jack	Description	Factory Setting	
		–001, –004, or –005 (bq24750/50A/52)	–002, –003, –006, or –007 (bq24751/51A/51B/53)
JP1	Pin 8 connection 1-2 (751) : OVPSET 2-3 (750) : TS	Jumper on 2-3	Jumper on 1-2
JP2	Disable LEARN mode when on	Jumper Off	Jumper On
JP3	JP3 The conduction of the AC MOSFET is indicated by LED when on	Jumper On	Jumper On
JP4	The pull-up power source supplies the LEDs when on. LED has no power source when off.	Jumper On	Jumper On
JP5	Pull-up power source setting 1-2: Use VREF as the pull-up source 2-3: Use external power supply as the pull-up source	Jumper on 1-2 (HI and VREF)	Jumper on 1-2 (HI and VREF)
JP6	Connect REGN to VADJ when on	Jumper On	Jumper On
JP7	VDAC voltage source setting 1-2 : Connect VREF to VDAC 2-3 : Connect external voltage source to VDAC	Jumper on 1-2 (VREF and VDAC)	Jumper on 1-2 (VREF and VDAC)
JP8	The conduction of the battery MOSFET is indicated by LED when on	Jumper On	Jumper On
JP9	Disable charge process when on	Jumper On	Jumper On
JP10	Number of cells selection 1-2 (HI-CELLS) : 4 cells 2-3 (CELLS-LO) : 3 cells Open: 2 cells	Jumper on 2-3 (3 cells)	Jumper on 2-3 (3 cells)

1.5 Recommended Operating Conditions

SYMBOL		DESCRIPTION	MIN	TYP	MAX	UNIT
V_{IN}	Supply voltage	Input voltage from ac adapter input	18	19	22	V
V_{BAT}	Battery voltage	Voltage applied at VBAT terminal of J8	6	7–16.8	20	V
I_{AC}	Supply current	Maximum input current from ac adapter	0		4.5	A
I_{chrg}	Charge current	Battery charge current	2	3 or 4	6	A
T_J	Operating junction temperature range		0		125	°C

2 Test Summary

2.1 Definitions

This procedure details how to configure the HPA207 evaluation board. On the test procedure the following naming conventions are followed. See the HPA207 schematic for details.

VXXX :	External voltage supply name (VADP, VBT, VSBT)
LOADW:	External load name (LOADR, LOADI)
V(TPyyy):	Voltage at HPA207 internal test point TPyyy. For example, V(TP12) means the voltage at TP12.
V(Jxx):	Voltage at HPA207 jack terminal Jxx.
V(TP(XXX)):	Voltage at test point *XXX*. For example, V(ACDET) means the voltage at the test point which is marked as *ACDET*.
V(XXX, YYY):	Voltage across point XXX and YYY.
I(JXX(YYY)):	Current going out from the YYY terminal of jack XX.
Jxx(BBB):	Terminal or pin BBB of jack xx
Jxx ON :	HPA207 internal jumper Jxx terminals are shorted
Jxx OFF:	HPA207 internal jumper Jxx terminals are open
Jxx (-YY-) ON:	HPA207 internal jumper Jxx adjacent terminals marked as *YY* are shorted
Measure: → A,B	Check specified parameters A, B. If measured values are not within specified limits the unit under test has failed.
Observe → A,B	Observe if A, B occur. If they do not occur, the unit under test has failed.

Assembly drawings have location for jumpers, test points and individual components.

2.2 Equipment

2.2.1 POWER SUPPLIES

Power Supply 1 (PS1): a power supply capable of supplying 20V at 5A is required.
Power Supply 2 (PS2): a power supply capable of supplying 5V at 1A is required. (for HPA207-001, -004, or -005 only)

2.2.2 LOAD 1

A 30V (or above), 5A (or above) electronic load that can operate at constant current mode

2.2.3 LOAD 2

A Kepco bipolar operational power supply/amplifier, 0 ± 20V (or above), 0 ± 6A (or above).

Or: A 20-V at 6-A (or above) dc power supply in parallel with a 3Ω, 100W+ power resistor which is thermally capable or well cooled for at least 100W power dissipation.

2.2.4 METERS

Seven Fluke 75 multimeters, (equivalent or better)
Or: Four equivalent voltage meters and three equivalent current meters.

The current meters must be capable of measuring 5A+ current.

2.2.5 OSCILLOSCOPES

An oscilloscope, a single voltage probe and a single current probe are required.

2.3 Equipment Setup

(A) Set the power supply 1 for 0V ± 100mVDC, 5.0 ± 0.1A current limit and then turn off supply.
(B) Connect the output of power supply 1 in series with a current meter (multimeter) to J1 (POS, GND).
(C) Connect a voltage meter across J1 (POS, GND).
(D) Set the power supply 2 for 1.6V ± 100mVDC, 1.0 ± 0.1A current limit and then disable the output.
(E) **(For HPA207-001, -004 or -005 only)** Connect the output of power supply 2 to J6 (TS, GND).
(F) Turn off Load 1.
(G) Set the voltage of Load 2 to 2V ± 1V. Turn off Load 2.
(H) Connect a voltage meter across J6 (BAT, GND).
(I) Connect a voltage meter across J6 (SYS, GND).
(J) JP3: ON, JP8: ON, JP9: ON, JP6: ON, JP4: ON, JP10 (LO, CELLS): ON, JP5 (HI, VREF): ON, JP7 (VREF, VDAC): ON.
(K) **(For HPA207-001, -004 or -005 only)** JP1(-750-): ON, JP2: OFF
(L) **(For HPA207-002, -003, -006, or -007 only)** JP1 (-751-): ON, JP2: ON

After the steps above, the test setup for HPA207-001, -004, or -005 (bq24750/50A/52 EVM) is shown in Figure 1. The test setup for HPA207-002, -003, -006, or -007 (bq24751/51A/51B/53 EVM) is shown in Figure 2.

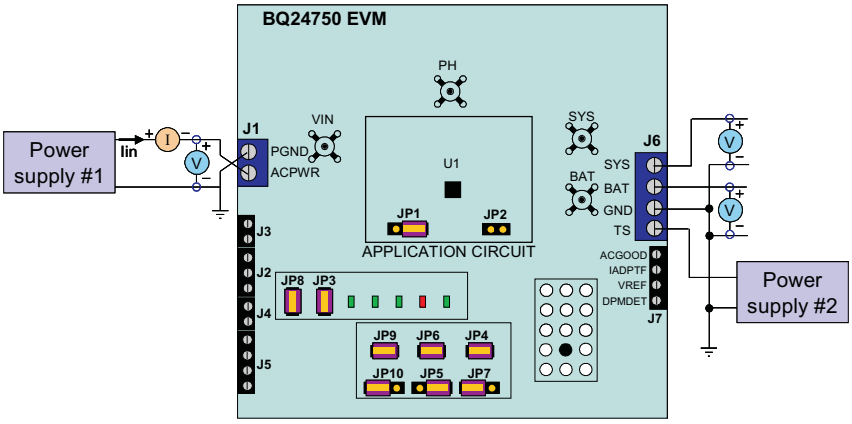


Figure 1. Original Test Setup for HPA207-001, -004, or -005

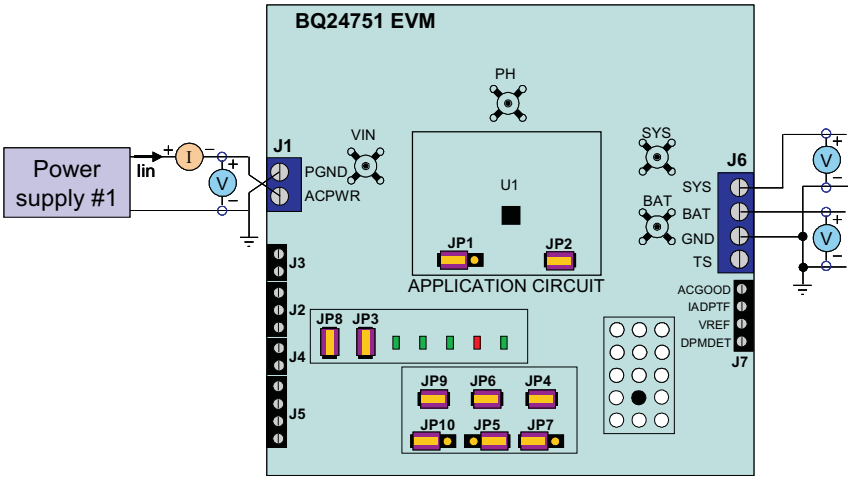


Figure 2. Original Test Setup for HPA207-002, -003, -006, or -007

2.4 Procedure

2.4.1 AC ADAPTER DETECTION THRESHOLD

1. Make sure EQUIPMENT SETUP steps are followed.
2. (For HPA207-001, -004, or -005 only) Turn on PS2.
3. Turn on PS1.
   Measure → V(J6(VSYS)) = 0 ± 500mV
   Measure → V(TP(VREF)) = 0V ± 500mV
   Measure → V(TP(REGN)) = 0V ± 500mV
4. Increase the output voltage of PS1 until D7 (ACGOOD) on but do not exceed 19V.
   Measure → V(TP(ACDET)) = 2.4V ± 150mV
   Measure → V(J1(POS)) = 17.8V ± 1V
   Measure → V(J6(SYS)) = 17.8V ± 1V
   Measure → V(TP(VREF)) = 3.3V ± 200mV
   Measure → V(TP(REGN)) = 6V ± 500V **(For HPA207-001, -002, or -004)**
   Measure → V(TP(REGN)) = 0.7V ± 700mV **(For HPA207-003, -005, -006, -007 only)**
   Measure → D4 (ACDRV) on. (Note: ignore D5 if testing HPA207-002, -003, -006, or -007)

2.4.2 SELECTION OF REGULATION VOLTAGE

1. Increase the voltage of PS1 until V(J5(POS)) = 19V± 0.1V.
   Measure → V(J6(BAT, GND)) = 0V ± 1V
   Uninstall JP9 (enable the charging)
   Observe → D3 (CHG EN) on
   Measure → V(J6(BAT)) = 12.6V ± 200mV
2. Install JP10 (CELLS, HI)
   Measure → V(J6(BAT)) = 16.8V ± 200mV
3. Install JP10 (CELLS, LO)
   Measure → V(J6(BAT)) = 12.6V ± 200mV

2.4.3 CHARGE CURRENT AND AC CURRENT REGULATION (DPM)

1. Install JP9 (Disable the charging).
2. Connect the Load 2 in series with a current meter (multimeter) to J6 (BAT, GND). Make sure a voltage meter is connected across J6 (BAT, GND). Turn on the Load 2. Set the output voltage to 10.5V.
3. Connect the output of the Load 1 in series with a current meter (multimeter) to J6 (SYS, GND). Make sure a voltage meter is connected across J6 (SYS, GND). Turn on the power of the Load 1. Set the load current to 4A ± 50mA but disable the output. The setup is now like Figure 3 for HPA207-001, -004 or -005 and like Figure 4 for HPA207-002, -003, -006, or -007. Make sure Ibat = 0A ± 10mA and Isys = 0A ± 10mA.

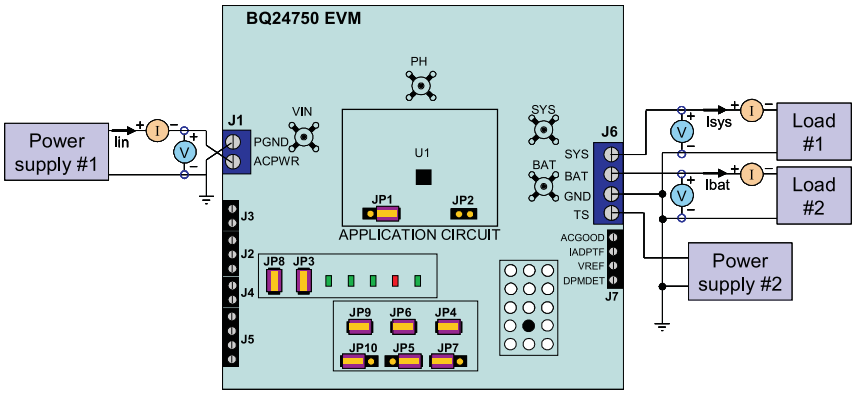


Figure 3. Test Setup for HPA207-001, -004, or -005

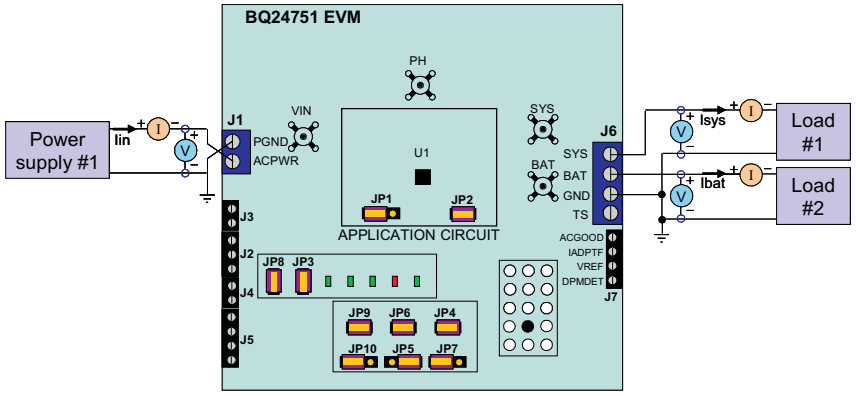


Figure 4. Test Setup for HPA207-002, -003, -006, or -007

4. Uninstall JP9 (Enable the charging).
   Observe → D3 (CHG EN) on
5. Measure → Ibat = 3000mA ± 200mA
   Measure → V(TP(IOUT)):= 300mV ± 100mV **(For HPA207-001, 002, -003, -005, -006, or -007)**
   Measure → V(TP(IOUT)):= 600mV ± 100mV **(For HPA207-004 only)**
6. Enable the output of the Load 1.
   Observe → D5 (DPMDET) on **(For HPA207-001, -004, or -005 only)**
   Measure → Isys = 4000mA ± 200mA, Ibat = 1000mA ± 500mA, Iin = 4500mA ± 400mA
7. Turn off the Load 1.
   Measure → Isys = 0 ± 100mA, Ibat = 3000mA ± 200mA

2.4.4 CHARGER CUT-OFF BY THERMISTOR (HPA207-001, -004, or -005 ONLY)

1. Slowly increase the output voltage of PS2 until Ibat = 0 ± 10mA.
   Measure → V(J6(TS)) = 2.44V ± 400mV
2. Slowly decrease the output voltage of PS2.
   Charge will resume. Continue to decrease the output voltage of PS2 slowly until Ibat = 0 ± 10mA.
   Measure → V(J6(TS)) = 0.97V ± 400mV
3. Slowly increase the output voltage of PS2 to 1.6V ± 100mV.
   Measure → Ibat = 3000mA ± 200mA

2.4.5 LEARN MODE (HPA207-002, -003, -006, or -007 ONLY)

1. *Measure* → V(J6(SYS)) = 19V ± 1V (adapter connected to system)
2. Uninstall JP2 (Enable the learn mode).
   Measure → V(J6(SYS)) = 10.5V ± 1V (battery connected to system)
3. Install JP2 (Disable the learn mode).
   Measure → V(J6(SYS)) = 19V ± 1V (adapter connected to system)

2.4.6 POWER PATH SELECTION

1. Install JP9 (Disable the charging).
   Measure → V(J6(SYS)) = 19V ± 1V (adapter connected to system)
   Observe → D4 (ACDRV) on, D6 (BATDRV) off.
2. Turn off PS1.
   Measure → V(J6(SYS)) = 10.5V ± 1V (battery connected to system)

3 PCB Layout Guideline

1. It is critical that the exposed power pad on the backside of the bq2475x package be soldered to the PCB ground. Make sure there are sufficient thermal vias right underneath the IC, connecting to the ground plane on the other layers.
2. The control stage and the power stage should be routed separately. At each layer, the signal ground and the power ground are connected only at the power pad.
3. AC current sense resistor must be connected to ACP (pin 3) and ACN (pin 2) with a Kelvin contact. The area of this loop must be minimized. The decoupling capacitors for these pins should be placed as close to the IC as possible.
4. Charge current sense resistor must be connected to SRP (pin 19), SRN (pin 18) with a Kelvin contact. The area of this loop must be minimized. The decoupling capacitors for these pins should be placed as close to the IC as possible.
5. Decoupling capacitors for PVCC (pin 28), VREF (pin 10), REGN (pin 24) should be placed underneath the IC (on the bottom layer) and make the interconnections to the IC as short as possible.
6. Decoupling capacitors for BAT (pin 17), IADAPT or IBAT (pin 15) must be placed close to the corresponding IC pins and make the interconnections to the IC as short as possible.
7. Decoupling capacitor(s) for the charger input must be placed close to Q3 drain and Q4 source.

4 Bill of Materials, Board Layout and Schematics

Table 1. Bill of Materials

'50 -001	'51 -002	'51A -003	'52 -004	'50A -005	'51B -006	'53 -007	RefDes	Value	Description	Size	Part Number	MFR
0	0	0	0	0	0	0	C1	Open	Capacitor, Electrolytic, 22uF, 25 VDC	0.207 X 0.209 inch	UUD1E220 MCR1GS	Nichicon
0	0	0	0	0	0	0	C10, C21, C25,C29, C32	Open	Capacitor, Ceramic, 50V, X7R, 10%	603	C1608X7R1 H104K	TDK
1	1	1	1	1	1	1	C11	0.47uF	Capacitor, Ceramic, 50V, X7R, 10%	805	GRM21BR7 1H474KA88 L	muRata
4	4	4	4	4	4	4	C12, C13, C23, C26	10uF	Capacitor, Ceramic, 25V, X5R, 10%	1210	Std	Taiyo Yuden
0	0	0	0	0	0	0	C14	Open	Capacitor, Ceramic, vvV	805		
1	1	1	1	1	1	1	C15	4.7uF	Capacitor, Ceramic, 25V, X7R, 20%	1206	C3216X7R1 E475M	TDK
1	1	1	1	1	1	1	C16	100pF	Capacitor, Ceramic, 50V, C0G, 5%	603	C1608C0G1 H101J	TDK
0	0	0	0	0	0	0	C2	Open	Capacitor, Ceramic, 25V, X5R, 10%	1210	Std	Taiyo Yuden
0	0	0	0	0	0	0	C22, C33	Open	Capacitor, Ceramic, 25V, X5R, 10%	1206	GRM31CR6 1E106KA12 L	muRata
2	2	2	2	2	2	2	C24, C30	10uF	Capacitor, Ceramic, 25V, X5R, 10%	1206	GRM31CR6 1E106KA12 L	muRata
0	0	0	0	0	0	0	C3	Open	Capacitor, Ceramic, 35V, X7R, 10%	1206	C3216X7R1 H105K	Taiyo Yuden
2	2	2	2	2	2	2	C4, C31	0.01uF	Capacitor, Ceramic, 50V, X7R, 10%	603	C1608X7R1 H104K	TDK
1	1	1	1	1	1	1	C5	22 uF	Capacitor, Electrolytic, 22uF, 25 VDC	0.207 X 0.209 inch	UUD1E220 MCR1GS	Nichicon
0	0	0	0	0	0	0	C6	Open	Capacitor, Ceramic, vvV, [temp], [tol]	1210	Std	Vishay
7	7	7	7	7	7	7	C7, C9, C18, C20,C27, C28, C34	0.1uF	Capacitor, Ceramic, 50V, X7R, 10%	603	C1608X7R1 H104K	TDK
3	3	3	3	3	3	3	C8, C17, C19	1.0uF	Capacitor, Ceramic, 50V, X7R, 10%	1206	C3216X7R1 H105K	TDK
1	1	1	1	1	1	1	D1	BAT54	Diode, Schottky, 200mA, 30V	SOT23	BAT54	Vishay-Liteon
1	1	1	1	1	1	1	D2	MBRS130	Diode, Schottky, 1A, 30V	SMB	MBRS130TR	IR
4	4	4	4	4	4	4	D3, D4, D6, D7	Green	Diode, LED, Green, 2.1V, 20mA, 6mcd	603	LTST-C190GKT	Lite On
1	1	1	1	1	1	1	D5	Red	Diode, LED, Red, 1.8V, 20mA, 20mcd	603	LTST-C190CKT	Lite On
1	1	1	1	1	1	1	J1	ED1609-ND	Terminal Block, 2 pin, 15A, 5.1mm	0.40 x 0.35 inch	ED1609	OST
1	1	1	1	1	1	1	J2	ED1515	Terminal Block, 3 pin, 6A, 3.5mm	0.41 x 0.25 inch	ED1515	OST

Table 1. Bill of Materials (continued)

'50 -001	'51 -002	'51A -003	'52 -004	'50A -005	'51B -006	'53 -007	RefDes	Value	Description	Size	Part Number	MFR
2	2	2	2	2	2	2	J3, J4	ED1514	Terminal Block, 2 pin, 6A, 3.5mm	0.27 x 0.25 inch	ED1514	OST
1	1	1	1	1	1	1	J6	ED2227	Terminal Block, 4 pin, 15A, 5.1mm	0.80 x 0.35 inch	ED2227	OST
2	2	2	2	2	2	2	J5, J7	ED1516	Terminal Block, 4 pin, 6A, 3.5mm	0.55 x 0.25 inch	ED1516	OST
4	4	4	4	4	4	4	JP1, JP5, JP7, JP10	PTC36SAAN	Header, 3 pin, 100mil spacing, (36-pin strip)	0.100 inch x 3	PTC36SAAN	Sullins
6	6	6	6	6	6	6	JP2, JP3, JP4, JP6, JP8, JP9	PTC36SAAN	Header, 2 pin, 100mil spacing, (36-pin strip)	0.100 inch x 2	PTC36SAAN	Sullins
1	1	1	1	1	1	1	L1	8.2uH	Inductor, SMT, 16A, 24.8milliohm	0.51 x 0.51 inch	IHLP5050CE8R2M01	Vishay
3	3	3	3	3	3	3	Q1, Q2, Q5	Si4435DY	MOSFET, P-ch, 30V, 8.0A, 20milliohm	SO8	Si4435DY	Siliconix
2	2	2	2	2	2	2	Q3, Q4	FDS6680A	Transistor, MOSFET, NChan, 30V, 12.5A, Rds 9.5 milliohm	SO8	FDS6680A	Fairchild
8	8	8	8	8	8	8	Q6, Q8, Q9, Q10, Q11, Q13, Q14, Q15	2N7002DICT	MOSFET, N-ch, 60V, 115mA, 1.2Ohms	SOT23	2N7002DICT	Vishay-Liteon
2	2	2	2	2	2	2	Q7, Q12	TP0610K	MOSFET, P-Ch, 60V, Rds 6 ohms, Id 185 mA	SOT-23	TP0610K	Vishay-Siliconix
1	1	1	1	1	1	1	R1	422k	Resistor, Chip, 1/10W, 1%	603	Std	Std
2	2	2	2	2	2	2	R10, R11	0	Resistor, Chip, 1/16W, 5%	402	Std	Std
3	3	3	3	3	3	3	R12, R14, R18	100k	Resistor, Chip, 1/10W, 0.1%	805	ERA-6YEB104V	Panasonic
1	1	1	1	1	1	1	R13	82k	Resistor, Chip, 1/10W, 0.1%	805	ERA-6YEB823V	Panasonic
1	1	1	1	1	1	1	R15	43k	Resistor, Chip, 1/10W, 0.1%	805	ERA-6YEB433V	Panasonic
1	1	1	1	1	1	1	R19	68k	Resistor, Chip, 1/10W, 0.1%	805	ERA-6YEB683V	Panasonic
1	1	1	1	1	1	1	R2	71.5k	Resistor, Chip, 1/10W, 1%	603	Std	Std
3	3	3	3	3	3	3	R21, R26, R33	20.0k	Resistor, Chip, 1/16W, 1%	603	Std	Std
5	5	5	5	5	5	5	R24, R25, R27, R30, R34	2.21k	Resistor, Chip, 1/16W, 1%	603	Std	Std
1	1	1	1	1	1	1	R3	390k	Resistor, Chip, 1/16W, 1%	603	Std	Std
1	1	1	1	1	1	1	R31	10.0k	Resistor, Chip, 1/16W, 1%	603	Std	Std
1	1	1	1	1	1	1	R4	60.4k	Resistor, Chip, 1/16W, 1%	603	Std	Std
1	1	1	1	1	1	1	R5	5.62k	Resistor, Chip, 1/16W, 1%	402	Std	Std
1	1	1	1	1	1	1	R6	118k	Resistor, Chip, 1/16W, 1%	402	Std	Std
6	6	6	6	6	6	6	R7, R20, R22, R23, R28, R29	100k	Resistor, Chip, 1/16W, 1%	603	Std	Std
3	3	3	3	3	3	3	R8, R16, R32	10.0k	Resistor, Chip, 1/16W, 1%	402	Std	Std

Table 1. Bill of Materials (continued)

'50 -001	'51 -002	'51A -003	'52 -004	'50A -005	'51B -006	'53 -007	RefDes	Value	Description	Size	Part Number	MFR
2	2	2	2	2	2	2	R9, R17	0.01	Resistor, Chip, 1/2W, 1%	2010	WSL2010R0100FEA	Dale
10	10	10	10	10	10	10	SJ1, SJ2, SJ3, SJ4, SJ5, SJ6, SJ7, SJ8, SJ9, SJ10	929950-00	Shorting jumpers, 2-pin, 100mil spacing,		929950-00	3M/ESD
4	4	4	4	4	4	4			6-32 NYL nuts			
4	4	4	4	4	4	4	ST1, ST2, ST3, ST4	4816	STANDOFF M/F HEX 6-32 NYL .500"	sf_thvt_325_rnd	Keystone	4816
2	2	2	2	2	2	2	TP1, TP20	5001	Test Point, Black, Thru Hole Color Keyed	0.100 x 0.100 inch	5001	Keystone
14	14	14	14	14	14	14	TP18,TP19, TP21,TP22, TP23,TP24, TP25,TP26, TP27,TP28, TP29,TP30, TP31,TP32	5002	Test Point, White, Thru Hole Color Keyed	0.100 x 0.100 inch	5002	Keystone
4	4	4	4	4	4	4	TP2,TP15,TP16,TP17	131-4244-00	Adaptor, 3.5-mm probe clip (or 131-5031-00)	0.200 inch	131-4244-00	Tektronix
0	0	0	0	0	0	0	TP3,TP4,TP5,TP6,TP7,TP8,TP9,TP10,TP11,TP12,TP13,TP14	STD	Test Point, 0.020 Hole		STD	STD
1	0	0	0	0	0	0	U1	BQ24750RHD	IC, Battery Charge Controller	QFN-28	BQ24750RHD	TI
0	1	0	0	0	0	0	U1	BQ24751RHD	IC, Battery Charge Controller	QFN-28	BQ24751RHD	TI
0	0	1	0	0	0	0	U1	BQ24751ARHD	IC, Battery Charge Controller	QFN-28	BQ24751ARHD	TI
0	0	0	1	0	0	0	U1	BQ24752RHD	IC, Battery Charge Controller	QFN-28	BQ24752RHD	TI
0	0	0	0	1	0	0	U1	BQ24750ARHD	IC, Battery Charge Controller	QFN-28	BQ24750ARHD	TI
0	0	0	0	0	1	0	U1	BQ24751BRHD	IC, Battery Charge Controller	QFN-28	BQ24751BRHD	TI
0	0	0	0	0	0	1	U1	BQ24753RHD	IC, Battery Charge Controller	QFN-28	BQ24753RHD	TI
1	1	1	1	1	1	1		HPA207	Printed Circuit board			Any

4.1 Board Layout

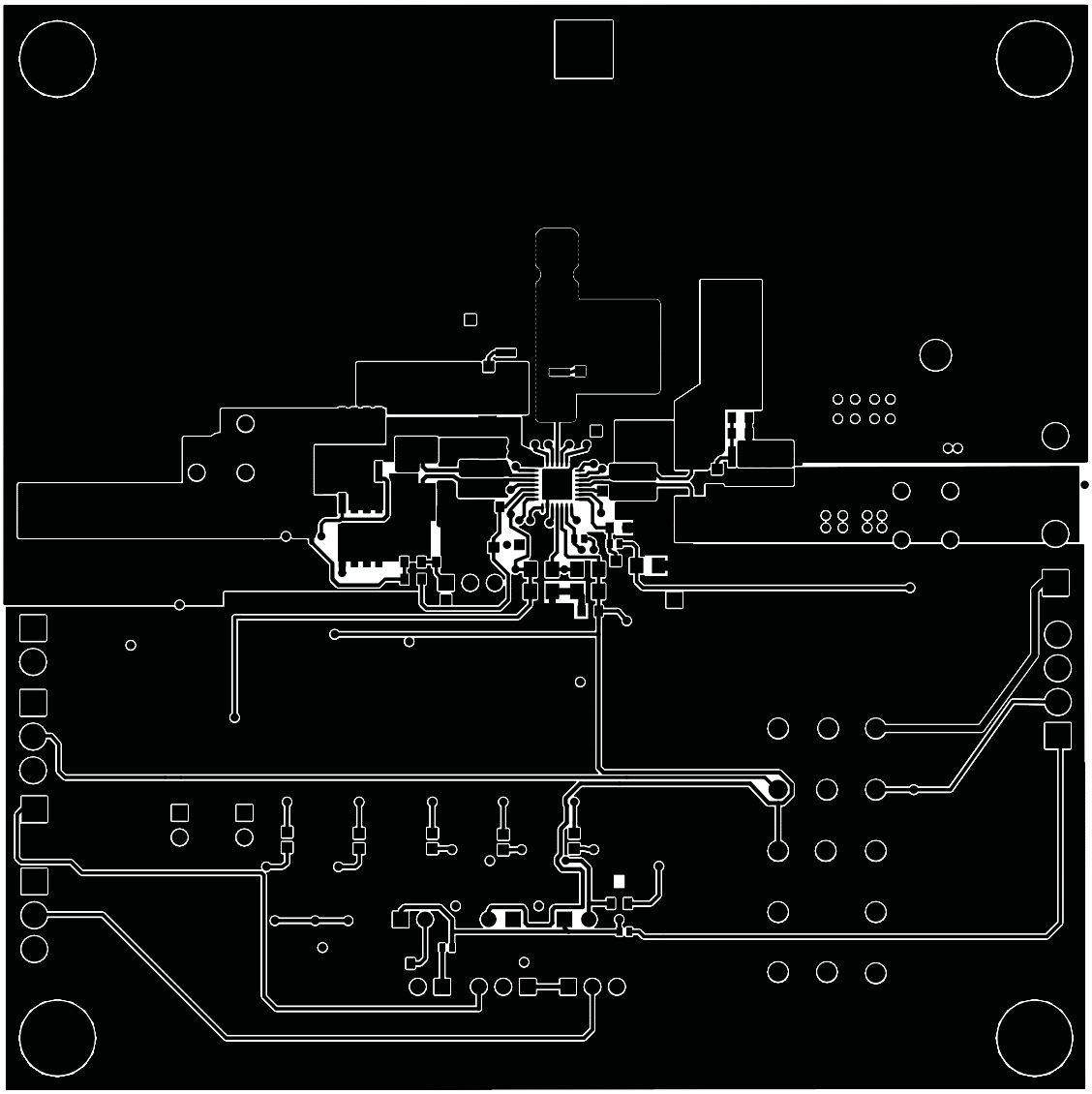


Figure 5. Top Layer

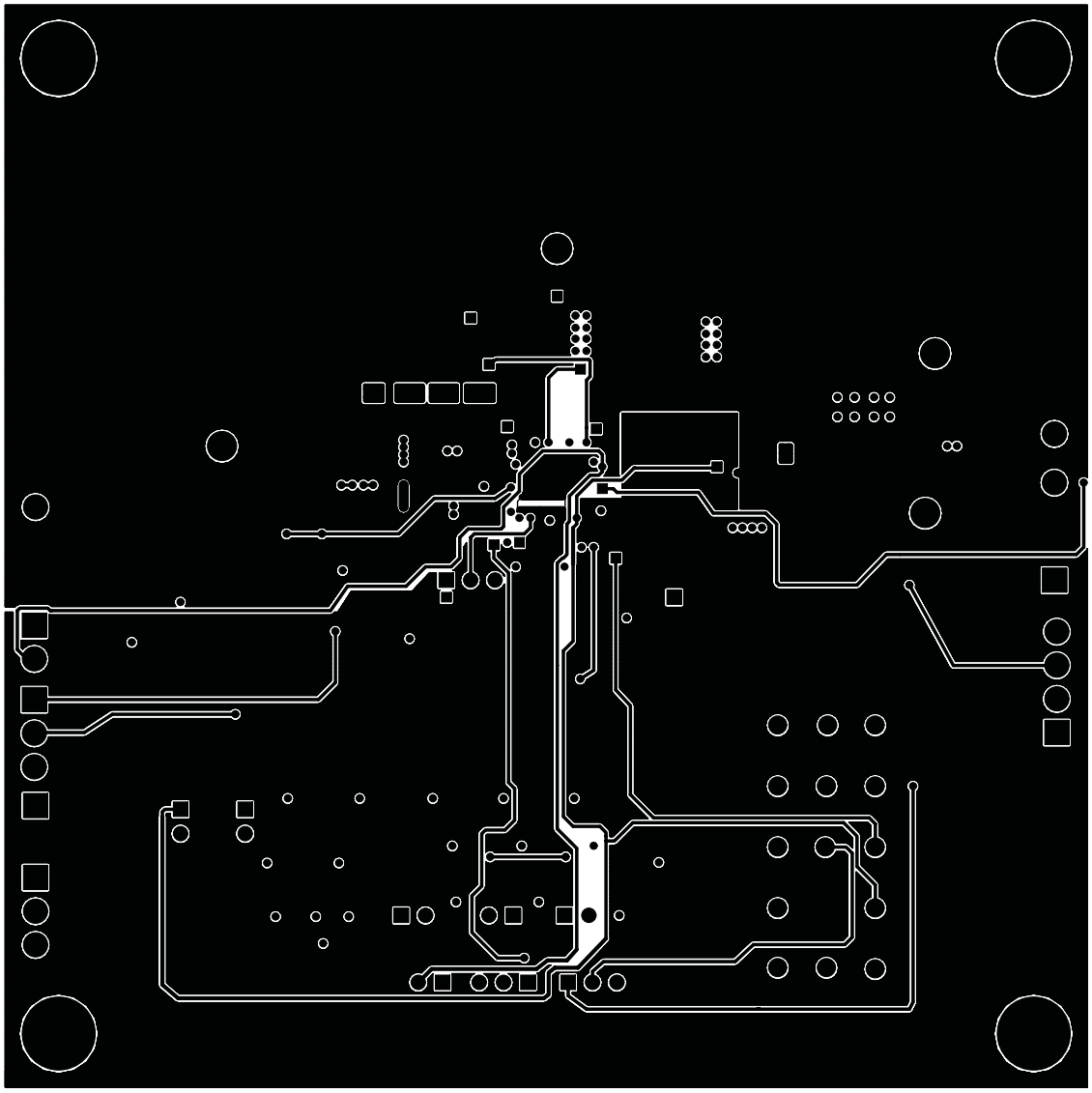


Figure 6. 2nd Layer

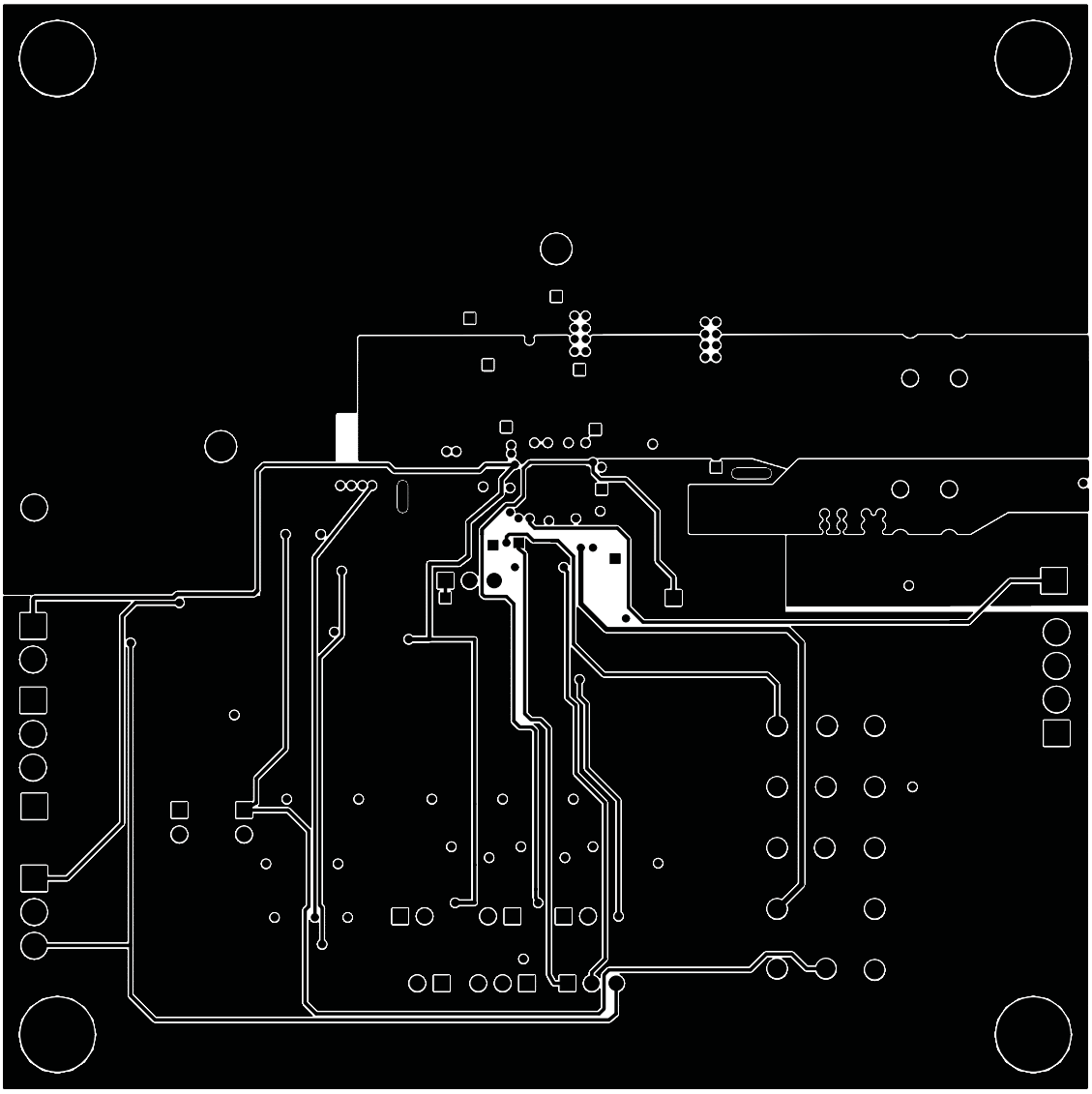


Figure 7. 3rd Layer

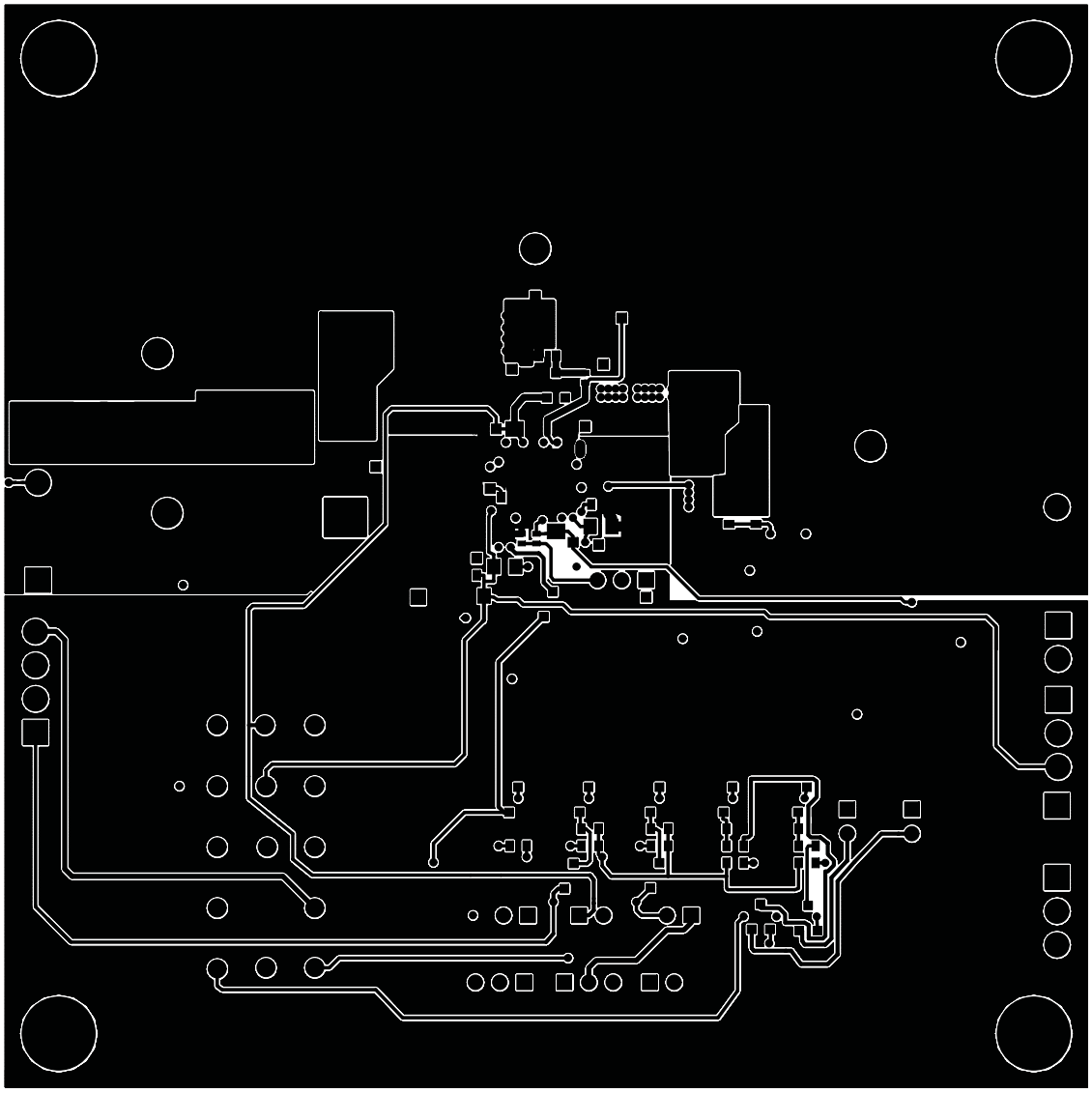


Figure 8. Bottom Layer

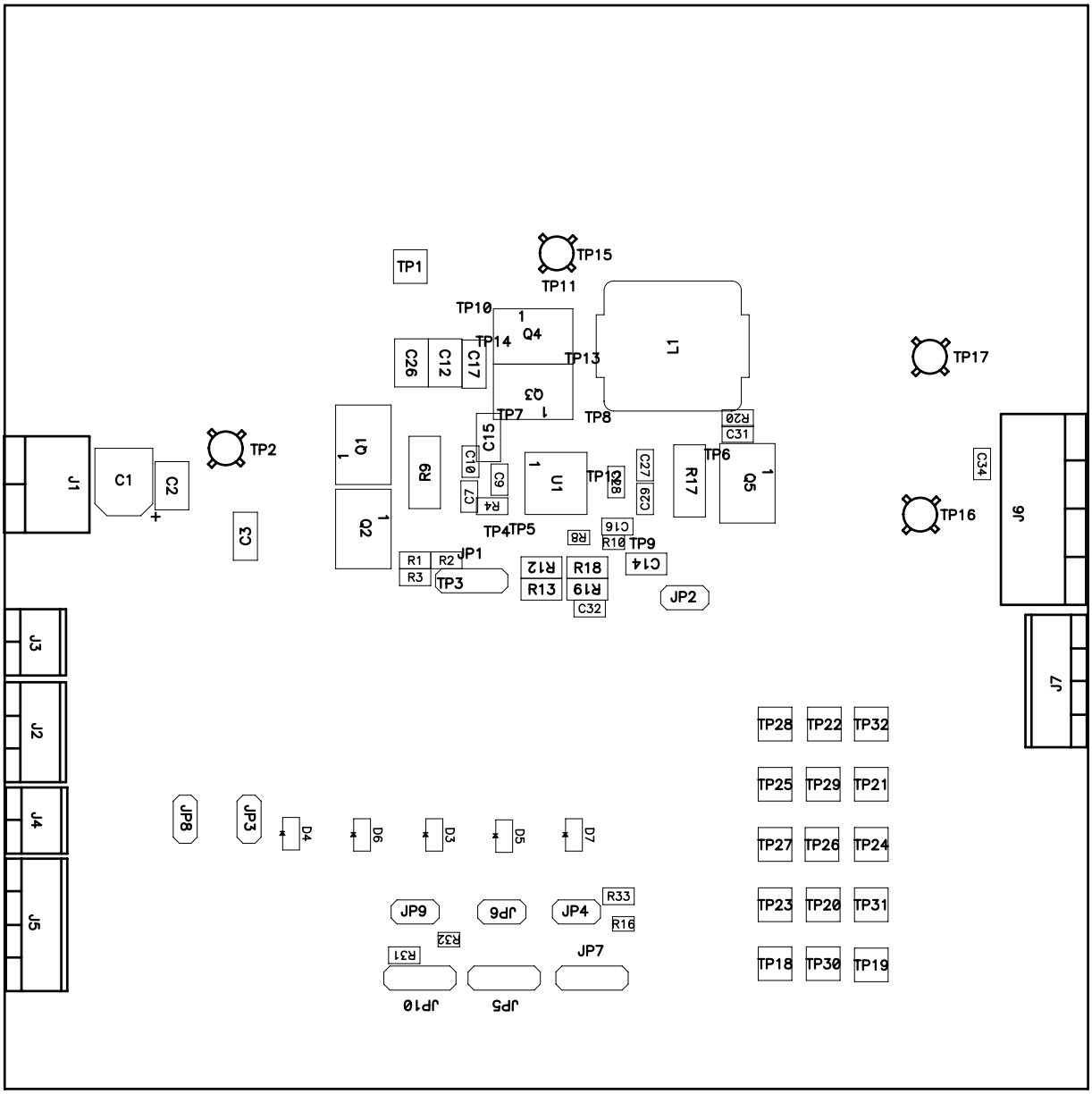


Figure 9. Top Assembly

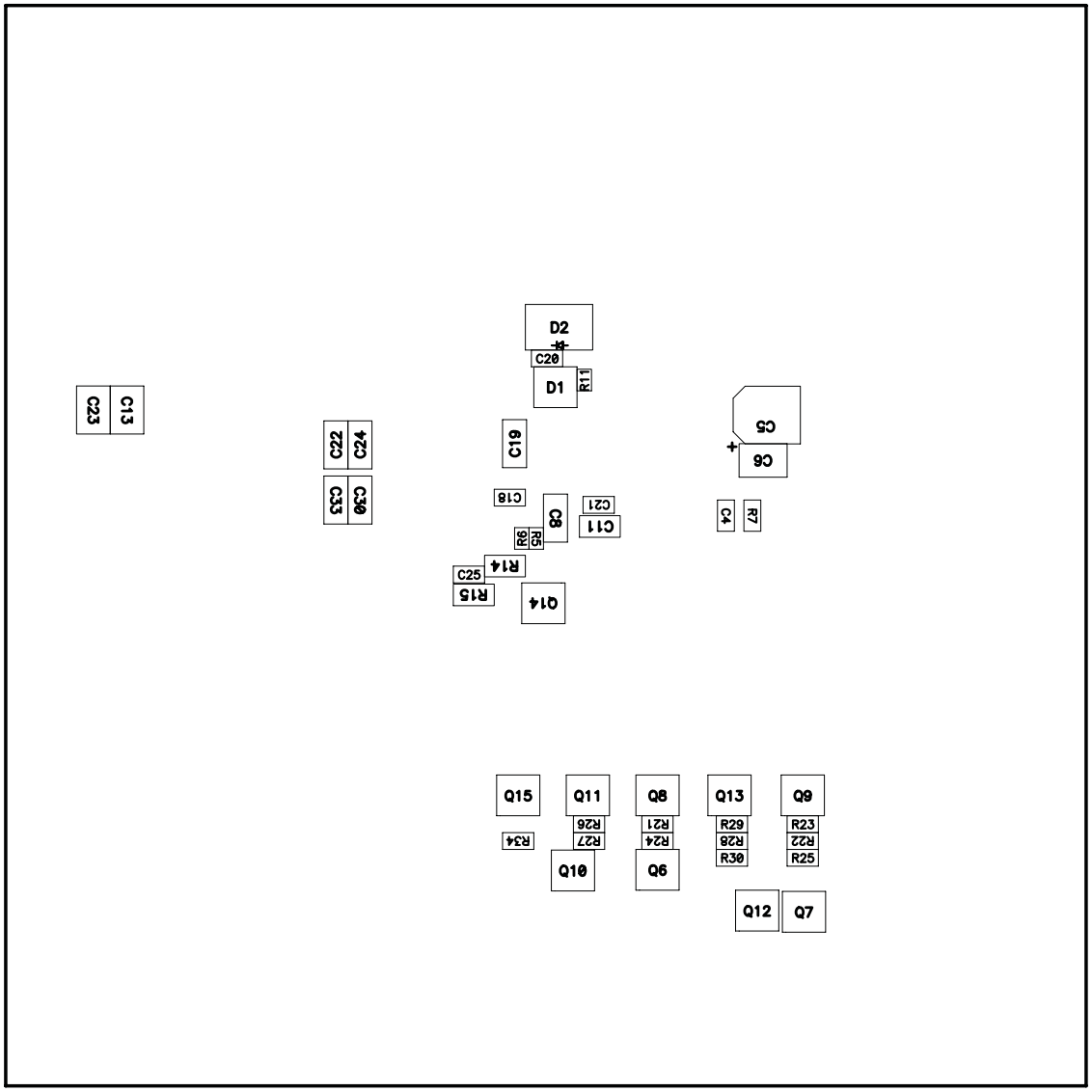


Figure 10. Bottom Assembly

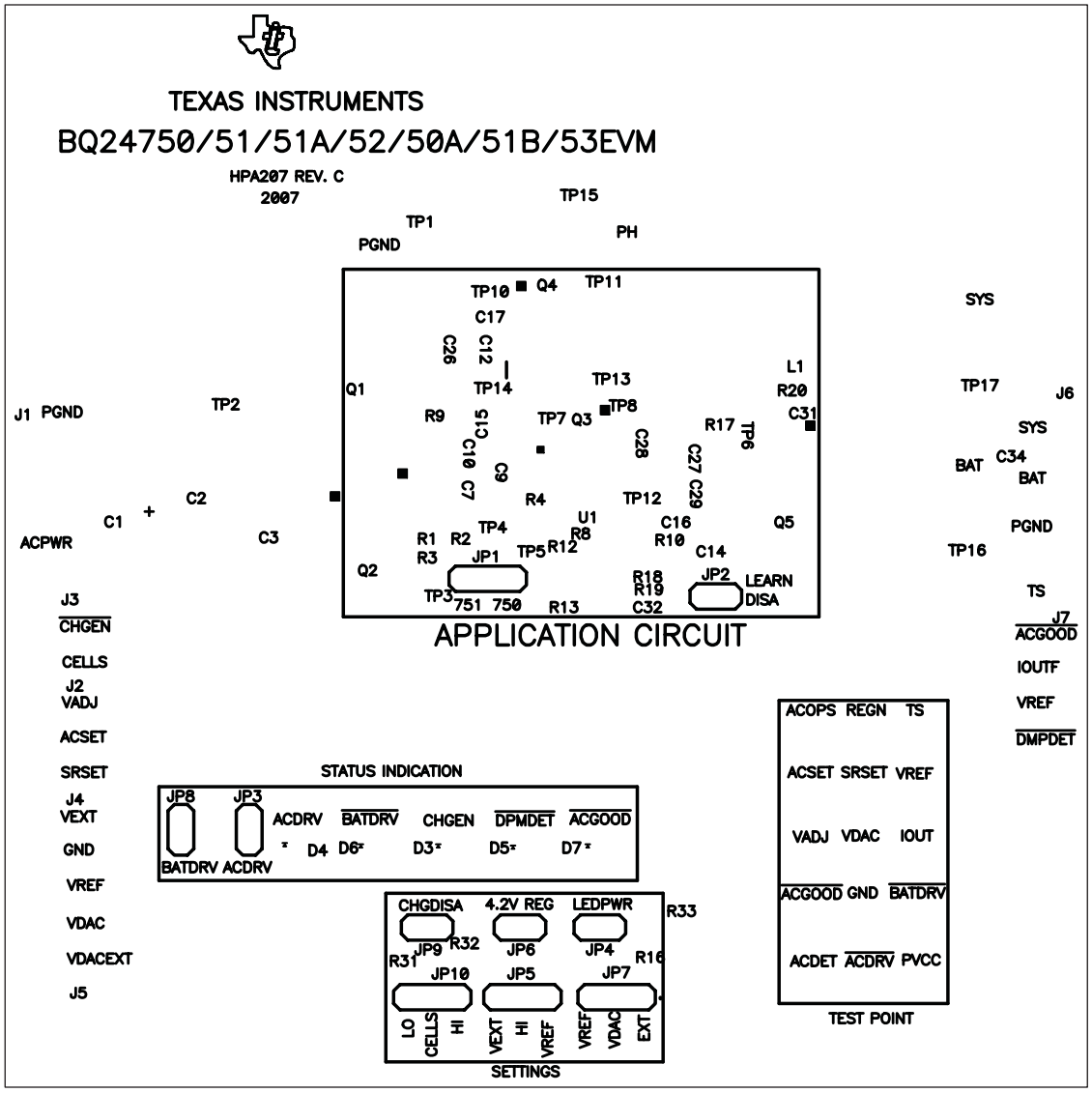
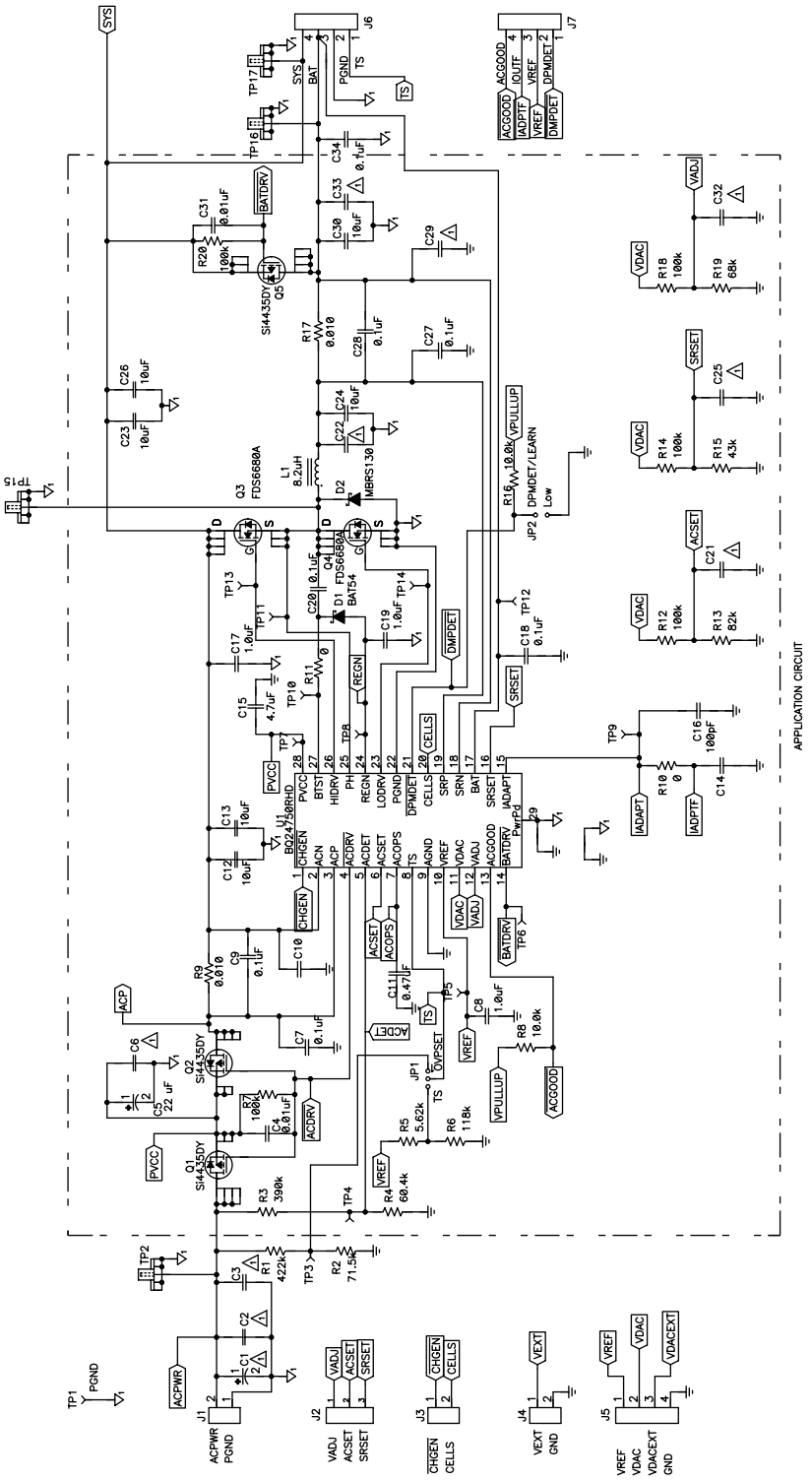
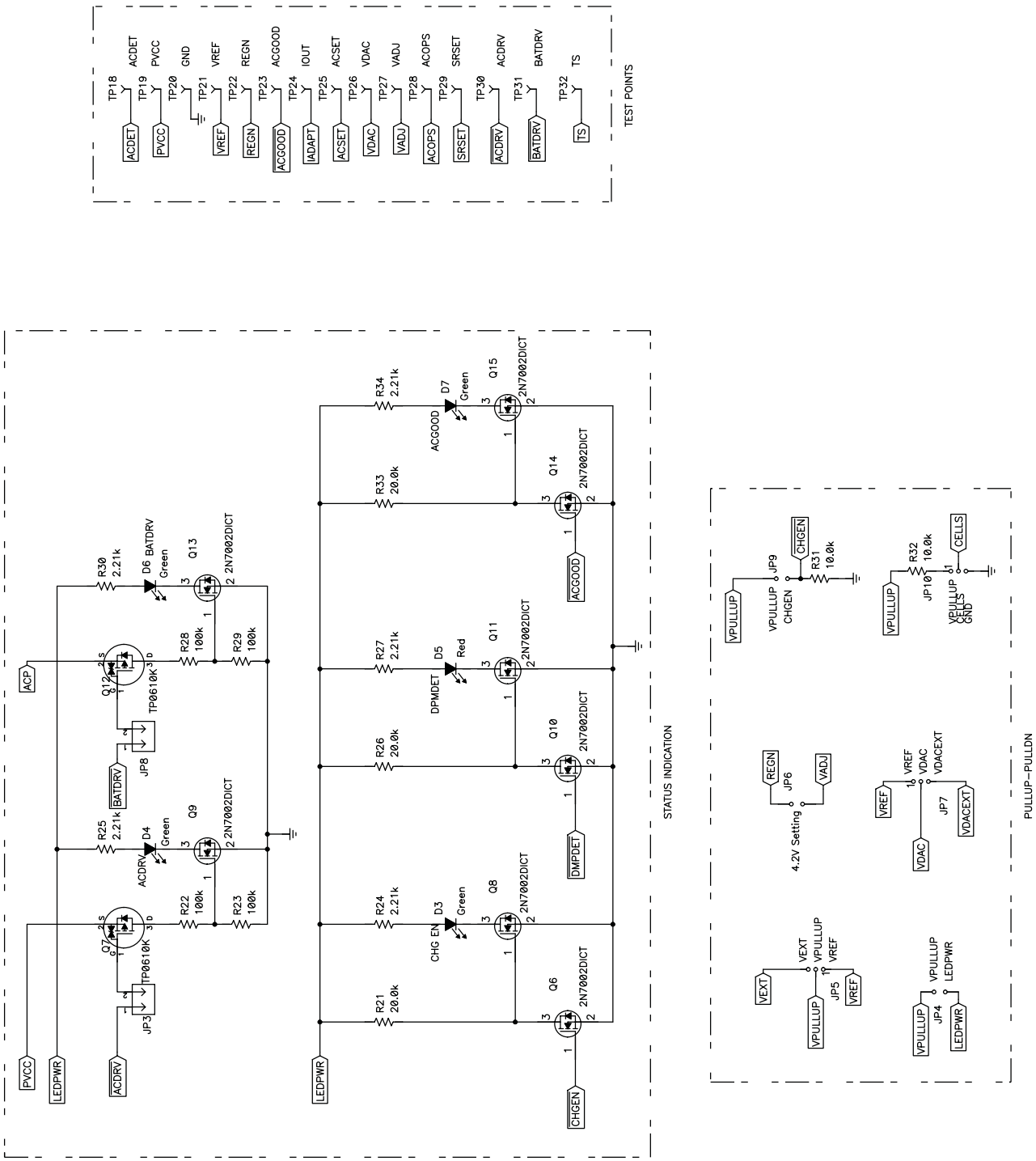


Figure 11. Top Silk

4.2 Schematics

The schematic is shown on the following page.





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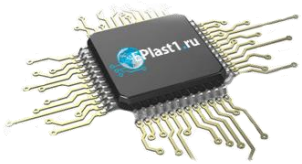

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Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.