

1. General description

Planar passivated very sensitive gate four quadrant triac in a SOT54 (TO-92) plastic package intended for use in applications requiring enhanced noise immunity and direct interfacing to logic ICs and low power gate drivers.

2. Features and benefits

- Direct interfacing to logic level ICs
- Enhanced current surge capability
- Enhanced noise immunity
- High blocking voltage capability
- · Planar passivated for voltage ruggedness and reliability
- Triggering in all four quadrants
- Very sensitive gate

3. Applications

- General purpose low power motor control
- Home appliances
- Industrial process control
- Low power AC Fan controllers

4. Quick reference data

Table 1. Qui	ck reference data					
Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
V _{DRM}	repetitive peak off- state voltage		-	-	800	V
I _{T(RMS)}	RMS on-state current	full sine wave; $T_{lead} \le 45 \text{ °C}$; Fig. 1; Fig. 2; Fig. 3	-	-	1	A
I _{TSM}	non-repetitive peak on- state current	full sine wave; $T_{j(init)} = 25 \text{ °C}$; $t_p = 20 \text{ ms}$; <u>Fig. 4</u> ; <u>Fig. 5</u>	-	-	12.5	Α
		full sine wave; $T_{j(init)}$ = 25 °C; t_p = 16.7 ms	-	-	13.8	A
Tj	junction temperature		-	-	125	°C
Static chara	acteristics					
I _{GT}	gate trigger current	V _D = 12 V; I _T = 0.1 A; T2+ G+; T _j = 25 °C; <u>Fig. 7</u>	0.3	-	5	mA
		V _D = 12 V; I _T = 0.1 A; T2+ G-; T _j = 25 °C; <u>Fig. 7</u>	0.3	-	5	mA

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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
		V _D = 12 V; I _T = 0.1 A; T2- G-; T _j = 25 °C; <u>Fig. 7</u>	0.3	-	5	mA
		V _D = 12 V; I _T = 0.1 A; T2- G+; T _j = 25 °C; <u>Fig. 7</u>	0.3	-	7	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; <u>Fig. 9</u>	-	-	10	mA
V _T	on-state voltage	I _T = 1 A; T _j = 25 °C; <u>Fig. 10</u>	-	1.3	1.6	V
Dynamic char	acteristics	·				
dV _D /dt	rate of rise of off-state voltage	V_{DM} = 536 V; T _j = 110 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit; Fig. 12	100	-	-	V/µs
dV _{com} /dt	rate of change of commutating voltage	V_D = 400 V; T _j = 110 °C; dI _{com} / dt = 0.44 A/ms; gate open circuit	1	-	-	V/µs

5. Pinning information

Table 2. F	Table 2. Pinning information								
Pin	Symbol	Description	Simplified outline	Graphic symbol					
1	T2	main terminal 2		T2T1					
2	G	gate		Sym051					
3	Τ1	main terminal 1	TO-92 (SOT54)						

6. Ordering information

Table 3. Ordering information							
Type number	Package						
	Name	Description	Version				
Z0107NA0	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54				

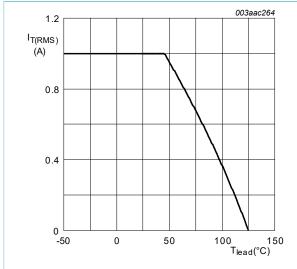
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7. Limiting values

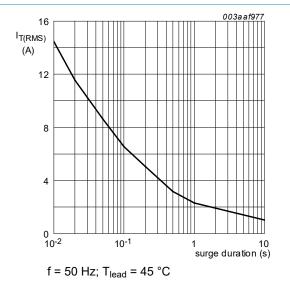
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DRM}	repetitive peak off-state voltage		-	800	V
I _{T(RMS)}	RMS on-state current	full sine wave; T _{lead} ≤ 45 °C; <u>Fig. 1; Fig. 2;</u> <u>Fig. 3</u>	-	1	A
I _{TSM}	non-repetitive peak on- state current	full sine wave; $T_{j(init)}$ = 25 °C; t_p = 20 ms; Fig. 4; Fig. 5	-	12.5	A
		full sine wave; T _{j(init)} = 25 °C; t _p = 16.7 ms	-	13.8	Α
l ² t	I ² t for fusing	t _p = 10 ms; SIN	-	0.78	A²s
dl _T /dt	rate of rise of on-state current	I _G = 20 mA; T2+ G+	-	50	A/µs
		I _G = 20 mA; T2+ G-	-	50	A/µs
		I _G = 20 mA; T2- G-	-	50	A/µs
		I _G = 20 mA; T2- G+	-	20	A/µs
I _{GM}	peak gate current		-	1	А
P _{GM}	peak gate power		-	2	W
P _{G(AV)}	average gate power	over any 20 ms period	-	0.1	W
T _{stg}	storage temperature		-40	150	°C
Tj	junction temperature		-	125	°C



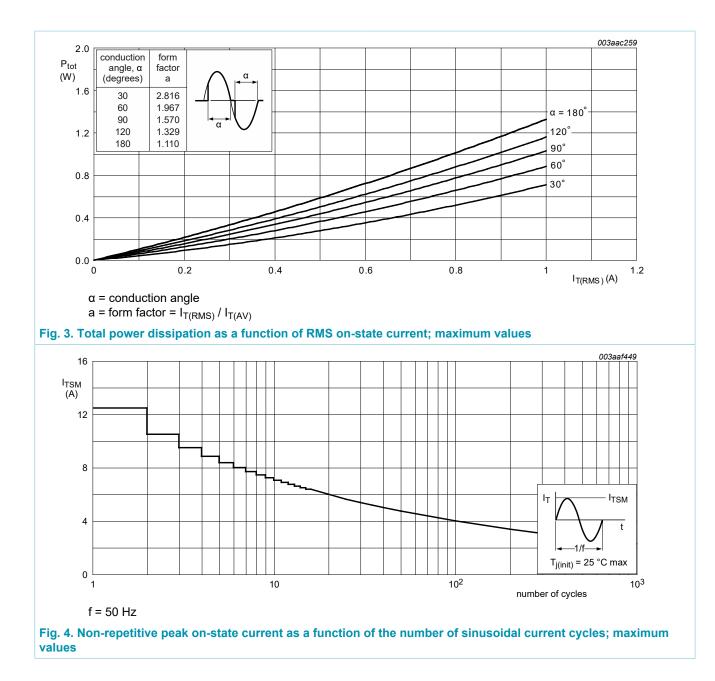






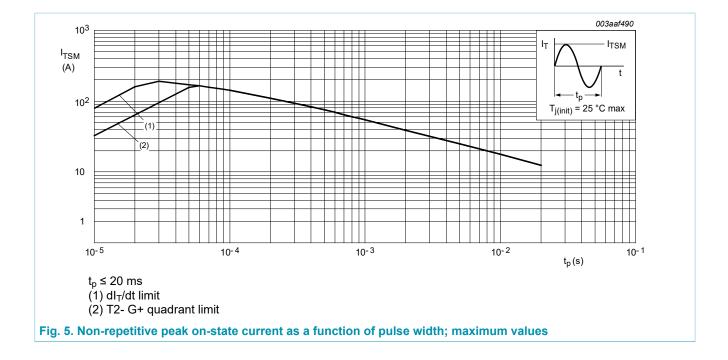
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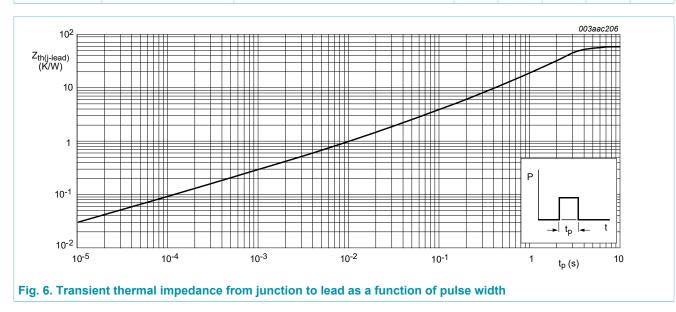
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8. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-lead)}$	thermal resistance from junction to lead	full cycle; <u>Fig. 6</u>	-	-	60	K/W
R _{th(j-a)}	thermal resistance from junction to ambient free air	full cycle; printed circuit board mounted; lead length 4 mm	-	150	-	K/W





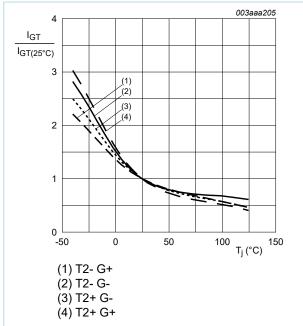
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9. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
I _{GT}	gate trigger current	$V_D = 12 V; I_T = 0.1 A; T2+ G+;$ T _j = 25 °C; Fig. 7	0.3	-	5	mA
		$V_D = 12 V; I_T = 0.1 A; T2+ G-;$ T _j = 25 °C; <u>Fig. 7</u>	0.3	-	5	mA
		V _D = 12 V; I _T = 0.1 A; T2- G-; T _j = 25 °C; <u>Fig. 7</u>	0.3	-	5	mA
		V _D = 12 V; I _T = 0.1 A; T2- G+; T _j = 25 °C; <u>Fig. 7</u>	0.3	-	7	mA
ΙL	latching current	V _D = 12 V; I _G = 0.1 A; T2+ G+; T _j = 25 °C; <u>Fig. 8</u>	-	-	10	mA
		V _D = 12 V; I _G = 0.1 A; T2+ G-; T _j = 25 °C; <u>Fig. 8</u>	-	-	25	mA
		V _D = 12 V; I _G = 0.1 A; T2- G-; T _j = 25 °C; <u>Fig. 8</u>	-	-	10	mA
		V _D = 12 V; I _G = 0.1 A; T2- G+; T _j = 25 °C; <u>Fig. 8</u>	-	-	10	mA
Чн	holding current	V _D = 12 V; T _j = 25 °C; <u>Fig. 9</u>	-	-	10	mA
√ _T	on-state voltage	I _T = 1 A; T _j = 25 °C; <u>Fig. 10</u>	-	1.3	1.6	V
V _{GT}	gate trigger voltage	V _D = 12 V; I _T = 0.1 A; T _j = 25 °C; Fig. 11	-	-	1	V
		V _D = 800 V; I _T = 0.1 A; T _j = 125 °C; Fig. 11	0.2	-	-	V
D	off-state current	V _D = 800 V; T _j = 125 °C	-	-	0.5	mA
Dynamic ch	naracteristics					
dV _D /dt	rate of rise of off-state voltage	V_{DM} = 536 V; T _j = 110 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; Fig. 12	100	-	-	V/µs
dV _{com} /dt	rate of change of commutating voltage	V_D = 400 V; T_j = 110 °C; $dI_{com}/$ dt = 0.44 A/ms; gate open circuit	1	-	-	V/µs

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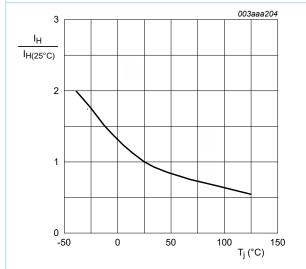
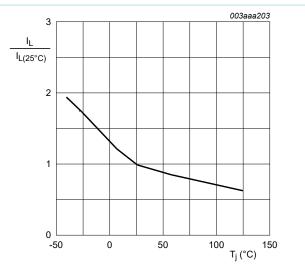
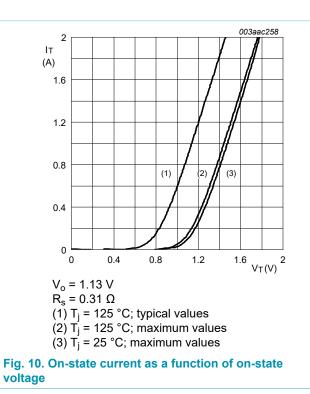


Fig. 9. Normalized holding current as a function of junction temperature

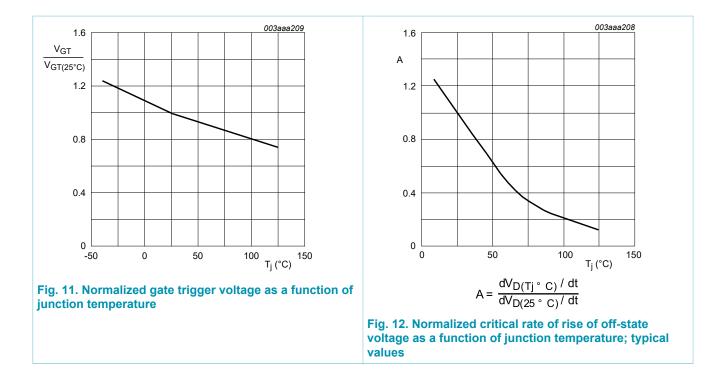






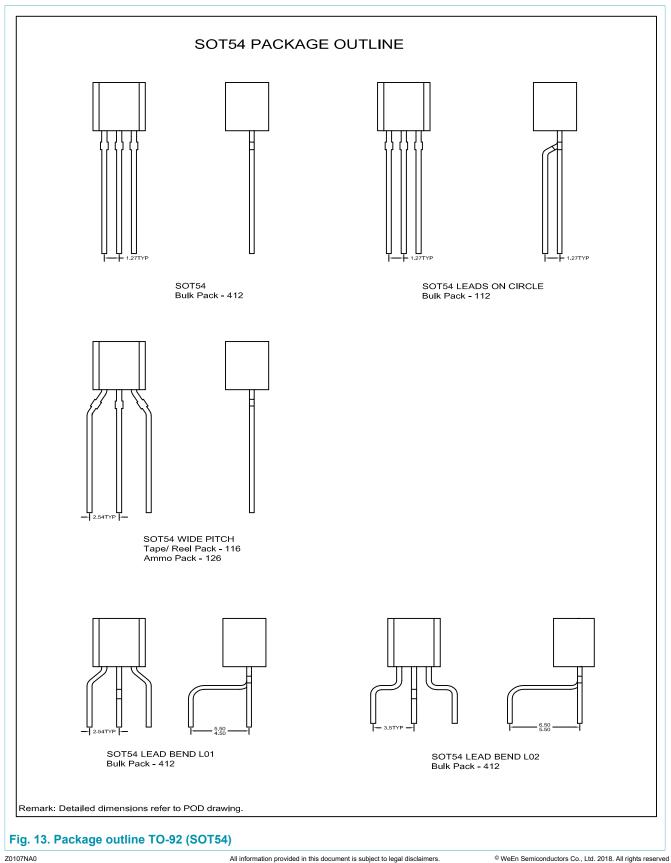
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10. Package outline



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11. Legal information

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Document status [1][2]	Product status [<u>3]</u>	Definition
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Product data sheet



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