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Renesas Electronics Corporation

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1. Overview

This MCU is built using the high-performance silicon gate CMOS process using a R8C/Tiny Series CPU core and is packaged in a 20-pin plastic molded LSSOP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1 Mbyte of address space, it is capable of executing instructions at high speed.

Furthermore, the data flash ROM (1KB × 2blocks) is embedded in the R8C/15 group.

The difference between R8C/14 and R8C/15 groups is only the existence of the data flash ROM. Their peripheral functions are the same.

1.1 Applications

Electric household appliance, office equipment, housing equipment (sensor, security), general industrial equipment, audio, etc.

1.2 Performance Overview

Table 1.1 lists the Performance Outline of the R8C/14 Group and Table 1.2 lists the Performance Outline of the R8C/15 Group.

Table 1.1 Performance Outline of the R8C/14 Group

| | Item | Performance |
|-------------------------------|--|---|
| CPU | Number of Basic Instructions | 89 instructions |
| | Minimum Instruction Execution Time | 50ns(f(XIN)=20MHz, VCC=3.0 to 5.5V) 100ns(f(XIN)=10MHz, VCC=2.7 to 5.5V) |
| | Operating Mode | Single-chip |
| | Memory Space | 1 Mbyte |
| | Memory Capacity | See Table 1.3 R8C/14 Group Product Information |
| Peripheral Function | Port | I/O port : 13 pins (including LED drive port), Input : 2 pins |
| | LED Drive Port | I/O port: 4 pins |
| | Timer | Timer X: 8 bits × 1 channel, Timer Z: 8 bits × 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits × 1 channel (Circuits of input capture and output compare) |
| | Serial Interface | 1 channel Clock synchronous serial I/O, UART |
| | Chip-Select Clock Synchronous Serial I/O (SSU) | 1 channel |
| | A/D Converter | 10-bit A/D converter: 1 circuit, 4 channels |
| | Watchdog Timer | 15 bits × 1 channel (with prescaler) Reset start selectable, Count source protection mode |
| | Interrupt | Internal: 9 factors, External: 4 factors, Software: 4 factors, Priority level: 7 levels |
| | Clock Generation Circuit | 2 circuits • Main clock oscillation circuit (Equipped with a built-in feedback resistor) • On-chip oscillator (high speed, low speed) Equipped with frequency adjustment function on high-speed on-chip oscillator |
| | Oscillation Stop Detection Function | Main clock oscillation stop detection function |
| | Voltage Detection Circuit | Included |
| | Power-On Reset Circuit | Included |
| Electric Characteristics | Supply Voltage | VCC=3.0 to 5.5V (f(XIN)=20MHz) VCC=2.7 to 5.5V (f(XIN)=10MHz) |
| | Power Consumption | Typ. 9mA (VCC=5.0V, f(XIN)=20MHz) Typ. 5mA (VCC=3.0V, f(XIN)=10MHz) Typ. 35μA (VCC=3.0V, wait mode, peripheral clock off) Typ. 0.7μA (VCC=3.0V, stop mode) |
| Flash Memory | Program/Erase Supply Voltage | VCC=2.7 to 5.5V |
| | Program/Erase Endurance | 100 times |
| Operating Ambient Temperature | | -20 to 85°C -40 to 85°C (D Version) |
| Package | | 20-pin plastic mold LSSOP |

Table 1.2 Performance Outline of the R8C/15 Group

| Item | | Performance |
|-------------------------------|--|--|
| CPU | Number of Basic Instructions | 89 instructions |
| | Minimum Instruction Execution Time | 50ns (f(XIN)=20MHz, VCC=3.0 to 5.5V) 100ns (f(XIN)=10MHz, VCC=2.7 to 5.5V) |
| | Operating Mode | Single-chip |
| | Memory Space | 1 Mbyte |
| | Memory Capacity | See Table 1.4 R8C/15 Group Product Information |
| Peripheral Function | Port | I/O : 13 pins (including LED drive port), Input : 2 pins |
| | LED drive port | I/O port: 4 pins |
| | Timer | Timer X: 8 bits × 1 channel, Timer Z: 8 bits × 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits × 1 channel (Circuits of input capture and output compare) |
| | Serial Interface | 1 channel Clock synchronous serial I/O, UART |
| | Chip-select clock synchronous serial I/O (SSU) | 1 channel |
| | A/D Converter | 10-bit A/D converter: 1 circuit, 4 channels |
| | Watchdog Timer | 15 bits × 1 channel (with prescaler) Reset start selectable, Count source protection mode |
| | Interrupt | Internal: 9 factors, External: 4 factors, Software: 4 factors Priority level: 7 levels |
| | Clock Generation Circuit | 2 circuits • Main clock generation circuit (Equipped with a built-in feedback resistor) • On-chip oscillator (high speed, low speed) Equipped with frequency adjustment function on high-speed on-chip oscillator |
| | Oscillation Stop Detection Function | Main clock oscillation stop detection function |
| | Voltage Detection Circuit | Included |
| | Power on Reset Circuit | Included |
| Electric Characteristics | Supply Voltage | VCC=3.0 to 5.5V (f(XIN)=20MHz) VCC=2.7 to 5.5V (f(XIN)=10MHz) |
| | Power Consumption | Typ. 9mA (VCC=5.0V, f(XIN)=20MHz) Typ. 5mA (VCC=3.0V, f(XIN)=10MHz) Typ. 35μA (VCC=3.0V, wait mode, peripheral clock off) Typ. 0.7μA (VCC=3.0V, stop mode) |
| Flash Memory | Program/Erase Supply Voltage | VCC=2.7 to 5.5V |
| | Program/Erase Endurance | 10,000 times (Data flash) 1,000 times (Program ROM) |
| Operating Ambient Temperature | | -20 to 85°C -40 to 85°C (D Version) |
| Package | | 20-pin plastic mold LSSOP |

1.3 Block Diagram

Figure 1.1 shows a Block Diagram.

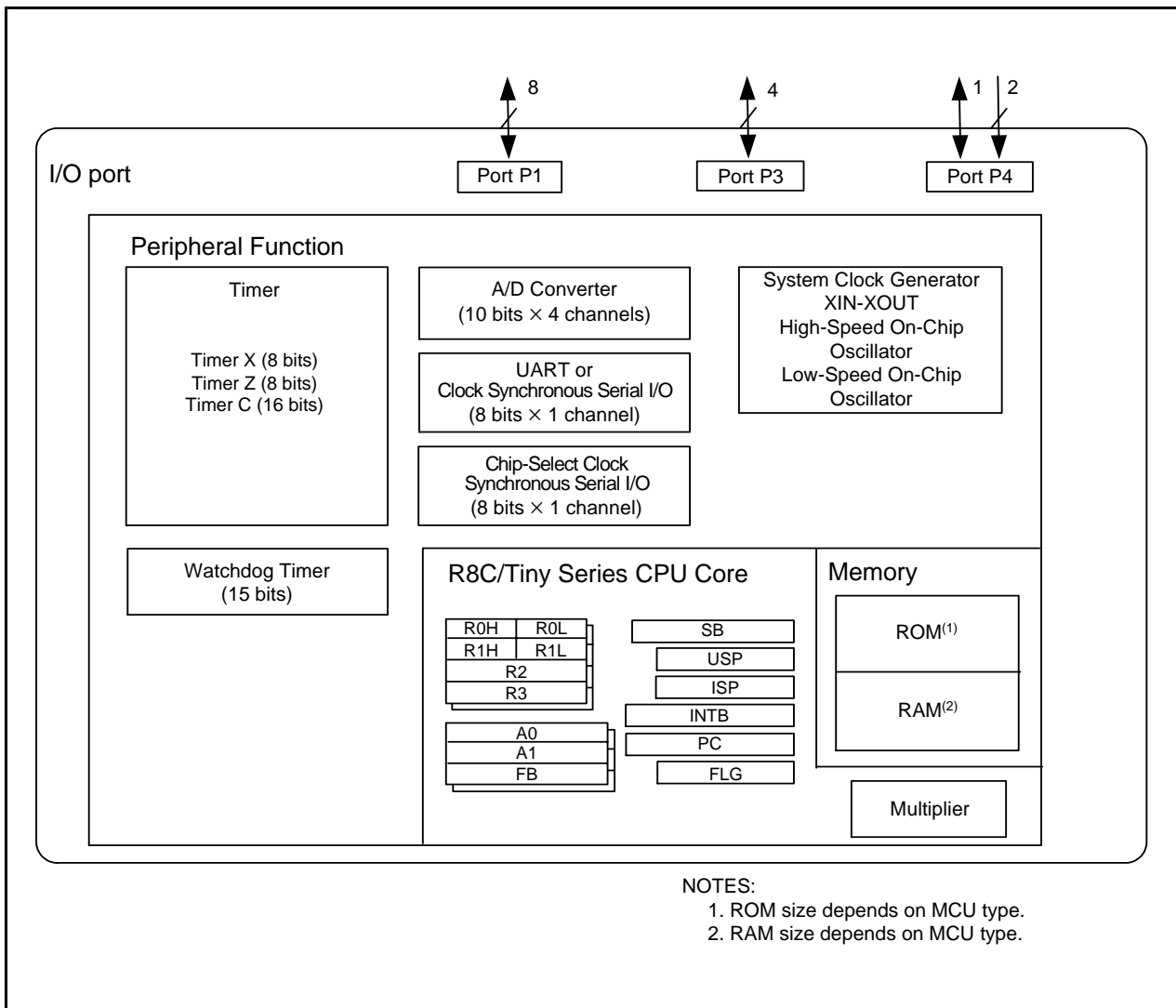


Figure 1.1 Block Diagram

1.4 Product Information

Table 1.3 lists the Product Information of R8C/14 Group and Table 1.4 lists the Product Information of R8C/15 Group.

Table 1.3 Product Information of R8C/14 Group As of Jan 2006

| Type No. | ROM capacity | RAM capacity | Package type | Remarks |
|-------------|--------------|--------------|--------------|----------------------|
| R5F21142SP | 8 Kbytes | 512 bytes | PLSP0020JB-A | Flash memory version |
| R5F21143SP | 12 Kbytes | 768 bytes | PLSP0020JB-A | |
| R5F21144SP | 16 Kbytes | 1 Kbyte | PLSP0020JB-A | |
| R5F21142DSP | 8 Kbytes | 512 bytes | PLSP0020JB-A | D version |
| R5F21143DSP | 12 Kbytes | 768 bytes | PLSP0020JB-A | |
| R5F21144DSP | 16 Kbytes | 1 Kbyte | PLSP0020JB-A | |

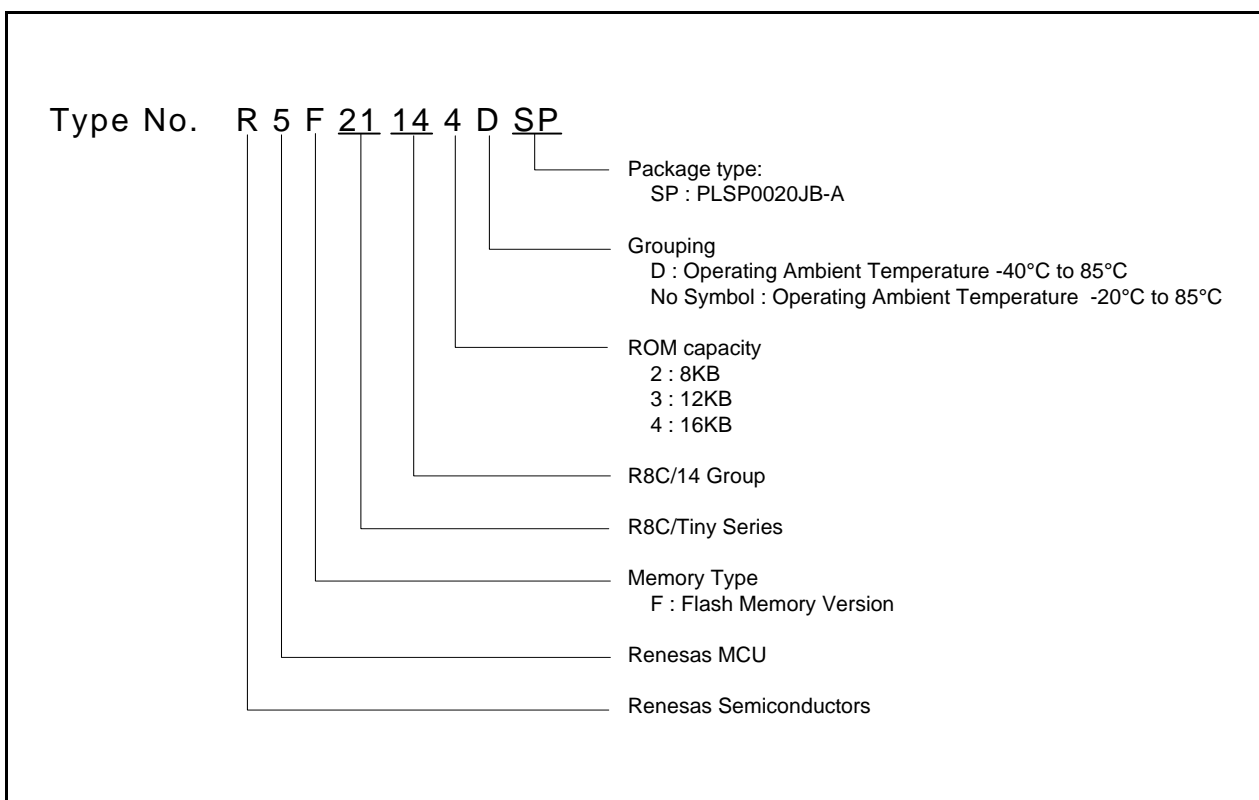


Figure 1.2 Part Number, Memory Size and Package of R8C/14 Group

Table 1.4 Product Information of R8C/15 Group **As of Jan 2006**

| Type No. | ROM capacity | | RAM capacity | Package type | Remarks | |
|-------------|--------------|-------------|--------------|--------------|----------------------|-----------|
| | Program ROM | Data flash | | | | |
| R5F21152SP | 8 Kbytes | 1 Kbyte x 2 | 512 bytes | PLSP0020JB-A | Flash memory version | |
| R5F21153SP | 12 Kbytes | 1 Kbyte x 2 | 768 bytes | PLSP0020JB-A | | |
| R5F21154SP | 16 Kbytes | 1 Kbyte x 2 | 1 Kbyte | PLSP0020JB-A | | |
| R5F21152DSP | 8 Kbytes | 1 Kbyte x 2 | 512 bytes | PLSP0020JB-A | | D version |
| R5F21153DSP | 12 Kbytes | 1 Kbyte x 2 | 768 bytes | PLSP0020JB-A | | |
| R5F21154DSP | 16 Kbytes | 1 Kbyte x 2 | 1 Kbyte | PLSP0020JB-A | | |

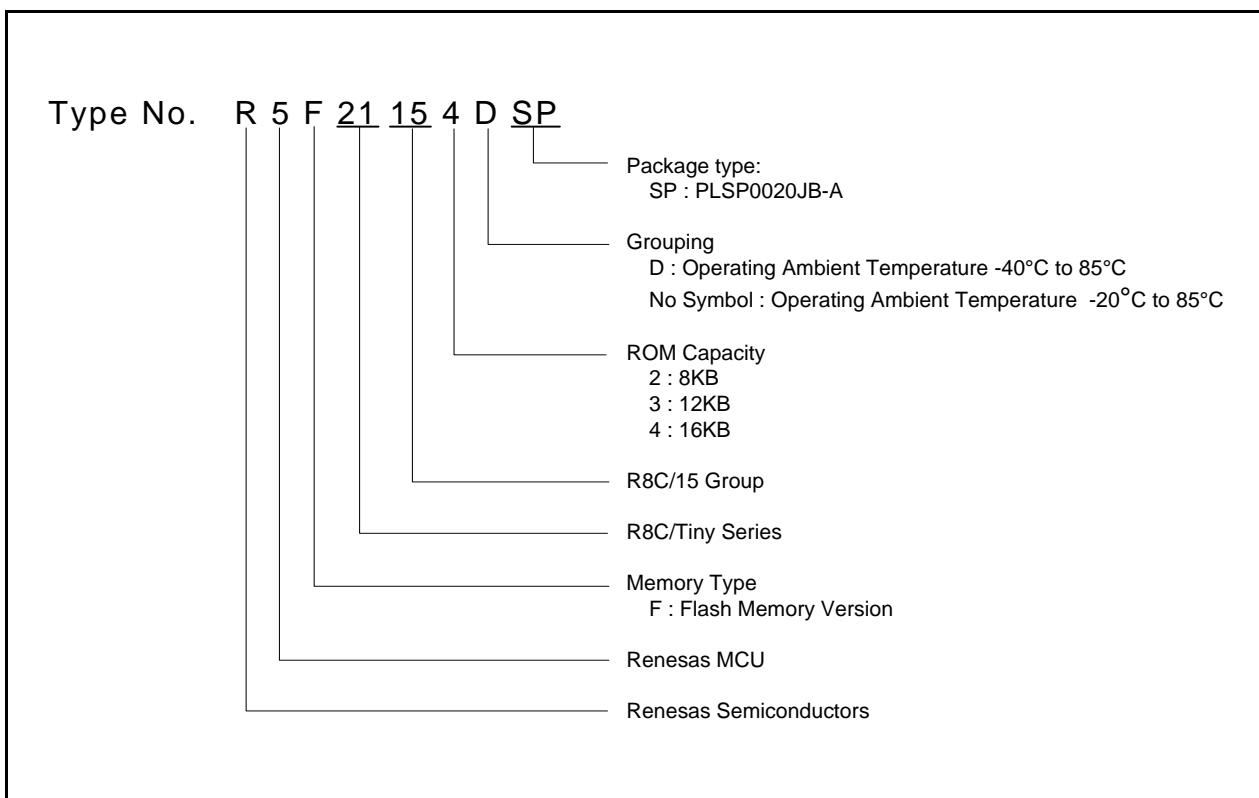


Figure 1.3 Part Number, Memory Size and Package of R8C/15 Group

1.5 Pin Assignments

Figure 1.4 shows the PLSP0020JB-A Package Pin Assignment (top view).

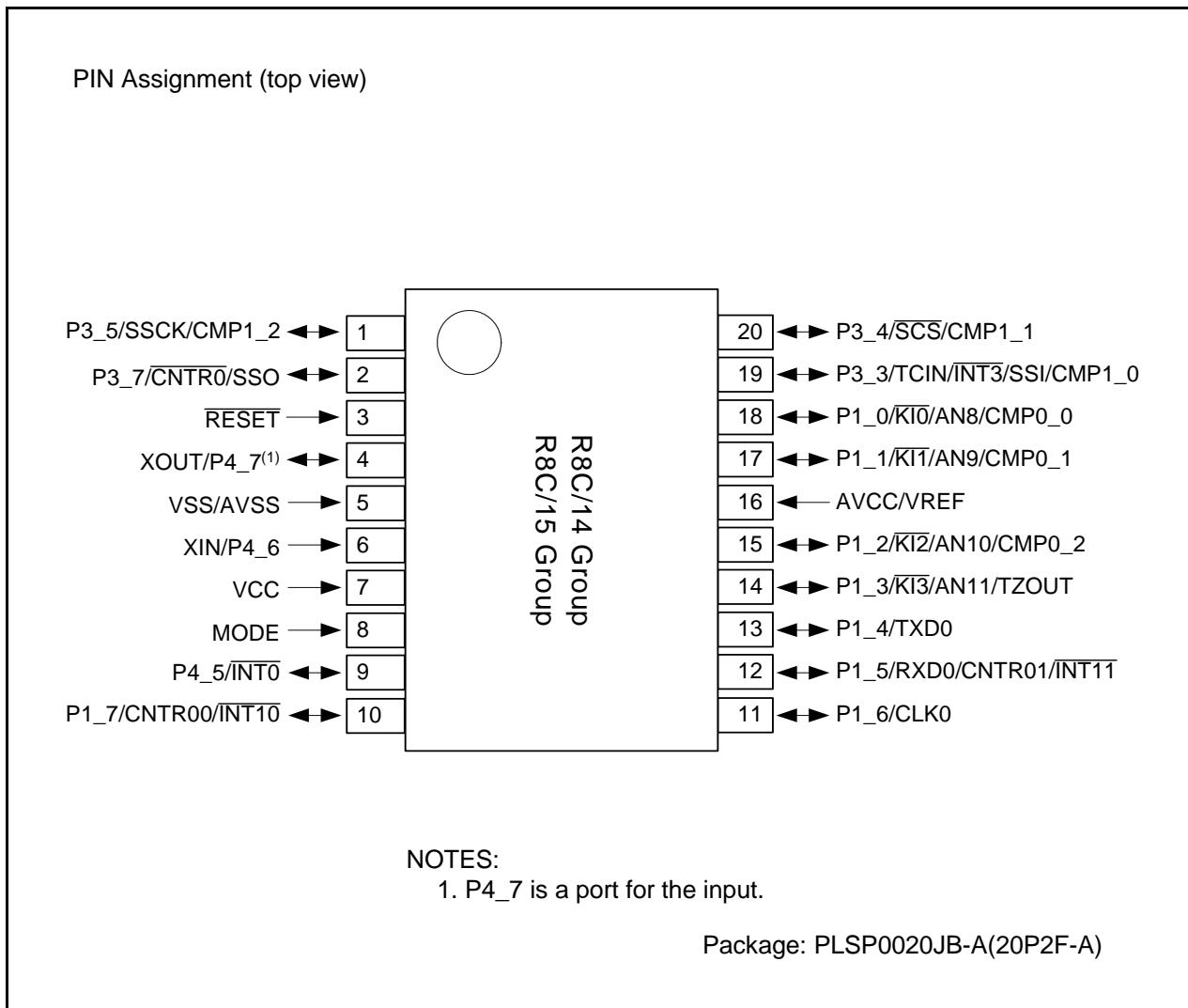


Figure 1.4 PLSP0020JB-A Package Pin Assignment (top view)

1.6 Pin Description

Table 1.5 lists the Pin Description and Table 1.6 lists the Pin Name Information by Pin Number.

Table 1.5 Pin Description

| Function | Pin name | I/O type | Description |
|-----------------------------------|--|----------|---|
| Power Supply Input | VCC VSS | I | Apply 2.7V to 5.5V to the VCC pin. Apply 0V to the VSS pin |
| Analog Power Supply Input | AVCC AVSS | I | Power supply input pins to A/D converter. Connect AVCC to VCC. Apply 0V to AVSS. Connect a capacitor between AVCC and AVSS. |
| Reset Input | $\overline{\text{RESET}}$ | I | Input "L" on this pin resets the MCU |
| MODE | MODE | I | Connect this pin to VCC via a resistor |
| Main Clock Input | XIN | I | These pins are provided for the main clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open. |
| Main Clock Output | XOUT | O | |
| $\overline{\text{INT}}$ Interrupt | $\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{INT3}}$ | I | INT interrupt input pins |
| Key Input Interrupt | KI0 to KI3 | I | Key input interrupt input pins |
| Timer X | CNTR0 | I/O | Timer X I/O pin |
| | $\overline{\text{CNTR0}}$ | O | Timer X output pin. |
| Timer Z | TZOUT | O | Timer Z output pin |
| Timer C | TCIN | I | Timer C input pin |
| | CMP0_0 to CMP0_2, CMP1_0 to CMP1_2 | O | Timer C output pins. |
| Serial Interface | CLK0 | I/O | Transfer clock I/O pin. |
| | RXD0 | I | Serial data input pin. |
| | TXD0 | O | Serial data output pin. |
| SSU | SSI | I/O | Data I/O pin. |
| | $\overline{\text{SCS}}$ | I/O | Chip-select signal I/O pin. |
| | SSCK | I/O | Clock I/O pin. |
| | SSO | I/O | Data I/O pin. |
| Reference Voltage Input | VREF | I | Reference voltage input pin to A/D converter Connect VREF to VCC |
| A/D Converter | AN8 to AN11 | I | Analog input pins to A/D converter |
| I/O Port | P1_0 to P1_7, P3_3 to P3_5, P3_7, P4_5 | I/O | These are CMOS I/O ports. Each port contains an I/O select direction register, allowing each pin in that port to be directed for input or output individually. Any port set to input can select whether to use a pull-up resistor or not by program. P1_0 to P1_3 also function as LED drive ports. |
| Input Port | P4_6, P4_7 | I | Port for input-only |

I: Input O: Output I/O: Input and output

Table 1.6 Pin Name Information by Pin Number

| Pin Number | Control Pin | Port | I/O Pin of Peripheral Function | | | | |
|------------|---------------------------|------|--------------------------------|---------------------------|------------------|---|---------------|
| | | | Interrupt | Timer | Serial Interface | Clock Synchronous Serial I/O with Chip Select | A/D Converter |
| 1 | | P3_5 | | CMP1_2 | | SSCK | |
| 2 | | P3_7 | | $\overline{\text{CNTR0}}$ | | SSO | |
| 3 | $\overline{\text{RESET}}$ | | | | | | |
| 4 | XOUT | P4_7 | | | | | |
| 5 | VSS/AVSS | | | | | | |
| 6 | XIN | P4_6 | | | | | |
| 7 | VCC | | | | | | |
| 8 | MODE | | | | | | |
| 9 | | P4_5 | $\overline{\text{INT0}}$ | | | | |
| 10 | | P1_7 | $\overline{\text{INT10}}$ | CNTR00 | | | |
| 11 | | P1_6 | | | CLK0 | | |
| 12 | | P1_5 | $\overline{\text{INT11}}$ | CNTR01 | RXD0 | | |
| 13 | | P1_4 | | | TXD0 | | |
| 14 | | P1_3 | $\overline{\text{KI3}}$ | TZOUT | | | AN11 |
| 15 | | P1_2 | $\overline{\text{KI2}}$ | CMP0_2 | | | AN10 |
| 16 | AVCC/VREF | | | | | | |
| 17 | | P1_1 | $\overline{\text{KI1}}$ | CMP0_1 | | | AN9 |
| 18 | | P1_0 | $\overline{\text{KI0}}$ | CMP0_0 | | | AN8 |
| 19 | | P3_3 | $\overline{\text{INT3}}$ | TCIN/CMP1_0 | | SSI | |
| 20 | | P3_4 | | CMP1_1 | | $\overline{\text{SCS}}$ | |

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Register. The CPU contains 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. Two sets of register banks are provided.

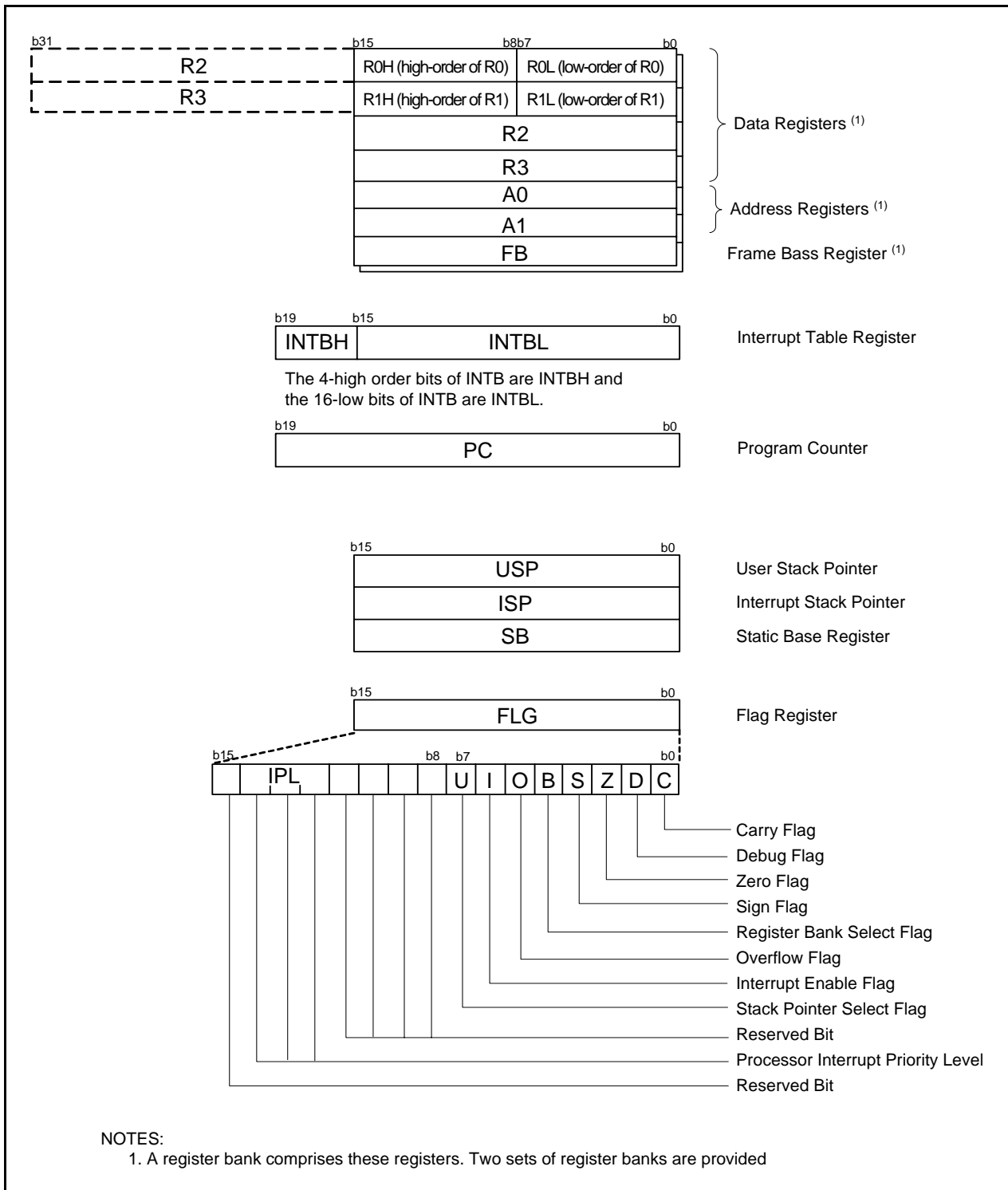


Figure 2.1 CPU Register

2.1 Data Registers (R0, R1, R2 and R3)

R0 is a 16-bit register for transfer, arithmetic and logic operations. The same applies to R1 to R3. The R0 can be split into high-order bit (R0H) and low-order bit (R0L) to be used separately as 8-bit data registers. The same applies to R1H and R1L as R0H and R0L. R2 can be combined with R0 to be used as a 32-bit data register (R2R0). The same applies to R3R1 as R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. They also are used for transfer, arithmetic and logic operations. The same applies to A1 as A0. A0 can be combined with A0 to be used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC, 20 bits wide, indicates the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointer (SP), USP and ISP, are 16 bits wide each. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is a 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic logic unit.

2.8.2 Debug Flag (D)

The D flag is for debug only. Set to "0".

2.8.3 Zero Flag (Z)

The Z flag is set to "1" when an arithmetic operation resulted in 0; otherwise, "0".

2.8.4 Sign Flag (S)

The S flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, "0".

2.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is "0". The register bank 1 is selected when this flag is set to "1".

2.8.6 Overflow Flag (O)

The O flag is set to "1" when the operation resulted in an overflow; otherwise, "0".

2.8.7 Interrupt Enable Flag (I Flag)

The I flag enables a maskable interrupt.

An interrupt is disabled when the I flag is set to "0", and are enabled when the I flag is set to "1". The I flag is set to "0" when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is set to "0", USP is selected when the U flag is set to "1".

The U flag is set to "0" when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has greater priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

When write to this bit, set to "0". When read, its content is indeterminate.

3. Memory

3.1 R8C/14 Group

Figure 3.1 is a Memory Map of R8C/14 Group. The R8C/14 group provides 1-Mbyte address space from addresses 00000h to FFFFFh.

The internal ROM is allocated lower addresses beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM is allocated addresses 0C000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal RAM is allocated higher addresses beginning with address 00400h. For example, a 1-Kbyte internal RAM is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but for calling subroutines and stacks when interrupt request is acknowledged.

Special function registers (SFR) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated them. All addresses, which have nothing allocated within the SFR, are reserved area and cannot be accessed by users.

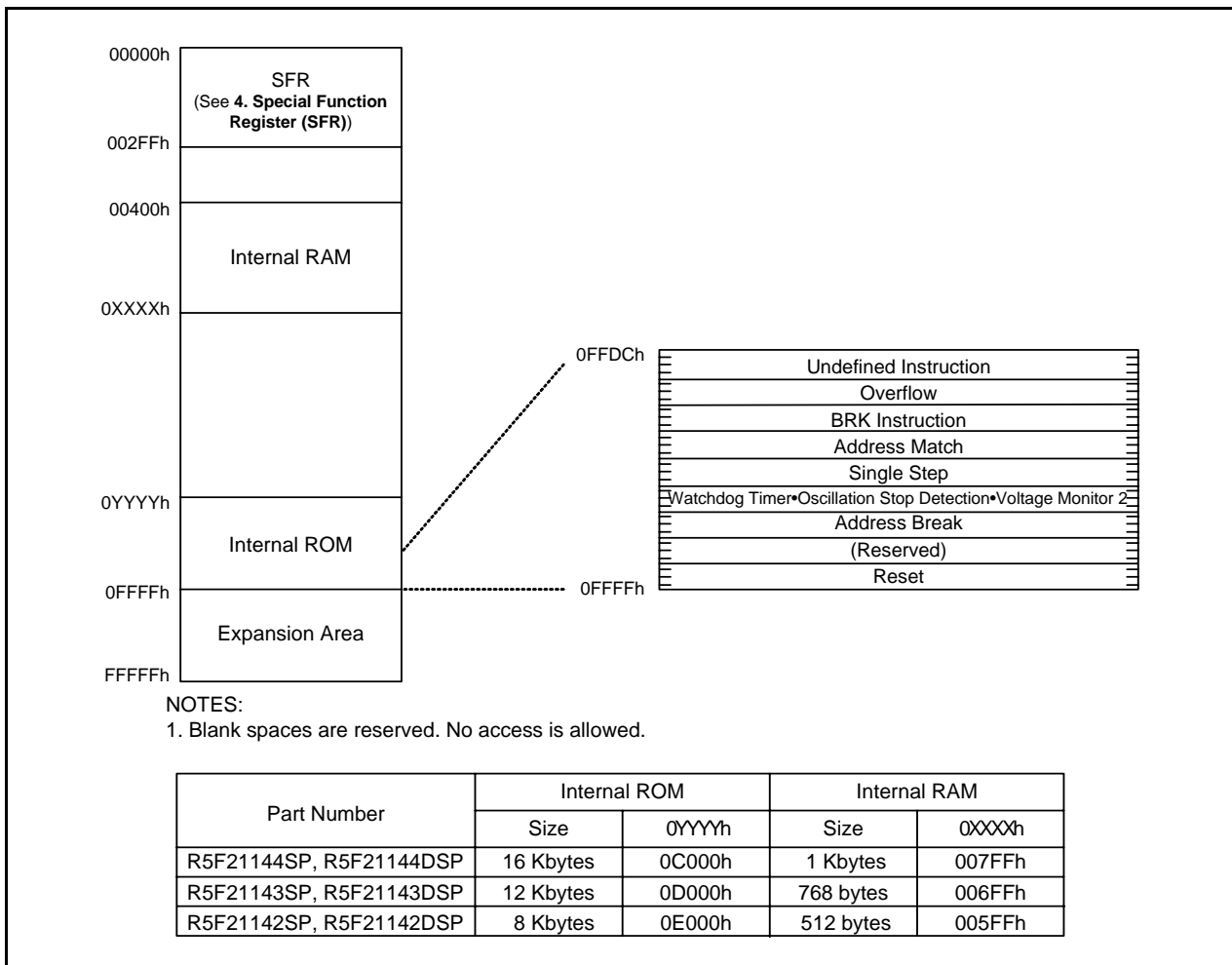


Figure 3.1 Memory Map of R8C/14 Group

3.2 R8C/15 Group

Figure 3.2 is a Memory Map of R8C/15 Group. The R8C/15 group provides 1-Mbyte address space from addresses 00000h to FFFFFh.

The internal ROM (program ROM) is allocated lower addresses beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM is allocated addresses 0C000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.

The internal RAM is allocated higher addresses beginning with address 00400h. For example, a 1-Kbyte internal RAM is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but for calling subroutines and stacks when interrupt request is acknowledged.

Special function registers (SFR) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated them. All addresses, which have nothing allocated within the SFR, are reserved area and cannot be accessed by users.

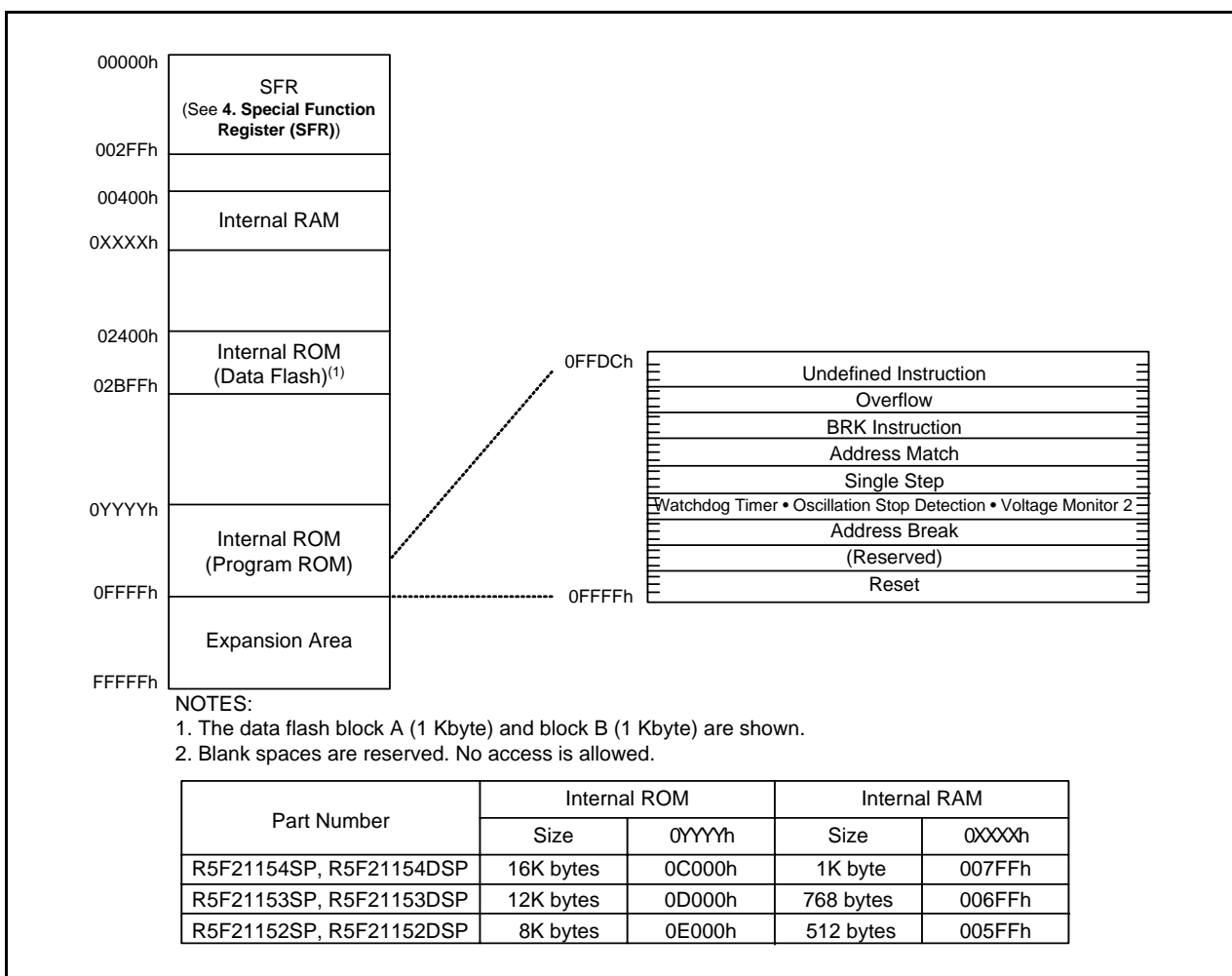


Figure 3.2 Memory Map of R8C/15 Group

4. Special Function Register (SFR)

SFR (Special Function Register) is the control register of peripheral functions. Tables 4.1 to 4.4 list the SFR information.

Table 4.1 SFR Information(1)(1)

| Address | Register | Symbol | After reset |
|---------|---|--------|--|
| 0000h | | | |
| 0001h | | | |
| 0002h | | | |
| 0003h | | | |
| 0004h | Processor Mode Register 0 | PM0 | 00h |
| 0005h | Processor Mode Register 1 | PM1 | 00h |
| 0006h | System Clock Control Register 0 | CM0 | 01101000b |
| 0007h | System Clock Control Register 1 | CM1 | 00100000b |
| 0008h | | | |
| 0009h | Address Match Interrupt Enable Register | AIER | 00h |
| 000Ah | Protect Register | PRCR | 00h |
| 000Bh | | | |
| 000Ch | Oscillation Stop Detection Register | OCD | 00000100b |
| 000Dh | Watchdog Timer Reset Register | WDTR | XXh |
| 000Eh | Watchdog Timer Start Register | WDTS | XXh |
| 000Fh | Watchdog Timer Control Register | WDC | 00011111b |
| 0010h | Address Match Interrupt Register 0 | RMAD0 | 00h |
| 0011h | | | 00h |
| 0012h | | | X0h |
| 0013h | | | |
| 0014h | Address Match Interrupt Register 1 | RMAD1 | 00h |
| 0015h | | | 00h |
| 0016h | | | X0h |
| 0017h | | | |
| 0018h | | | |
| 0019h | | | |
| 001Ah | | | |
| 001Bh | | | |
| 001Ch | Count Source Protection Mode Register | CSPR | 00h |
| 001Dh | | | |
| 001Eh | INT0 Input Filter Select Register | INT0F | 00h |
| 001Fh | | | |
| 0020h | High-Speed On-Chip Oscillator Control Register 0 | HRA0 | 00h |
| 0021h | High-Speed On-Chip Oscillator Control Register 1 | HRA1 | When shipping |
| 0022h | High-Speed On-Chip Oscillator Control Register 2 | HRA2 | 00h |
| 0023h | | | |
| 0024h | | | |
| 0025h | | | |
| 0026h | | | |
| 0027h | | | |
| 0028h | | | |
| 0029h | | | |
| 002Ah | | | |
| 002Bh | | | |
| 002Ch | | | |
| 002Dh | | | |
| 002Eh | | | |
| 002Fh | | | |
| 0030h | | | |
| 0031h | Voltage Detection Register 1 ⁽²⁾ | VCA1 | 00001000b |
| 0032h | Voltage Detection Register 2 ⁽²⁾ | VCA2 | 00h ⁽³⁾ 01000000b ⁽⁴⁾ |
| 0033h | | | |
| 0034h | | | |
| 0035h | | | |
| 0036h | Voltage Monitor 1 Circuit Control Register ⁽²⁾ | VW1C | 0000X000b ⁽³⁾ 0100X001b ⁽⁴⁾ |
| 0037h | Voltage Monitor 2 Circuit Control Register ⁽⁵⁾ | VW2C | 00h |
| 0038h | | | |
| 0039h | | | |
| 003Ah | | | |
| 003Bh | | | |
| 003Ch | | | |
| 003Dh | | | |
| 003Eh | | | |
| 003Fh | | | |

X: Undefined

NOTES:

- Blank spaces are reserved. No access is allowed.
- Software reset, the watchdog timer reset or the voltage monitor 2 reset does not affect this register.
- Owing to Hardware reset.
- Owing to Power-on reset or the voltage monitor 1 reset.
- Software reset, the watchdog timer reset or the voltage monitor 2 reset does not affect the b2 and b3.

Table 4.2 SFR Information(2)(1)

| Address | Register | Symbol | After reset |
|---------|---|--------|-------------|
| 0040h | | | |
| 0041h | | | |
| 0042h | | | |
| 0043h | | | |
| 0044h | | | |
| 0045h | | | |
| 0046h | | | |
| 0047h | | | |
| 0048h | | | |
| 0049h | | | |
| 004Ah | | | |
| 004Bh | | | |
| 004Ch | | | |
| 004Dh | Key Input Interrupt Control Register | KUPIC | XXXXX000b |
| 004Eh | A/D Conversion Interrupt Control Register | ADIC | XXXXX000b |
| 004Fh | SSU Interrupt Control Register | SSUAIC | XXXXX000b |
| 0050h | Compare 1 Interrupt Control Register | CMP1IC | XXXXX000b |
| 0051h | UART0 Transmit Interrupt Control Register | S0TIC | XXXXX000b |
| 0052h | UART0 Receive Interrupt Control Register | S0RIC | XXXXX000b |
| 0053h | | | |
| 0054h | | | |
| 0055h | | | |
| 0056h | Timer X Interrupt Control Register | TXIC | XXXXX000b |
| 0057h | | | |
| 0058h | Timer Z Interrupt Control Register | TZIC | XXXXX000b |
| 0059h | INT1 Interrupt Control Register | INT1IC | XXXXX000b |
| 005Ah | INT3 Interrupt Control Register | INT3IC | XXXXX000b |
| 005Bh | Timer C Interrupt Control Register | TCIC | XXXXX000b |
| 005Ch | Compare 0 Interrupt Control Register | CMP0IC | XXXXX000b |
| 005Dh | INT0 Interrupt Control Register | INT0IC | XX00X000b |
| 005Eh | | | |
| 005Fh | | | |
| 0060h | | | |
| 0061h | | | |
| 0062h | | | |
| 0063h | | | |
| 0064h | | | |
| 0065h | | | |
| 0066h | | | |
| 0067h | | | |
| 0068h | | | |
| 0069h | | | |
| 006Ah | | | |
| 006Bh | | | |
| 006Ch | | | |
| 006Dh | | | |
| 006Eh | | | |
| 006Fh | | | |
| 0070h | | | |
| 0071h | | | |
| 0072h | | | |
| 0073h | | | |
| 0074h | | | |
| 0075h | | | |
| 0076h | | | |
| 0077h | | | |
| 0078h | | | |
| 0079h | | | |
| 007Ah | | | |
| 007Bh | | | |
| 007Ch | | | |
| 007Dh | | | |
| 007Eh | | | |
| 007Fh | | | |

X: Undefined

NOTES:

- Blank spaces are reserved. No access is allowed.

Table 4.3 SFR Information(3)(1)

| Address | Register | Symbol | After reset |
|---------|---|--------|--------------------|
| 0080h | Timer Z Mode Register | TZMR | 00h |
| 0081h | | | |
| 0082h | | | |
| 0083h | | | |
| 0084h | Timer Z Waveform Output Control Register | PUM | 00h |
| 0085h | Prescaler Z Register | PREZ | FFh |
| 0086h | Timer Z Secondary Register | TZSC | FFh |
| 0087h | Timer Z Primary Register | TZPR | FFh |
| 0088h | | | |
| 0089h | | | |
| 008Ah | Timer Z Output Control Register | TZOC | 00h |
| 008Bh | Timer X Mode Register | TXMR | 00h |
| 008Ch | Prescaler X Register | PREX | FFh |
| 008Dh | Timer X Register | TX | FFh |
| 008Eh | Timer Count Source Setting Register | TCSS | 00h |
| 008Fh | | | |
| 0090h | Timer C Register | TC | 00h |
| 0091h | | | 00h |
| 0092h | | | |
| 0093h | | | |
| 0094h | | | |
| 0095h | | | |
| 0096h | External Input Enable Register | INTEN | 00h |
| 0097h | | | |
| 0098h | Key Input Enable Register | KIEN | 00h |
| 0099h | | | |
| 009Ah | Timer C Control Register 0 | TCC0 | 00h |
| 009Bh | Timer C Control Register 1 | TCC1 | 00h |
| 009Ch | Capture, Compare 0 Register | TM0 | 00h |
| 009Dh | | | 00h ⁽²⁾ |
| 009Eh | Compare 1 Register | TM1 | FFh |
| 009Fh | | | FFh |
| 00A0h | UART0 Transmit/Receive Mode Register | U0MR | 00h |
| 00A1h | UART0 Bit Rate Register | U0BRG | XXh |
| 00A2h | UART0 Transmit Buffer Register | U0TB | XXh |
| 00A3h | | | XXh |
| 00A4h | UART0 Transmit/Receive Control Register 0 | U0C0 | 00001000b |
| 00A5h | UART0 Transmit/Receive Control Register 1 | U0C1 | 00000010b |
| 00A6h | UART0 Receive Buffer Register | U0RB | XXh |
| 00A7h | | | XXh |
| 00A8h | | | |
| 00A9h | | | |
| 00AAh | | | |
| 00ABh | | | |
| 00ACh | | | |
| 00ADh | | | |
| 00AEh | | | |
| 00AFh | | | |
| 00B0h | UART Transmit/Receive Control Register 2 | U0CON | 00h |
| 00B1h | | | |
| 00B2h | | | |
| 00B3h | | | |
| 00B4h | | | |
| 00B5h | | | |
| 00B6h | | | |
| 00B7h | | | |
| 00B8h | SS Control Register H | SSCRH | 00h |
| 00B9h | SS Control Register L | SSCRL | 7Dh |
| 00BAh | SS Mode Register | SSMR | 18h |
| 00BBh | SS Enable Register | SSER | 00h |
| 00BCh | SS Status Register | SSSR | 00h |
| 00BDh | SS Mode Register 2 | SSMR2 | 00h |
| 00BEh | SS Transmit Data Register | SSTDR | FFh |
| 00BFh | SS Receive Data Register | SSRDR | FFh |

X: Undefined

NOTES:

- Blank spaces are reserved. No access is allowed.
- When output compare mode (the TCC13 bit in the TCC1 register = 1) is selected, the value after reset is "FFFFh".

Table 4.4 SFR Information(4)(1)

| Address | Register | Symbol | After reset |
|---------|---|--------|-------------|
| 00C0h | A/D Register | AD | XXh |
| 00C1h | | | XXh |
| 00C2h | | | |
| 00C3h | | | |
| 00C4h | | | |
| 00C5h | | | |
| 00C6h | | | |
| 00C7h | | | |
| 00C8h | | | |
| 00C9h | | | |
| 00CAh | | | |
| 00CBh | | | |
| 00CCh | | | |
| 00CDh | | | |
| 00CEh | | | |
| 00CFh | | | |
| 00D0h | | | |
| 00D1h | | | |
| 00D2h | | | |
| 00D3h | | | |
| 00D4h | A/D Control Register 2 | ADCON2 | 00h |
| 00D5h | | | |
| 00D6h | A/D Control Register 0 | ADCON0 | 00000XXb |
| 00D7h | A/D Control Register 1 | ADCON1 | 00h |
| 00D8h | | | |
| 00D9h | | | |
| 00DAh | | | |
| 00DBh | | | |
| 00DCh | | | |
| 00DDh | | | |
| 00DEh | | | |
| 00DFh | | | |
| 00E0h | | | |
| 00E1h | Port P1 Register | P1 | XXh |
| 00E2h | | | |
| 00E3h | Port P1 Direction Register | PD1 | 00h |
| 00E4h | | | |
| 00E5h | Port P3 Register | P3 | XXh |
| 00E6h | | | |
| 00E7h | Port P3 Direction Register | PD3 | 00h |
| 00E8h | Port P4 Register | P4 | XXh |
| 00E9h | | | |
| 00EAh | Port P4 Direction Register | PD4 | 00h |
| 00EBh | | | |
| 00ECh | | | |
| 00EDh | | | |
| 00EEh | | | |
| 00EFh | | | |
| 00F0h | | | |
| 00F1h | | | |
| 00F2h | | | |
| 00F3h | | | |
| 00F4h | | | |
| 00F5h | | | |
| 00F6h | | | |
| 00F7h | | | |
| 00F8h | | | |
| 00F9h | | | |
| 00FAh | | | |
| 00FBh | | | |
| 00FCh | Pull-Up Control Register 0 | PUR0 | 00XX0000b |
| 00FDh | Pull-Up Control Register 1 | PUR1 | XXXXXX0Xb |
| 00FEh | Port P1 Drive Capacity Control Register | DRR | 00h |
| 00FFh | Timer C Output Control Register | TCOUT | 00h |
| 01B3h | Flash Memory Control Register 4 | FMR4 | 01000000b |
| 01B4h | | | |
| 01B5h | Flash Memory Control Register 1 | FMR1 | 1000000Xb |
| 01B6h | | | |
| 01B7h | Flash Memory Control Register 0 | FMR0 | 00000001b |
| 0FFFh | Optional Function Select Register | OFS | (2) |

X: Undefined

NOTES:

- Blank columns, 0100h to 01B2h and 01B8h to 02FFh are all reserved. No access is allowed.
- The OFS register cannot be changed by program. Use a flash programmer to write to it.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

| Symbol | Parameter | Condition | Rated value | Unit |
|------------------|-------------------------------|------------------------------------|-----------------------------------|------|
| V _{CC} | Supply Voltage | V _{CC} = AV _{CC} | -0.3 to 6.5 | V |
| AV _{CC} | Analog Supply Voltage | V _{CC} = AV _{CC} | -0.3 to 6.5 | V |
| V _I | Input Voltage | | -0.3 to V _{CC} +0.3 | V |
| V _O | Output Voltage | | -0.3 to V _{CC} +0.3 | V |
| P _d | Power Dissipation | T _{opr} = 25°C | 300 | mW |
| T _{opr} | Operating Ambient Temperature | | -20 to 85 / -40 to 85 (D version) | °C |
| T _{stg} | Storage Temperature | | -65 to 150 | °C |

Table 5.2 Recommended Operating Conditions

| Symbol | Parameter | | Conditions | Standard | | | Unit |
|-----------------------|--|--|-------------------------------|--------------------|----------------------------------|--------------------|------|
| | | | | Min. | Typ. | Max. | |
| V _{CC} | Supply Voltage | | | 2.7 | – | 5.5 | V |
| AV _{CC} | Analog Supply Voltage | | | – | V _{CC} (³) | – | V |
| V _{SS} | Supply Voltage | | | – | 0 | – | V |
| AV _{SS} | Analog Supply Voltage | | | – | 0 | – | V |
| V _{IH} | Input “H” Voltage | | | 0.8V _{CC} | – | V _{CC} | V |
| V _{IL} | Input “L” Voltage | | | 0 | – | 0.2V _{CC} | V |
| I _{OH(sum)} | Peak Sum Output “H” Current | Sum of All Pins I _{OH} (peak) | | – | – | -60 | mA |
| I _{OH(peak)} | Peak Output “H” Current | | | – | – | -10 | mA |
| I _{OH(avg)} | Average Output “H” Current | | | – | – | -5 | mA |
| I _{OL(sum)} | Peak Sum Output “L” Currents | Sum of All Pins I _{OL} (peak) | | – | – | 60 | mA |
| I _{OL(peak)} | Peak Output “L” Currents | Except P1_0 to P1_3 | | – | – | 10 | mA |
| | | P1_0 to P1_3 | Drive Capacity HIGH | – | – | 30 | mA |
| | | | Drive Capacity LOW | – | – | 10 | mA |
| I _{OL(avg)} | Average Output “L” Current | Except P1_0 to P1_3 | | – | – | 5 | mA |
| | | P1_0 to P1_3 | Drive Capacity HIGH | – | – | 15 | mA |
| | | | Drive Capacity LOW | – | – | 5 | mA |
| f _(XIN) | Main Clock Input Oscillation Frequency | | 3.0V ≤ V _{CC} ≤ 5.5V | 0 | – | 20 | MHz |
| | | | 2.7V ≤ V _{CC} < 3.0V | 0 | – | 10 | MHz |

NOTES:

1. V_{CC} = AV_{CC} = 2.7 to 5.5V at T_{opr} = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. The typical values when average output current is 100ms.
3. Hold V_{CC} = AV_{CC}.

Table 5.3 A/D Converter Characteristics

| Symbol | Parameter | | Conditions | Standard | | | Unit |
|--------------|--|-----------------------|---|----------|----------------|-----------|---------------|
| | | | | Min. | Typ. | Max. | |
| – | Resolution | | $V_{ref} = V_{CC}$ | – | – | 10 | Bits |
| – | Absolute Accuracy | 10-Bit Mode | $\phi_{AD} = 10\text{MHz}$, $V_{ref} = V_{CC} = 5.0\text{V}$ | – | – | ± 3 | LSB |
| | | 8-Bit Mode | $\phi_{AD} = 10\text{MHz}$, $V_{ref} = V_{CC} = 5.0\text{V}$ | – | – | ± 2 | LSB |
| | | 10-Bit Mode | $\phi_{AD} = 10\text{MHz}$, $V_{ref} = V_{CC} = 3.3\text{V}^{(3)}$ | – | – | ± 5 | LSB |
| | | 8-Bit Mode | $\phi_{AD} = 10\text{MHz}$, $V_{ref} = V_{CC} = 3.3\text{V}^{(3)}$ | – | – | ± 2 | LSB |
| R_{ladder} | Resistor Ladder | | $V_{ref} = V_{CC}$ | 10 | – | 40 | $k\Omega$ |
| t_{conv} | Conversion Time | 10-Bit Mode | $\phi_{AD} = 10\text{MHz}$, $V_{ref} = V_{CC} = 5.0\text{V}$ | 3.3 | – | – | μs |
| | | 8-Bit Mode | $\phi_{AD} = 10\text{MHz}$, $V_{ref} = V_{CC} = 5.0\text{V}$ | 2.8 | – | – | μs |
| V_{ref} | Reference voltage | | | – | $V_{CC}^{(4)}$ | – | V |
| V_{IA} | Analog Input Voltage | | | 0 | – | V_{ref} | V |
| – | A/D Operating Clock Frequency ⁽²⁾ | Without Sample & Hold | | 0.25 | – | 10 | MHz |
| | | With Sample & Hold | | 1 | – | 10 | MHz |

NOTES:

1. $V_{CC} = AV_{CC} = 2.7$ to 5.5V at $T_{opr} = -20$ to $85\text{ }^\circ\text{C}$ / -40 to $85\text{ }^\circ\text{C}$, unless otherwise specified.
2. If f_1 exceeds 10MHz , divide the f_1 and hold A/D operating clock frequency (ϕ_{AD}) 10MHz or below.
3. If the AV_{CC} is less than 4.2V , divide the f_1 and hold A/D operating clock frequency (ϕ_{AD}) $f_1/2$ or below.
4. Hold $V_{CC} = V_{ref}$

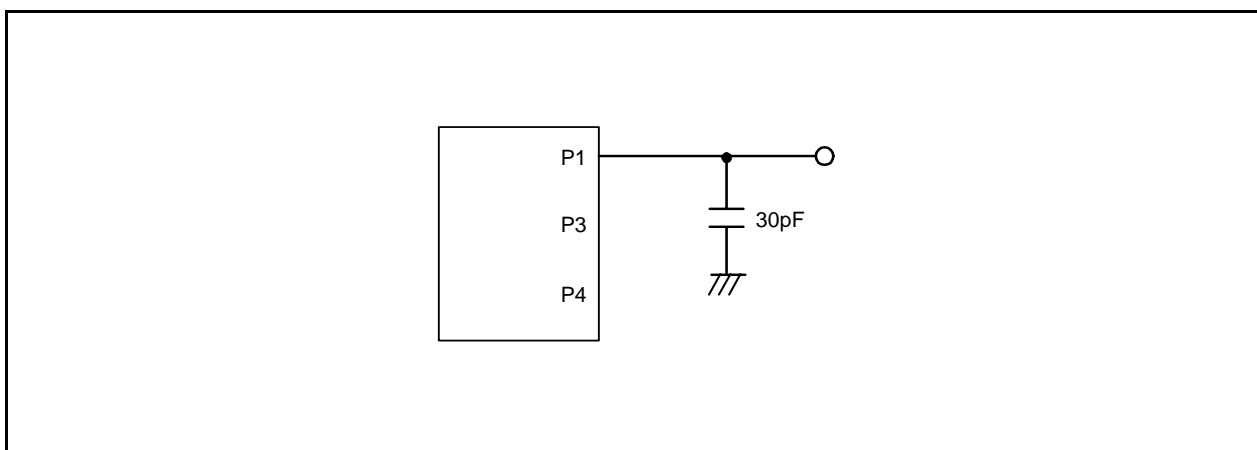
**Figure 5.1 Port P1, P3 and P4 Measurement Circuit**

Table 5.4 Flash Memory (Program ROM) Electrical Characteristics

| Symbol | Parameter | Conditions | Standard | | | Unit |
|------------------------|---|---|----------------------|------|------|-------|
| | | | Min. | Typ. | Max. | |
| – | Program/Erase Endurance ⁽²⁾ | R8C/14 Group | 100 ⁽³⁾ | – | – | times |
| | | R8C/15 Group | 1,000 ⁽³⁾ | – | – | times |
| – | Byte Program Time | V _{CC} = 5.0 V at T _{opr} = 25 °C | – | 50 | 400 | μs |
| – | Block Erase Time | V _{CC} = 5.0 V at T _{opr} = 25 °C | – | 0.4 | 9 | s |
| t _d (SR-ES) | Time Delay from Suspend Request until Erase Suspend | | – | – | 8 | ms |
| – | Erase Suspend Request Interval | | 10 | – | – | ms |
| – | Program, Erase Voltage | | 2.7 | – | 5.5 | V |
| – | Read Voltage | | 2.7 | – | 5.5 | V |
| – | Program, Erase Temperature | | 0 | – | 60 | °C |
| – | Data Hold Time ⁽⁷⁾ | Ambient temperature = 55 °C | 20 | – | – | year |

NOTES:

- V_{CC} = AV_{CC} = 2.7 to 5.5V at T_{opr} = 0 to 60 °C, unless otherwise specified.
- Definition of program and erase
The program and erase endurance shows an erase endurance for every block.
If the program and erase endurance is “n” times (n = 100, 10000), “n” times erase can be performed for every block.
For example, if performing 1-byte write to the distinct addresses on Block A of 1Kbyte block 1,024 times and then erasing that block, program and erase endurance is counted as one time.
However, do not perform multiple programs to the same address for one time erase.(disable overwriting).
- Endurance to guarantee all electrical characteristics after program and erase.(1 to “Min.” value can be guaranteed).
- In the case of a system to execute multiple programs, perform one erase after programming as reducing effective reprogram endurance not to leave blank area as possible such as programming write addresses in turn . If programming a set of 16 bytes, programming up to 128 sets and then erasing them one time can reduce effective reprogram endurance. Additionally, averaging erase endurance for Block A and B can reduce effective reprogram endurance more. To leave erase endurance for every block as information and determine the restricted endurance are recommended.
- If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error does not occur.
- Customers desiring Program/Erase failure rate information should contact their Renesas technical support representative.
- The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics

| Symbol | Parameter | Conditions | Standard | | | Unit |
|------------------------|--|---|-----------------------|------|------|-------|
| | | | Min. | Typ. | Max. | |
| – | Program/Erase Endurance ⁽²⁾ | | 10,000 ⁽³⁾ | – | – | times |
| – | Byte Program Time (Program/Erase Endurance ≤ 1,000 Times) | V _{CC} = 5.0 V at T _{opr} = 25 °C | – | 50 | 400 | μs |
| – | Byte Program Time (Program/Erase Endurance > 1,000 Times) | V _{CC} = 5.0 V at T _{opr} = 25 °C | – | 65 | – | μs |
| – | Block Erase Time (Program/Erase Endurance ≤ 1,000 Times) | V _{CC} = 5.0 V at T _{opr} = 25 °C | – | 0.2 | 9 | s |
| – | Block Erase Time (Program/Erase Endurance > 1,000 Times) | V _{CC} = 5.0 V at T _{opr} = 25 °C | – | 0.3 | – | s |
| t _d (SR-ES) | Time Delay from Suspend Request until Erase Suspend | | – | – | 8 | ms |
| – | Erase Suspend Request Interval | | 10 | – | – | ms |
| – | Program, Erase Voltage | | 2.7 | – | 5.5 | V |
| – | Read Voltage | | 2.7 | – | 5.5 | V |
| – | Program, Erase Temperature | | -20 ⁽⁸⁾ | – | 85 | °C |
| – | Data Hold Time ⁽⁹⁾ | Ambient temperature = 55 °C | 20 | – | – | year |

NOTES:

- V_{CC} = AV_{CC} = 2.7 to 5.5V at T_{opr} = –20 to 85 °C / –40 to 85 °C, unless otherwise specified.
- Definition of program and erase
The program and erase endurance shows an erase endurance for every block.
If the program and erase endurance is “n” times (n = 100, 10000), “n” times erase can be performed for every block.
For example, if performing 1-byte write to the distinct addresses on Block A of 1Kbyte block 1,024 times and then erasing that block, program and erase endurance is counted as one time.
However, do not perform multiple programs to the same address for one time erase.(disable overwriting).
- Endurance to guarantee all electrical characteristics after program and erase.(1 to “Min.” value can be guaranteed).
- Standard of Block A and Block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times aer the same as that in program area.
- In the case of a system to execute multiple programs, perform one erase after programming as reducing effective reprogram endurance not to leave blank area as possible such as programming write addresses in turn . If programming a set of 16 bytes, programming up to 128 sets and then erasing them one time can reduce effective reprogram endurance. Additionally, averaging erase endurance for Block A and B can reduce effective reprogram endurance more. To leave erase endurance for every block as information and determine the restricted endurance are recommended.
- If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error does not occur.
- Customers desiring Program/Erase failure rate information should contact their Renesas technical support representative.
- 40 °C for D version.
- The data hold time includes time that the power supply is off or the clock is not supplied.

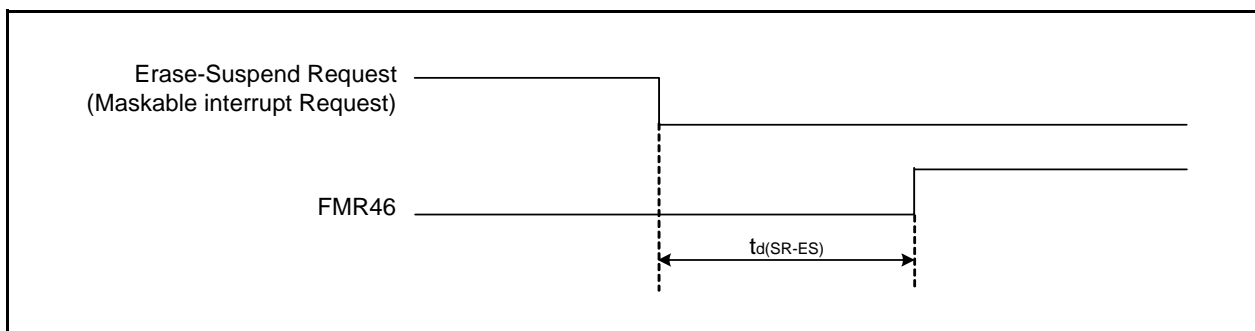


Figure 5.2 Time delay from Suspend Request until Erase Suspend

Table 5.6 Voltage Detection 1 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---------------------|--|-----------------------------------|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| V _{det1} | Voltage Detection Level ⁽³⁾ | | 2.70 | 2.85 | 3.00 | V |
| – | Voltage Detection Circuit Self Power Consumption | VCA26 = 1, V _{CC} = 5.0V | – | 600 | – | nA |
| t _{d(E-A)} | Waiting Time until Voltage Detection Circuit Operation Starts ⁽²⁾ | | – | – | 100 | μs |
| V _{ccmin} | Microcomputer Operating Voltage Minimum Value | | 2.7 | – | – | V |

NOTES:

1. The measurement condition is V_{CC} = AV_{CC} = 2.7V to 5.5V and T_{opr} = -40°C to 85 °C.
2. Necessary time until the voltage detection circuit operates when setting to “1” again after setting the VCA26 bit in the VCA2 register to “0”.
3. Hold V_{det2} > V_{det1}.

Table 5.7 Voltage Detection 2 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---------------------|--|-----------------------------------|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| V _{det2} | Voltage Detection Level ⁽⁴⁾ | | 3.00 | 3.30 | 3.60 | V |
| – | Voltage Monitor 2 Interrupt Request Generation Time ⁽²⁾ | | – | 40 | – | μs |
| – | Voltage Detection Circuit Self Power Consumption | VCA27 = 1, V _{CC} = 5.0V | – | 600 | – | nA |
| t _{d(E-A)} | Waiting Time until Voltage Detection Circuit Operation Starts ⁽³⁾ | | – | – | 100 | μs |

NOTES:

1. The measurement condition is V_{CC} = AV_{CC} = 2.7V to 5.5V and T_{opr} = -40°C to 85 °C.
2. Time until the voltage monitor 2 interrupt request is generated since the voltage passes V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to “1” again after setting the VCA27 bit in the VCA2 register to “0”.
4. Hold V_{det2} > V_{det1}.

Table 5.8 Reset Circuit Electrical Characteristics (When Using Voltage Monitor 1 Reset)

| Symbol | Parameter | Condition | Standard | | | Unit |
|----------------------------|---|---|----------|------|------------|------|
| | | | Min. | Typ. | Max. | |
| V_{por2} | Power-On Reset Valid Voltage | $-20^{\circ}\text{C} \leq T_{opr} < 85^{\circ}\text{C}$ | – | – | V_{det1} | V |
| $t_{w(V_{por2}-V_{det1})}$ | Supply Voltage Rising Time When Power-On Reset is Deasserted ⁽¹⁾ | $-20^{\circ}\text{C} \leq T_{opr} < 85^{\circ}\text{C}$, $t_{w(por2)} \geq 0\text{s}^{(3)}$ | – | – | 100 | ms |

NOTES:

1. This condition is not applicable when using with $V_{cc} \geq 1.0\text{V}$.
2. When turning power on after the time to hold the external power below effective voltage (V_{por1}) exceeds 10s, refer to **Table 5.9 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset)**.
3. $t_{w(por2)}$ is time to hold the external power below effective voltage (V_{por2}).

Table 5.9 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset)

| Symbol | Parameter | Condition | Standard | | | Unit |
|----------------------------|--|---|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| V_{por1} | Power-On Reset Valid Voltage | $-20^{\circ}\text{C} \leq T_{opr} < 85^{\circ}\text{C}$ | – | – | 0.1 | V |
| $t_{w(V_{por1}-V_{det1})}$ | Supply Voltage Rising Time When Power-On Reset is Deasserted | $0^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$, $t_{w(por1)} \geq 10\text{s}^{(2)}$ | – | – | 100 | ms |
| $t_{w(V_{por1}-V_{det1})}$ | Supply Voltage Rising Time When Power-On Reset is Deasserted | $-20^{\circ}\text{C} \leq T_{opr} < 0^{\circ}\text{C}$, $t_{w(por1)} \geq 30\text{s}^{(2)}$ | – | – | 100 | ms |
| $t_{w(V_{por1}-V_{det1})}$ | Supply Voltage Rising Time When Power-On Reset is Deasserted | $-20^{\circ}\text{C} \leq T_{opr} < 0^{\circ}\text{C}$, $t_{w(por1)} \geq 10\text{s}^{(2)}$ | – | – | 1 | ms |
| $t_{w(V_{por1}-V_{det1})}$ | Supply Voltage Rising Time When Power-On Reset is Deasserted | $0^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$, $t_{w(por1)} \geq 1\text{s}^{(2)}$ | – | – | 0.5 | ms |

NOTES:

1. When not using the voltage monitor 1 reset, use with $V_{cc} \geq 2.7\text{V}$.
2. $t_{w(por1)}$ is time to hold the external power below effective voltage (V_{por1}).

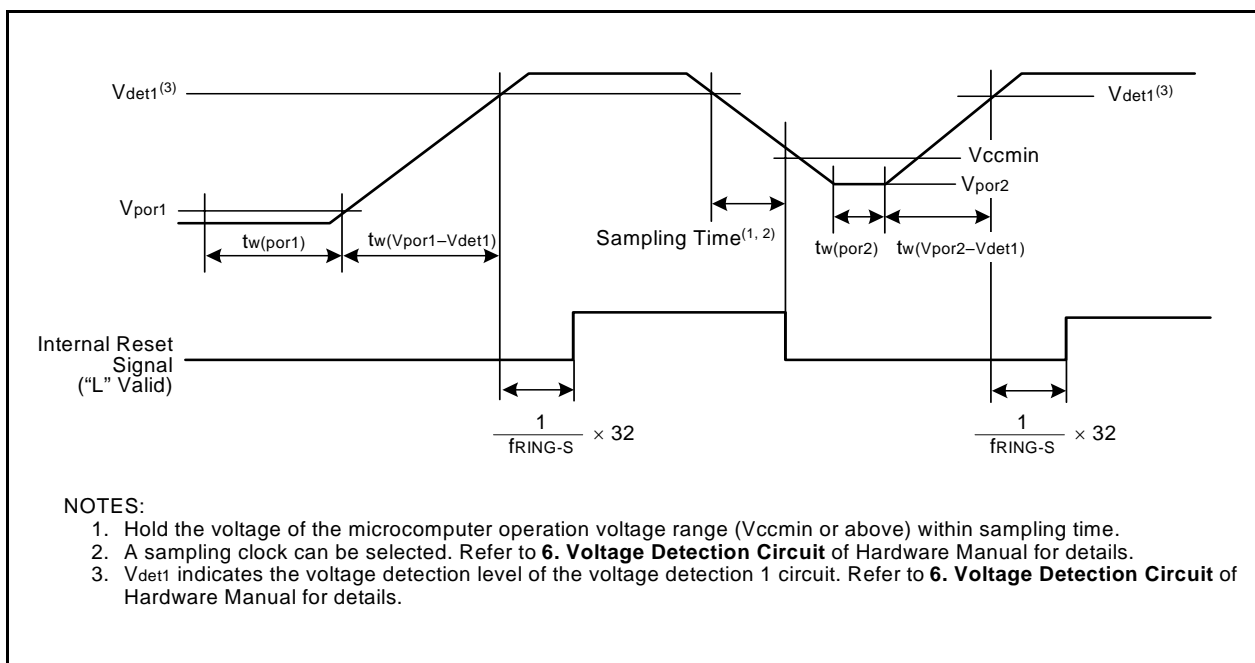
**Figure 5.3 Reset Circuit Electrical Characteristics**

Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|--------|---|--|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| – | High-Speed On-Chip Oscillator Frequency When the Reset is Deasserted | $V_{CC} = 5.0V, T_{opr} = 25\text{ }^{\circ}C$ | – | 8 | – | MHz |
| – | High-Speed On-Chip Oscillator Frequency Temperature • Supply Voltage Dependence | 0 to +60 °C / 5 V ± 5 % ⁽²⁾ | 7.44 | – | 8.56 | MHz |
| | | –20 to +85 °C / 2.7 to 5.5 V ⁽²⁾ | 7.04 | – | 8.96 | MHz |
| | | –40 to +85 °C / 2.7 to 5.5 V ⁽²⁾ | 6.80 | – | 9.20 | MHz |

NOTES:

- The measurement condition is $V_{CC} = AV_{CC} = 5.0V$ and $T_{opr} = 25\text{ }^{\circ}C$.
- The standard value shows when the HRA1 register is assumed as the value in shipping and the HRA2 register value is set to 00h.

Table 5.11 Power Supply Circuit Timing Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|--------------|---|-----------|----------|------|------|---------|
| | | | Min. | Typ. | Max. | |
| $t_{d(P-R)}$ | Time for Internal Power Supply Stabilization during Power-On ⁽²⁾ | | 1 | – | 2000 | μs |
| $t_{d(R-S)}$ | STOP Exit Time ⁽³⁾ | | – | – | 150 | μs |

NOTES:

- The measurement condition is $V_{CC} = AV_{CC} = 2.7$ to $5.5V$ and $T_{opr} = 25\text{ }^{\circ}C$.
- Waiting time until the internal power supply generation circuit stabilizes during power-on.
- Time until CPU clock supply starts since the interrupt is acknowledged to exit stop mode.

Table 5.12 Timing Requirements of Clock Synchronous Serial I/O (SSU) with Chip Select⁽¹⁾

| Symbol | Parameter | | Conditions | Standard | | | Unit |
|-------------|---------------------------------|--------|------------|---------------|------|------------------|-----------------|
| | | | | Min. | Typ. | Max. | |
| t_{SUCYC} | SSCK Clock Cycle Time | | | 4 | – | – | $t_{CYC}^{(2)}$ |
| t_{HI} | SSCK Clock "H" Width | | | 0.4 | – | 0.6 | t_{SUCYC} |
| t_{LO} | SSCK Clock "L" Width | | | 0.4 | – | 0.6 | t_{SUCYC} |
| t_{RISE} | SSCK Clock Rising Time | Master | | – | – | 1 | $t_{CYC}^{(2)}$ |
| | | Slave | | – | – | 1 | μs |
| t_{FALL} | SSCK Clock Falling Time | Master | | – | – | 1 | $t_{CYC}^{(2)}$ |
| | | Slave | | – | – | 1 | μs |
| t_{SU} | SSO, SSI Data Input Setup Time | | | 100 | – | – | ns |
| t_{H} | SSO, SSI Data Input Hold Time | | | 1 | – | – | $t_{CYC}^{(2)}$ |
| t_{LEAD} | \overline{SCS} Setup Time | Slave | | $1t_{CYC}+50$ | – | – | ns |
| t_{LAG} | \overline{SCS} Hold Time | Slave | | $1t_{CYC}+50$ | – | – | ns |
| t_{OD} | SSO, SSI Data Output Delay Time | | | – | – | 1 | $t_{CYC}^{(2)}$ |
| t_{SA} | SSI Slave Access Time | | | – | – | $1.5t_{CYC}+100$ | ns |
| t_{OR} | SSI Slave Out Open Time | | | – | – | $1.5t_{CYC}+100$ | ns |

NOTES:

- $V_{CC} = AV_{CC} = 2.7$ to $5.5V$, $V_{SS} = 0V$ at $T_{opr} = -20$ to $85\text{ }^{\circ}C$ / -40 to $85\text{ }^{\circ}C$, unless otherwise specified.
- $1t_{CYC} = 1/f_1(s)$

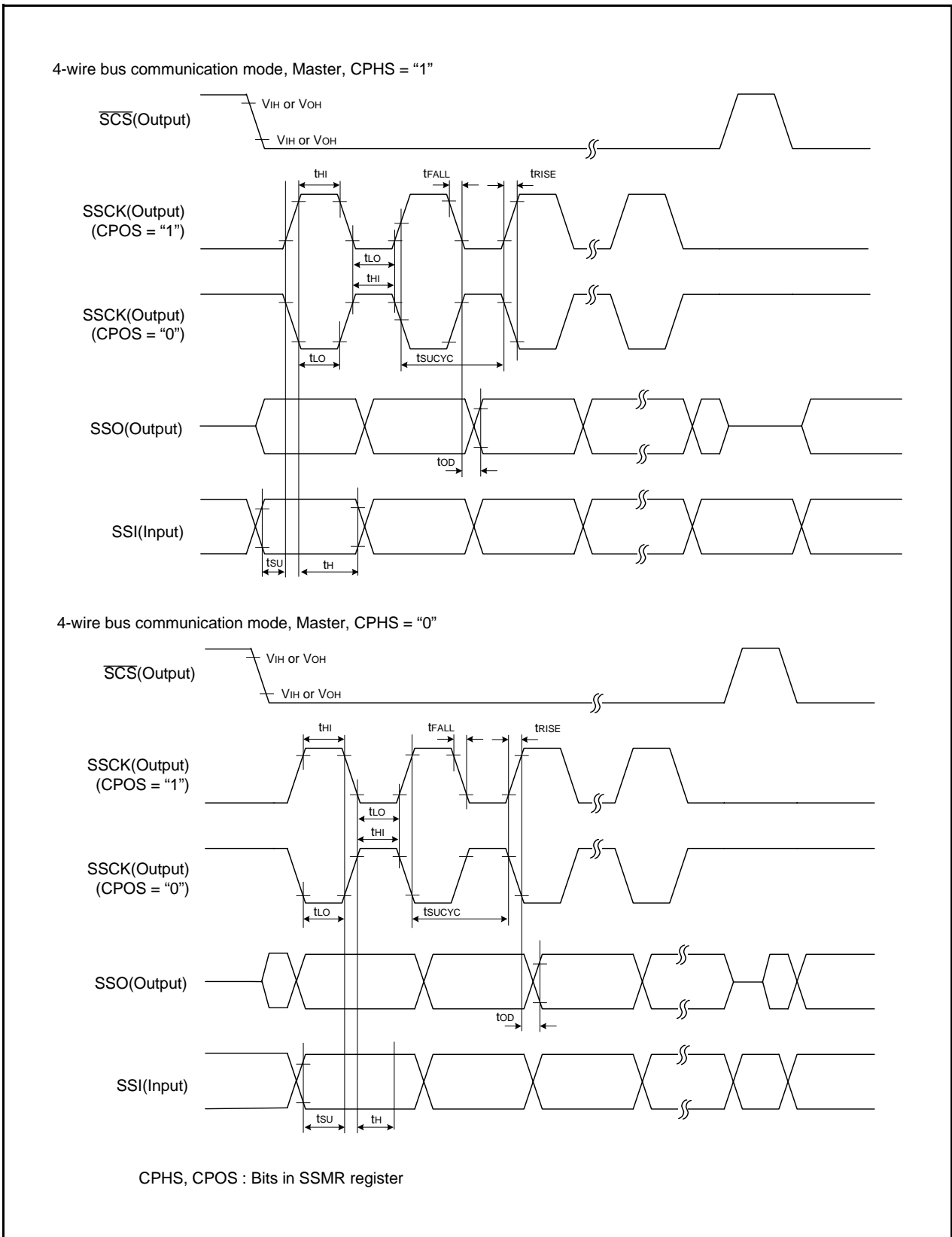


Figure 5.4 I/O Timing of Clock Synchronous Serial I/O (SSU) with Chip Select (Master)

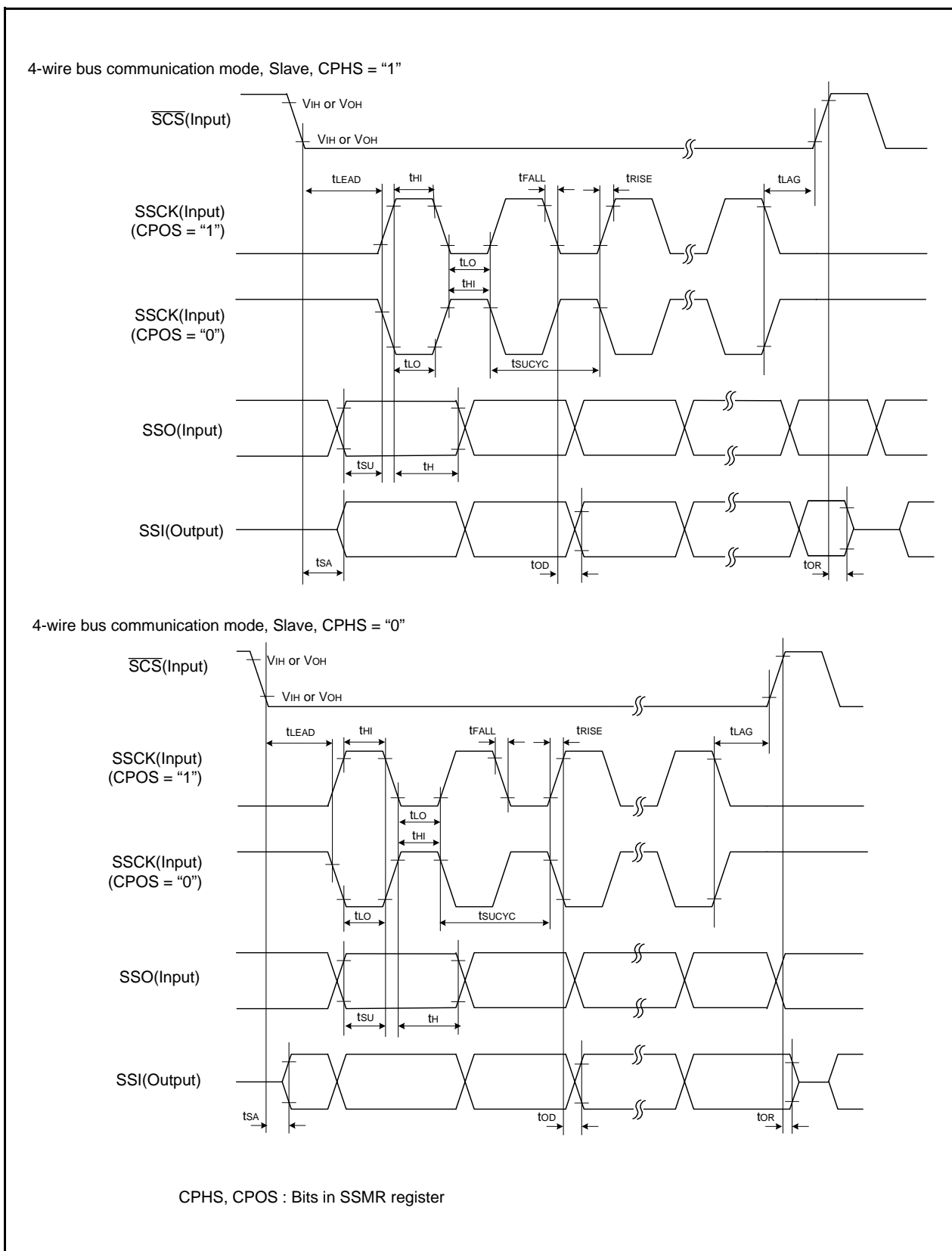


Figure 5.5 I/O Timing of Clock Synchronous Serial I/O (SSU) with Chip Select (Slave)

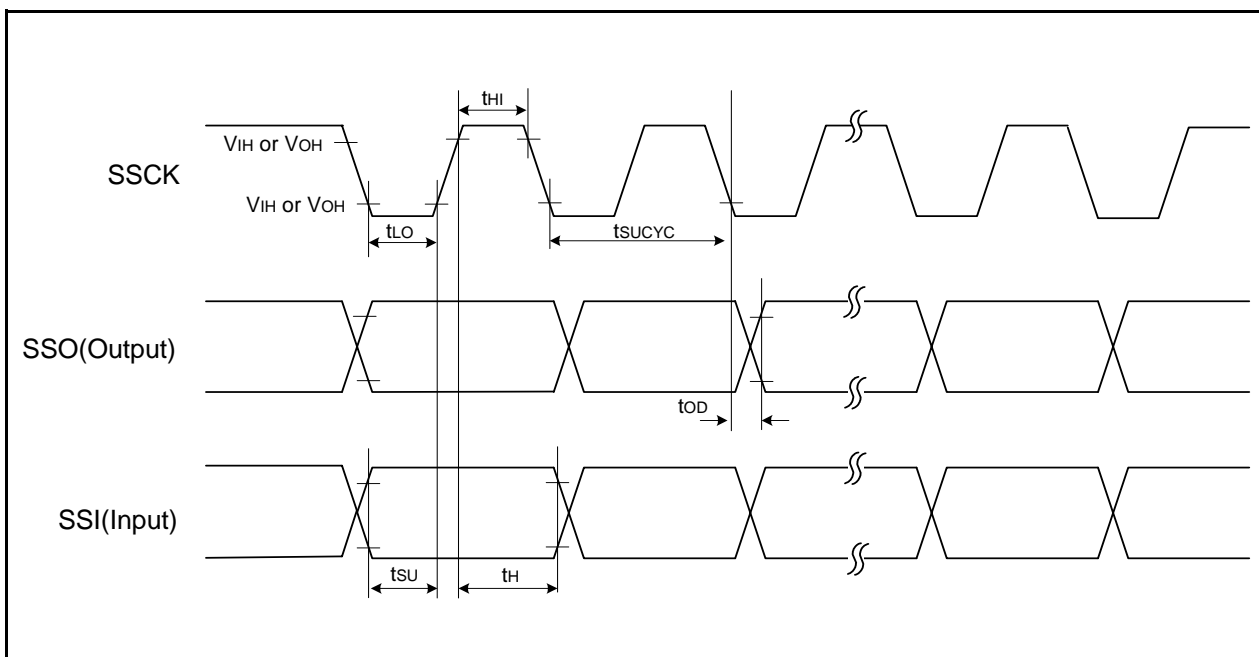


Figure 5.6 I/O Timing of Clock Synchronous Serial I/O (SSU) with Chip Select (Clock Synchronous Communication Mode)

Table 5.13 Electrical Characteristics (1) [Vcc = 5V]

| Symbol | Parameter | | Condition | | Standard | | | Unit |
|------------------|--|---------------------------|---------------------|---|-----------|------|------|------|
| | | | | | Min. | Typ. | Max. | |
| VOH | Output "H" Voltage | Except XOUT | IOH = -5mA | | Vcc - 2.0 | - | Vcc | V |
| | | | IOH = -200μA | | Vcc - 0.3 | - | Vcc | V |
| | | XOUT | Drive capacity HIGH | IOH = -1mA | Vcc - 2.0 | - | Vcc | V |
| | | | Drive capacity LOW | IOH = -500μA | Vcc - 2.0 | - | Vcc | V |
| VOL | Output "L" Voltage | Except P1_0 to P1_3, XOUT | IOL = 5mA | | - | - | 2.0 | V |
| | | | IOL = 200μA | | - | - | 0.45 | V |
| | | P1_0 to P1_3 | Drive capacity HIGH | IOL = 15mA | - | - | 2.0 | V |
| | | | Drive capacity LOW | IOL = 5mA | - | - | 2.0 | V |
| | | | Drive capacity LOW | IOL = 200μA | - | - | 0.45 | V |
| | | XOUT | Drive capacity HIGH | IOL = 1mA | - | - | 2.0 | V |
| | | | Drive capacity LOW | IOL = 500μA | - | - | 2.0 | V |
| | | VT+-VT- | Hysteresis | INT0, INT1, INT3, KI0, KI1, KI2, KI3, CNTR0, CNTR1, TCIN, RXD0, SSO | | | 0.2 | - |
| RESET | | | | 0.2 | - | 2.2 | V | |
| IiH | Input "H" current | | VI = 5V | | - | - | 5.0 | μA |
| IiL | Input "L" current | | VI = 0V | | - | - | -5.0 | μA |
| RPULLUP | Pull-Up Resistance | | VI = 0V | | 30 | 50 | 167 | kΩ |
| RfXIN | Feedback Resistance | XIN | | | - | 1.0 | - | MΩ |
| fRING-S | Low-Speed On-Chip Oscillator Frequency | | | | 40 | 125 | 250 | kHz |
| V _{RAM} | RAM Hold Voltage | | During stop mode | | 2.0 | - | - | V |

NOTES:

1. Vcc = AVcc = 4.2 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C, f(XIN)=20MHz, unless otherwise specified.

Table 5.14 Electrical Characteristics (2) [Vcc = 5V] (Topr = -40 to 85 °C, unless otherwise specified.)

| Symbol | Parameter | Condition | Standard | | | Unit | |
|--------|--|------------------------------------|--|------|------|------|----|
| | | | Min. | Typ. | Max. | | |
| Icc | Power Supply Current (Vcc=3.3 to 5.5V) In single-chip mode, the output pins are open and other pins are Vss | High-Speed Mode | XIN = 20MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz No division | – | 9 | 15 | mA |
| | | | XIN = 16MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz No division | – | 8 | 14 | mA |
| | | | XIN = 10MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz No division | – | 5 | – | mA |
| | | Medium-Speed Mode | XIN = 20MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8 | – | 4 | – | mA |
| | | | XIN = 16MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8 | – | 3 | – | mA |
| | | | XIN = 10MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8 | – | 2 | – | mA |
| | | High-Speed On-Chip Oscillator Mode | Main clock off High-speed on-chip oscillator on=8MHz Low-speed on-chip oscillator on=125kHz No division | – | 4 | 8 | mA |
| | | | Main clock off High-speed on-chip oscillator on=8MHz Low-speed on-chip oscillator on=125kHz Divide-by-8 | – | 1.5 | – | mA |
| | | Low-Speed On-Chip Oscillator Mode | Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8 | – | 470 | 900 | μA |
| | | Wait Mode | Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz While a WAIT instruction is executed Peripheral clock operation VCA26 = VCA27 = 0 | – | 40 | 80 | μA |
| | | Wait Mode | Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz While a WAIT instruction is executed Peripheral clock off VCA26 = VCA27 = 0 | – | 38 | 76 | μA |
| | | Stop Mode | Main clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0 | – | 0.8 | 3.0 | μA |

Timing Requirements (Unless otherwise specified: $V_{CC} = 5V$, $V_{SS} = 0V$ at $T_{op} = 25\text{ }^{\circ}\text{C}$) [$V_{CC} = 5V$]**Table 5.15 XIN Input**

| Symbol | Parameter | Standard | | Unit |
|---------------|----------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(XIN)}$ | XIN Input Cycle Time | 50 | – | ns |
| $t_{WH(XIN)}$ | XIN Input “H” Width | 25 | – | ns |
| $t_{WL(XIN)}$ | XIN Input “L” Width | 25 | – | ns |

Table 5.16 CNTR0 Input, CNTR1 Input, $\overline{INT1}$ Input

| Symbol | Parameter | Standard | | Unit |
|-----------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(CNTR0)}$ | CNTR0 Input Cycle Time | 100 | – | ns |
| $t_{WH(CNTR0)}$ | CNTR0 Input “H” Width | 40 | – | ns |
| $t_{WL(CNTR0)}$ | CNTR0 input “L” Width | 40 | – | ns |

Table 5.17 TCIN Input, $\overline{INT3}$ Input

| Symbol | Parameter | Standard | | Unit |
|----------------|-----------------------|--------------------|------|------|
| | | Min. | Max. | |
| $t_{c(TCIN)}$ | TCIN Input Cycle Time | 400 ⁽¹⁾ | – | ns |
| $t_{WH(TCIN)}$ | TCIN Input “H” Width | 200 ⁽²⁾ | – | ns |
| $t_{WL(TCIN)}$ | TCIN input “L” Width | 200 ⁽²⁾ | – | ns |

NOTES:

1. When using Timer C input capture mode, adjust the cycle time ($1/\text{Timer C count source frequency} \times 3$) or above.
2. When using Timer C input capture mode, adjust the width ($1/\text{Timer C count source frequency} \times 1.5$) or above.

Table 5.18 Serial Interface

| Symbol | Parameter | Standard | | Unit |
|---------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(CLK)}$ | CLKi Input Cycle Time | 200 | – | ns |
| $t_{W(CLKH)}$ | CLKi Input “H” Width | 100 | – | ns |
| $t_{W(CLKL)}$ | CLKi Input “L” Width | 100 | – | ns |
| $t_{d(C-Q)}$ | TXDi Output Delay Time | – | 50 | ns |
| $t_{h(C-Q)}$ | TXDi Hold Time | 0 | – | ns |
| $t_{su(D-C)}$ | RXDi Input Setup Time | 50 | – | ns |
| $t_{h(C-D)}$ | RCDi Input Hold Time | 90 | – | ns |

Table 5.19 External Interrupt $\overline{INT0}$ Input

| Symbol | Parameter | Standard | | Unit |
|--------------|-----------------------------------|--------------------|------|------|
| | | Min. | Max. | |
| $t_{W(INH)}$ | $\overline{INT0}$ Input “H” Width | 250 ⁽¹⁾ | – | ns |
| $t_{W(INL)}$ | $\overline{INT0}$ Input “L” Width | 250 ⁽²⁾ | – | ns |

NOTES:

1. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input HIGH width to the greater value, either ($1/\text{digital filter clock frequency} \times 3$) or the minimum value of standard.
2. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input LOW width to the greater value, either ($1/\text{digital filter clock frequency} \times 3$) or the minimum value of standard.

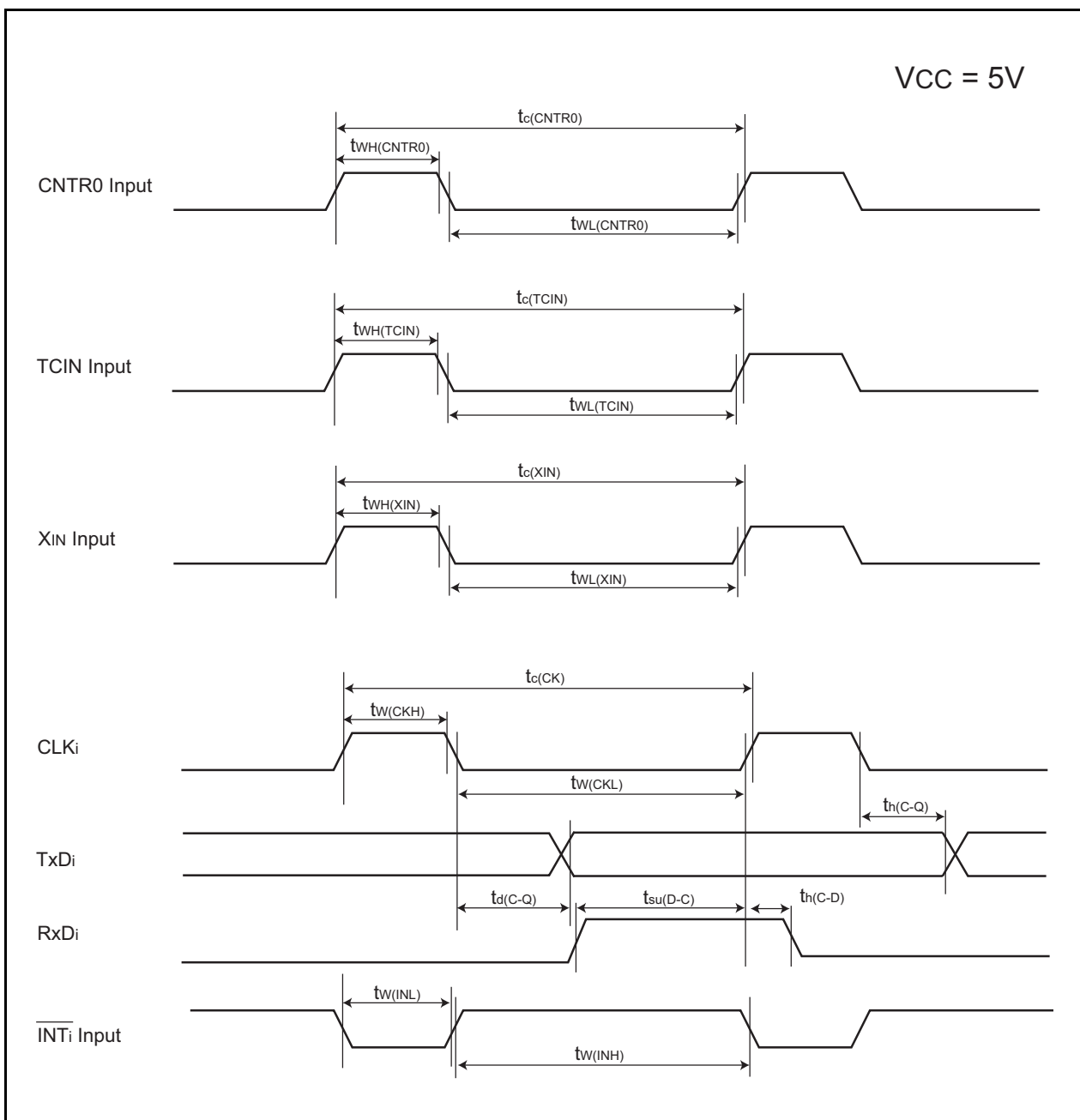


Figure 5.7 Timing Diagram When $V_{CC} = 5V$

Table 5.20 Electrical Characteristics (3) [V_{CC} = 3V]

| Symbol | Parameter | | Condition | | Standard | | | Unit |
|----------------------------------|--|---|------------------------|--------------------------|-----------------------|------|-----------------|------|
| | | | | | Min. | Typ. | Max. | |
| V _{OH} | Output "H" Voltage | Except X _{OUT} | I _{OH} = -1mA | | V _{CC} - 0.5 | - | V _{CC} | V |
| | | X _{OUT} | Drive capacity HIGH | I _{OH} = -0.1mA | V _{CC} - 0.5 | - | V _{CC} | V |
| | | | Drive capacity LOW | I _{OH} = -50μA | V _{CC} - 0.5 | - | V _{CC} | V |
| V _{OL} | Output "L" Voltage | Except P1_0 to P1_3, X _{OUT} | I _{OL} = 1mA | | - | - | 0.5 | V |
| | | P1_0 to P1_3 | Drive capacity HIGH | I _{OL} = 2mA | - | - | 0.5 | V |
| | | | Drive capacity LOW | I _{OL} = 1mA | - | - | 0.5 | V |
| | | X _{OUT} | Drive capacity HIGH | I _{OL} = 0.1mA | - | - | 0.5 | V |
| | | | Drive capacity LOW | I _{OL} = 50μA | - | - | 0.5 | V |
| V _{T+} -V _{T-} | Hysteresis | <u>INT0</u> , <u>INT1</u> , <u>INT3</u> , <u>KI0</u> , <u>KI1</u> , <u>KI2</u> , <u>KI3</u> , <u>CNTR0</u> , <u>CNTR1</u> , <u>TCIN</u> , <u>RXD0</u> , <u>SSO</u> | | | 0.2 | - | 0.8 | V |
| | | <u>RESET</u> | | | 0.2 | - | 1.8 | V |
| I _{IH} | Input "H" Current | | V _I = 3V | | - | - | 4.0 | μA |
| I _{IL} | Input "L" Current | | V _I = 0V | | - | - | -4.0 | μA |
| R _{PULLUP} | Pull-Up Resistance | | V _I = 0V | | 66 | 160 | 500 | kΩ |
| R _{iXIN} | Feedback Resistance | X _{IN} | | | - | 3.0 | - | MΩ |
| f _{FRING-S} | Low-Speed On-Chip Oscillator Frequency | | | | 40 | 125 | 250 | kHz |
| V _{RAM} | RAM Hold Voltage | | During stop mode | | 2.0 | - | - | V |

NOTES:

- V_{CC} = AV_{CC} = 2.7 to 3.3V at T_{opr} = -20 to 85 °C / -40 to 85 °C, f(X_{IN})=10MHz, unless otherwise specified.

Table 5.21 Electrical Characteristics (4) [Vcc = 3V] (Topr = -40 to 85 °C, unless otherwise specified.)

| Symbol | Parameter | Condition | Standard | | | Unit | |
|--------|--|------------------------------------|--|------|------|------|----|
| | | | Min. | Typ. | Max. | | |
| Icc | Power Supply Current (Vcc=2.7 to 3.3V) In single-chip mode, the output pins are open and other pins are Vss | High-Speed Mode | XIN = 20MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz No division | – | 8 | 13 | mA |
| | | | XIN = 16MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz No division | – | 7 | 12 | mA |
| | | | XIN = 10MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz No division | – | 5 | – | mA |
| | | Medium-Speed Mode | XIN = 20MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8 | – | 3 | – | mA |
| | | | XIN = 16MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8 | – | 2.5 | – | mA |
| | | | XIN = 10MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8 | – | 1.6 | – | mA |
| | | High-Speed On-Chip Oscillator Mode | Main clock off High-speed on-chip oscillator on=8MHz Low-speed on-chip oscillator on=125kHz No division | – | 3.5 | 7.5 | mA |
| | | | Main clock off High-speed on-chip oscillator on=8MHz Low-speed on-chip oscillator on=125kHz Divide-by-8 | – | 1.5 | – | mA |
| | | Low-Speed On-Chip Oscillator Mode | Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8 | – | 420 | 800 | μA |
| | | Wait Mode | Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz While a WAIT instruction is executed Peripheral clock operation VCA26 = VCA27 = 0 | – | 37 | 74 | μA |
| | | Wait Mode | Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz While a WAIT instruction is executed Peripheral clock off VCA26 = VCA27 = 0 | – | 35 | 70 | μA |
| | | Stop Mode | Main clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0 | – | 0.7 | 3.0 | μA |

Timing requirements (Unless otherwise specified: Vcc = 3V, Vss = 0V at Topr = 25 °C) [Vcc = 3V]**Table 5.22 XIN Input**

| Symbol | Parameter | Standard | | Unit |
|-----------------------|----------------------|----------|------|------|
| | | Min. | Max. | |
| t _c (XIN) | XIN Input Cycle Time | 100 | – | ns |
| t _{WH} (XIN) | XIN Input “H” Width | 40 | – | ns |
| t _{WL} (XIN) | XIN Input “L” Width | 40 | – | ns |

Table 5.23 CNTR0 Input, CNTR1 Input, $\overline{\text{INT1}}$ Input

| Symbol | Parameter | Standard | | Unit |
|-------------------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| t _c (CNTR0) | CNTR0 Input Cycle Time | 300 | – | ns |
| t _{WH} (CNTR0) | CNTR0 Input “H” Width | 120 | – | ns |
| t _{WL} (CNTR0) | CNTR0 Input “L” Width | 120 | – | ns |

Table 5.24 TCIN Input, $\overline{\text{INT3}}$ Input

| Symbol | Parameter | Standard | | Unit |
|------------------------|-----------------------|----------------------|------|------|
| | | Min. | Max. | |
| t _c (TCIN) | TCIN Input Cycle Time | 1,200 ⁽¹⁾ | – | ns |
| t _{WH} (TCIN) | TCIN Input “H” Width | 600 ⁽²⁾ | – | ns |
| t _{WL} (TCIN) | TCIN Input “L” Width | 600 ⁽²⁾ | – | ns |

NOTES:

1. When using the Timer C input capture mode, adjust the cycle time (1/Timer C count source frequency x 3) or above.
2. When using the Timer C input capture mode, adjust the width (1/Timer C count source frequency x 1.5) or above.

Table 5.25 Serial Interface

| Symbol | Parameter | Standard | | Unit |
|-----------------------|-----------------------------------|----------|------|------|
| | | Min. | Max. | |
| t _c (CK) | CLKi Input Cycle Time | 300 | – | ns |
| t _W (CKH) | CLKi Input “H” Width | 150 | – | ns |
| t _W (CKL) | CLKi Input “L” Width | 150 | – | ns |
| t _d (C-Q) | TXDi Output Delay Time | – | 80 | ns |
| t _h (C-Q) | TXDi Hold Time | 0 | – | ns |
| t _{su} (D-C) | RXD _i Input Setup Time | 70 | – | ns |
| t _h (C-D) | RCD _i Input Hold Time | 90 | – | ns |

Table 5.26 External Interrupt $\overline{\text{INT0}}$ Input

| Symbol | Parameter | Standard | | Unit |
|----------------------|--|--------------------|------|------|
| | | Min. | Max. | |
| t _W (INH) | $\overline{\text{INT0}}$ Input “H” Width | 380 ⁽¹⁾ | – | ns |
| t _W (INL) | $\overline{\text{INT0}}$ Input “L” Width | 380 ⁽²⁾ | – | ns |

NOTES:

1. When selecting the digital filter by the $\overline{\text{INT0}}$ input filter select bit, use the $\overline{\text{INT0}}$ input HIGH width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the $\overline{\text{INT0}}$ input filter select bit, use the $\overline{\text{INT0}}$ input LOW width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.

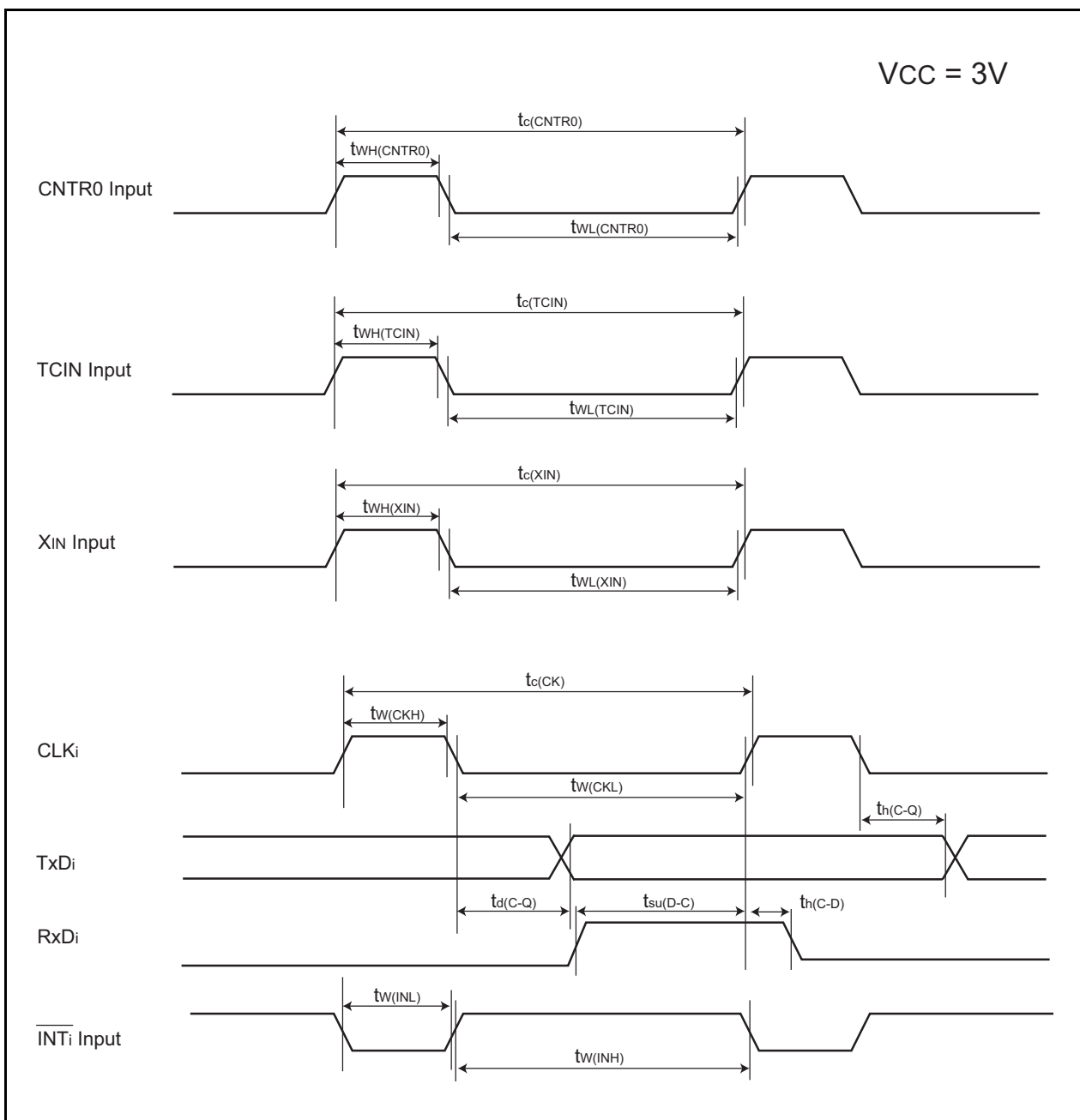
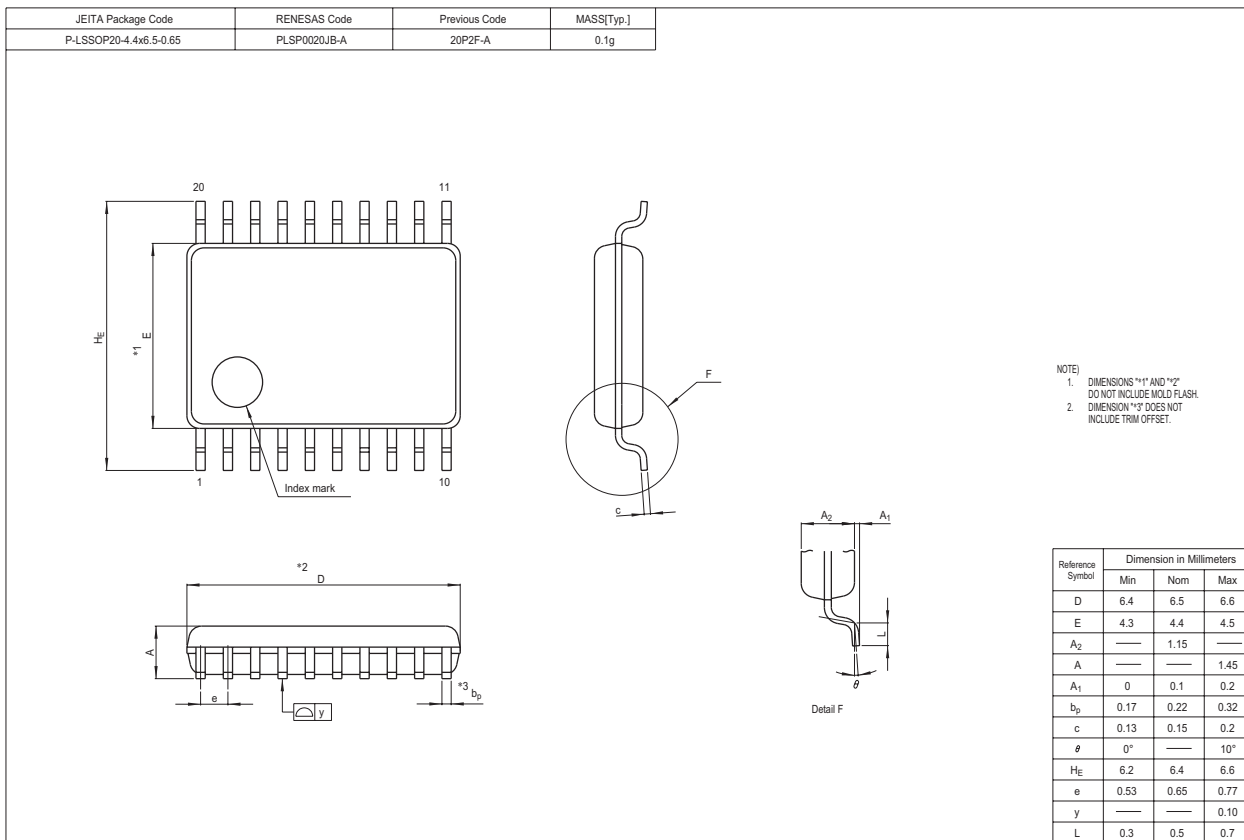


Figure 5.8 Timing Diagram When $V_{CC} = 3V$

Package Dimensions



REVISION HISTORY

R8C/14 Group, R8C/15 Group Datasheet

| Rev. | Date | Description | |
|------|--------------|---|--|
| | | Page | Summary |
| 0.10 | Sep 06, 2004 | – | First Edition issued |
| 1.00 | Feb 25, 2005 | 2-3 5 6 7-8 16 18 21 22 24 25 26-28 29 30 31, 35 33 34 37 | Tables 1.1 and 1.2 revised Table 1.3 and figure 1.2 revised Table 1.4 and figure 1.3 revised Figures 1.4 and 1.5 revised Table 4.1 revised: - 000Fh: 000XXXXXb → 00011111b - 0036h: 00001000b → 0000X000b and 01001001b → 0100X001b Tabel 4.3 revised: - 009Ch: FFh → 00h; NOTES2 added - 009Dh: FFh → 00h - 00BCh: 10000000b → 00h Table 5.3 revised Tables 5.4 and 5.5 revised Tables 5.8 and 5.9 revised Table 5.11 revised; Table 5.12 added Figures 5.4 to 5.6 added Table 5.13 revised Table 5.14 revised Table 5.16 and 5.23 revised: Table title “INT2” → “INT1” Table 5.20 revised; NOTE revised Table 5.21 revised Package Dimensions revised |
| 1.10 | Jul 07, 2005 | 5, 6 16 22 26 27 29 33 | Tables 1.3 and 1.4 revised Table 4.1 revised: - 0009h: XXXXXX00b → 00h - 000Ah: 00XXX000b → 00h - 001Eh: XXXXX000b → 00h Table 5.5 revised; NOTE revised Figure 5.4 revised Figure 5.5 revised Table 5.13 revised Table 5.20 revised |
| 2.00 | Jan 30, 2006 | 1 2 3 4 5, 6 | 1. Overview; “20-pin plastic molded LSSOP or SDIP” → “20-pin plastic molded LSSOP” revised Table 1.1 Performance Outline of the R8C/14 Group; Package: “20-pin plastic molded SDIP” deleted Table 1.2 Performance Outline of the R8C/15 Group; Package: “20-pin plastic molded SDIP” deleted, Flash Memory: (Data area) → (Data flash) (Program area) → (Program ROM) revised Figure 1.1 Block Diagram; “Peripheral Function” added, “System Clock Generation” → “System Clock Generator” revised Table 1.3 Product Information of R8C/14 Group, Table 1.4 Product Information of R8C/15 Group; revised. Figure 1.2 Part Number, Memory Size and Package of R8C/14 Group, Figure 1.3 Part Number, Memory Size and Package of R8C/15 Group; Package type: “DD : PRDP0020BA-A” deleted |

REVISION HISTORY

R8C/14 Group, R8C/15 Group Datasheet

| Rev. | Date | Description | |
|------|--------------|-------------|--|
| | | Page | Summary |
| 2.00 | Jan 30, 2006 | 8 | Figure 1.5 PRDP0020BA-A Package Pin Assignment (top view) deleted Table 1.5 Pin Description; Timer C: "CMP0_0 to CMP0_3, CMP1_0 to CMP1_3" → "CMP0_0 to CMP0_2, CMP1_0 to CMP1_2" revised |
| | | 10 | Figure 2.1 CPU Register; "Reserved Area" → "Reserved Bit" revised |
| | | 12 | 2.8.10 Reserved Area; "Reserved Area" → "Reserved Bit" revised |
| | | 13 | Figure 3.1 Memory Map of R8C/14 Group revised |
| | | 14 | 3.2 R8C/15 Group; "(data area)" → "(data flash)", "(program area)" → "(program ROM)" revised Figure 3.2 Memory Map of R8C/15 Group revised |
| | | 15 | Table 4.1 SFR Information(1); 0009h: "XXXXXX00b" → "00h" 000Ah: "00XXX000b" → "00h" 001Eh: "XXXXX000b" → "00h" |
| | | 17 | Table 4.3 SFR Information(3); 0085h: "Prescaler Z" → "Prescaler Z Register" 0086h: "Timer Z Secondary" → "Timer Z Secondary Register" 0087h: "Timer Z Primary" → "Timer Z Primary Register" 008Ch: "Prescaler X" → "Prescaler X Register" 008Dh: "Timer X" → "Timer X Register" 0090h, 0091h: "Timer C" → "Timer C Register" revised |
| | | 21 | Table 5.4 Flash Memory (Program ROM) Electrical Characteristics; •NOTES 1 to 7 added •"Topr" → "Ambient temperature", "Program area" → "Program ROM" revised |
| | | 22 | Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics; •NOTE1 revised, NOTE9 added •"Topr" → "Ambient temperature", "Data area" → "Data flash" revised |
| | | 23 | Figure 5.2 Time delay from Suspend Request until Erase Suspend revised |
| | | 24 | Table 5.8 Reset Circuit Electrical Characteristics (When Using Voltage Monitor 1 Reset); NOTE2 revised Table 5.9 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset); NOTE1 revised |
| | | 25 | Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics; revised Table 5.12 Timing Requirements of Clock Synchronous Serial I/O (SSU) with Chip Select; revised |
| | | 30 | Table 5.14 Electrical Characteristics (2) [Vcc = 5V]; revised |
| | | 31 | "Timing Requirements (Unless ... at Ta = 25°C) [VCC = 5V]" → "Timing Requirements (Unless ... at Topr = 25°C) [VCC = 5V]" revised |
| | | 34 | Table 5.18 Serial Interface; "35" → "50", "80" → "50" |
| | | 34 | Table 5.21 Electrical Characteristics (4) [Vcc = 3V]; revised |
| | | 35 | "Timing requirements (Unless ... at Ta = 25°C) [VCC = 3V]" → "Timing requirements (Unless ... at Topr = 25°C) [VCC = 3V]" revised |
| | | 35 | Table 5.25 Serial Interface; "55" → "70", "160" → "80" |
| | | 37 | Package Dimensions; Package "PRDP0020BA-A" deleted |

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