

FEATURES

Ultralow power consumption with $I_{CC} = 92 \text{ nA}$ (typical)

Continuous monitoring with no blank time

Pretrimmed voltage monitoring threshold options

10 options from 2 V to 4.63 V for the [ADM8611](#)

20 options from 0.5 V to 1.9 V for the [ADM8612/ADM8615](#)

5 options from 2.32 V to 4.63 V for the [ADM8613/ADM8614](#)

$\pm 1.3\%$ threshold accuracy over full temperature range

Manual reset input ([ADM8611/ADM8612/ADM8613/ADM8615](#))

200 ms (typical) reset timeout

Low voltage input monitoring down to 0.5 V ([ADM8612/ADM8615](#))

Watchdog timer ([ADM8613/ADM8614/ADM8615](#))

Watchdog function disable input ([ADM8613/ADM8614](#) only)

Watchdog timeout extension input ([ADM8614](#) only)

Active low, open-drain RESET output

Power supply glitch immunity

Available in 1.46 mm $\times$ 0.96 mm WLCSP

Operational temperature range: -40°C to $+85^\circ\text{C}$

APPLICATIONS

Portable/battery-operated equipment

Microprocessor systems

Energy metering

Energy harvesting

GENERAL DESCRIPTION

The [ADM8611/ADM8612/ADM8613/ADM8614/ADM8615](#) are voltage supervisory circuits that monitor power supply voltage levels and code execution integrity in microprocessor-based systems. Apart from providing power-on reset signals, an on-chip watchdog timer can reset the microprocessor if it fails to strobe within a preset timeout period. A reset signal can also be asserted by an external push-button through a manual reset input.

The ultralow power consumption of these devices makes them suitable for power efficiency sensitive systems, such as battery-powered portable devices and energy meters.

The features of each member of the device family are shown in Table 9. Each device subdivides into submodels with differences in factory preset voltage monitoring threshold options. In the range of 2 V to 4.63 V, 10 options are available for the [ADM8611](#). In the range of 2.32 V to 4.63 V, five options are available for

FUNCTIONAL BLOCK DIAGRAMS

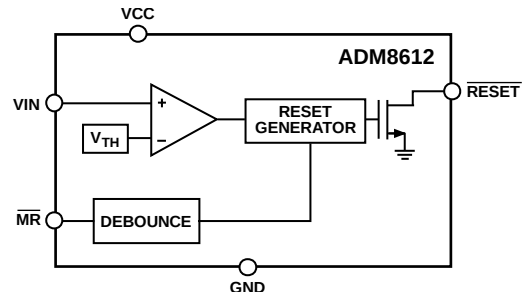


Figure 1. [ADM8612](#) Functional Block Diagram

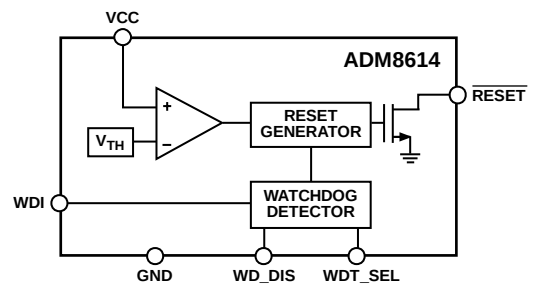


Figure 2. [ADM8614](#) Functional Block Diagram

both the [ADM8613](#) and [ADM8614](#). A separate supply input allows the [ADM8612](#) and [ADM8615](#) to monitor 20 different low voltage levels from 0.5 V to 1.9 V.

The [ADM8611](#), [ADM8612](#), [ADM8613](#), and [ADM8615](#) can reset on demand through the manual reset input. The watchdog function on the [ADM8613](#), [ADM8614](#), and [ADM8615](#) monitors the heartbeat of the microprocessor through the WDI pin. The [ADM8613](#) and [ADM8614](#) have a watchdog disable input, which allows the user to disable the watchdog function, if required. The [ADM8614](#) also has a watchdog timeout extension input, allowing the watchdog timeout to be extended from 1.6 sec to 100 sec.

The [ADM8611/ADM8612/ADM8613/ADM8614/ADM8615](#) are available in a 6-ball, 1.46 mm $\times$ 0.96 mm WLCSP. These devices are specified over the temperature range of -40°C to $+85^\circ\text{C}$.

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REVISION HISTORY

4/15—Rev. 0 to Rev. A

Changes to Reset Threshold Hysteresis Parameter, Table 1..... 3

1/15—Revision 0: Initial Version

SPECIFICATIONS

$V_{CC} = 2\text{ V to } 5.5\text{ V}$, $V_{IN} < V_{CC} + 0.3\text{ V}$, $T_A = -40^\circ\text{C to } +85^\circ\text{C}$, unless otherwise noted. Typical values are at $T_A = 25^\circ\text{C}$.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
OPERATING VOLTAGE RANGE ADM8611, ADM8613, ADM8614 ADM8612, ADM8615	V_{CC}	0.9		5.5	V	Guarantees valid $\overline{\text{RESET}}$ output
		2		5.5	V	Guarantees valid $\overline{\text{RESET}}$ output
		0.9			V	Guarantees $\overline{\text{RESET}}$ output low
UNDERVOLTAGE LOCKOUT (ADM8612, ADM8615) Input Voltage Rising Input Voltage Falling Hysteresis	$UVLO_{\text{RISE}}$ $UVLO_{\text{FALL}}$ $UVLO_{\text{HYS}}$	1.6	90	1.95	V	
					V	
					mV	
INPUT CURRENT VCC Quiescent Current VIN Average Input Current	I_{CC}		92	190	nA	$V_{CC} = 2\text{ V to } 5.5\text{ V}$, $\overline{\text{RESET}}$ deasserts, $V_{WDI} = V_{CC}$
				110	nA	$V_{CC} = 2\text{ V to } 5.5\text{ V}$, $\overline{\text{RESET}}$ deasserts, $V_{WDI} = V_{CC}$, $T_A = 25^\circ\text{C}$
			4	8.5	nA	$V_{IN} = 2\text{ V}$, $V_{CC} = 5.5\text{ V}$
			4	32	nA	$V_{IN} = 2\text{ V}$, $V_{CC} = 2\text{ V}$
RESET THRESHOLD VOLTAGE ADM8611, ADM8613, ADM8614 ADM8612, ADM8615	V_{TH}	$V_{TH} - 1.3\%$	V_{TH}	$V_{TH} + 1.3\%$	V	Input falling
		$V_{TH} - 1.3\%$	V_{TH}	$V_{TH} + 1.3\%$	V	See Table 10 and Table 12
		$V_{TH} - 1.4\%$	1.1	$V_{TH} + 1.4\%$	V	$V_{TH} \geq 1.2\text{ V}$, see Table 11
		$V_{TH} - 1.6\%$	1	$V_{TH} + 1.6\%$	V	1.1 V threshold option
		$V_{TH} - 1.6\%$	0.95	$V_{TH} + 1.6\%$	V	1 V threshold option
		$V_{TH} - 1.7\%$	0.9	$V_{TH} + 1.7\%$	V	0.95 V threshold option
		$V_{TH} - 1.8\%$	0.85	$V_{TH} + 1.8\%$	V	0.9 V threshold option
		$V_{TH} - 1.8\%$	0.8	$V_{TH} + 1.8\%$	V	0.85 V threshold option
		$V_{TH} - 1.9\%$	0.75	$V_{TH} + 1.9\%$	V	0.8 V threshold option
		$V_{TH} - 1.9\%$	0.7	$V_{TH} + 1.9\%$	V	0.75 V threshold option
		$V_{TH} - 2.0\%$	0.65	$V_{TH} + 2.0\%$	V	0.7 V threshold option
		$V_{TH} - 2.1\%$	0.6	$V_{TH} + 2.1\%$	V	0.65 V threshold option
		$V_{TH} - 2.1\%$	0.55	$V_{TH} + 2.1\%$	V	0.6 V threshold option
		$V_{TH} - 2.2\%$	0.5	$V_{TH} + 2.2\%$	V	0.55 V threshold option
					V	0.5 V threshold option
RESET THRESHOLD HYSTERESIS ADM8611, ADM8613, ADM8614 ADM8612, ADM8615	V_{HYS}		$0.9\% \times V_{TH}$		V	
			$0.9\% \times V_{TH}$		V	$V_{TH} > 1\text{ V}$
			10.3		mV	$V_{TH} \leq 1\text{ V}$
RESET TIMEOUT PERIOD	t_{RP}	170	200	240	ms	
PROPAGATION DELAY VCC to $\overline{\text{RESET}}$ ADM8611, ADM8613, ADM8614 VIN to $\overline{\text{RESET}}$ ADM8612, ADM8615	t_{PD_VCC}	18	26	37	μs	V_{CC} falling with $V_{TH} \times 10\%$ overdrive
	t_{PD_VIN}	13.5	23	35	μs	V_{IN} falling with $V_{TH} \times 10\%$ overdrive
INPUT GLITCH REJECTION VCC Glitch Rejection ADM8611, ADM8613, ADM8614 VIN Glitch Rejection ADM8612, ADM8615	t_{GR_VCC}	13.5	23	32	μs	V_{CC} falling, with $V_{TH} \times 10\%$ overdrive
	t_{GR_VIN}	13.5	21	27	μs	V_{IN} falling with $V_{TH} \times 10\%$ overdrive

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
WATCHDOG INPUT, WDI (ADM8613, ADM8614, ADM8615) Watchdog Timeout Period ADM8613, ADM8615 ADM8614 Leakage Current Input Threshold High Low WDI Pulse Width WDI Glitch Rejection	t_{WD} t_{WPR} t_{WPF}	$t_{WD} - 13\%$ $t_{WD} - 13\%$ $t_{WD} - 13\%$ 0.9 85 300	t_{WD} t_{WD} t_{WD} 60	$t_{WD} + 19\%$ $t_{WD} + 19\%$ $t_{WD} + 19\%$ 5 0.4	sec sec sec nA V V ns ns ns	Base period, WD_DIS low Extended period, WD_DIS high $V_{WDI} = V_{CC} = 5.5 V$ High pulse Low pulse
RESET OUTPUT Output Voltage Low Leakage Current	V_{RST_OL}			0.4 0.4 0.4 0.4 5	V V V V nA	$V_{CC} > 4.25 V$, $I_{SINK} = 6.5 mA$ $V_{CC} > 2.5 V$, $I_{SINK} = 6 mA$ $V_{CC} > 1.2 V$, $I_{SINK} = 4.6 mA$ $V_{CC} > 0.9 V$, $I_{SINK} = 0.9 mA$ $V_{RESET} = V_{CC} = 5.5 V$
MANUAL RESET INPUT, MR (ADM8611, ADM8612, ADM8613, ADM8615) V_{IL} V_{IH} MR Minimum Input Pulse Width MR Glitch Rejection MR To Reset Delay MR Pull-Up Resistance	t_{D_MR}	0.9 1	0.4 0.65	0.4	V V μs μs μs k Ω	
WATCHDOG TIMEOUT DISABLE INPUT, WD_DIS (ADM8613, ADM8614) V_{IL} V_{IH} Leakage Current Glitch Rejection		0.9 -5	0.1	0.4 +5	V V nA μs	$V_{WD_DIS} = 0 V$ to V_{CC}
WATCHDOG TIMEOUT SELECTION INPUT, WDT_SEL (ADM8614) V_{IL} V_{IH} Leakage Current		0.9 -5		0.4 +5	V V nA	$V_{WDT_SEL} = 0 V$ to V_{CC}

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VCC	−0.3 V to +6 V
WD_DIS	−0.3 V to +6 V
RESET	−0.3 V to +6 V
VIN	−0.3 V to +6 V
MR	−0.3 V to V _{CC} + 0.3 V
WDI	−0.3 V to V _{CC} + 0.3 V
WDT_SEL	−0.3 V to V _{CC} + 0.3 V
Input/Output Current	10 mA
Storage Temperature Range	−40°C to +150°C
Operating Temperature Range	−40°C to +85°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for a device soldered on an FR4 board with a minimum footprint.

Table 3.

Package Type	θ_{JA}	Unit
6-Ball WLCSP	105.6	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

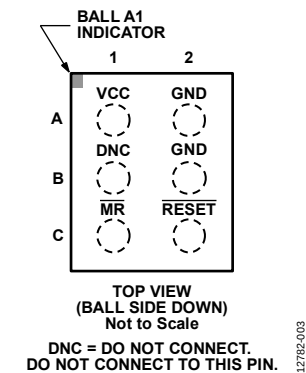


Table 4. ADM8611 Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	VCC	Power Supply Input. The voltage on the VCC pin is monitored on the ADM8611. It is recommended to place a 0.1 μ F decoupling capacitor as close as possible to the device between the VCC pin and the GND pin.
A2	GND	Ground. Both GND pins on the ADM8611 must be grounded.
B1	DNC	Do Not Connect. Do not connect to this pin.
B2	GND	Ground. Both GND pins on the ADM8611 must be grounded.
C1	$\overline{\text{MR}}$	Manual Reset Input, Active Low.
C2	$\overline{\text{RESET}}$	Active Low, Open-Drain $\overline{\text{RESET}}$ Output.

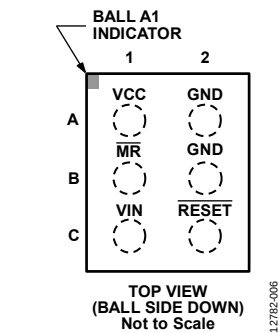


Table 5. ADM8612 Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	VCC	Power Supply Input. The voltage on the VCC pin is not monitored on the ADM8612. It is recommended to place a 0.1 μ F decoupling capacitor as close as possible to the device between the VCC pin and the GND pin.
A2	GND	Ground. Both GND pins on the ADM8612 must be grounded.
B1	$\overline{\text{MR}}$	Manual Reset Input, Active Low.
B2	GND	Ground. Both GND pins on the ADM8612 must be grounded.
C1	VIN	Low Voltage Monitoring Input. This separate supply input allows the ADM8612 to monitor low voltages on the VIN pin to 0.5 V.
C2	$\overline{\text{RESET}}$	Active Low, Open-Drain $\overline{\text{RESET}}$ Output.

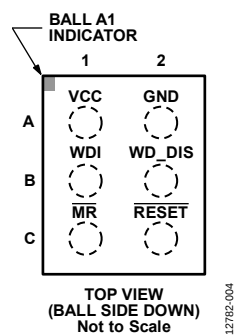


Figure 5. ADM8613 Pin Configuration

Table 6. ADM8613 Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	VCC	Power Supply Input. The voltage on the VCC pin is monitored on the ADM8613. It is recommended to place a 0.1 μ F decoupling capacitor as close as possible to the device between the VCC pin and the GND pin.
A2	GND	Ground.
B1	WDI	Watchdog Timer Input.
B2	WD_DIS	Watchdog Function Disable Input. Tie this pin high to disable the watchdog function of the device. Connect this pin to ground if it is not used.
C1	$\overline{\text{MR}}$	Manual Reset Input, Active Low.
C2	$\overline{\text{RESET}}$	Active Low, Open-Drain $\overline{\text{RESET}}$ Output.

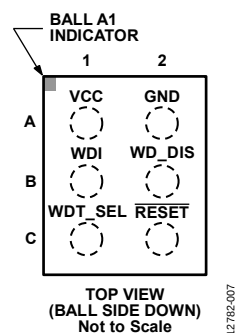


Figure 6. ADM8614 Pin Configuration

Table 7. ADM8614 Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	VCC	Power Supply Input. The voltage on the VCC pin is monitored on the ADM8614. It is recommended to place a 0.1 μ F decoupling capacitor as close as possible to the device between the VCC pin and the GND pin.
A2	GND	Ground.
B1	WDI	Watchdog Timer Input.
B2	WD_DIS	Watchdog Function Disable Input. Tie this pin high to disable the watchdog function of the device. Connect this pin to ground if it is not used.
C1	WDT_SEL	Watchdog Timeout Selection Input. Pull this pin high to extend the watchdog timeout period of the ADM8614 to 100 sec. Pull this pin low to return the watchdog timeout period to its base value. Toggling WDT_SEL resets the watchdog timer.
C2	$\overline{\text{RESET}}$	Active Low, Open-Drain $\overline{\text{RESET}}$ Output.

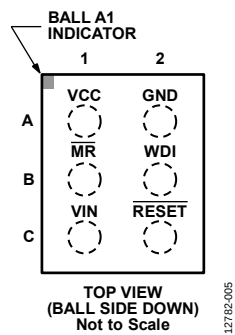
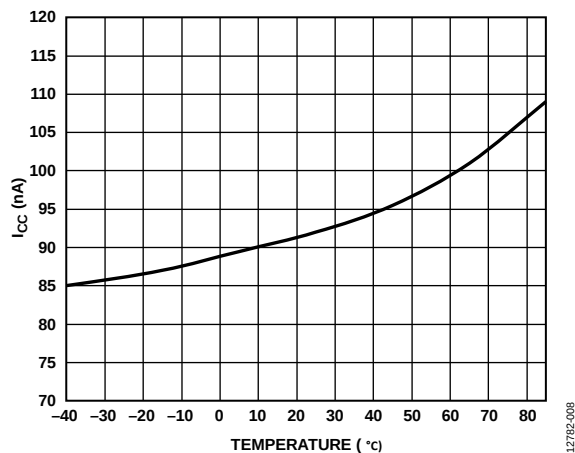
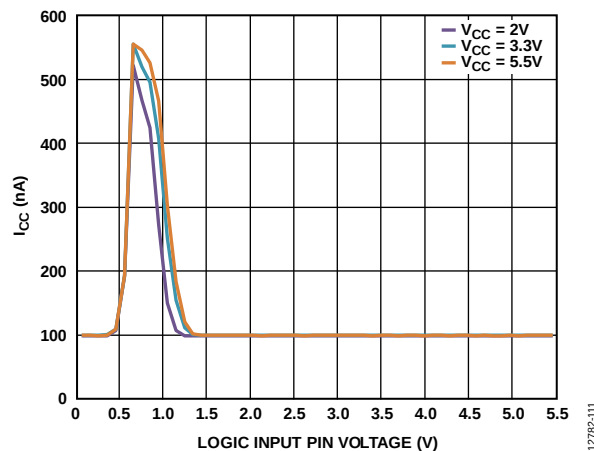
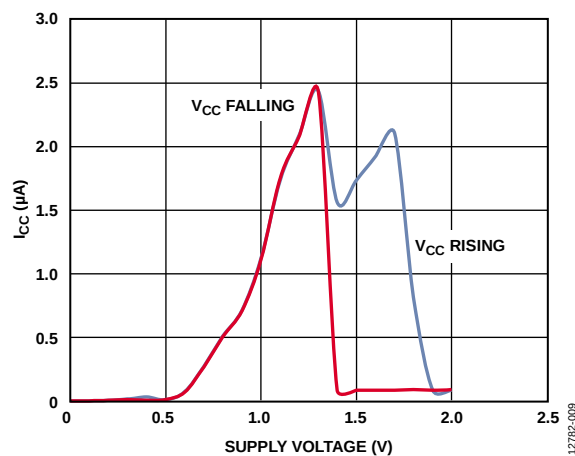
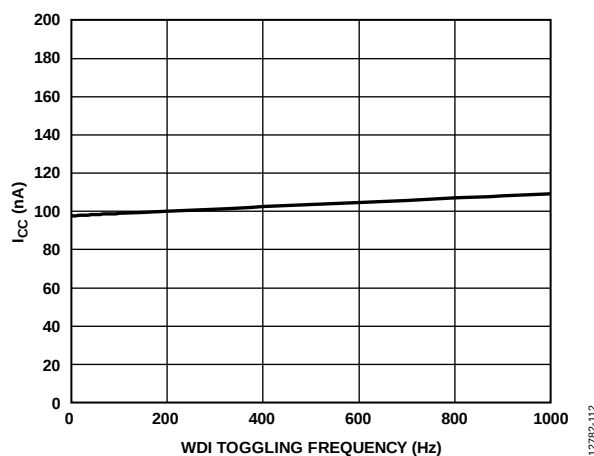
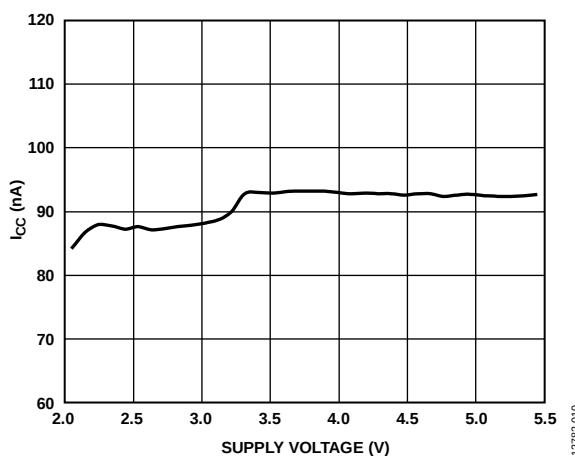
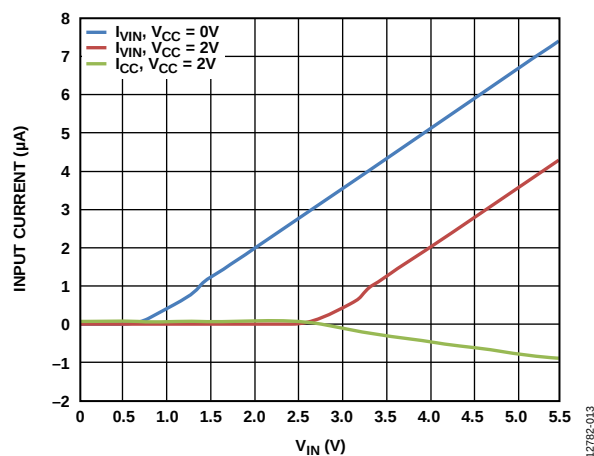


Figure 7. ADM8615 Pin Configuration

Table 8. ADM8615 Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	VCC	Power Supply Input. The voltage on the VCC pin is not monitored on the ADM8615. It is recommended to place a 0.1 μ F decoupling capacitor as close as possible to the device between the VCC pin and the GND pin.
A2	GND	Ground.
B1	MR	Manual Reset Input, Active Low.
B2	WDI	Watchdog Timer Input.
C1	VIN	Low Voltage Monitoring Input. This separate supply input allows the ADM8615 to monitor low voltages on the VIN pin to 0.5 V.
C2	RESET	Active Low, Open-Drain RESET Output.

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 8. Supply Current (I_{CC}) vs. TemperatureFigure 11. Supply Current (I_{CC}) vs. Logic Input Pin Voltage, with the Exception of the MR PinFigure 9. Supply Current (I_{CC}) vs. Supply Voltage, $V_{CC} < 2V$ Figure 12. Average Supply Current (I_{CC}) vs. WDI Toggling Frequency, Using a Square Pulse Signal with a Duty Cycle of 50%Figure 10. Supply Current (I_{CC}) vs. Supply VoltageFigure 13. V_{IN} Pin and V_{CC} Pin Input Current vs. V_{IN}

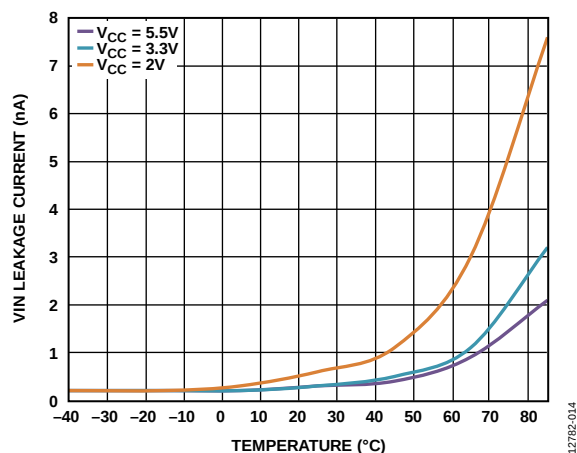


Figure 14. VIN Leakage Current vs. Temperature

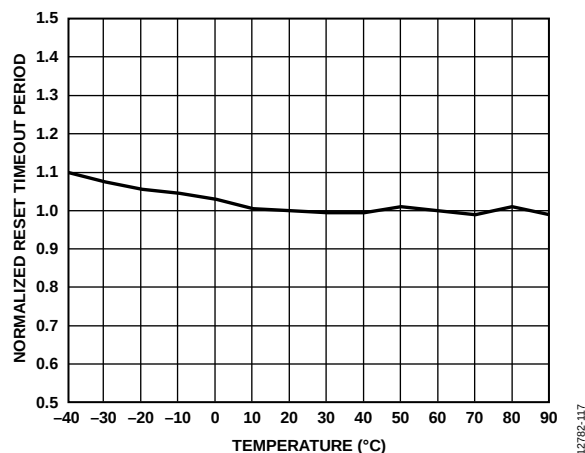


Figure 17. Normalized Reset Timeout Period vs. Temperature

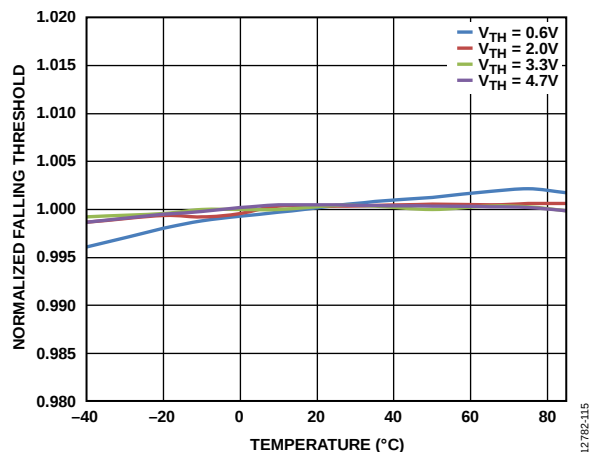


Figure 15. Normalized Falling Threshold vs. Temperature

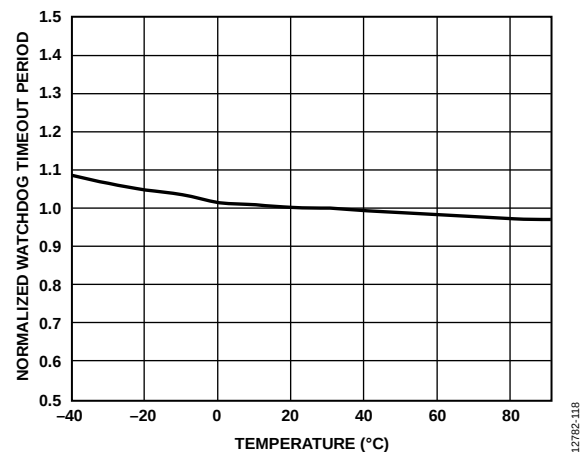


Figure 18. Normalized Watchdog Timeout Period vs. Temperature

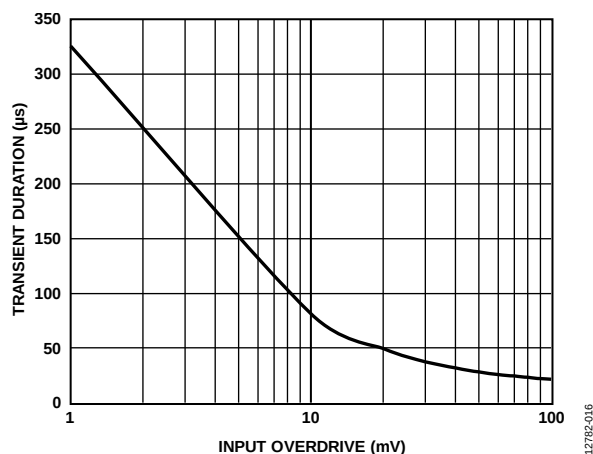


Figure 16. Maximum Transient Duration vs. Input Overdrive, V_{CC} and V_{IN} Falling

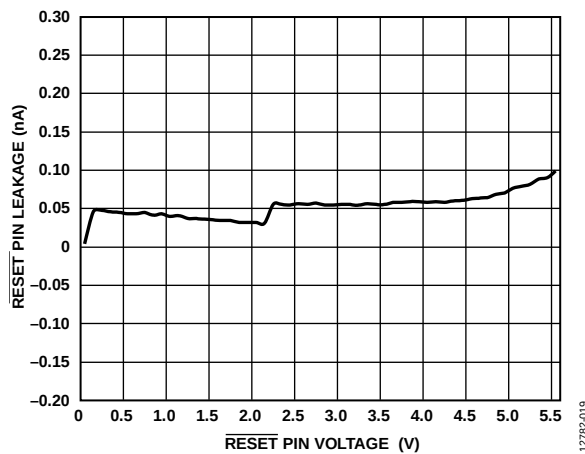


Figure 19. $\overline{RESET}$ Pin Leakage vs. $\overline{RESET}$ Pin Voltage

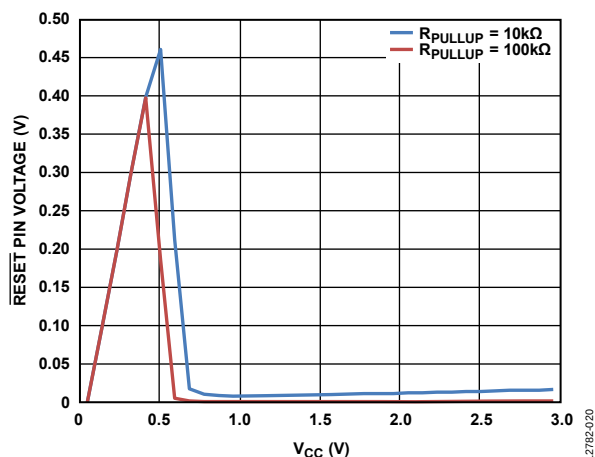


Figure 20. $\overline{\text{RESET}}$ Pin Voltage vs. Voltage on VCC
(with the $\overline{\text{RESET}}$ Pin Pulled up to the VCC Pin Through R_{PULLUP})

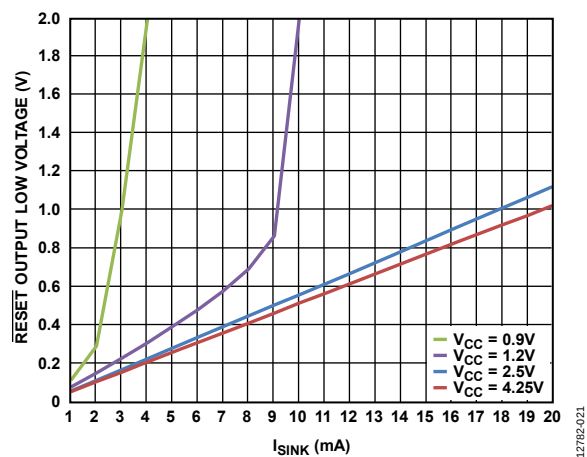


Figure 21. $\overline{\text{RESET}}$ Output Low Voltage ($V_{\text{RST_OL}}$) vs. Sink Current (I_{SINK})

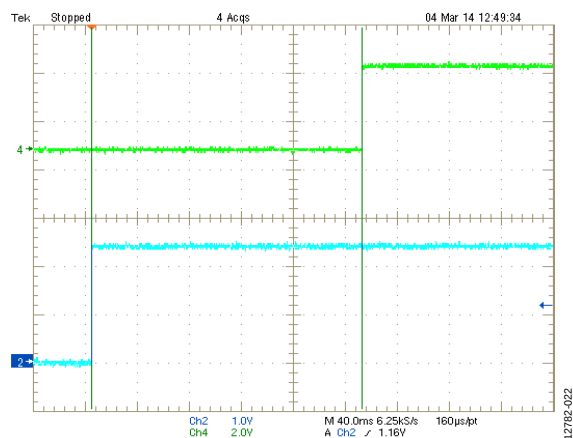


Figure 22. $\overline{\text{RESET}}$ Timeout Delay With V_{CC} and V_{IN} Rising

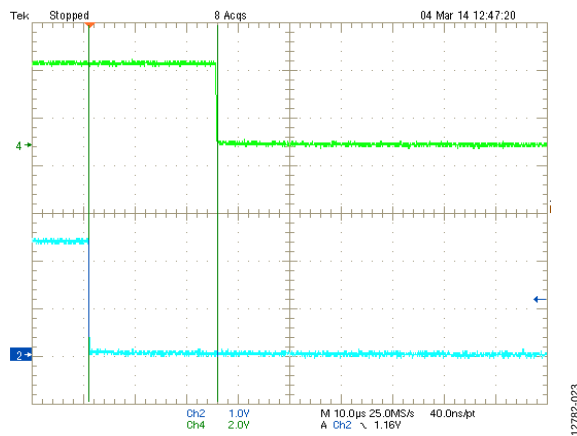


Figure 23. $\overline{\text{RESET}}$ Timeout Delay With V_{CC} and V_{IN} Falling

THEORY OF OPERATION

The ADM8611/ADM8612/ADM8613/ADM8614/ADM8615 low power voltage supervisors protect the integrity of system operation by ensuring the proper operation during power-up, power-down, and brownout conditions. These devices monitor the input voltage level and compare it against an internal reference. The RESET output asserts whenever the monitored voltage level is below the reference threshold, keeping the processor in a reset state. The RESET output deasserts if the monitored voltage rises above the threshold reference for a minimum period, the active reset timeout period. This ensures that the supply voltage for the processor is raised to an adequate level and stable before exiting reset.

The ultralow supply current makes the ADM8611/ADM8612/ADM8613/ADM8614/ADM8615 devices particularly suitable for use in low power, portable equipment.

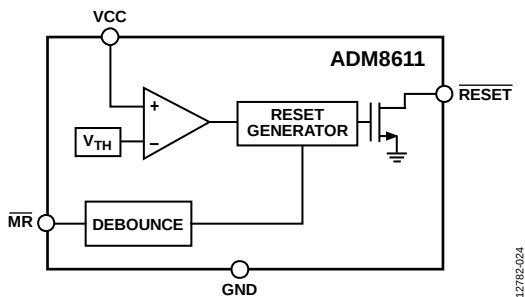


Figure 24. Functional Diagram of the ADM8611

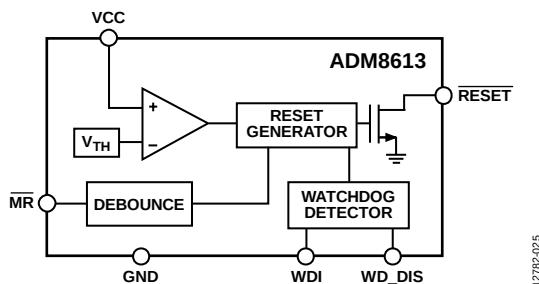


Figure 25. Functional Diagram of the ADM8613

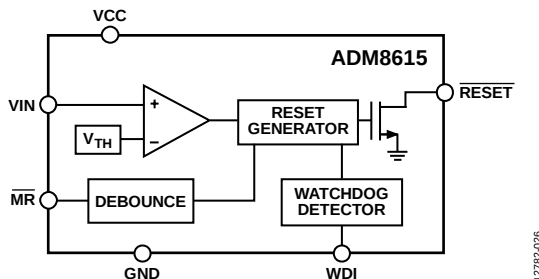


Figure 26. Functional Diagram of the ADM8615

VOLTAGE MONITORING INPUT

The VCC pin of the ADM8611/ADM8613/ADM8614 acts as both a device power input node and a voltage monitoring input node. The ADM8612 uses separate pins for supply and voltage monitoring to achieve a low voltage monitoring threshold to 0.5 V. It is recommended to place a 0.1 μ F decoupling capacitor as close as possible to the device between the VCC pin and the GND pin.

VIN AS AN ADJUSTABLE INPUT

Due to the low leakage nature of the VIN pin, the ADM8612 or ADM8615 can be used as devices with an adjustable threshold. Use an external resistor divider circuit to program the desired voltage monitoring threshold based on the VIN threshold, as shown in Figure 27.

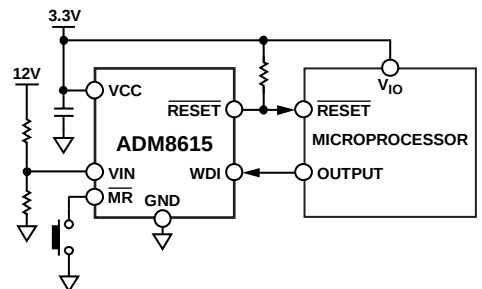


Figure 27. ADM8615 Typical Application Circuit

TRANSIENT IMMUNITY

To avoid unnecessary resets caused by fast power supply transients, an input glitch filter is added to the VCC pin of the ADM8611/ADM8613/ADM8614 and the VIN pin of the ADM8612 and ADM8615 to filter out the transient glitches on these pins.

Figure 16 shows the comparator overdrive (that is, the maximum magnitude of negative going pulses with respect to the typical threshold) vs. the pulse duration without a reset.

RESET OUTPUT

The ADM8611/ADM8612/ADM8613/ADM8614/ADM8615 devices all have an active low, open-drain reset output. For the ADM8611/ADM8613/ADM8614, the state of the output is guaranteed to be valid as soon as V_{CC} is greater than 0.9 V. For the ADM8612 and ADM8615, the output is guaranteed to be held low from when $V_{CC} = 0.9$ V to when the device exits ULVO.

When the monitored voltage falls below its associated threshold, RESET is asserted within 23 μ s to 26 μ s (typical). Asserting RESET this quickly ensures that the entire system can be reset at once before any part of the system voltage falls below its recommended operating voltage. This system reset can avoid dangerous and/or erroneous operation of a microprocessor-based system.

MANUAL RESET INPUT

The ADM8611, ADM8612, ADM8613, and ADM8615 feature a manual reset input (MR). Drive MR low to assert the reset output. When MR transitions from low to high, the reset remains asserted for the duration of the reset timeout period before deasserting. The MR input has a 600 k Ω internal pull-up resistor so that the input is always high when unconnected. To drive the MR input, use an external signal or a push-button switch to ground; debounce circuitry is integrated on-chip for this purpose. Noise immunity is provided on the MR input, and fast, negative going transients of up to 0.4 μ s (typical) are ignored. If required, a 0.1 μ F capacitor between the MR pin and ground provides additional noise immunity.

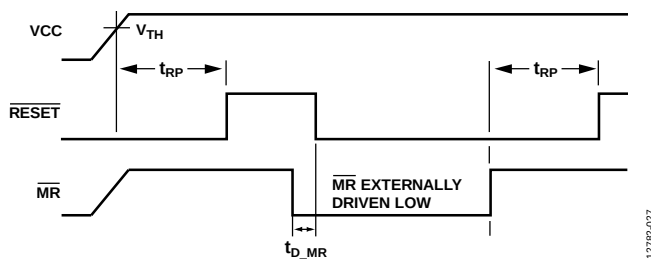


Figure 28. Manual Reset Timing

WATCHDOG TIMER

The ADM8613/ADM8614/ADM8615 feature a watchdog timer that monitors microprocessor activity. A timer circuit is cleared with every low to high or high to low logic transition on the watchdog input pin (WDI), which detects pulses as short as 85 ns. If the timer counts through the preset watchdog timeout period (t_{WD}), a RESET output is asserted. The microprocessor must toggle the WDI pin to avoid being reset. Failure of the microprocessor to toggle the WDI pin within the timeout period indicates a code execution error, and the reset pulse generated restarts the microprocessor in a known state.

In addition to logic transitions on WDI, the watchdog timer is also cleared by a reset assertion caused by an undervoltage condition on the VCC pin, WDT_SEL toggling, or MR being pulled low. When RESET is asserted, the watchdog timer is cleared and does not begin counting again until the RESET output is deasserted. The watchdog timer can be disabled by driving the watchdog disable input (WD_DIS) high.

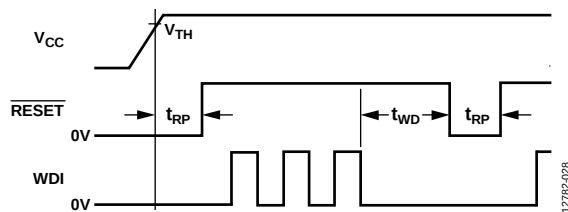


Figure 29. Watchdog Timer Timing

WATCHDOG TIMEOUT SELECT INPUT

Pulling the watchdog timeout select input (WDT_SEL) on the ADM8614 high allows the device to extend its watchdog timeout period from 1.6 sec (typical) to 100 sec (typical). This function allows processors to have a long initialization time during startup.

The long timeout period also enables the processor to stay in low power mode for a long period and work only intermittently, reducing overall system power consumption.

TYPICAL APPLICATION CIRCUITS

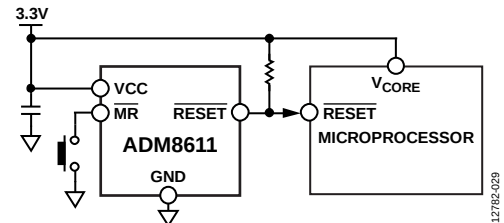


Figure 30. ADM8611 Typical Application Circuit

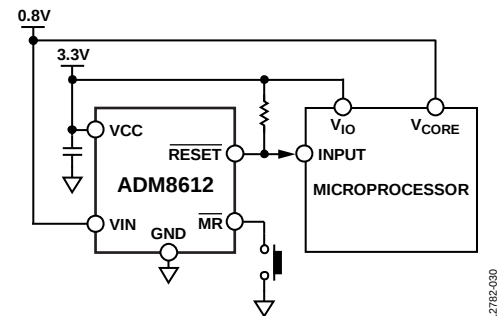


Figure 31. ADM8612 Typical Application Circuit

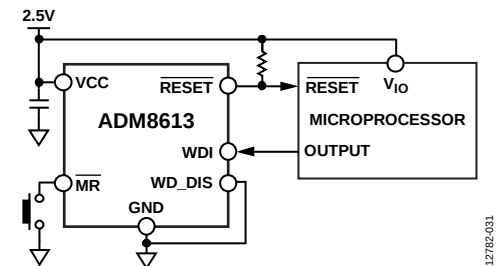


Figure 32. ADM8613 Typical Application Circuit

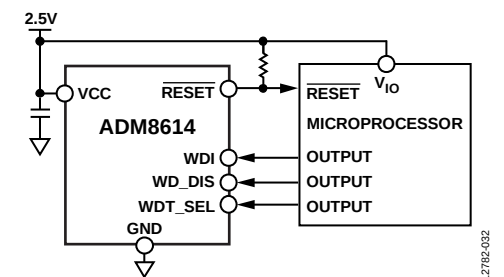


Figure 33. ADM8614 Typical Application Circuit

LOW POWER DESIGN TECHNIQUES

With their ultralow power consumption level, the ADM8611/ADM8612/ADM8613/ADM8614/ADM8615 are ideal for battery-powered, low power applications where every bit of power matters. In addition to using low power ICs, good circuit design practices can help the user further reduce the overall system power loss.

Digital Inputs

The digital inputs of the ADM8611/ADM8612/ADM8613/ADM8614/ADM8615 voltage supervisors are designed with CMOS technology to minimize power consumption. The nature of the CMOS structure leads to an increase of the device I_{CC} , while the voltage level on the input approaches its undefined logic range, as shown in Figure 11. To minimize this effect, follow these recommendations:

- If the digital input does not need to be toggled in a particular design, tie it directly to the VCC or GND pin of the device.
- Push-pull outputs with logic high levels close to the VCC of the ADM8611/ADM8612/ADM8613/ADM8614/ADM8615 are the ideal choice for driving the digital signal line.
- Using push-pull outputs with a logic high level near the minimum logic high specification of the digital input is usually not recommended. One exception is if the input is required to be driven high only infrequently for a relatively short period.
- Open-drain outputs with a pull-up resistor to VCC can be used to drive digital signal lines. Open-drain outputs are best suited for driving lines that are required to be driven low only infrequently for a relatively short period.
- The leakage current on both the digital input and the open-drain output determines the size of the pull-up resistor needed and, in turn, decides the power loss through the resistor while driving the input low.
- The MR pin on the ADM8611, ADM8612, ADM8613, and ADM8615 features an internal pull-up resistor. The infrequent usage of this pin makes its power loss while driven to logic low negligible.

WDI Input

When the watchdog input (WDI) is driven by a push-pull input/output with a logic high level near the VCC level of the ADM8613/ADM8614/ADM8615, neither a high nor a low input logic causes the system to consume additional current. To reduce the total current consumption, increase the speed of the input transition to the number of transitions. One high to low or low to high transition within the watchdog timeout period is sufficient to prevent the watchdog timer from generating a reset output.

If the watchdog input is driven by a push-pull output with a logic high level near the minimum logic high specification of the digital input, then a logic high input may cause CMOS shoot through and increase the bias current (I_{CC}) of the ADM8613/ADM8614/ADM8615. To minimize the power loss in this setup, use short positive pulses to drive the WDI pin. The ideal pulse width is as small as possible but greater than the required minimum pulse width of the WDI input. One pulse within the watchdog timeout period is sufficient to prevent the watchdog timer from generating a reset output.

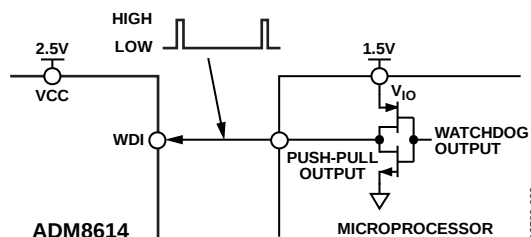


Figure 34. Using a Push-Pull Output with a Lower Logic High Level to VCC, Driving the WDI Pin with Short Positive Pulse to Reduce I_{CC}

Similarly, if an open-drain input/output with a pull-up resistor to VCC is used to drive WDI, a logic low input causes additional current flowing through the pull-up resistor. A short negative pulse technique can minimize the long-term current consumption.

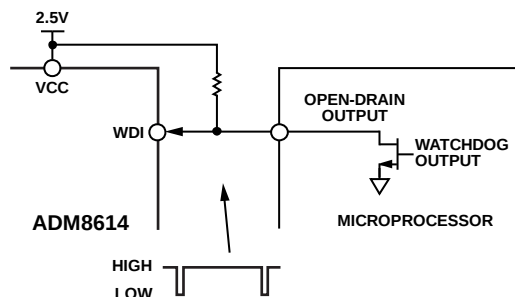


Figure 35. Short Negative Pulse on the WDI Pin to Reduce Leakage Current Through the Pull-Up Resistor

WD_DIS Input

For the ADM8613 and ADM8614, the watchdog disable input (WD_DIS) disables the watchdog function during system prototyping or during power-up to allow extra time for processor initialization.

To disable the watchdog timer function during power-up after a reset deassertion, the processor configures its input/output and drives WD_DIS high within the watchdog timeout period. If there is not enough time to configure the input/output or if an open-drain input/output is used to drive WD_DIS, an external pull-up resistor is required to keep the watchdog function disabled during power-up. Extra current is consumed through the pull-up resistor to enable the watchdog function. The leakage current on both WD_DIS and the input/output that drives it determines the size of the pull-up resistor needed and, in turn, determines the power loss through the resistor while driving the input low.

DEVICE OPTIONS

Table 9. Selection Table

Device Number	Low Voltage Monitoring	Manual Reset	Watchdog Timer	Watchdog Disable Input	Watchdog Timeout Selection Input
ADM8611	No	Yes	No	No	No
ADM8612	Yes	Yes	No	No	No
ADM8613	No	Yes	Yes	Yes	No
ADM8614	No	No	Yes	Yes	Yes
ADM8615	Yes	Yes	Yes	No	No

Table 10. ADM8611 V_{CC} Reset Threshold Voltage (V_{TH}) Options ($T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$)

Reset Threshold Number	Min	Typ	Max	Unit
200	1.974	2	2.026	V
220	2.171	2.2	2.229	V
232	2.290	2.32	2.350	V
263	2.596	2.63	2.664	V
280	2.764	2.8	2.836	V
293	2.892	2.93	2.968	V
300	2.961	3	3.039	V
308	3.040	3.08	3.120	V
440	4.343	4.4	4.457	V
463	4.570	4.63	4.690	V

Table 11. ADM8612 and ADM8615 V_{IN} Reset Threshold Voltage (V_{TH}) Options ($T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$)

Reset Threshold Number	Min	Typ	Max	Unit
050	0.489	0.5	0.511	V
055	0.538	0.55	0.562	V
060	0.588	0.6	0.612	V
065	0.637	0.65	0.663	V
070	0.686	0.7	0.714	V
075	0.736	0.75	0.764	V
080	0.785	0.8	0.815	V
085	0.835	0.85	0.865	V
090	0.885	0.9	0.915	V
095	0.935	0.95	0.965	V
100	0.984	1	1.016	V
110	1.084	1.1	1.116	V
120	1.184	1.2	1.216	V
130	1.283	1.3	1.317	V
140	1.382	1.4	1.418	V
150	1.481	1.5	1.520	V
160	1.579	1.6	1.621	V
170	1.678	1.7	1.722	V
180	1.777	1.8	1.823	V
190	1.875	1.9	1.925	V

Table 12. ADM8613 and ADM8614 V_{CC} Reset Threshold Voltage (V_{TH}) Options (T_A = –40°C to +85°C)

Reset Threshold Number	Min	Typ	Max	Unit
232	2.290	2.32	2.350	V
263	2.596	2.63	2.664	V
293	2.892	2.93	2.968	V
308	3.040	3.08	3.120	V
463	4.570	4.63	4.690	V

Table 13. ADM8613 and ADM8615 Watchdog Timeout Options (T_A = –40°C to +85°C)

Watchdog Timeout Period Code	Min	Typ	Max	Unit	Test Condition/Comments
Y	1.4	1.6	1.9	sec	WD_DIS low
Z	22.3	25.6	30.5	sec	WD_DIS low

Table 14. ADM8614 Watchdog Timeout Options (T_A = –40°C to +85°C)

Watchdog Timeout Period Code	Min	Typ	Max	Unit	Test Condition/Comments
Y	1.4	1.6	1.9	sec	WD_DIS low, WDT_SEL low
	87	100	119	sec	WD_DIS low, WDT_SEL high

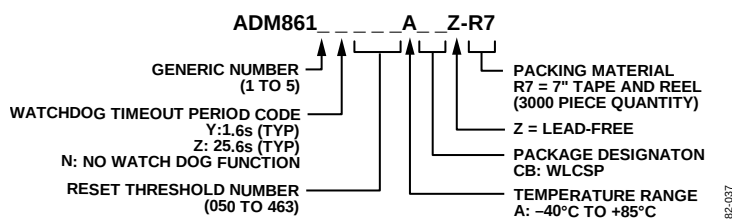


Figure 36. Ordering Code Structure

OUTLINE DIMENSIONS

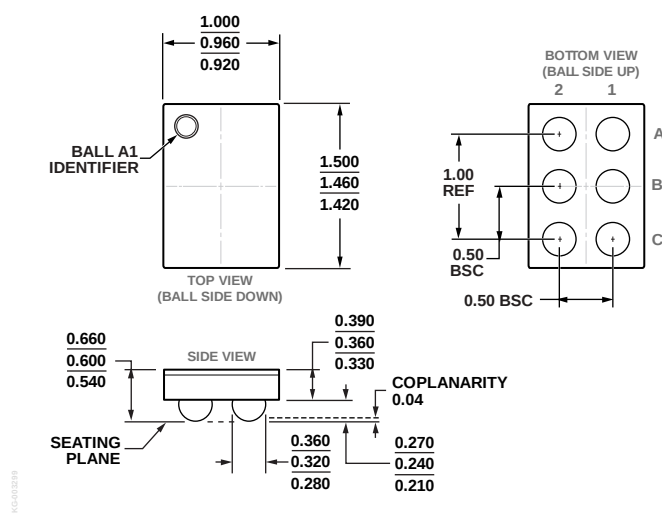


Figure 37. 6-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-6-17)

Dimensions shown in millimeters

ORDERING GUIDE

Model ^{1, 2, 3}	Temperature Range	Package Description	Package Option	Branding
ADM8611N263ACBZ-R7	−40°C to +85°C	6-Ball Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-17	DJ
ADM8612N110ACBZ-R7	−40°C to +85°C	6-Ball Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-17	DV
ADM8613Y232ACBZ-R7	−40°C to +85°C	6-Ball Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-17	DQ
ADM8614Y263ACBZ-R7	−40°C to +85°C	6-Ball Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-17	DR
ADM8615Y100ACBZ-R7	−40°C to +85°C	6-Ball Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-17	DS

¹ Z = RoHS Compliant Part.

² If ordering nonstandard models, complete the ordering code shown in Figure 36 by inserting the model number, reset threshold, reset timeout, and watchdog timeout. Contact Analog Devices, Inc., sales for availability of nonstandard models, quoting ADM861x-NTSD first, and then the complete ordering code.

³ A minimum of 10,000 must be ordered for nonstandard models.



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