# PCA2003

**32 kHz watch circuit with programmable adaptive motor pulse and pulse period**

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## 1. General description

The PCA2003 is a CMOS integrated circuit for battery operated wrist watches with a 32 kHz quartz crystal as timing element and a bipolar 1 Hz stepping motor. The quartz crystal oscillator and the frequency divider are optimized for minimum power consumption. A timing accuracy of 1 ppm is achieved with a programmable, digital frequency adjustment.

To obtain the minimum overall power consumption for the watch, an automatic motor pulse adaptation function is provided. The circuit supplies only the minimum drive current, which is necessary to ensure a correct motor step. Changing the drive current of the motor is achieved by chopping the motor pulse with a variable duty cycle. The pulse period and the range of the variable duty cycle can be programmed to suit different types of motors. The automatic pulse adaptation scheme is based on a safe dynamic detection of successful motor steps.

A pad RESET is provided (used for stopping the motor) for accurate time setting and for accelerated testing of the watch.

## 2. Features and benefits

- Amplitude-regulated 32 kHz quartz crystal oscillator, with excellent frequency stability and high immunity to leakage currents
- Electrically programmable time calibration with 1 ppm resolution stored in One Time Programmable (OTP) memory
- The quartz crystal is the only external component connected
- Very low supply current, typical 90 nA
- One second output pulses for bipolar stepping motor
- Five different programmable output periods (1 s to 30 s)
- Minimum power consumption for the entire watch, due to self adaptation of the motor drive according to the required torque
- Reliable step detection circuit
- Motor pulse width, pulse modulation, and pulse adaptation range programmable in a wide range, stored in OTP memory
- Stop function for accurate time setting and power saving during shelf life
- Test mode for accelerated testing of the mechanical parts of the watch and the IC
- Test bits for type recognition

## 3. Applications

- Driver circuits for bipolar stepping motors
- High immunity motor drive circuits

## 4. Ordering information

**Table 1. Ordering information**

| Type number | Topside marking | Package | | |
| --- | --- | --- | --- | --- |
| | | **Name** | **Description** | **Version** |
| PCA2003U/10AC/1 | PC 2003-1 | wire bond die | 8 bonding pads - 1.16 x 0.86 x 0.2 mm | PCA200xU |

### 4.1 Ordering options

**Table 2. Ordering options**

| Type number | Orderable part number | Package | Packing method | Minimum order quantity | Temperature |
| --- | --- | --- | --- | --- | --- |
| PCA2003U/10AC/1 | PCA2003U/10AC/1,00 | wire bond die | Sawn wafer on Film Frame Carrier (FFC) | 15064 | $T_{amb}$ = −10 °C to +60 °C |
| | PCA2003U/10AC/1Z | wire bond die | Reel 7" Q2 Die in tape reel DP | 2000 | $T_{amb}$ = −10 °C to +60 °C |

## 5. Block diagram
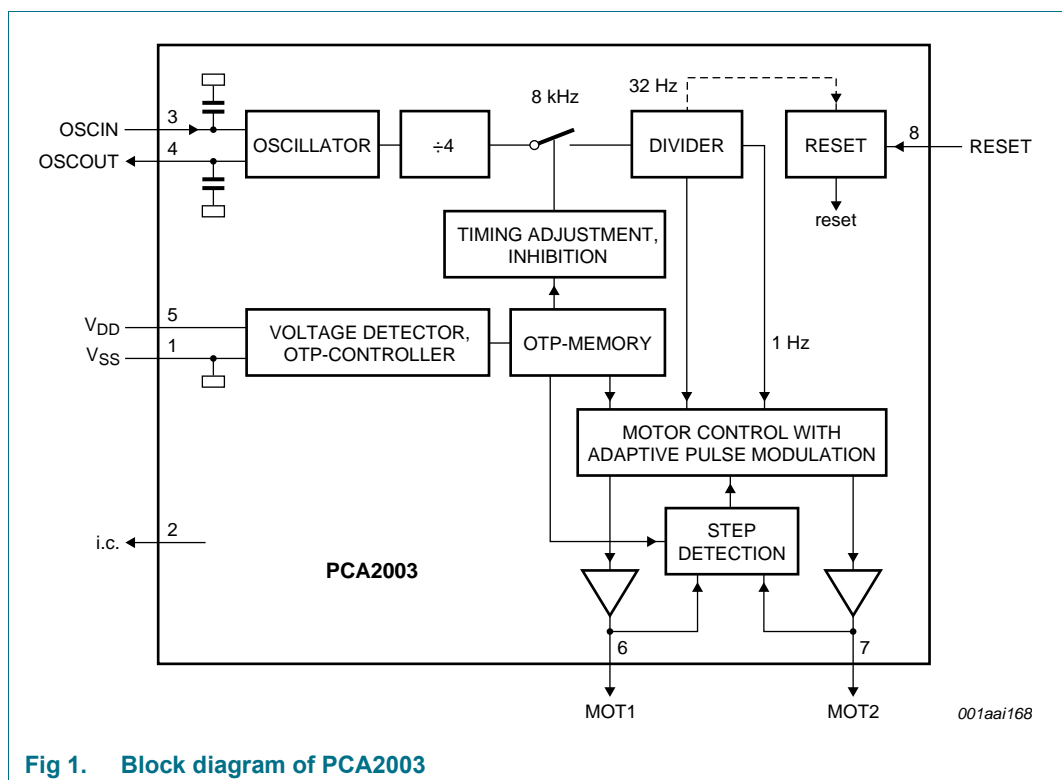


**Fig 1. Block diagram of PCA2003**

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# 6. Pinning information

## 6.1 Pinning

**PCA200xU**



*001aai177*

Top view. For mechanical details, see Figure 13.

**Fig 2.** **Pin configuration of PCA2003**
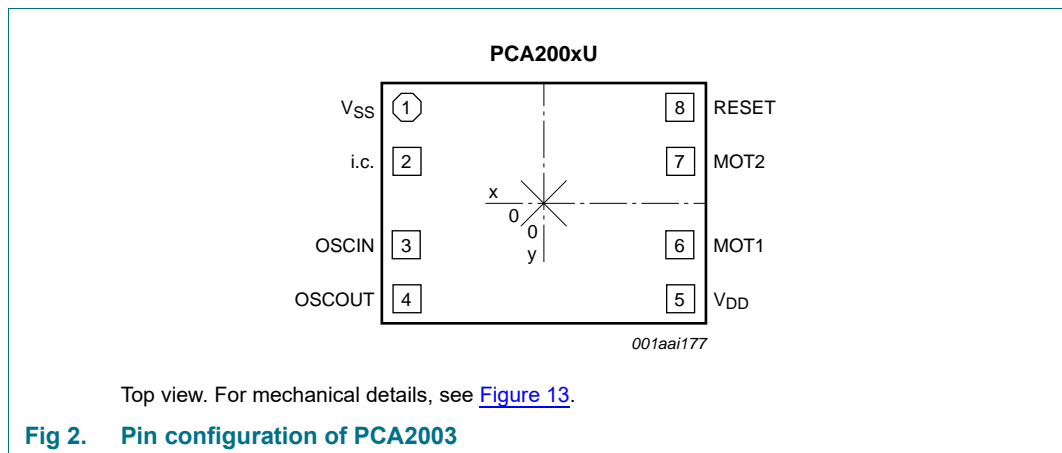
## 6.2 Pin description

**Table 3.** **Pin description**

| Symbol | Pin | Description |
|---|---|---|
| $V_{SS}$ | 1 | ground |
| i.c. | 2 | internally connected |
| OSCIN | 3 | oscillator input |
| OSCOUT | 4 | oscillator output |
| $V_{DD}$ | 5 | supply voltage |
| MOT1 | 6 | motor 1 output |
| MOT2 | 7 | motor 2 output |
| RESET | 8 | reset input |

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# 7. Functional description

## 7.1 Motor pulse

The motor output supplies pulses of different driving stages, depending on the torque required to turn on the motor. The number of different stages can be selected between three and six. With the exception of the highest driving stage, each motor pulse ($t_p$ in Figure 3 and Figure 6) is followed by a detection phase during which the motor movement is monitored, in order to check whether the motor has turned correctly or not.
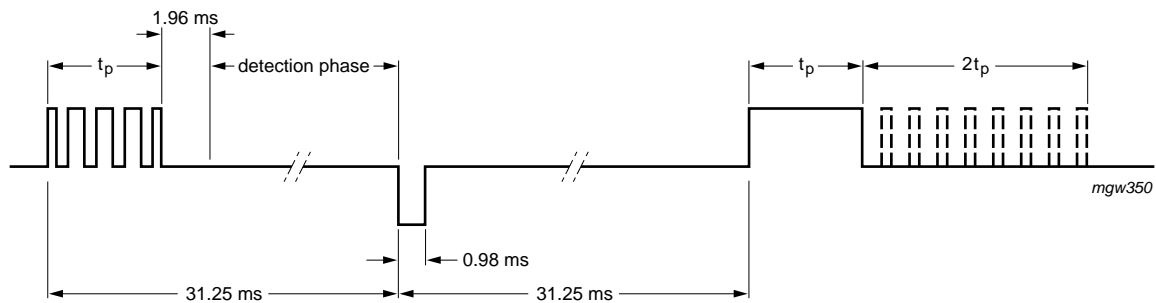


**Fig 3.** **Correction sequence after failed motor step**

If a missing step is detected, a correction sequence is generated (see Figure 3) and the driving stage is switched to the next level. The correction sequence consists of two pulses: first a short pulse in the opposite direction (0.98 ms, modulated with the maximum duty cycle) to give the motor a defined position, followed by a motor pulse of the strongest driving level. Every 4 minutes, the driving level is lowered again by one stage.
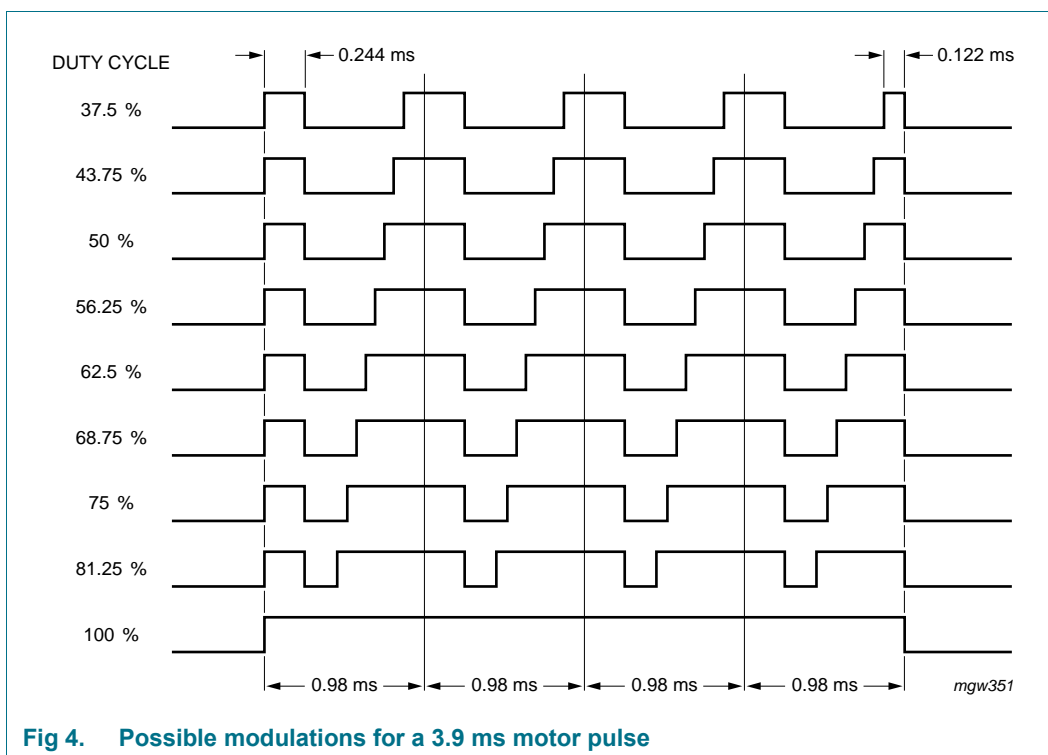
The motor pulse has a constant pulse width. The driving level is regulated by chopping the driving pulse with a variable duty cycle. The driving level starts from the programmed minimum value and increases by 6.25 % after each failed motor step. The strongest driving stage, which is not followed by a detection phase, is programmed separately.

Therefore, it is possible to program a larger energy gap between the pulses with step detection and the strongest, not monitored, pulse. This might be necessary to ensure a reliable and stable operation under adverse conditions (magnetic fields and vibrations). If the watch works in the highest driving stage, the driving level jumps after the 4-minute period directly to the lowest stage, and not just one stage lower.

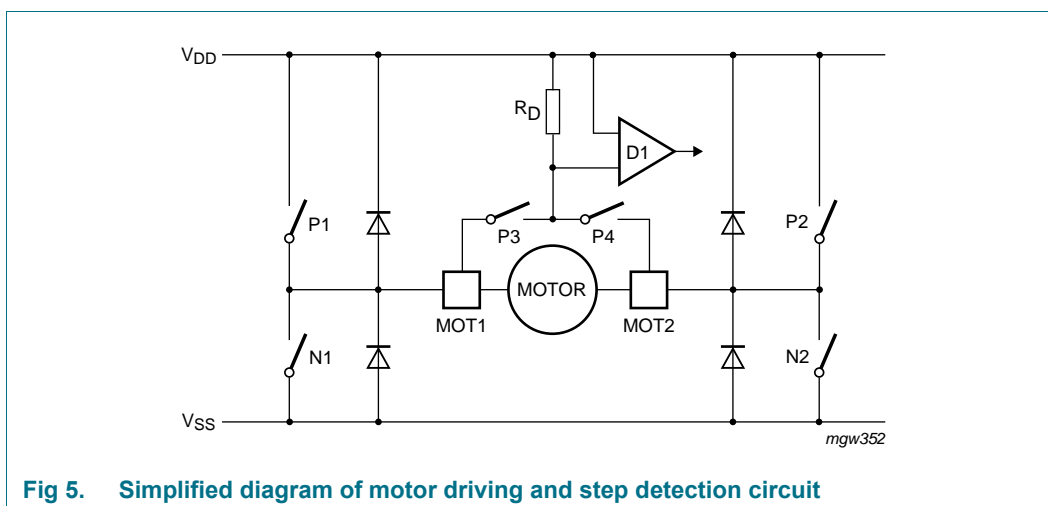To optimize the performance for different motors, the following parameters can be programmed:

- Pulse width: 0.98 ms to 7.8 ms in steps of 0.98 ms
- Duty cycle of lowest driving level: 37.5 % to 56.25 % in steps of 6.25 %
- Number of driving levels (including the highest driving level): 3 to 6
- Duty cycle of the highest driving level: 75 % or 100 %
- Enlargement pulse for the highest driving level: on or off

The enlargement pulse has a duty cycle of 25 % and a pulse width which is twice the programmed motor pulse width. The repetition period for the chopping pattern is 0.98 ms. Figure 4 shows an example of a 3.9 ms pulse.

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**Fig 4.     Possible modulations for a 3.9 ms motor pulse**

## 7.2  Step detection

Figure 5 shows a simplified diagram of the motor driving and step detection circuit, and Figure 6 shows the step detection sequence and corresponding sampling current. Between the motor driving pulses, the switches P1 and P2 are closed, which means the motor is short-circuited. For a pulse in one direction, P1 and N2 are open, and P2 and N1 are closed with the appropriate duty cycle; for a pulse in the opposite direction, P2 and N1 are open, and P1 and N2 closed.



**Fig 5.     Simplified diagram of motor driving and step detection circuit**

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The step detection phase is initiated after the motor driving pulse. In phase 1 P1 and P2 are first closed for 0.98 ms and then in phase 2 all four drive switches (P1, N1, P2 and N2) are opened for 0.98 ms. As a result, the energy stored in the motor inductance is reduced as fast as possible.

The induced current caused by the residual motor movement is then sampled in phase 3 (closing P3 and P2) and in phase 4 (closing P1 and P4). For step detection in the opposite direction P1 and P4 are closed during phase 3 and P2 and P3 during phase 4 (see Figure 6).
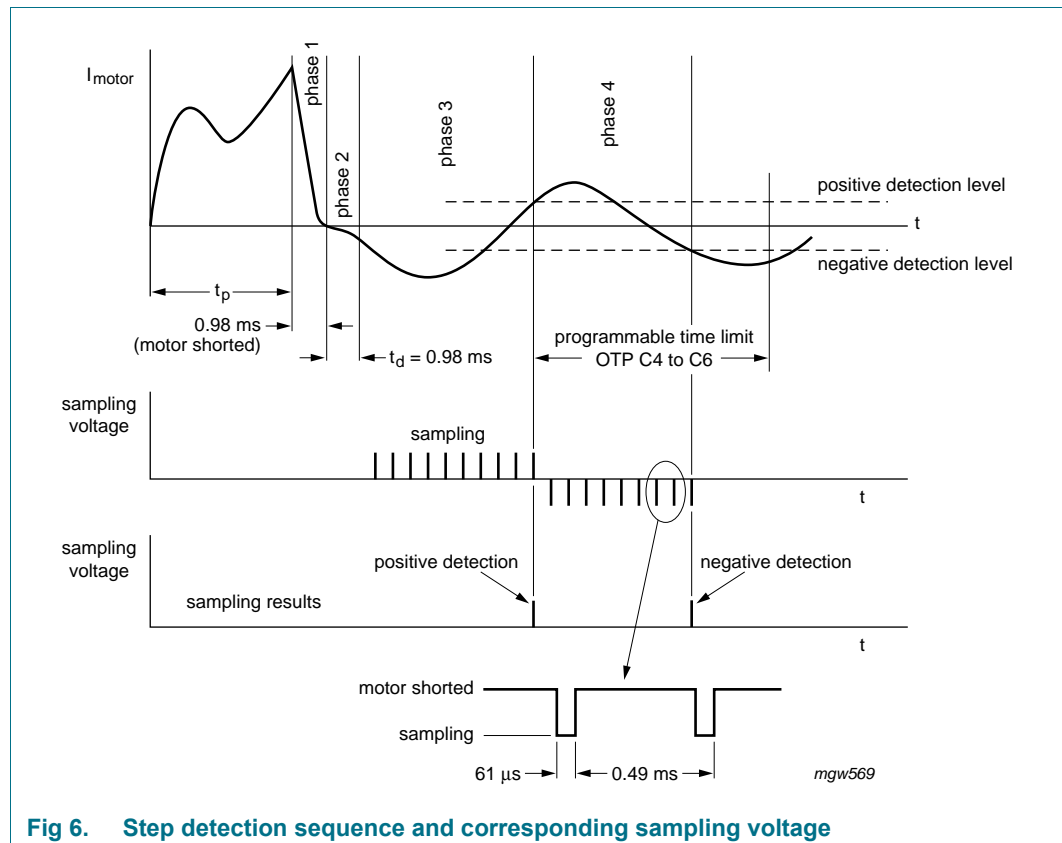


**Fig 6.** **Step detection sequence and corresponding sampling voltage**

The condition for a successful motor step is a positive step detection pulse (current in the same direction as in the driving phase) followed by a negative detection pulse within a given time limit. This time limit can be programmed between 3.9 ms and 10.7 ms (in steps of 0.98 ms) in order to ensure a safe and correct step detection under all conditions (for instance magnetic fields). The step detection phase stops after the last 31.25 ms, after the start of the motor driving pulse.

## 7.3 Time calibration

The quartz crystal oscillator has an integrated capacitance of 5.2 pF, which is lower than the specified capacitance ($C_L$) of 8.2 pF for the quartz crystal (see Table 11). Therefore, the oscillator frequency is typically 60 ppm higher than 32.768 kHz. This positive frequency offset is compensated by removing the appropriate number of 8192 Hz pulses in the divider chain (maximum 127 pulses), every 1 or 2 minutes. The time correction is given in Table 4.

**Table 4.    Time calibration**

| Calibration period | Correction per step (n = 1) | | Correction per step (n = 127) | |
|---|---|---|---|---|
| | ppm | Seconds per day | ppm | Seconds per day |
| 1 minute | 2.03 | 0.176 | 258 | 22.3 |
| 2 minutes | 1.017 | 0.088 | 129 | 11.15 |

After measuring the effective oscillator frequency, the number of correction pulses must be calculated and stored together with the calibration period in the OTP memory (see Section 7.7).

The oscillator frequency can be measured at pad RESET, where a square wave signal with the frequency of $\frac{1}{1024} \times f_{osc}$ is provided. This frequency shows a jitter every minute or every two minutes, which originates from the time calibration, depending on the programmed calibration period.

Details on how to measure the oscillator frequency and the programmed inhibition time are given in Section 7.10.

## 7.4  Reset

At pad RESET an output signal with a frequency of $\frac{1}{1024} \times f_{osc} = 32\ Hz$ is provided.

Connecting pad RESET to $V_{DD}$ stops the motor drive and opens all four (P1, N1, P2 and N2) driver switches (see Figure 5). Connecting pad RESET to $V_{SS}$ activates the test mode. In this mode the motor output frequency is 32 Hz, which can be used to test the mechanical function of the watch.

After releasing the pad RESET, the motor starts exactly one second later with the smallest duty cycle and with the opposite polarity to the last pulse before stopping. The debounce time for the RESET function is between 31 ms and 62 ms.

## 7.5  Programming possibilities

The programming data is stored in OTP cells (EPROM cells). At delivery, all memory cells are in state 0. The cells can be programmed to the state 1, but then there is no more set back to state 0. The programming data is organized in an array of four 8-bit words (see Table 5): word A contains the time calibration, words B and C contain the setting for the monitor pulses and word D contains the type recognition.

**Table 5.    Words and bits**

| Word | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| A | number of 8 192 Hz pulses to be removed | | | | | | | calibration period |
| B | lowest stage: duty cycle | | number of driving stages | | highest stage: duty cycle | pulse stretching | output period | |
| C | pulse width | | | | maximum time delay between positive and negative detection pulses | | output period | factory test bit |
| D | type | | | | factory test bits | | | |

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**Table 6.** **Description of word A bits**

| Bit | Value | Description |
|---|---|---|
| **Inhibition time** | | |
| 1 to 7 | - | adjust the number of the 8 192 Hz pulses to be removed; bit 1 is the MSB and bit 7 is the LSB |
| **Calibration period** | | |
| 8 | 0 | 1 minute |
| | 1 | 2 minutes |

**Table 7.** **Description of word B bits**

| Bit | Value | Description |
|---|---|---|
| **Duty cycle lowest driving stage** | | |
| 1 to 2 | 00 | 37.5 % |
| | 01 | 43.75 % |
| | 10 | 50 % |
| | 11 | 56.25 % |
| **Number of driving stages** | | |
| 3 to 4 | 00 | 3 |
| | 01 | 4 |
| | 10 | 5 |
| | 11 | 6[1] |
| **Duty cycle highest driving stage** | | |
| 5 | 0 | 75 %[2] |
| | 1 | 100 % |
| **Pulse stretching** | | |
| 6 | 0 | no pulse stretching |
| | 1 | pulse of $2 \times t_p$ and duty cycle of 25 % are added |
| **Output period** | | |
| 7 to 8 | 00 | 1 s |
| | 01 | 5 s |
| | 10 | 10 s |
| | 11 | 20 s |

[1] Including the highest driving stage, which one has no motor step detection.

[2] If the maximum duty cycle of 75 % is selected, not all programming combinations are possible since the second highest level must be smaller than the highest driving level.

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**Table 8.    Description of word C bits**

| Bit | Value | Description |
|-----|-------|-------------|
| **Pulse width $t_p$** | | |
| 1 to 3 | 000 | 0.98 ms |
|        | 001 | 1.95 ms |
|        | 010 | 2.90 ms |
|        | 011 | 3.90 ms |
|        | 100 | 4.90 ms |
|        | 101 | 5.90 ms |
|        | 110 | 6.80 ms |
|        | 111 | 7.80 ms |
| **Time delay $t_{d(max)}$ [1]** | | |
| 4 to 6 | 000 | 3.91 ms |
|        | 001 | 4.88 ms |
|        | 010 | 5.86 ms |
|        | 011 | 6.84 ms |
|        | 100 | 7.81 ms |
|        | 101 | 8.79 ms |
|        | 110 | 9.77 ms |
|        | 111 | 10.74 ms |
| **Output period** | | |
| 7 | 0 | bit 7 and 8 of word B active |
|   | 1 | 30 s, bit 7 and 8 of word B inactive |
| **Factory test bit** | | |
| 8 | - | - |

[1]    Between positive and negative detection pulses.

Byte D is read to determine which type of the PCA200x family is used in a particular application.

**Table 9.    Description of word D bits**

| Bit | Value | Description |
|-----|-------|-------------|
| **Type recognition** | | |
| 1 to 4 | 0000 | PCA2002 |
|        | 1000 | PCA2000 |
|        | 0100 | PCA2001 |
|        | 1100 | PCA2003 |
| **Factory test bits** | | |
| 5 to 8 | - | - |

## 7.6 Programming procedure

For a watch it is essential that the timing calibration can be made after the watch is fully assembled. In this situation, the supply pads are often the only terminals which are still accessible.

Writing to the OTP cells and performing the related functional checks is achieved in the PCA2003 by modulating the supply voltage. The necessary control circuit consists basically of a voltage level detector, an instruction counter which determines the function to be performed, and an 8-bit shift register which allows writing to the OTP cells of an 8-bit word in one step and acts as a data pointer for checking the OTP content.

There are six different instruction states (state 3 and state 5 are handled as state 4):

- State 1: measurement of the quartz crystal oscillator frequency (divided by 1024)
- State 2: measurement of the inhibition time
- State 3: write/check word A
- State 4: write/check word B
- State 5: write/check word C
- State 6: check word D (type recognition)

Each instruction state is switched on with a pulse to $V_{P(prog)(start)}$. After this large pulse, an initial waiting time of $t_0$ is required. The programming instructions are then entered by modulating the supply voltage with small pulses (amplitude $V_{P(mod)}$ and pulse width $t_{mod}$). The first small pulse defines the start time, the following pulses perform three different functions, depending on the time delay ($t_d$) from the preceding pulse (see Figure 7, Figure 8, Figure 11 and Figure 12):

- $t_d = t_1$ (0.7 ms); increments the instruction counter
- $t_d = t_2$ (1.7 ms); clocks the shift register with data = logic 0
- $t_d = t_3$ (2.7 ms); clocks the shift register with data = logic 1

The programming procedure requires a stable oscillator. This means that a waiting time, determined by the start-up time of the oscillator is necessary after power-on of the circuit.

After the $V_{P(prog)(start)}$ pulse, the instruction counter is in state 1 and the data shift register is cleared.

The instruction state ends with a second pulse to $V_{P(prog)(stop)}$ or with a pulse to $V_{store}$.

In any case, the instruction states are terminated automatically 2 seconds after the last supply modulation pulse.

## 7.7 Programming the memory cells

Applying the two-stage programming pulse (see Figure 7) transfers the stored data in the shift register to the OTP cells.

Perform the following to program a memory word:

1. Starting with a $V_{P(prog)(start)}$ pulse wait for the time period $t_0$ then set the instruction counter to the word to be written ($t_d = t_1$).

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2. Enter the data to be stored in the shift register ($t_d = t_2$ or $t_3$). LSB first (bit 8) and the MSB last (bit 1).

3. Applying the two-stage programming pulse $V_{prestore}$ followed by $V_{store}$ stores the word. The delay between the last data bit and the prestore pulse $V_{prestore}$ is $t_d = t_4$. Store the word by raising the supply voltage to $V_{store}$; the delay between the last data bit and the store pulse is $t_d$.

The example shown in Figure 7 performs the following functions:

- Start

- Setting instruction counter to state 4 (word B)

- Entering data word 110101 into the shift register (sequence: LSB first and MSB last)

- Writing to the OTP cells for word B
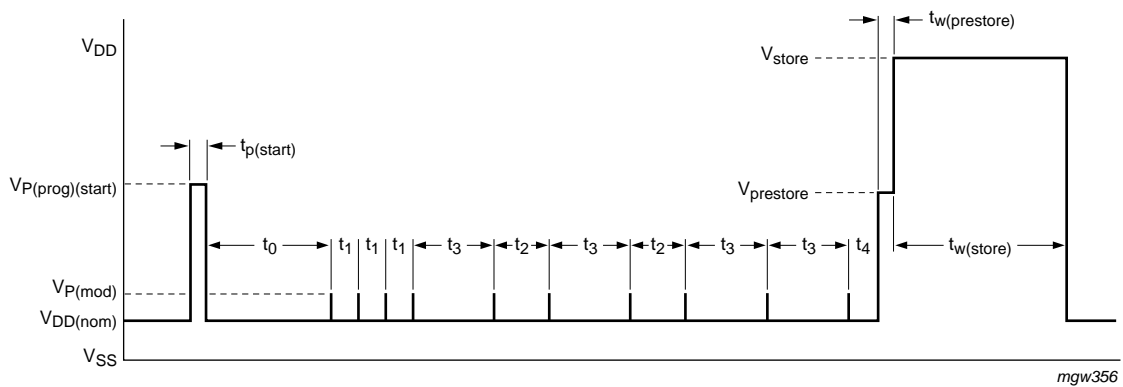


$V_{DD(nom)}$: nominal supply voltage.

The example shows the programming of B = 110101 (the sequence is MSB first and LSB last).

**Fig 7.** **Supply voltage modulation for programming**

## 7.8 Checking memory content

The stored data of the OTP array can be checked bit wise by measuring the supply current. The array word is selected by the instruction state and the bit is addressed by the shift register.

To read a word, the word is first selected ($t_d = t_1$), and a logic 1 is written into the first cell of the shift register ($t_d = t_3$). This logic 1 is then shifted through the entire shift register ($t_d = t_2$), so that it points with each clock pulse to the next bit.

If the addressed OTP cell contains a logic 1, a 30 k$\Omega$ resistor is connected between $V_{DD}$ and $V_{SS}$, which increases the supply current accordingly.

Figure 8 shows the supply voltage modulation for reading word B, with the corresponding supply current variation for word B = 110101 (sequence: first MSB and last LSB).



$V_{DD(nom)}$: nominal supply voltage.

(1) $\Delta I_{DD} = \dfrac{V_{DD}}{30\ k\Omega}$
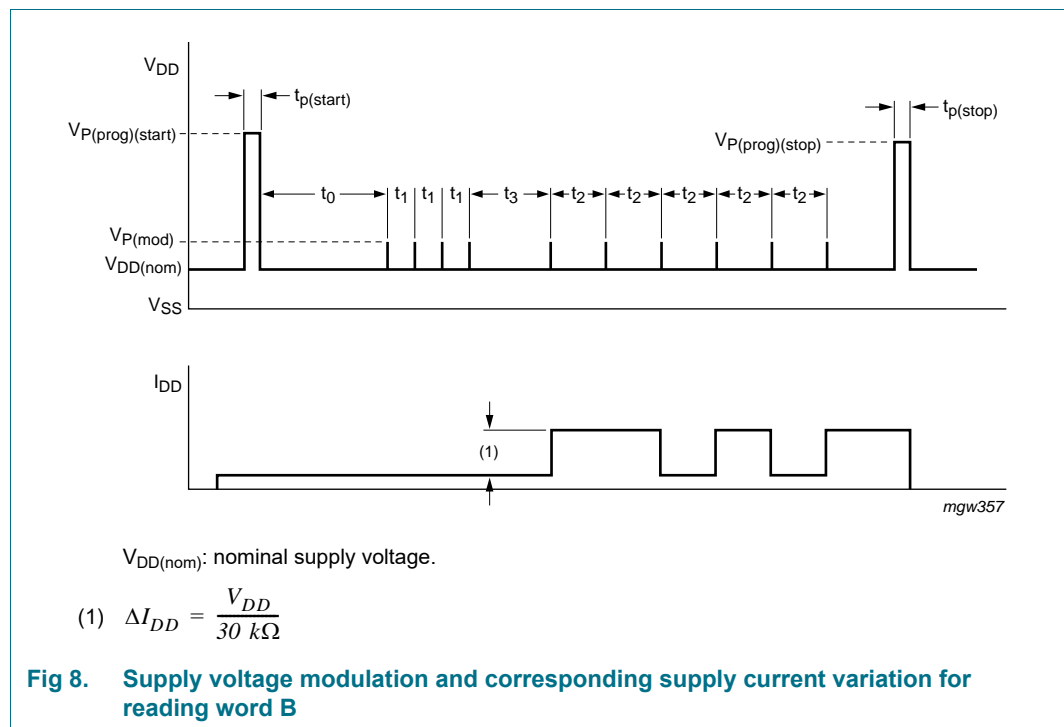
**Fig 8. Supply voltage modulation and corresponding supply current variation for reading word B**

## 7.9 Frequency tuning of assembled watch

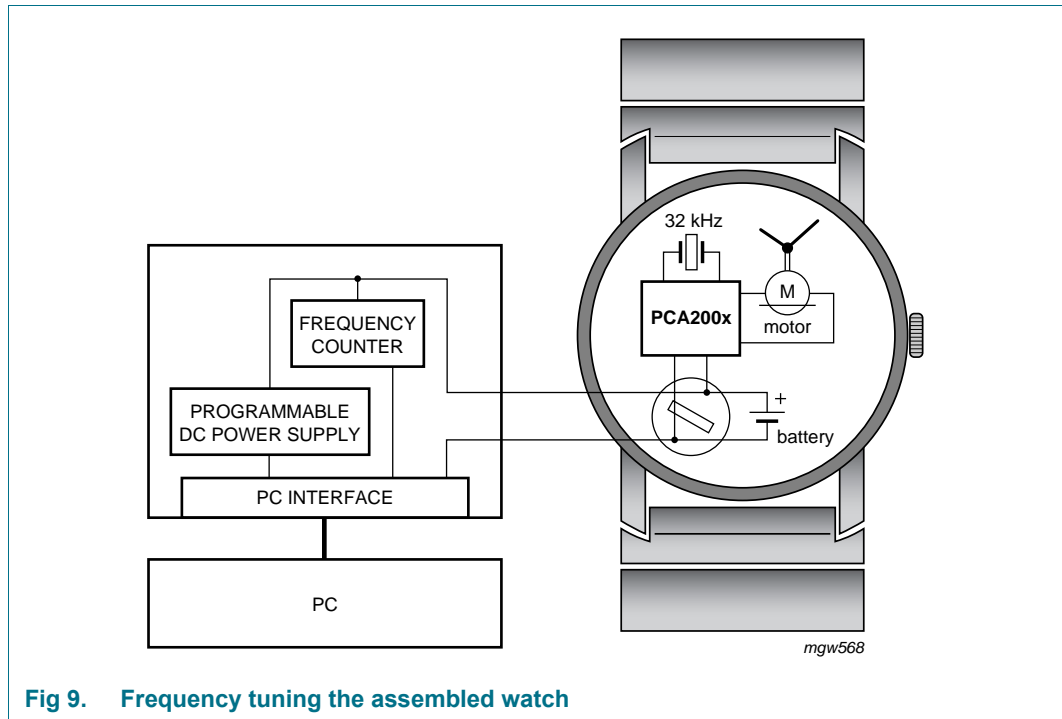Figure 9 shows the test set-up for frequency tuning the assembled watch.



**Fig 9. Frequency tuning the assembled watch**

## 7.10 Measurement of oscillator frequency and inhibition time

The output of the two measuring states can either be monitored directly at pad RESET or as a modulation of the supply voltage (a modulating resistor of 30 k$\Omega$ is connected between $V_{DD}$ and $V_{SS}$ when the signal at pad RESET is at HIGH-level).

The supply voltage modulation must be followed as shown in Figure 10 in order to guarantee the correct start-up of the circuit during production and testing.
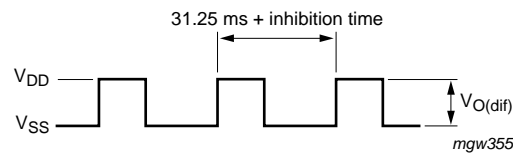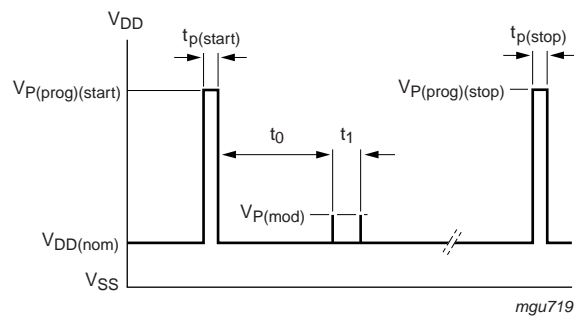


$V_{DD(nom)}$: nominal supply voltage.
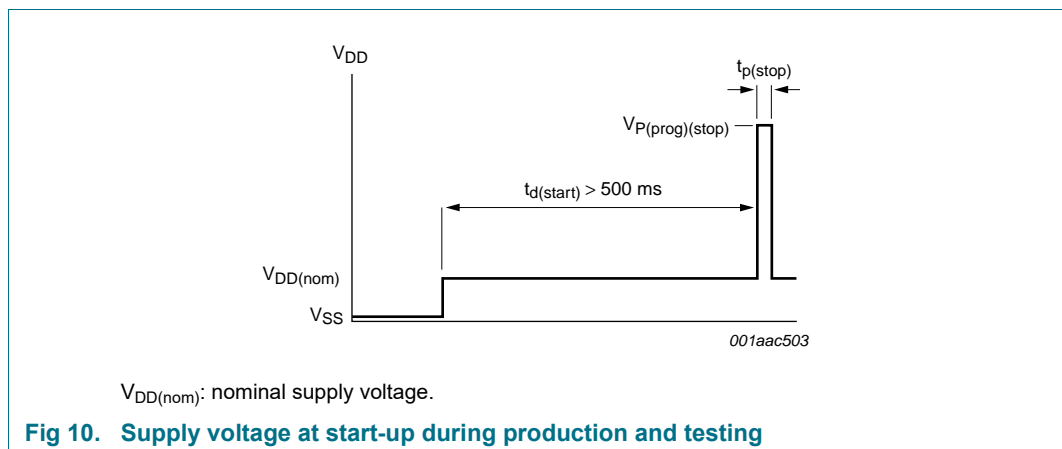
**Fig 10. Supply voltage at start-up during production and testing**

Measuring states:

- State 1: quartz crystal oscillator frequency divided by 1024; state 1 starts with a pulse to $V_P$ and ends with a second pulse to $V_P$
- State 2: inhibition time has a value of $n \times 0.122$ ms. A signal with periodicity of 31.25 ms + $n \times 0.122$ ms appears at pad RESET and as current modulation at pad $V_{DD}$ (see Figure 11 and Figure 12)



**Fig 11. Output waveform at pad RESET for instruction state 2**



$V_{DD(nom)}$: nominal supply voltage.

**Fig 12. Supply voltage modulation for starting and stopping of instruction state 2**

## 7.11 Customer testing

Connecting pad RESET to $V_{SS}$ activates the test mode. In this test mode, the motor output frequency is 8 Hz; the duty cycle reduction and battery check occurs every second, instead of every 4 minutes.

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# 8. Limiting values

**Table 10. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | $V_{SS}$ = 0 V | [1][2] | −1.8 | +7.0 | V |
| $V_I$ | input voltage | on all supply pins | | −0.5 | +7.5 | V |
| $t_{sc}$ | short circuit duration time | output | | - | indefinite | s |
| $T_{amb}$ | ambient temperature | | | −10 | +60 | °C |
| $V_{ESD}$ | electrostatic discharge voltage | HBM | [3] | - | ±2000 | V |
| | | MM | [4] | - | ±200 | V |
| $I_{lu}$ | latch-up current | | [5] | - | 100 | mA |
| $T_{stg}$ | storage temperature | | [6] | −30 | +100 | °C |

[1] When writing to the OTP cells, the supply voltage ($V_{DD}$) can be raised to a maximum of 12 V for a time period of 1 s.

[2] Connecting the battery with reversed polarity does not destroy the circuit, but in this condition a large current flows, which rapidly discharges the battery.

[3] Pass level; Human Body Model (HBM), according to Ref. 4 "JESD22-A114".

[4] Pass level; Machine Model (MM), according to Ref. 5 "JESD22-A115".

[5] Pass level; latch-up testing according to Ref. 6 "JESD78" at maximum ambient temperature ($T_{amb(max)}$).

[6] According to the NXP store and transport requirements (see Ref. 8 "NX3-00092") the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %. For long term storage products deviant conditions are described in that document.

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# 9. Characteristics

**Table 11.   Characteristics**

*$V_{DD}$ = 1.55 V; $V_{SS}$ = 0 V; $f_{osc}$ = 32.768 kHz; $T_{amb}$ = 25 °C; quartz crystal: $R_S$ = 40 kΩ, $C_1$ = 2 fF to 3 fF, $C_L$ = 8.2 pF; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Supply** | | | | | | | |
| $V_{DD}$ | supply voltage | normal operating mode; $T_{amb}$ = −10 °C to +60 °C | | 1.1 | 1.55 | 3.60 | V |
| $\Delta V_{DD}$ | supply voltage variation | $\Delta V/\Delta t$ = 1 V/μs | | - | - | 0.25 | V |
| $I_{DD}$ | supply current | between motor pulses | | - | 90 | 120 | nA |
| | | between motor pulses at $V_{DD}$ = 3.5 V | | - | 120 | 180 | nA |
| | | $T_{amb}$ = −10 °C to +60 °C | | - | - | 200 | nA |
| | | stop mode; pad RESET connected to $V_{DD}$ | | - | 100 | 135 | nA |
| **Motor output** | | | | | | | |
| $V_{sat}$ | saturation voltage | $R_{motor}$ = 2 kΩ; $T_{amb}$ = −10 °C to +60 °C | [1] | - | 150 | 200 | mV |
| $Z_{o(sc)}$ | output impedance (short circuit) | between motor pulses; $I_{motor}$ < 1 mA | | - | 200 | 300 | Ω |
| **Oscillator** | | | | | | | |
| $V_{start}$ | start voltage | | | 1.1 | - | - | V |
| $g_m$ | transconductance | $V_{i(osc)} \leq$ 50 mV (p-p) | | 5 | 10 | - | μS |
| $t_{startup}$ | start-up time | | | - | 0.3 | 0.9 | s |
| $\Delta f/f$ | frequency stability | $\Delta V_{DD}$ = 100 mV | | - | 0.05 | 0.20 | ppm |
| $C_{L(itg)}$ | integrated load capacitance | | | 4.3 | 5.2 | 6.3 | pF |
| $R_{par}$ | parasitic resistance | allowed resistance between adjacent pads | | 20 | - | - | MΩ |
| **Pad RESET** | | | | | | | |
| $f_o$ | output frequency | | | - | 32 | - | Hz |
| $V_{O(dif)}$ | differential output voltage | $R_L$ = 1 MΩ; $C_L$ = 10 pF | [2] | 1.4 | - | - | V |
| $t_r$ | rise time | $R_L$ = 1 MΩ; $C_L$ = 10 pF | [2] | - | 1 | - | μs |
| $t_f$ | fall time | $R_L$ = 1 MΩ; $C_L$ = 10 pF | [2] | - | 1 | - | μs |
| $I_{i(AV)}$ | average input current | pad RESET connected to $V_{DD}$ or $V_{SS}$ | | - | 10 | 20 | nA |

[1]   P1 + ... + P4 + N1 + N2 (see Section 7.2).

[2]   $R_L$ and $C_L$ are a load resistor and load capacitor, externally connected to pad RESET.

# 10. OTP programming characteristics

**Table 12.   Specifications for OTP programming**
*See Figure 7, Figure 8 and Figure 12.*

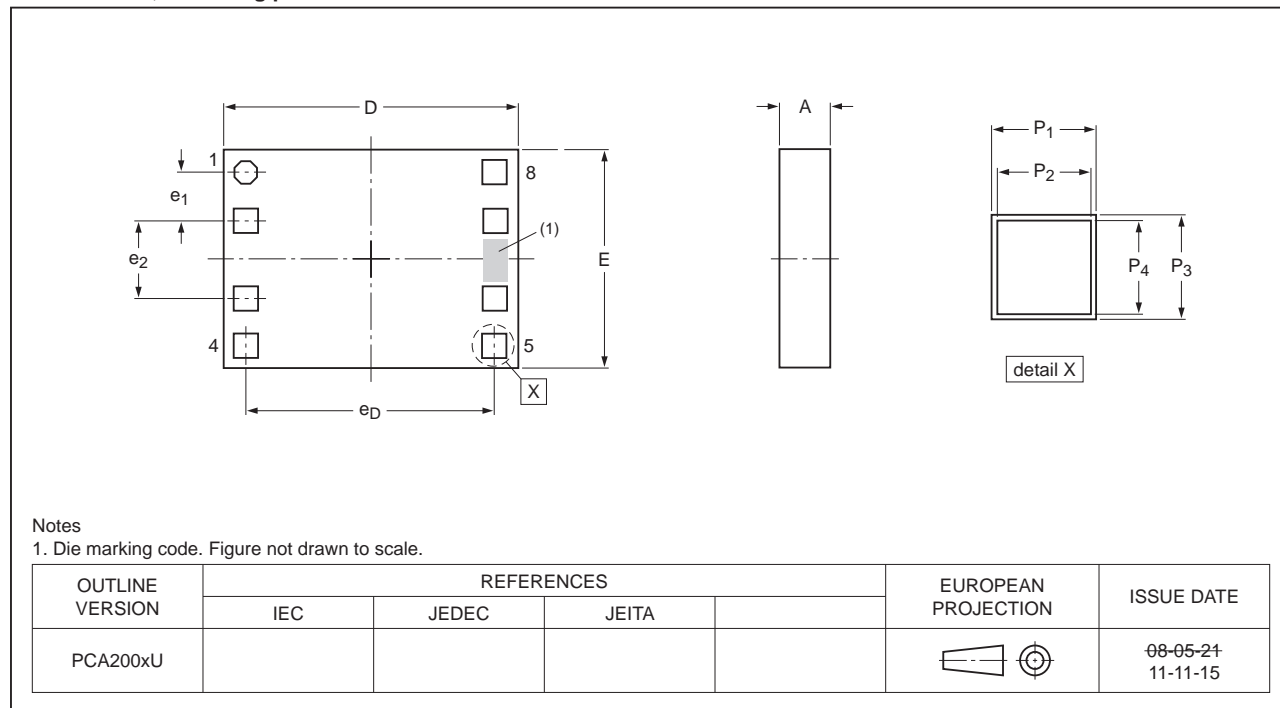| Symbol | Parameter[1] | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | during programming procedure | 1.5 | - | 3.0 | V |
| $V_{P(prog)(start)}$ | programming supply voltage (start) | | 6.6 | - | 6.8 | V |
| $V_{P(prog)(stop)}$ | programming supply voltage (stop) | | 6.2 | - | 6.4 | V |
| $V_{P(mod)}$ | supply voltage modulation | for entering instructions, referred to $V_{DD}$ | 320 | 350 | 380 | mV |
| $V_{prestore}$ | prestore voltage | for prestore pulse | 6.2 | - | 6.4 | V |
| $V_{store}$ | store voltage | for writing to the OTP cells | 9.9 | 10.0 | 10.1 | V |
| $I_{store}$ | store current | for writing to the OTP cells | - | - | 10 | mA |
| $t_{p(start)}$ | start pulse width | | 8 | 10 | 12 | ms |
| $t_{p(stop)}$ | pulse width of stop pulse | | 0.05 | - | 0.5 | ms |
| $t_{mod}$ | modulation pulse width | | 25 | 30 | 40 | µs |
| $t_{w(prestore)}$ | prestore pulse width | | 0.05 | - | 0.5 | ms |
| $t_{w(store)}$ | store pulse width | for writing to the OTP cells | 95 | 100 | 110 | ms |
| $t_0$ | time 0 | waiting time after start pulse | 20 | - | 30 | ms |
| $t_1$ | time 1 | pulse distance for incrementing the state counter | 0.6 | 0.7 | 0.8 | ms |
| $t_2$ | time 2 | pulse distance for clocking the data register with data = logic 0 | 1.6 | 1.7 | 1.8 | ms |
| $t_3$ | time 3 | pulse distance for clocking the data register with data = logic 1 | 2.6 | 2.7 | 2.8 | ms |
| $t_4$ | time 4 | waiting time for writing to OTP cells | 0.1 | 0.2 | 0.3 | ms |
| SR | slew rate | for modulation of the supply voltage | 0.5 | - | 5.0 | V/µs |
| $R_{mod}$ | modulation resistance | supply current modulation read-out resistor | 18 | 30 | 45 | kΩ |

[1]   Program each word once only.

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## 11. Bare die outline



**Wire bond die; 8 bonding pads** **PCA200xU**

Notes
1. Die marking code. Figure not drawn to scale.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| PCA200xU | | | | | | ~~08-05-21~~ 11-11-15 |

**Fig 13.   Bare die outline of PCA2003U (for dimensions see Table 13, for pin location see Table 14)**

**Table 13.    Dimensions of PCA2003U**
*Original dimensions are in mm.*

| Unit (mm) | A | D | E | $e_1$ | $e_2$ | $e_D$ | $P_1$ | $P_2$ | $P_3$ | $P_4$ |
|---|---|---|---|---|---|---|---|---|---|---|
| max | 0.22 | - | - | - | - | - | 0.099 | 0.089 | 0.099 | 0.089 |
| nom | 0.20 | 1.16 | 0.86 | 0.17 | 0.32 | 0.96 | 0.096 | 0.086 | 0.096 | 0.086 |
| min | 0.18 | - | - | - | - | - | 0.093 | 0.083 | 0.093 | 0.083 |

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**Table 14.** **Bonding pad description**

| Symbol | Pin | X[1] | Y[1] | Type | Description |
|---|---|---|---|---|---|
| $V_{SS}$[2] | 1 | −480 | +330 | supply | ground |
| i.c.[3] | 2 | −480 | +160 | - | internally connected |
| OSCIN | 3 | −480 | −160 | input | oscillator input |
| OSCOUT | 4 | −480 | −330 | output | oscillator output |
| $V_{DD}$ | 5 | +480 | −330 | supply | supply voltage |
| MOT1 | 6 | +480 | −160 | output | motor 1 output |
| MOT2 | 7 | +480 | +160 | output | motor 2 output |
| RESET | 8 | +480 | +330 | input | reset input |

[1]   All coordinates are referenced, in $\mu$m, to the center of the die (see Figure 13).

[2]   The substrate (rear side of the chip) is connected to $V_{SS}$. Therefore the die pad must be either floating or connected to $V_{SS}$.

[3]   Pad i.c. is used for factory tests; in normal operation it should be left open-circuit, and it has an internal pull-down resistance to $V_{SS}$.

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## 12. Abbreviations

**Table 15. Abbreviations**

| Acronym | Description |
|---------|-------------|
| CMOS | Complementary Metal Oxide Semiconductor |
| HBM | Human Body Model |
| LSB | Least Significant Bit |
| MM | Machine Model |
| MSB | Most Significant Bit |
| OTP | One Time Programmable |

## 13. References

[1] **AN10706 —** Handling bare die

[2] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[3] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[4] **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[5] **JESD22-A115 —** Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)

[6] **JESD78 —** IC Latch-Up Test

[7] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[8] **NX3-00092 —** NXP store and transport requirements

## 14. Revision history

**Table 16. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-------------|--------------|-------------------|---------------|------------|
| PCA2003 v.5 | 20190501 | Product data sheet | - | PCA2003 v.4 |
| Modifications: | • Added PCA2003U/10AC/1Z | | | |
| PCA2003 v.4 | 20111125 | Product data sheet | - | PCA2003_3 |
| Modifications: | • Added die marking information | | | |
| PCA2003_3 | 20100507 | Product data sheet | - | PCA2003_2 |
| PCA2003_2 | 20090721 | Product data sheet | - | PCA2003_1 |
| PCA2003_1 | 20081215 | Product data sheet | - | - |

## 15. Legal information

### 15.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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**Product data sheet**

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# 17. Contents

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