ISL8210M

10A High Efficiency Step-Down Power Module

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The ISL8210M power module is a single channel, synchronous step-down, non-isolated complete power supply featuring the proprietary Renesas R4™ Technology. The module supports a wide 4.5V to 16.5V input voltage range and a wide 0.5V to 5V output range capable of delivering up to 10A of continuous current and is optimized for high power density. Integrated LDOs provide module bias voltage, allowing for single supply operation.

The proprietary Renesas R4 control scheme has extremely fast transient performance, accurately regulated frequency control, and all internal compensation. An efficiency enhancing PFM mode greatly improves light-load efficiency. The ISL8210M allows for easy R4 loop optimization, resulting in fast transient performance across a wide range of applications, including all ceramic output filters.

The power module integrates all power and most passive components and requires only a few external components to operate. A set of optional external resistors provides very flexible configuration options (such as frequency, V_{OUT}, and AV gain). The ISL8210M also features remote voltage sensing and completely eliminates any potential difference between remote and local grounds, improving regulation and protection accuracy. A programmable soft-start reduces the inrush current from the input supply. A precision enable input and power-good (PGOOD) flag are available to coordinate the start-up of the ISL8210M with other voltage rails, which is especially useful for power sequencing. Excellent efficiency and low thermal resistance permit full power operation without heatsinks.

Input Undervoltage Lockout (UVLO), over-temperature, overcurrent, output overvoltage, and output prebias start-up protections ensure safe operations under abnormal operating conditions.

The ISL8210M is available in a compact RoHS compliant thermally-enhanced 12mmx11mmx5.3mm HDA package.

Applications

- Servers, telecom, storage, and datacom
- Industrial/ATE and networking equipment
- Graphics cards
- General purpose power for ASIC, FPGA, DSP, and memory

Features

- R4 Technology
  - Linear control loop for optimal transient response
  - Variable frequency and duty cycle control during load transient for fastest possible response
  - Inherent voltage feed-forward for wide range input
- Input voltage range: 4.5V to 16.5V
- Output voltage range: 0.5V to 5V
- ±1.5% load and line regulation with remote sense
- Supports all ceramic solutions
- Integrated LDOs for single input rail solution
- 256 output voltage levels with a configuration pin
- Seven switching frequency options from 300kHz to 1MHz
- PFM operation option for improved light-load efficiency
- Start-up into precharged load
- Power-good monitor for soft-start and fault detection
- Comprehensive fault protection for high system reliability
  - Over-temperature protection
  - Output overcurrent and short-circuit protection
  - Output overvoltage and undervoltage protection
  - Open remote sense protection
  - Input UVLO and power sequence as well as fault reset
- Thermally enhanced 12mmx11mmx5.3mm HDA package

Related Literature

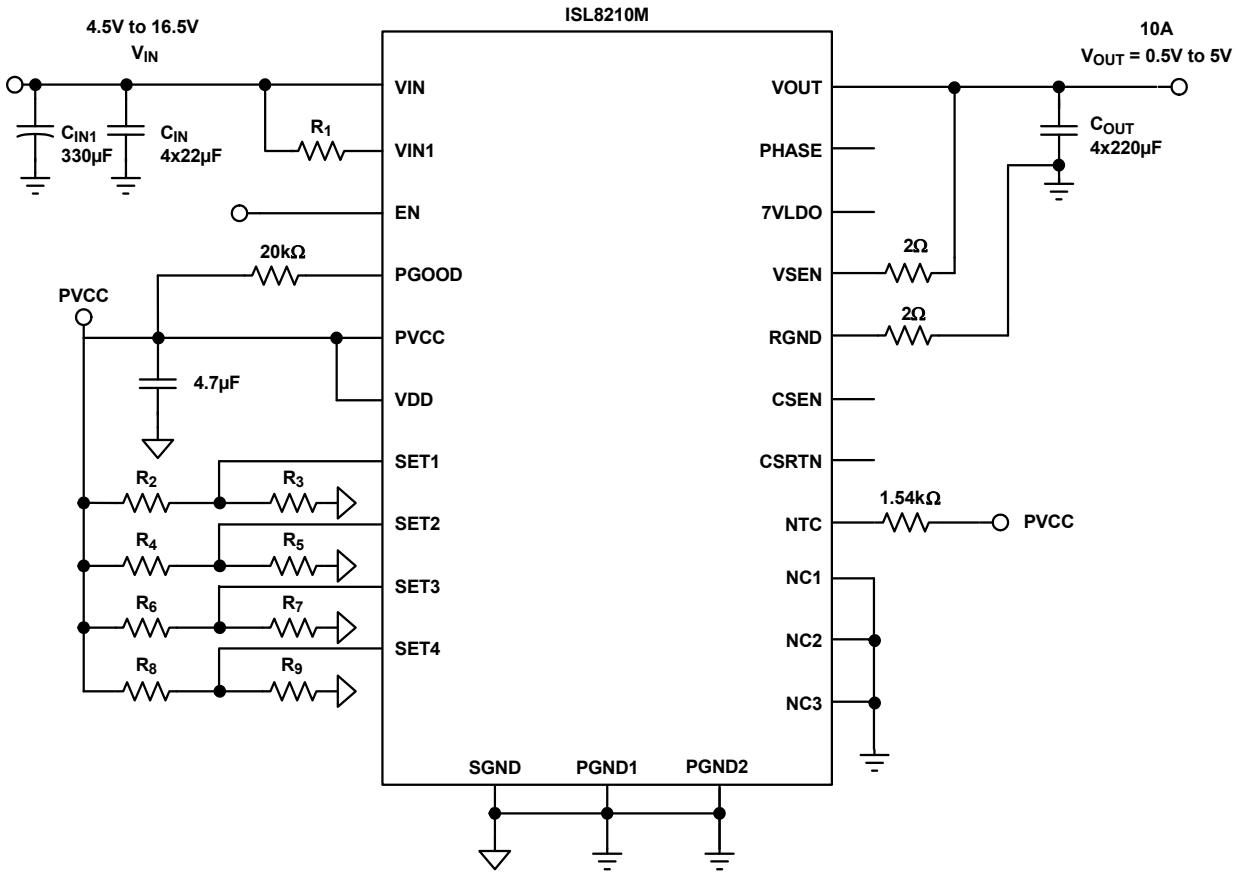
For a full list of related documents, visit our website:

- ISL8210M device page

Contents

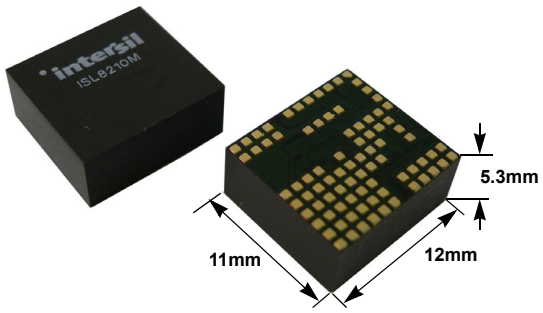
1. Overview

1.1 Typical Application Circuit



- For V_{OUT} = 3. 3V, minimum V_{IN} is 5.5V; for V_{OUT}= 5V, minimum V_{IN} is 8V.
- R_1: see Table 2 on page 7.
- R_2 and R_3: to set output voltage, see Table 4 on page 21 for typical V_{OUT}.
- R_4 and R_5: to set PFM/PWM mode and temperature compensation, see Table 5 on page 22.
- R_6 and R_7: to set f_{SW}, AV gain, OCP hiccup/latch off, and ultrasonic PWM enable, see Table 6 on page 23.
- R_8 and R_9: to set soft start, RR impedance, and AV gain multiplier (1x or 2x), see Table 7 on page 23.
- R_2 to R_9, see Table 2 for typical output voltage selections.

Figure 1. Typical Application Circuit 5V Input Applications



1.2 Block Diagram

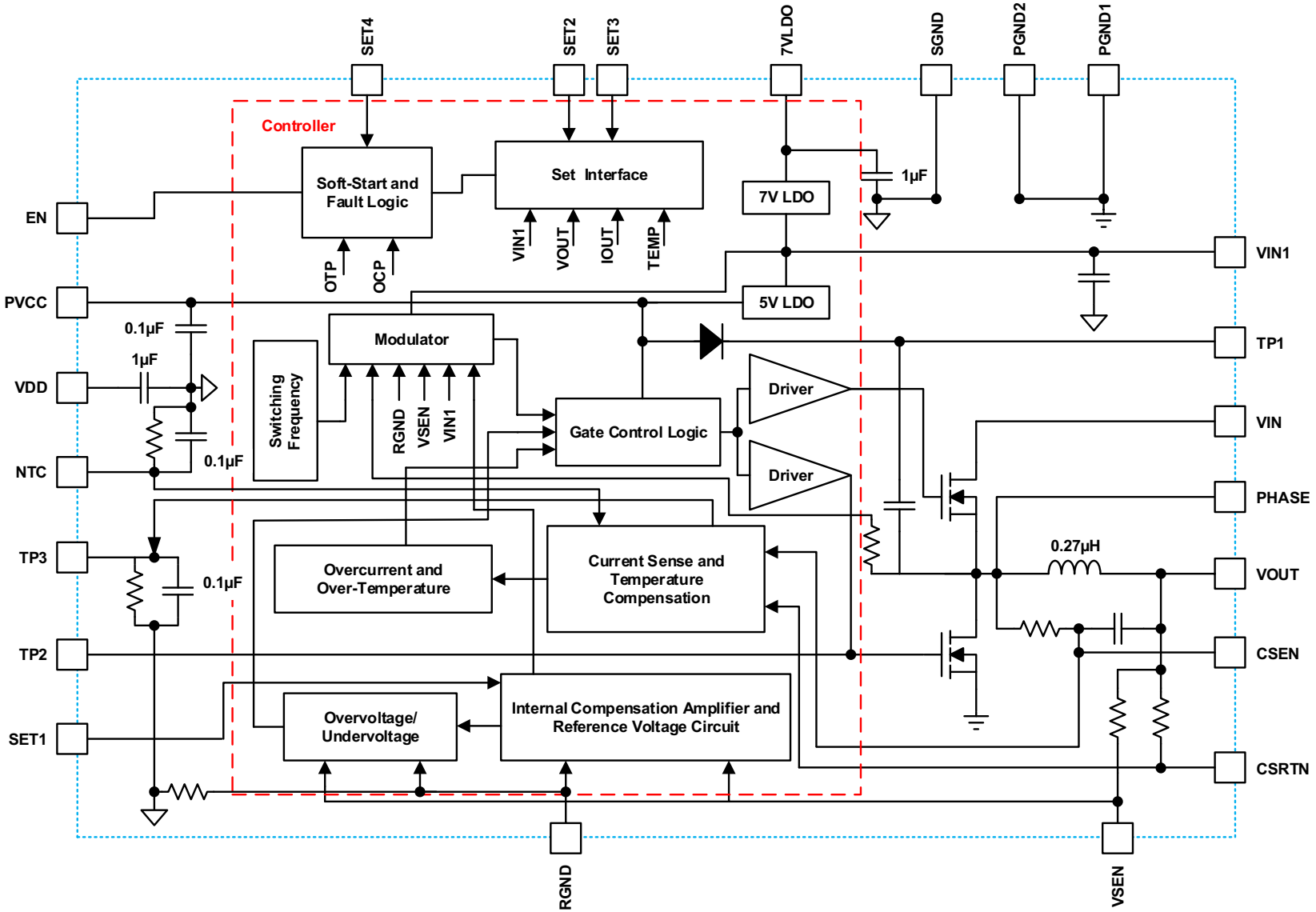


Figure 2. Block Diagram

1.3 Ordering Information

Part Number (Notes 2, 3)	Part Marking	Temp Range (°C)	Tape and Reel (Units) (Note 1)	Package (RoHS Compliant)	Pkg. Dwg. #
ISL8210MFRZ	ISL8210M	-40 to +125	-	83 Ld 12x11 HDA Module	Y83.12x11
ISL8210MFRZ-T	ISL8210M	-40 to +125	720	83 Ld 12x11 HDA Module	Y83.12x11
ISL8210MFRZ-T1	ISL8210M	-40 to +125	100	83 Ld 12x11 HDA Module	Y83.12x11
ISL8210MEVAL1Z	Evaluation Board				

Notes:

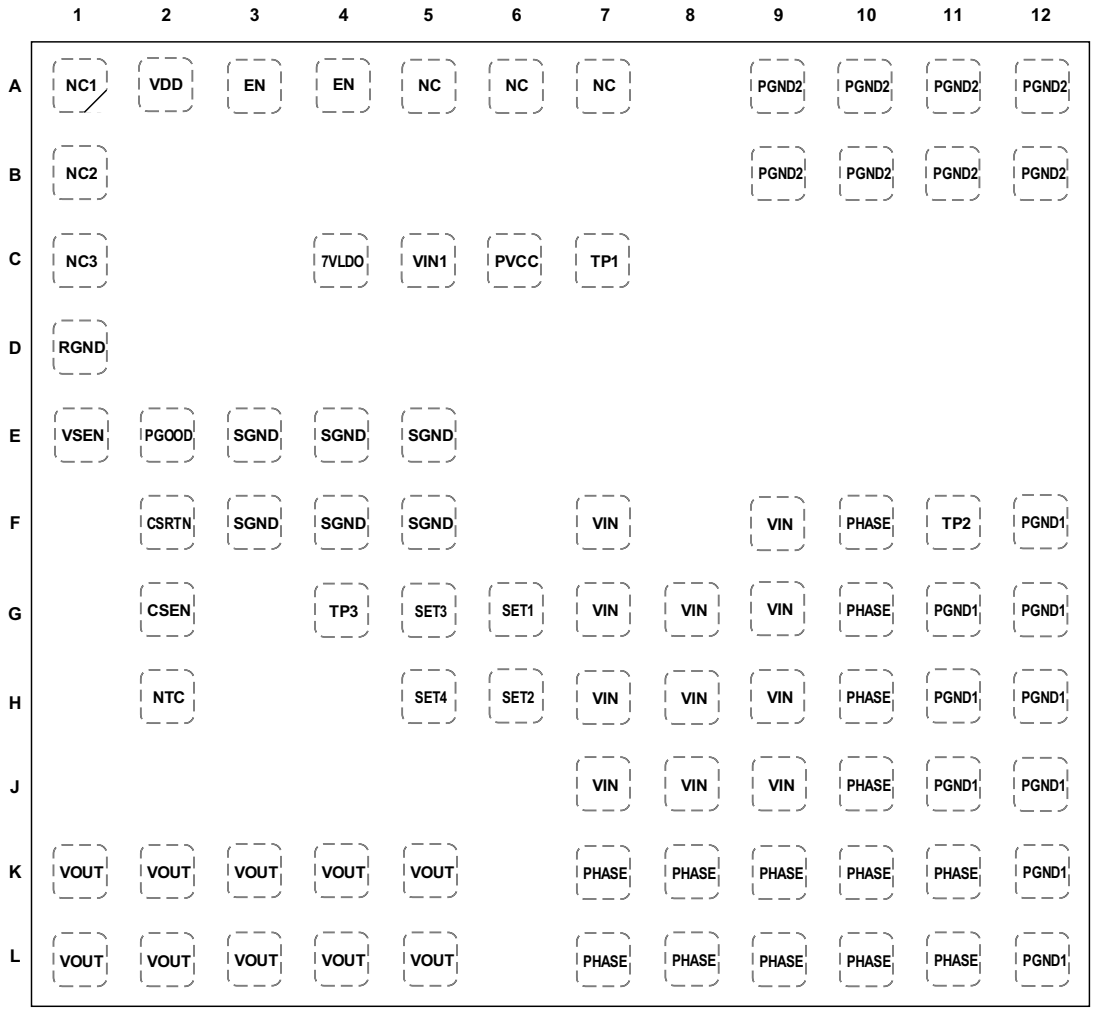
1. See TB347 for details about reel specifications.
2. These plastic packaged products are RoHS compliant by EU exemption 7C-I and employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish which is compatible with both SnPb and Pb-free soldering operations. RoHS compliant products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL8210M device page. For more information about MSL, see TB363.

Table 1. Key Differences Between Family of Parts

Parameters	ISL8282M	ISL8280M	ISL8212M	ISL8210M
Load Current (A)	15	10	15	10
Minimum V_{IN} (V)	4.5	4.5	4.5	4.5
Maximum V_{IN} (V)	16.5	16.5	16.5	16.5
Minimum V_{OUT} (V)	0.5	0.5	0.5	0.5
Maximum V_{OUT} (V)	5	5	5	5
Peak efficiency (%)	95.2	95.2	95.2	95.2
POR	Yes	Yes	Yes	Yes
Minimum Switching Frequency (kHz)	255	255	255	255
Maximum Switching Frequency (kHz)	1130	1130	1130	1130
Control Type	R4	R4	R4	R4
Sync Capability	No	No	No	No
Load Sharing	No	No	No	No
PMBus	Yes	Yes	No	No

1.4 Pin Configuration

83 Ld 12x11 HDA
Top View



1.5 Functional Pin Descriptions

Pin Number	Symbol	Description
A5, A6, A7	NC	No connection pads. The pads dissipate the inductor heat and provide good thermal performance. Do not connect to any other circuits.
A9, A10, A11, A12, B9, B10, B11, B12	PGND2	Power ground. The pads are connected to the source of the low-side MOSFET inside the module and remove heat from the module.
F7, F9, G7, G8, G9, H7, H8, H9, J7, J8, J9	VIN	Power input. Connect the pads directly to an input rail in the range of 4.5V to 16.5V. Connect the input ceramic capacitors between VIN and PGND1 as close as possible to the module.
F10, G10, H10, J10, K7, K8, K9, K10, K11, L7, L8, L9, L10, L11	PHASE	Phase node connection. The pads are connected to the source of high-side MOSFET, the drain of low-side MOSFET, output filter inductor, and return path for the UGATE high-side MOSFET driver.
F12, G11, G12, H11, H12, J11, J12, K12, L12	PGND1	Power ground. The pads are the sources of the lower MOSFET inside the module and should be connected to the (-) terminals of the external input capacitors and output capacitors.
K1, K2, K3, K4, K5, L1, L2, L3, L4, L5	VOUT	Regulated power module output. Apply the output load between VOUT and PGND1.

Pin Number	Symbol	Description
A1	NC1	Connected to power ground.
A2	VDD	Logic bias supply. Connect this pin externally to the PVCC rail.
A3, A4	EN	Precision enable input. Pulling EN above the rising threshold voltage initiates the soft-start sequence. Pulling EN below the failing threshold voltage suspends module operation.
B1	NC2	Connected to power ground.
C1	NC3	Connected to power ground.
C4	7V LDO	7V LDO used to bias the current sensing amplifier.
C5	VIN1	Input voltage pin for the R4 loop (5V) and LDO (7V). Place a high quality low ESR ceramic capacitor (1.0µF, X7R) in close proximity to the pin.
C6	PVCC	Output of the 5V LDO that biases internal control circuits and MOSFET drivers of the ISL8210M. Place a high quality low ESR capacitor (4.7µFX7R) in close proximity to this pin.
C7	TP1	Test pad, leave this pin open.
D1	RGND	Monitors the negative rail of the module output. Connect to ground at the point of regulation.
E1	VSEN	Monitors the positive rail of the module output. Connect to the point of regulation.
E2	PGOOD	Open-drain indicator output. The PGOOD signal is asserted when the output voltage is within ±12.5% of the nominal set output voltage and deasserted when the output voltage is outside of the stated range or the EN pin is pulled low.
E3, E4, E5, F3, F4, F5	SGND	Signal ground pads. The small-signal ground is common to all control circuitry and all voltage levels are measured with respect to this pin. Tie SGND to a solid low noise GND plane.
F2	CSRTN	This pin monitors the negative flow of output current for overcurrent protection and telemetry.
F11	TP2	Test pad, leave this pin open.
G2	CSEN	Monitors the positive flow of output current for overcurrent protection
G4	TP3	Test pad, leave this pin open.
G5	SET3	Programming pin for ultrasonic PFM operation, fault behavior, switching frequency, and R4 (AV) control loop gain.
G6	SET1	Programming pin for output voltage.
H2	NTC	Input pin for the temperature measurement. An NTC thermistor and a decoupling capacitor inside the module are connected between this pin and SGND. Connect this pin through a resistor (1.54kΩ) to a VDD pad externally. The voltage at this pin is inversely proportional to the module temperature.
H5	SET4	Programming pin for modulator (R4) RR impedance and output slew rate during Soft-Start (SS). It also sets the AV gain multiplier to 1x or 2x and determines the AV gain on SET3.
H6	SET2	Programming pin for PWM/PFM mode and temperature compensation.

Table 2. ISL8210M Design Guide Matrix of Typical Applications

V_{OUT} (V)	V_{IN} (V)	Frequency (kHz)	AV Gain	RR (Ω)	TCOMP (°C)	R_1 (Ω)
0.5	5	400	49	200k	5	0
	10					
	12					
	15					
0.6	5	400	49	200k	5	0
	10					
	12					
	15					

Table 2. ISL8210M Design Guide Matrix of Typical Applications (Continued)

V_{OUT} (V)	V_{IN} (V)	Frequency (kHz)	AV Gain	RR (Ω)	TCOMP (°C)	R_1 (Ω)
0.75	5	400	49	200k	5	0
	10					
	12					
	15					
0.9	5	400	49	200k	5	0
	10					
	12					
	15					
1	5	400	49	200k	5	0
	10					
	12					
	15					
1.2	5	400	26	200k	5	0
	10					
	12					
	15					
1.5	5	500	26	200k	5	0
	10					
	12					
	15					
1.8	5	500	26	200k	5	0
	10					
	12					
	15					
2.5	5	600	26	200k	5	0
	10					
	12					
	15					
3.3	5.5	700	26	200k	5	0
	10					
	12					
	15					121 (Note 4)
5	8	850	26	200k	5	0
	10					
	12					121 (Note 4)
	15					

Note:
4. A 121Ω resistor is needed only when OCP behavior is set to Retry.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
VDD, PVCC, VSEN	-0.3	7	V
Module Input Voltage, VIN	-0.3	20	V
Module Input Voltage, VIN1	-0.3	20	V
7VLDO	-0.3	7.75	V
BOOT Voltage ($V_{BOOT-GND}$)	-0.3	30	V
BOOT to PHASE Voltage ($V_{BOOT-PHASE}$) (DC)	-0.3	7	V
BOOT to PHASE Voltage ($V_{BOOT-PHASE}$) (<10ns)	-0.3	9	V
PHASE Voltage	-0.3	25	V
PHASE Voltage (<20ns Pulse Width, 10µJ)	-9	25	V
All Other Pins	-0.3 to GND	V_{DD} + 0.3	V
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per JS-001-2017)	2		kV
Charged Device Model (Tested per JS-002-2014)	750		V
Machine Model (Tested per JESD22-A115C)	200		V
Latch-Up (Tested per JESD78E; Class 2, Level A)	100 at +125°C		mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
83 Ld HDA Module (Notes 5, 6)	16.8	5.6

Notes:

5. θ_{JA} is measured in free air with the module mounted on a 6-layer thermal test board 3x3 inches in size with significant coverage of 2oz Cu on all layers, with numerous vias.
6. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Junction Temperature Range	-55	+150	°C
Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	See Figure 48 on page 38		

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Junction Temperature Range	-40	+125	°C
Application Input Voltage, V_{IN}, Figure 1	4.5	16.5	V
Output Voltage, V_{OUT}, Figure 1	0.5	5	V
Output Current, I_{OUT}, Figure 1	0	10	A

2.4 Electrical Specifications

All typical specifications T_A = +25°C, V_{IN} = 12, V_{IN1} =12V, V_{OUT} = 1V. **Boldface limits apply across the junction temperature range, -40°C to +125°C (Note 7), unless otherwise stated.**

Parameter	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
V_{IN} Supply						
Input Voltage Range	V_{IN}		**4.5**		**16.5**	V
V_{IN} Supply Current						
Input Supply Current in PFM mode Operation	$I_{S(PFM)}$	PFM mode, V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 0A		0.2		mA
Input Supply Current in PWM mode Operation	$I_{S(PWM)}$	PWM mode, V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 0A		35		mA
Input Supply Current in PWM mode Operation	$I_{S(PWM)}$	PWM mode, V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 10A		0.98		A
Input Supply Current in Shutdown	$I_{S(SHUTDOWN)}$	Shutdown		0.05		µA
V_{IN1} Supply Current						
Shutdown Current	I_{VIN1Q}	EN = 0, PGOOD is floating, V_{IN1} = 12V		14.5	**17**	mA
Operating Current	I_{VIN1OP}	PGOOD is floating, V_{IN1} = 12V		19	**25**	mA
V_{DD} and V_{IN} POR Threshold						
V_{DD}, PVCC Rising POR Threshold Voltage				4.2	**4.35**	V
V_{DD}, PVCC Falling POR Threshold Voltage			**3.8**	3.95	**4.15**	V
V_{IN}, 7VLDO Rising POR Threshold Voltage				4.2	**4.35**	V
V_{IN}, 7VLDO Falling POR Threshold Voltage			**3.8**	3.95	**4.15**	V
Output Regulation						
Output Continuous Current Range	I_{OUT}	(Note 9)	**0**		**10**	A
Output Voltage Range	V_{OUT_RANGE}		**0.5**		**5**	V
Output Voltage Set-Point Accuracy		0.5V ≤ V_{OUT} < 0.75V, Total variation with line, load, and temperature (-40°C ≤ T_J ≤ +125°C)	**-12.5**		**12.5**	mV
Output Voltage Set-Point Accuracy		0.75V ≤ V_{OUT} < 0.9V, Total variation with line, load, and temperature (-40°C ≤ T_J ≤ +125°C)	**-15**		**15**	mV
Output Voltage Set-Point Accuracy		0.9V ≤ V_{OUT} ≤ 5V, Total variation with line, load, and temperature (-40°C ≤ T_J ≤ +125°C)	**-1.5**		**1.5**	%
Line Regulation	$\Delta V_{OUT}/V_{OUT\_SET}$	V_{OUT} = 1V, V_{IN} from 4.5V to 16.5V, I_L = 0A	**-1.2**		**1.2**	%
		V_{OUT} = 1.8V, V_{IN} from 4.5V to 16.5V, I_L = 0A	**-1.2**		**1.2**	%
Load Regulation	$\Delta V_{OUT}/V_{OUT\_SET}$	From 0A to 10A, V_{IN} = 5V/12V, V_{OUT} = 1V	**-1.2**		**1.2**	%
		From 0A to 10A, V_{IN} = 5V/12V, V_{OUT} = 1.8V	**-1.2**		**1.2**	%
Output Ripple Voltage	$V_{OUT(AC)}$	V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 10A, 4x220µF ceramic capacitor		8		mV_{P-P}

All typical specifications T_A = +25°C, V_{IN} = 12, V_{IN1} =12V, V_{OUT} = 1V. **Boldface limits apply across the junction temperature range, -40°C to +125°C (Note 7), unless otherwise stated. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Dynamic Characteristics						
Voltage Change of Positive Load Step	V_{OUT_DP}	Current slew rate = 2.5A/µs, V_{IN} = 12V, 4x220µF ceramic capacitor V_{OUT} = 1V, I_{OUT} from 0A to 5A		10		mV
Voltage Change of Negative Load Step	V_{OUT_DN}	Current slew rate = 2.5A/µs, V_{IN} = 12V, 4x220µF ceramic capacitor V_{OUT} = 1V, I_{OUT} from 5A to 0A		10		mV
Enable Input						
EN High Threshold Voltage	V_{ENTHR}		**0.81**	0.84	**0.87**	V
EN Low Threshold Voltage	V_{ENTHF}		**0.71**	0.76	**0.81**	V
Channel Frequency						
300kHz Configuration		PWM Mode	**255**	300	**340**	kHz
400kHz Configuration			**340**	400	**455**	kHz
500kHz Configuration			**425**	500	**565**	kHz
600kHzConfiguration			**510**	600	**680**	kHz
700kHz Configuration			**600**	700	**790**	kHz
850kHz Configuration			**720**	850	**960**	kHz
1000kHz Configuration			**855**	1000	**1130**	kHz
Soft-Start						
SS Rate = 0.157mV/µs			**0.125**	0.157	**0.18**	mV/µs
SS Rate = 0.315mV/µs			**0.25**	0.315	**0.37**	mV/µs
SS Rate = 0.625mV/µs			**0.52**	0.625	**0.7**	mV/µs
SS Rate = 1.25mV/µs			**1**	1.25	**1.4**	mV/µs
SS Rate = 2.5mV/µs			**2**	2.5	**2.8**	mV/µs
SS Rate = 5mV/µs			**4.1**	5	**5.6**	mV/µs
SS Rate = 10mV/µs			**8.4**	10	**10.9**	mV/µs
Soft-Start Delay from Enable High		Excluding 5.5ms POR timeout	**140**	200	**260**	µs
Remote Sense						
Bias Current of VSEN and RGND Pins					**250**	µA
Maximum Differential Input Voltage			**5.8**			V
Power-Good						
PGOOD Pull-Down Impedance	R_{PG}	PGOOD = 5mA sink		10	**50**	Ω
PGOOD Leakage Current	I_{PG}	PGOOD = 5V			**1**	µA
LDOs						
5V LDO Regulation		V_{IN} = 12V, 5VLDO load = 50mA	**4.8**	5	**5.15**	V
5V LDO Regulation		V_{IN} = 4.75V, 5VLDO load = 50mA	**4.15**			V
5V LDO Maximmum Load Capability			**100**			mA
7V LDO Regulation		7VLDO 250µA load	**7.15**	7.4	**7.5**	V
7V Dropout		V_{IN} = 4.75V, 7VLDO 250µA load	**4.3**			V
7V LDO Current Capability		Not recommended for external use	**2**			mA

All typical specifications T_A = +25°C, V_{IN} = 12, V_{IN1} =12V, V_{OUT} = 1V. **Boldface limits apply across the junction temperature range, -40°C to +125°C (Note 7), unless otherwise stated. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Current Sense						
OCP	I_{OCP}	V_{IN} = 12V, V_{OUT} = 1V	**10**	14.3		A
Maximum Common-Mode Input Voltage		7VLDO = 7.4V	**5.7**			V
		V_{DD} = PVCC = 7VLDO = 4.5V	**2.8**			V
Fault Protection						
UVP Threshold Voltage		0.5V ≤ V_{OUT} ≤ 0.7V	**67**	74	**88**	%V_{OUT}
		0.7V ≤ V_{OUT} <1V	**68**	74	**85**	%V_{OUT}
		1V ≤ V_{OUT} <1.5V	**68**	74	**82**	%V_{OUT}
		1.5V ≤ V_{OUT} ≤ 5V	**68**	74	**80**	%V_{OUT}
Start-Up OVP Threshold Voltage		0V ≤ V_{OUT} ≤ 1.08V	**1.1**	1.15	**1.25**	V
		1.08V < V_{OUT} ≤ 1.55V	**1.58**	1.65	**1.75**	V
		1.55V < V_{OUT} ≤ 1.85V	**1.88**	1.95	**2.05**	V
		1.85V < V_{OUT} ≤ 2.08V	**2.09**	2.15	**2.25**	V
		2.08V < V_{OUT} ≤ 2.53V	**2.56**	2.65	**2.75**	V
		2.53V < V_{OUT} ≤ 3.33V	**3.36**	3.45	**3.6**	V
		3.33V < V_{OUT} ≤ 5V	**5.52**	5.65	**5.85**	V
Start-Up OVP Hysteresis				100		mV
OVP Rising Threshold Voltage	V_{OVRTH}	0.5V ≤ V_{OUT} ≤ 0.7V	**111**	120	**136**	% V_{OUT}
		0.7V ≤ V_{OUT} <1V	**113**	120	**132**	%V_{OUT}
		1V ≤ V_{OUT} <1.5V	**114**	120	**128**	%V_{OUT}
		1.5V ≤ V_{OUT} ≤ 5V	**114**	120	**127**	%V_{OUT}
OVP Falling Threshold Voltage	V_{OVFTH}	0.5V ≤ V_{OUT} ≤ 0.7V	**93**	100	**115**	% V_{OUT}
		0.7V ≤ V_{OUT} <1V	**95**	100	**111**	%V_{OUT}
		1V ≤ V_{OUT} <1.5V	**96**	100	**109**	%V_{OUT}
		1.5V ≤ V_{OUT} ≤ 5V	**96**	100	**108**	%V_{OUT}
Over-Temperature Shutdown Threshold		22.31%V_{DD} (~+136°C)	**20**	22.31	**26**	% V_{DD}
Over-Temperature Shutdown Reset Threshold		27.79%V_{DD} (~+122°C)	**25**	27.79	**30**	% V_{DD}

Notes:

7. The ISL8210M is tested under pulsed-load conditions such that $T_J \approx T_A$.
8. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
9. See output current derating curves for different V_{OUT} and T_A located in "Derating Curves" on page 18.
10. See Table 2 on page 7.

3. Typical Performance Curves

3.1 Efficiency Performance

Operating conditions: T_A=25°C, no air flow, PWM mode. Typical values are used unless otherwise noted. The efficiency curves were measured on the evaluation board. For the test conditions, see Table 2 on page 7.

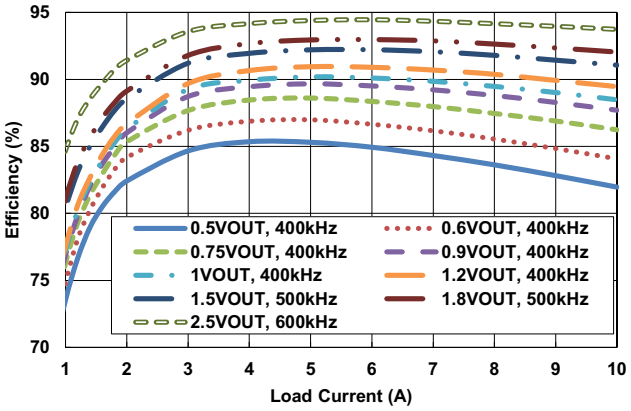


Figure 3. Efficiency vs Load Current at $5V_{IN}$ (PWM)

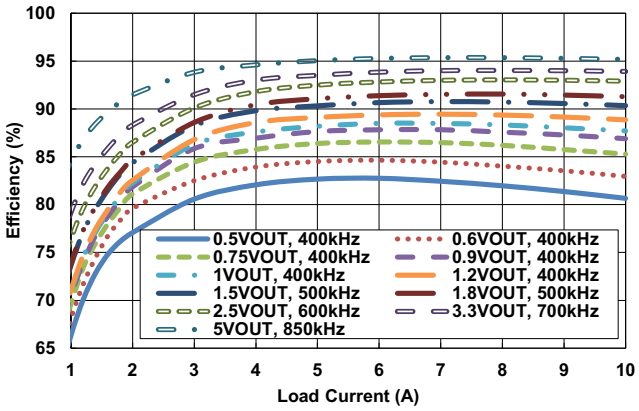


Figure 4. Efficiency vs Load Current at $8V_{IN}$ (PWM)

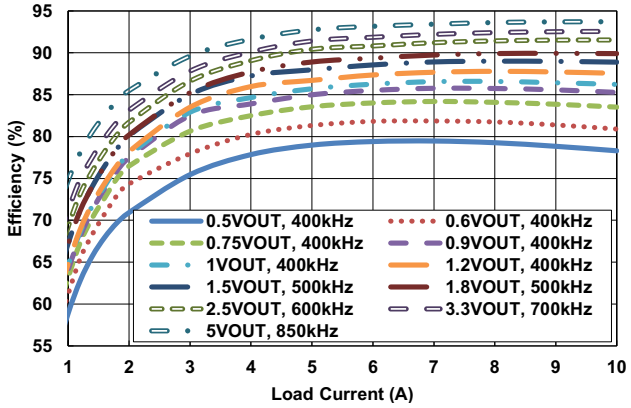


Figure 5. Efficiency vs Load Current at $12V_{IN}$ (PWM)

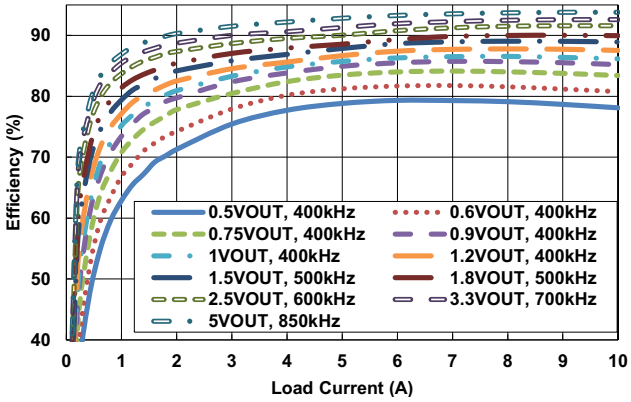


Figure 6. Efficiency vs Load Current at $12V_{IN}$ (PFM)

3.2 Output Voltage Ripple

Operating conditions: T_A = +25°C, no air flow, PWM mode, C_{OUT} = 4 x 220µF Ceramic, RR = 200kΩ. Typical values are used unless otherwise noted. For the test conditions, see Table 2 on page 7.

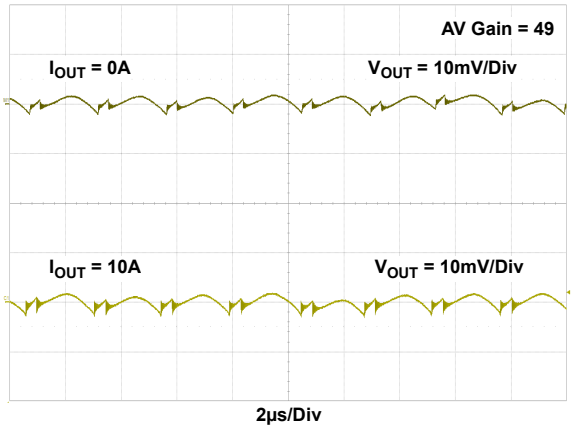


Figure 7. Output Ripple at $5V_{IN}$ and $0.75V_{OUT}$, 400kHz

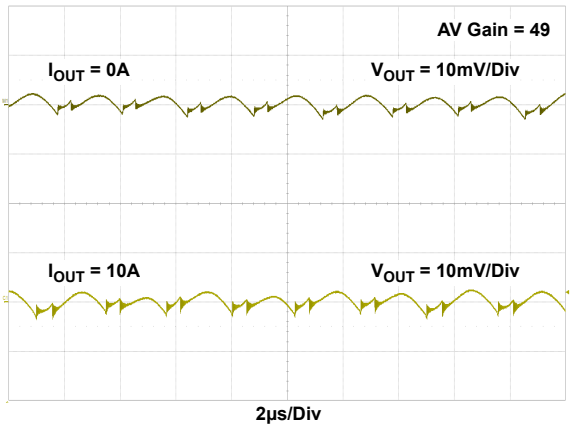


Figure 8. Output Ripple at $5V_{IN}$ and $1V_{OUT}$, 400kHz

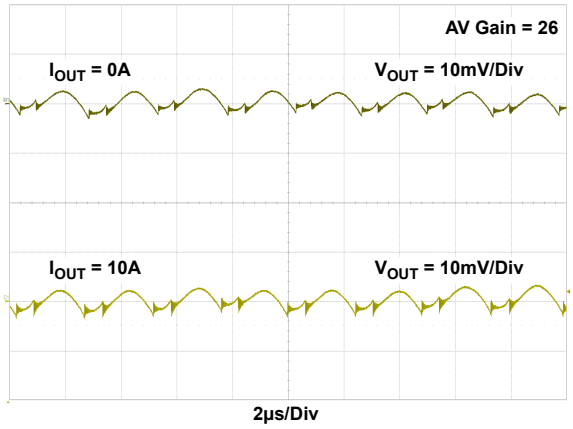


Figure 9. Output Ripple at $5V_{IN}$ and $1.2V_{OUT}$, 400kHz

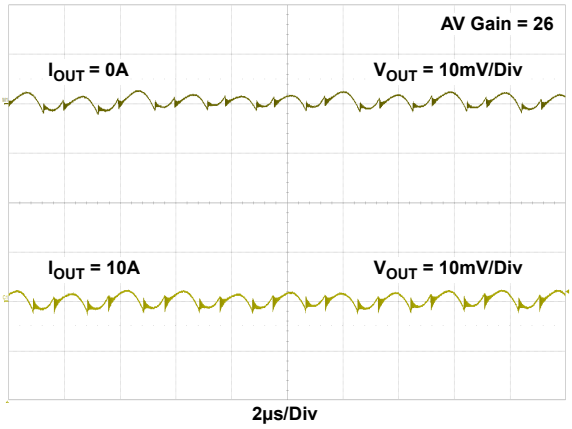


Figure 10. Output Ripple at $5V_{IN}$ and $1.8V_{OUT}$, 500kHz

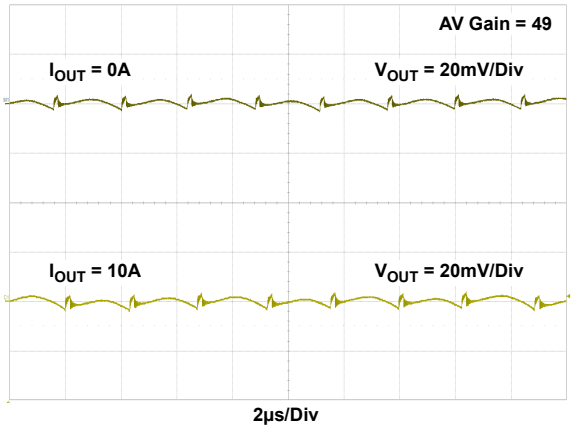


Figure 11. Output Ripple at $12V_{IN}$ and $0.75V_{OUT}$, 400kHz

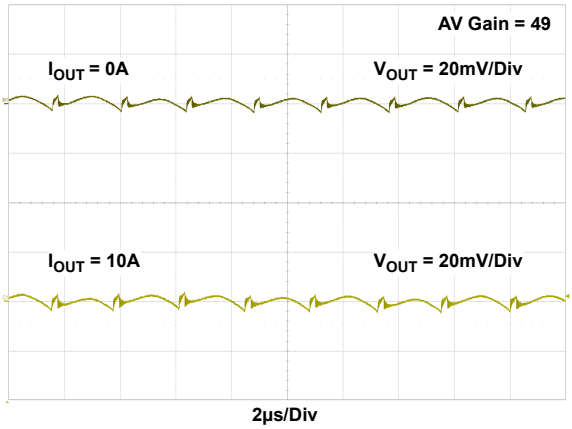


Figure 12. Output Ripple at $12V_{IN}$ and $1V_{OUT}$, 400kHz

Operating conditions: T_A = +25°C, no air flow, PWM mode, C_{OUT} = 4 x 220µF Ceramic, RR = 200kΩ. Typical values are used unless otherwise noted. For the test conditions, see Table 2 on page 7. **(Continued)**

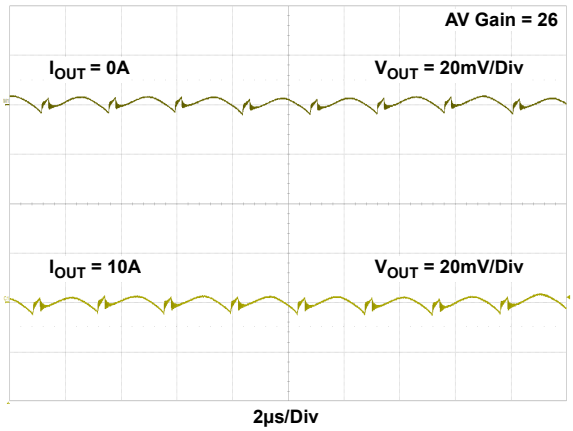


Figure 13. Output Ripple at $12V_{IN}$ and $1.2V_{OUT}$, 400kHz

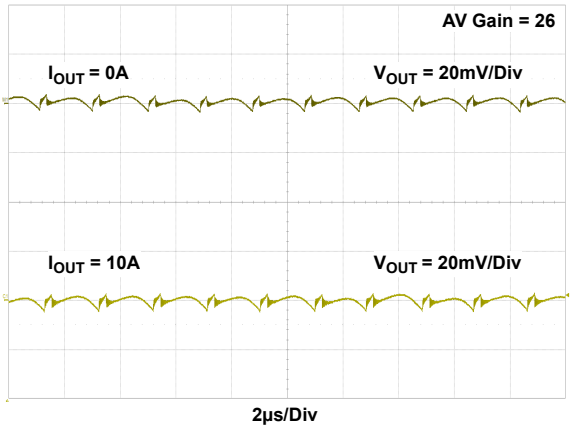


Figure 14. Output Ripple at $12V_{IN}$ and $1.5V_{OUT}$, 500kHz

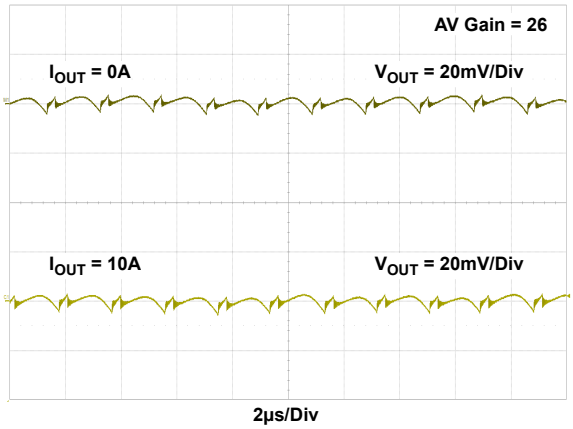


Figure 15. Output Ripple at $12V_{IN}$ and $1.8V_{OUT}$, 500kHz

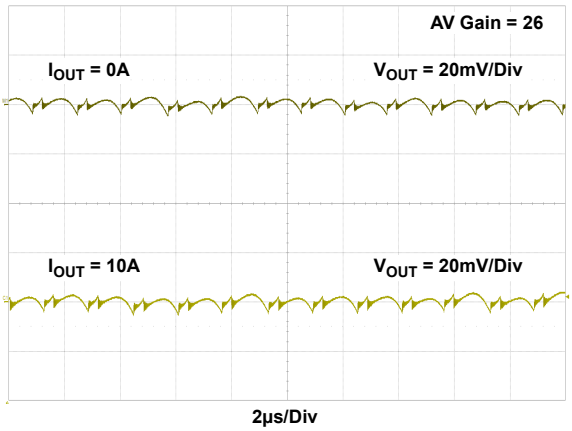


Figure 16. Output Ripple at $12V_{IN}$ and $2.5V_{OUT}$, 600kHz

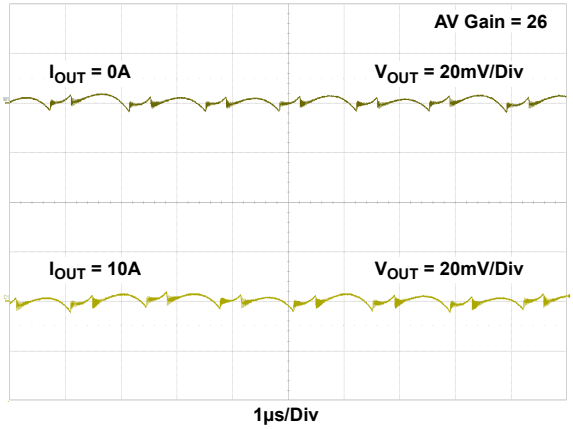


Figure 17. Output Ripple at $12V_{IN}$ and $3.3V_{OUT}$, 700kHz

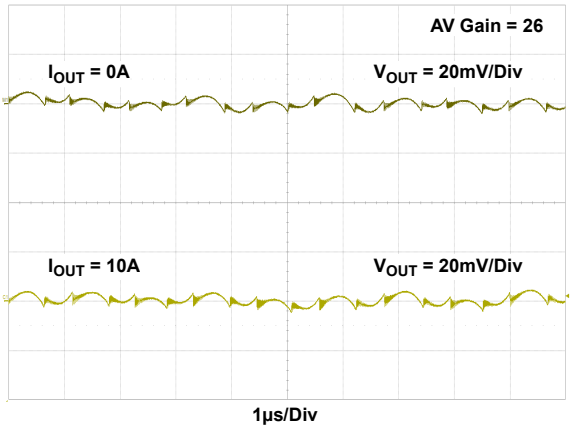


Figure 18. Output Ripple at $12V_{IN}$ and $5V_{OUT}$, 850kHz

3.3 Load Transient Response Performance

Operating conditions: T_A = +25°C, no air flow, V_{IN} = 12V, PWM mode, C_{OUT} = 4 x 220µF Ceramic, 0A to 5A step load at 5A/µs slew rate, RR = 200kΩ. Typical values are used unless otherwise noted. For the test conditions, see Table 2 on page 7.

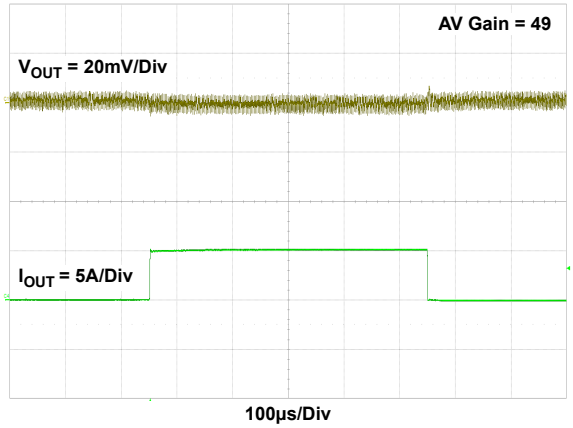


Figure 19. Load Transient Response at 0.75V_{OUT}, 400kHz

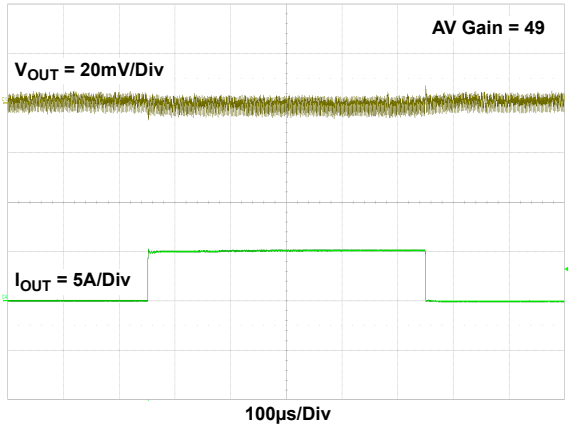


Figure 20. Load Transient Response at 1V_{OUT}, 400kHz

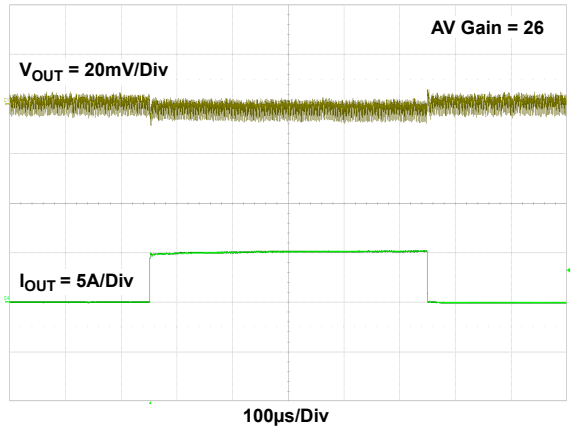


Figure 21. Load Transient Response at 1.8V_{OUT}, 500kHz

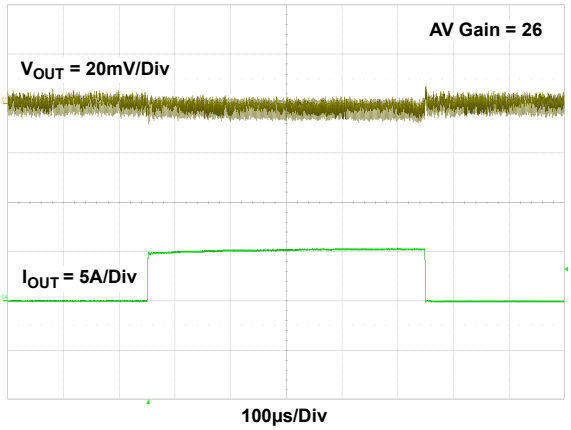


Figure 22. Load Transient Response at 2.5V_{OUT}, 600kHz

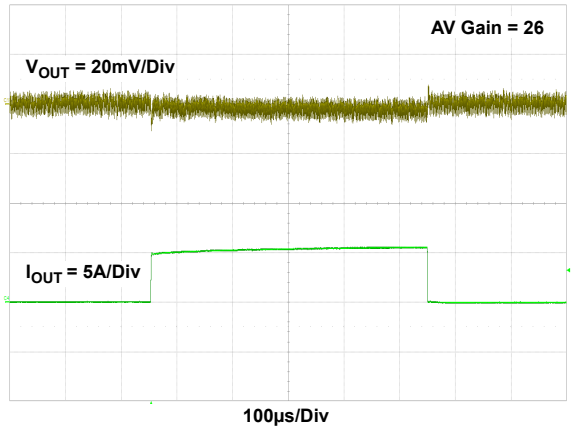


Figure 23. Load Transient Response at 3.3V_{OUT}, 700kHz

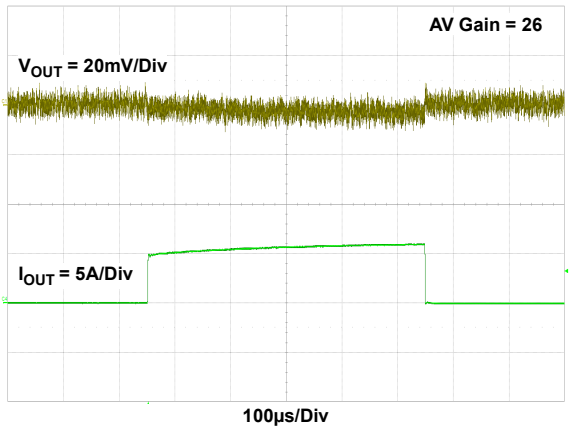


Figure 24. Load Transient Response at 5V_{OUT}, 850kHz

3.4 Start-Up and Shutdown

Operating conditions: T_A = +25°C, no air flow, V_{IN} = 12V, V_{OUT} = 1V, PWM mode. Typical values are used unless otherwise noted. For the test conditions, see Table 2 on page 7.

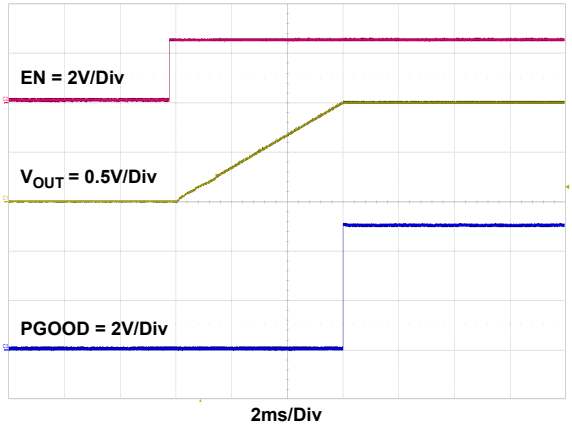


Figure 25. Start-Up Waveform, I_{OUT} = 0A

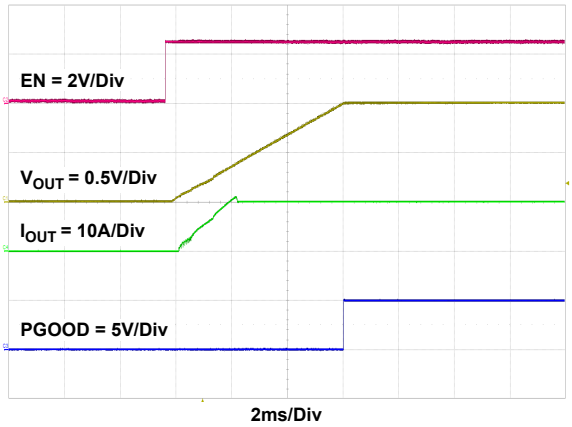


Figure 26. Start-Up Waveform, I_{OUT} = 10A

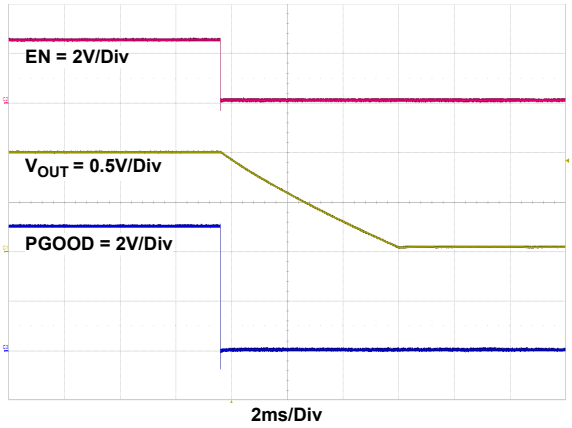


Figure 27. Shutdown Waveform, I_{OUT} = 0A

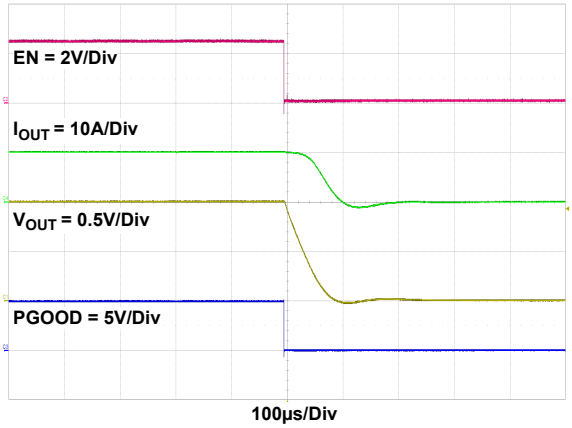


Figure 28. Shutdown Waveform, I_{OUT} = 10A

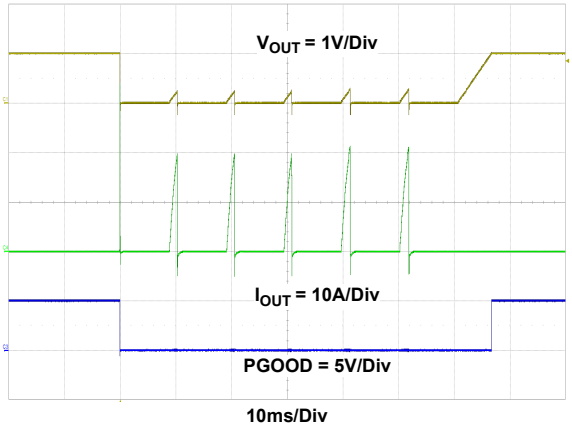


Figure 29. OCP Response; Output Short-Circuited from No Load to Ground and Released, I_{OUT} = 0A

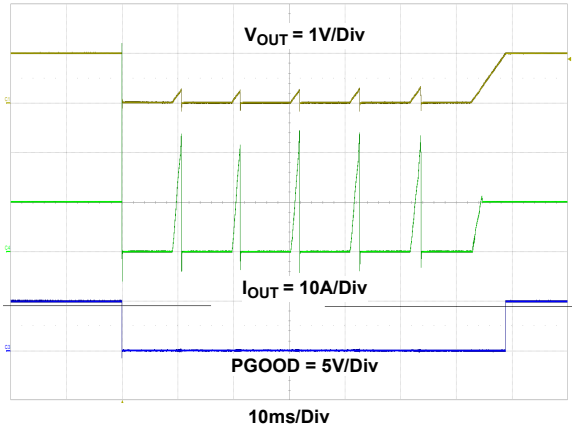


Figure 30. OCP Response; Output Short-Circuited from No Load to Ground and Released, I_{OUT} = 10A

3.5 Derating Curves

Operating conditions: V_{IN} = 12V, PWM mode. All of the following curves were plotted at T_J = +125°C. The derating curves were measured on the evaluation board. For the test conditions, see Table 2 on page 7.

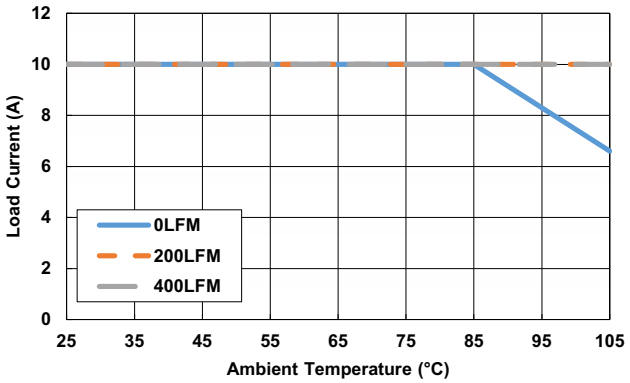


Figure 31. 0.6V_{OUT}

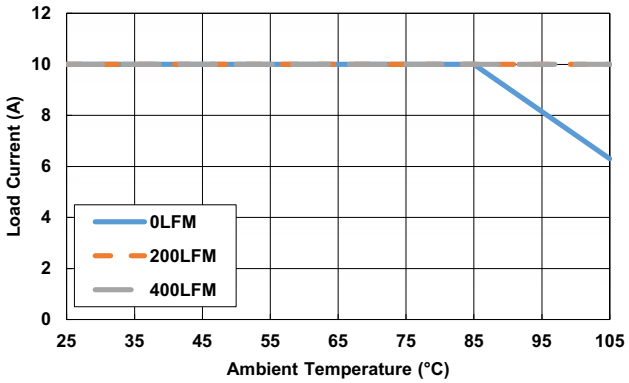


Figure 32. 0.8V_{OUT}

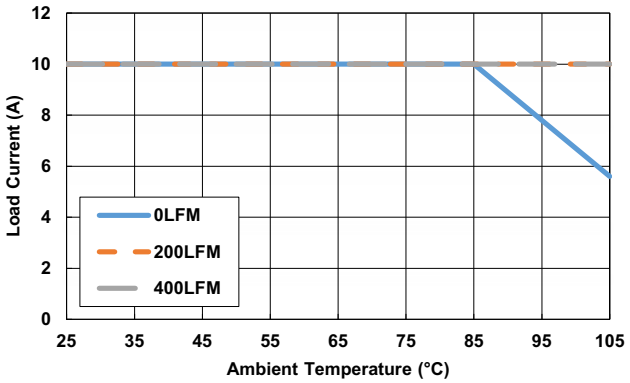


Figure 33. 1V_{OUT}

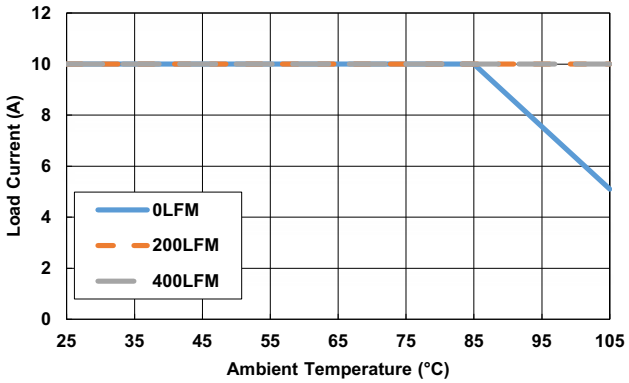


Figure 34. 1.2V_{OUT}

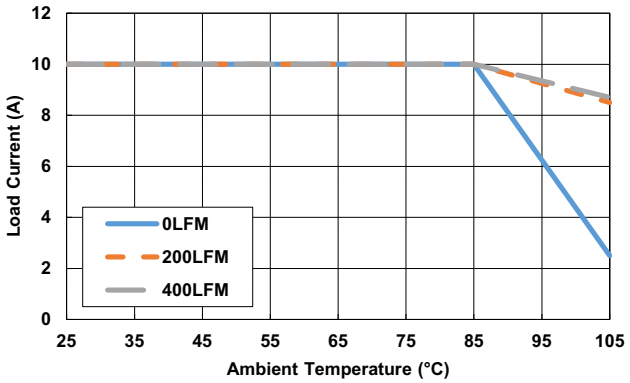


Figure 35. 1.8V_{OUT}

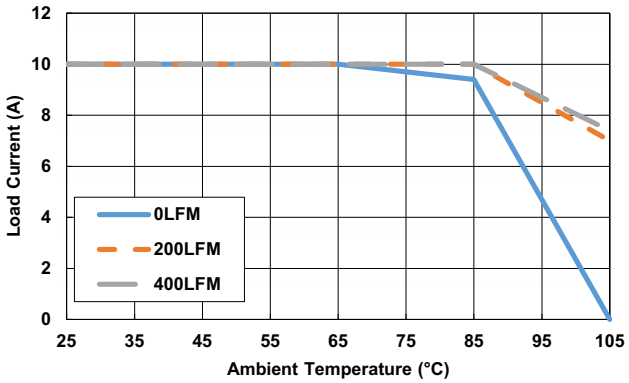


Figure 36. 2.5V_{OUT}

Operating conditions: V_{IN} = 12V, PWM mode. All of the following curves were plotted at T_J = +125°C. The derating curves were measured on the evaluation board. For the test conditions, see Table 2 on page 7. **(Continued)**

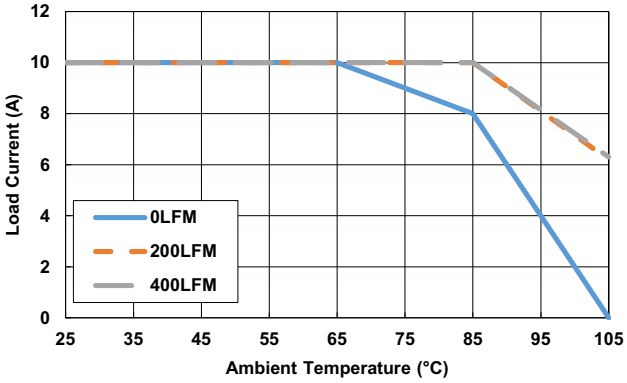


Figure 37. 3.3V_{OUT}

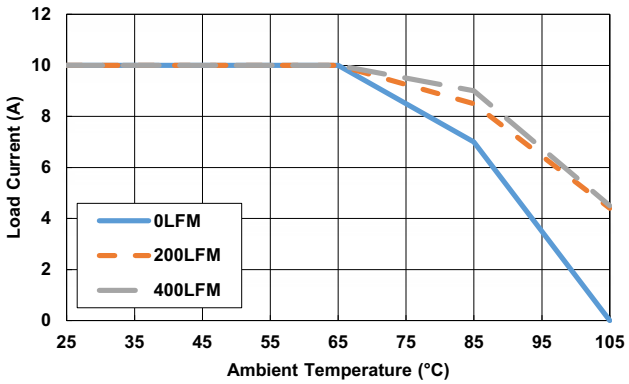


Figure 38. 5V_{OUT}

4. Operating the ISL8210M

The following sections describe the operation of the ISL8210M.

4.1 Configuring Internal Bias and LDO

The ISL8210M has four bias pins: VIN1, 7VLDO, PVCC, and VDD. The PVCC and 7VLDO voltage rails are 5V LDO and 7V LDO supplied by VIN1, respectively, while the VDD pin needs to connect to the PVCC rail externally to be biased.

4.2 Enabling and Disabling the ISL8210M

The module is enabled until the 7VLDO, PVCC, VDD, VIN1, and EN pins increase above their respective rising threshold voltages and the typical 5.5ms timeout expires (worst case = 6.5ms). The module becomes disabled when the 7VLDO, PVCC, VDD, VIN, or EN pins drop below their respective falling POR threshold voltages.

The precision threshold EN pin allows you to set a precision input UVLO level with an external resistor divider, as shown in Figure 39.

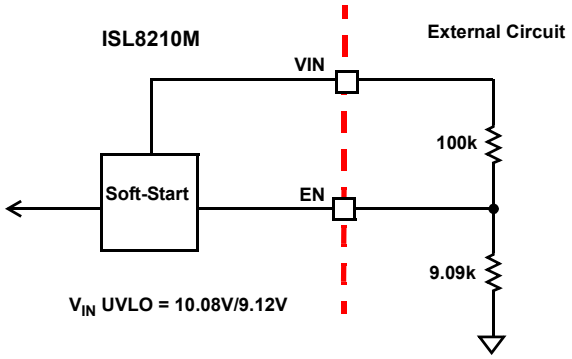


Figure 39. Input UVP Configuration

For 5V input applications or wide range input applications, the EN pin can directly connect to VDD, as shown in Figure 40. If an external enable control signal is available and is an open-drain signal, a pull-up impedance (100k or higher) can be used to connect the pull-up resistor to VDD.

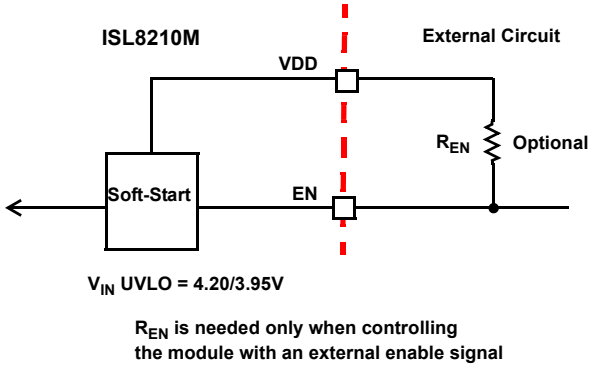


Figure 40. 5V Input or Wide Range Input Configuration

4.3 Setting Up Resistors

The ISL8210M offers four setting up pins (SETx) to customize module specifications. The details of these pins are summarized in Table 3, followed by a detailed description of resistor reader operation.

Table 3. Definition of SET Pins

Pin	Name	Description
SET1	Output Voltage	Sets the 256 output voltage options: 0V, 0.5V to 5V (see Table 9).
SET2	PWM/PFM	Enables PFM mode or forced PWM.
	Temperature Compensation	Adjusts NTC temperature compensation: OFF, +5°C, +15°C, +30°C.
	Not Used	Not used
SET3	uSPFM	Ultrasonic (25kHz clamp) PFM enable.
	Fault Behavior	OCP fault behavior: Latch, Infinite 9ms retry.
	FSW	Sets/Selects the switching frequency (f_{SW}).
	AV Gain	Sets/Selects the error amplifier gain (AV).
SET4	RAMP_RATE	Sets/Selects the soft-start ramp rate.
	RR	Sets/Selects the RR impedance for R4 loop.
	AVMLTI	Sets/Selects the AV Gain Multiplier (1x or 2x).
	Not Used	Not used

Renesas has developed a high resolution ADC using a patented technique with a simple 1%, 100ppm/K or better temperature coefficient resistor divider. Renesas recommends using the same type of resistor in the design so the ADC has similar change over temperature. The divider is compared to the internal divider off VDD and SGND nodes and therefore must refer to the VDD and SGND pins, not through any RC decoupling network.

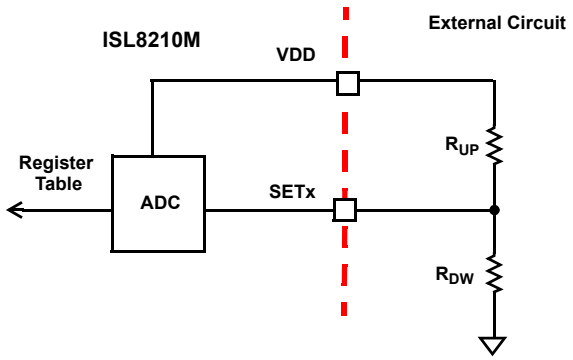


Figure 41. Simplified Resistor Divider ADC

Tables 4 through 7 show the R_{UP} and R_{DW} values of each pin for a specific system design with some tie-high and tie-low options that enable easy programming with reduced resistors. You can use the tie-high and tie-low options to validate the module operation during In-Circuit Test (ICT) for 0V output voltage option. Note that more options are described in the ISL8210MEVAL1Z User's Manual and the case of 10kΩ tie-high or tie-low is equivalent to 0Ω tie-high or tie-low.

Table 4. SET1 Resistor Reader Example

R_{UP} (kΩ)	R_{DW} (kΩ)	V_{OUT} (V)
499	Open	0.000
49.9	12.4	0.5

Table 4. SET1 Resistor Reader Example (Continued)

R_{UP} (kΩ)	R_{DW} (kΩ)	V_{OUT} (V)
23.2	17.8	0.594
22.1	18.2	0.602
97.6	27.4	0.742
90.9	28.7	0.75
82.5	28.7	0.758
Open	34.8	0.898
34	57.6	0.906
133	46.4	0.992
Open	75	1.000
118	49.9	1.008
45.3	150	1.195
Open	499	1.203
221	113	1.492
21.5	Open	1.500
200	121	1.508
34.8	Open	1.797
196	226	1.805
576	200	2.492
52.3	Open	2.500
499	210	2.508
105	Open	3.297
249	357	3.305
374	422	4.992
147	Open	5.000
348	464	5.008

Table 5. SET2 Resistor Reader Example

R_{UP} (kΩ)	R_{DW} (kΩ)	PWM/PFM	Temp Comp
Open	0	Enabled	30
Open	21.5	Enabled	15
Open	34.8	Enabled	5
Open	52.3	Enabled	OFF
Open	75	Disabled	30
Open	105	Disabled	15
Open	147	Disabled	5
Open	499	Disabled	OFF

Table 6. SET3 Resistor Reader Example

R_{UP} (kΩ)	R_{DW} (kΩ)	Ultrasonic PFM	OCP and Short-Circuit Behavior	f_{SW} (kHz)	AV Gain	
					1x	2x
25.5	16.5	Disabled	Retry	400	24.5	49
88.7	57.6	Disabled	Latch	400	24.5	49
374	243	Enabled	Latch	400	24.5	49
191	124	Enabled	Retry	400	24.5	49
23.2	17.8	Disabled	Retry	400	13	26
80.6	61.9	Disabled	Latch	400	13	26
340	261	Enabled	Latch	400	13	26
174	133	Enabled	Retry	400	13	26
16.9	24.3	Disabled	Retry	500	13	26
59	84.5	Disabled	Latch	500	13	26
249	357	Enabled	Latch	500	13	26
127	182	Enabled	Retry	500	13	26
13.3	39.2	Disabled	Retry	600	13	26
46.4	137	Disabled	Latch	600	13	26
196	576	Enabled	Latch	600	13	26
100	294	Enabled	Retry	600	13	26
76.8	29.4	Disabled	Retry	700	13	26
187	71.5	Disabled	Latch	700	13	26
715	274	Enabled	Latch	700	13	26
374	143	Enabled	Retry	700	13	26
49.9	38.3	Disabled	Retry	850	13	26
121	93.1	Disabled	Latch	850	13	26
464	357	Enabled	Latch	850	13	26
243	187	Enabled	Retry	850	13	26

Table 7. SET 4 Resistor Reader Example

R_{UP} (kΩ)	R_{DW} (kΩ)	SS Rate (mV/µs)	RR (kΩ)	AV MULTI
Open	0	1.25	200	1
Open	20	2.5	200	1
Open	34.8	5	200	1
Open	52.3	10	200	1
Open	105	0.157	200	1
Open	147	0.315	200	1
Open	499	0.625	200	1
31.6	14.7	1.25	200	2
68.1	31.6	2.5	200	2
110	51.1	5	200	2
165	76.8	10	200	2
332	154	0.157	200	2

Table 7. SET 4 Resistor Reader Example (Continued)

R_{UP} (kΩ)	R_{DW} (kΩ)	SS Rate (mV/µs)	RR (kΩ)	AV MULTI
464	215	0.315	200	2
634	294	0.625	200	2
0	Open	1.25	800	2
20	Open	2.5	800	2
34.8	Open	5	800	2
52.3	Open	10	800	2
105	Open	0.157	800	2
147	Open	0.315	800	2
499	Open	0.625	800	2

4.4 Soft-Starting

The ISL8210M begins the soft-start ramp after the following two conditions are met.

- 5.5ms (worst case = 6.5ms) time out after bias supply (VDD, PVCC, 7VLDO) above POR threshold
- A fixed 200µs delay after EN pin above its 0.84V threshold

The output voltage reaches the output voltage at a fixed slew rate set by the SET4 pin. The ramp time can be calculated based on Equation 1.

$$t_{ss} = \frac{V_{OUT}}{RAMP\_RATE}(\mu s) \quad \text{(EQ. 1)}$$

The ISL8210M supports precharged start-up. It initiates the first PWM pulse until the internal reference (DAC) reaches the pre-charged level at the RAMP_RATE programmed by SET4. When the precharged level is below V_{OUT}, the output walks up to the V_{OUT} at RAMP_RATE and releases PGOOD when soft-start finishes. When the precharged output is above V_{OUT} but below OVP, it walks down to V_{OUT} at RAMP_RATE and releases PGOOD. The ramp time is defined in Equation 2 on page 24, and is clearly longer than a normal start-up.

$$t_{D2} = \frac{V_{PRECHARGED}}{RAMP\_RATE} + \frac{V_{PRECHARGED} - V_{OUT}}{RAMP\_RATE}(\mu s) \quad \text{(EQ. 2)}$$

If the boot capacitor voltage is high enough, the ISL8210M is able to handle up to 5.5Vprecharged load. However, it is hard to ensure high boot voltage for all precharged loads. If the precharged load is above 2.5V and the precharged start-up time is long, the boot capacitor is discharged to "PVCC - V_{OUT} - V_D" by the high-side drive circuits' standby current. For a 4V precharged load, the boot capacitor can be discharged to less than 1V, which is insufficient to turn on the high-side MOSFET. In this case, Renesas recommends letting the output drop below 2.5V with an external bleed resistor before soft-start, or using a high RAMP_RATE to reduce the start-up time.

4.5 Output Voltage Programming

The SET1 pin is used for output voltage set up, which offers 256 options: 0V and 0.5V to 5.5V, as shown in Table 8. The most popular output voltage levels are summarized in Table 4 on page 21. 0V output voltage is considered "OFF"; the driver is in tri-state and the internal DAC sets to 0V.

Table 8. Output Voltage Set Up

V_{OUT} (V)	R_{UP} (kΩ)	R_{DW} (kΩ)
0	499	OPEN
0.5	49.9	12.4

Table 8. Output Voltage Set Up (Continued)

V_{OUT} (V)	R_{UP} (kΩ)	R_{DW} (kΩ)
0.508	45.3	12.7
0.516	42.2	13.3
0.523	38.3	13.3
0.531	35.7	13.7
0.539	34	14.3
0.547	31.6	14.7
0.555	29.4	15
0.562	28	15.4
0.57	26.7	16.2
0.578	25.5	16.5
0.586	24.3	17.4
0.594	23.2	17.8
0.602	22.1	18.2
0.609	21	19.1
0.617	20	19.6
0.625	19.6	20.5
0.633	18.7	21.5
0.641	18.2	22.6
0.648	17.4	23.2
0.656	16.9	24.3
0.664	16.5	26.1
0.672	15.8	26.7
0.68	15.4	28.7
0.688	15	30.1
0.695	14.7	32.4
0.703	14	34
0.711	13.7	36.5
0.719	13.3	39.2
0.727	13	43.2
0.734	107	26.7
0.742	97.6	27.4
0.75	90.9	28.7
0.758	82.5	28.7
0.766	76.8	29.4
0.773	71.5	30.1
0.781	68.1	31.6
0.789	63.4	32.4
0.797	OPEN	10
0.805	57.6	34.8
0.812	54.9	35.7
0.82	52.3	37.4

Table 8. Output Voltage Set Up (Continued)

V_{OUT} (V)	R_{UP} (kΩ)	R_{DW} (kΩ)
0.828	49.9	38.3
0.836	47.5	39.2
0.844	45.3	41.2
0.852	OPEN	21.5
0.859	42.2	44.2
0.867	40.2	45.3
0.875	39.2	48.7
0.883	37.4	49.9
0.891	36.5	52.3
0.898	OPEN	34.8
0.906	34	57.6
0.914	33.2	61.9
0.922	32.4	66.5
0.93	30.9	68.1
0.938	30.1	73.2
0.945	29.4	78.7
0.953	OPEN	52.3
0.961	28	93.1
0.969	174	43.2
0.977	158	44.2
0.984	147	46.4
0.992	133	46.4
1	OPEN	75
1.008	118	49.9
1.016	110	51.1
1.023	102	52.3
1.031	97.6	53.6
1.039	93.1	56.2
1.047	OPEN	105
1.055	84.5	60.4
1.062	80.6	61.9
1.07	76.8	63.4
1.078	73.2	66.5
1.086	69.8	68.1
1.094	68.1	71.5
1.102	OPEN	147
1.109	63.4	78.7
1.117	60.4	80.6
1.125	59	84.5
1.133	57.6	90.9
1.141	54.9	93.1

Table 8. Output Voltage Set Up (Continued)

V_{OUT} (V)	R_{UP} (kΩ)	R_{DW} (kΩ)
1.148	53.6	100
1.156	52.3	105
1.164	49.9	110
1.172	48.7	118
1.18	47.5	127
1.188	46.4	137
1.195	45.3	150
1.203	OPEN	499
1.211	237	66.5
1.219	221	69.8
1.227	200	69.8
1.234	187	71.5
1.242	178	75
1.25	165	76.8
1.258	154	78.7
1.266	147	80.6
1.273	140	84.5
1.281	133	86.6
1.289	127	90.9
1.297	121	93.1
1.305	115	95.3
1.312	110	100
1.32	105	102
1.328	102	107
1.336	97.6	110
1.344	95.3	118
1.352	10	OPEN
1.359	88.7	127
1.367	86.6	137
1.375	82.5	140
1.383	80.6	150
1.391	78.7	162
1.398	75	165
1.406	73.2	178
1.414	71.5	191
1.422	69.8	205
1.43	68.1	226
1.438	374	93.1
1.445	340	95.3
1.453	316	100
1.461	287	100

Table 8. Output Voltage Set Up (Continued)

V_{OUT} (V)	R_{UP} (kΩ)	R_{DW} (kΩ)
1.469	267	102
1.477	255	107
1.484	237	110
1.492	221	113
1.5	21.5	OPEN
1.508	200	121
1.516	191	124
1.523	182	130
1.531	174	133
1.539	165	137
1.547	158	143
1.555	150	147
1.562	147	154
1.57	140	158
1.578	137	169
1.586	130	174
1.594	127	182
1.602	124	196
1.609	118	200
1.617	115	215
1.625	113	232
1.633	110	243
1.641	105	255
1.648	102	274
1.656	100	294
1.664	97.6	324
1.672	523	130
1.68	475	133
1.688	442	140
1.695	402	140
1.703	374	143
1.711	357	150
1.719	332	154
1.727	309	158
1.734	294	162
1.742	280	169
1.75	267	174
1.758	255	182
1.766	243	187
1.773	232	191
1.781	221	200

Table 8. Output Voltage Set Up (Continued)

V_{OUT} (V)	R_{UP} (kΩ)	R_{DW} (kΩ)
1.789	210	205
1.797	34.8	OPEN
1.805	196	226
1.812	191	237
1.82	182	243
1.828	178	255
1.836	174	274
1.914	165	280
1.992	162	301
2.07	158	324
2.148	154	340
2.227	147	357
2.305	143	383
2.383	140	412
2.461	137	453
2.469	732	182
2.477	665	187
2.484	619	196
2.492	576	200
2.5	52.3	OPEN
2.508	499	210
2.516	464	215
2.523	432	221
2.602	412	226
2.68	392	237
2.758	374	243
2.836	357	255
2.914	340	261
2.992	324	267
3	75	OPEN
3.07	309	280
3.148	301	294
3.227	287	301
3.281	274	309
3.289	267	332
3.297	105	OPEN
3.305	249	357
3.312	243	383
3.32	232	392
3.328	226	422
3.406	221	453

Table 8. Output Voltage Set Up (Continued)

V_{OUT} (V)	R_{UP} (kΩ)	R_{DW} (kΩ)
3.484	215	475
3.562	205	499
3.641	200	536
3.719	196	576
3.797	191	634
3.875	1000	249
3.953	909	255
4.031	845	267
4.109	768	267
4.188	715	274
4.266	665	280
4.344	634	294
4.422	590	301
4.5	562	309
4.578	536	324
4.656	511	332
4.734	487	348
4.812	464	357
4.891	442	365
4.969	422	383
4.977	402	392
4.984	392	412
4.992	374	422
5	147	OPEN
5.008	348	464
5.016	340	487
5.023	324	511
5.031	316	536
5.109	309	576
5.188	301	604
5.266	287	634
5.344	280	681
5.422	274	732
5.492	267	787
5.5	261	866

As shown in Table 8, one step is 2^{-7} = 7.8125mV and some selections are higher than one step from adjacent codes. However, the resolution is ±7.8125mV around the popular voltage regulation points, as in Table 4 on page 21, for fine-tuning. For finer than 7.8125mV tuning, place a large ratio resistor divider on the VSEN pin between the output (V_{OUT}) and RGND for positive offset or VDD for negative offset, as shown in Figure 42 on page 31.

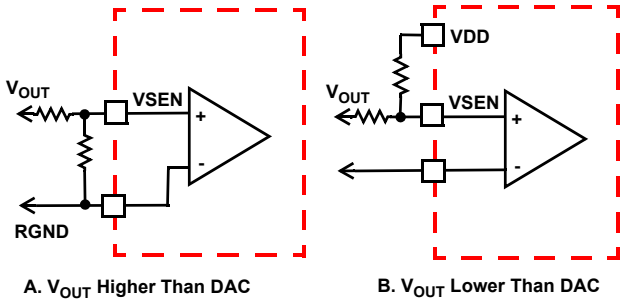


Figure 42. External Programmable Regulation

4.6 Thermal Monitoring and Compensation

The thermal monitoring block diagram is shown in Figure 43. Inside the module, a 10kΩ NTC resistor (P/N: NCP15XH103J03RC from Murata, β = 3380) is placed close to the power stage to sense the operational temperature, and a 1.54kΩ pull-up resistor, R_{TM}, forms the voltage dividers for the NTC pin. As the power stage temperature increases, the NTC resistance reduces, resulting in the reduced voltage at the NTC pin.

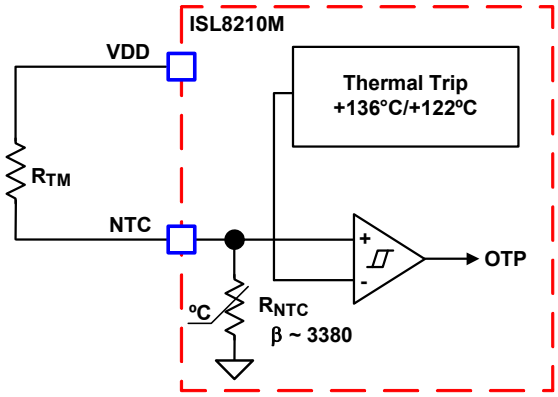


Figure 43. Block Diagram of Thermal Monitoring and Protection

Figure 44 on page 31 shows the TM voltage across the temperature. Renesas recommends using a 1.54kΩ resistor for accurate temperature compensation because the internal thermal digital code is based on it.

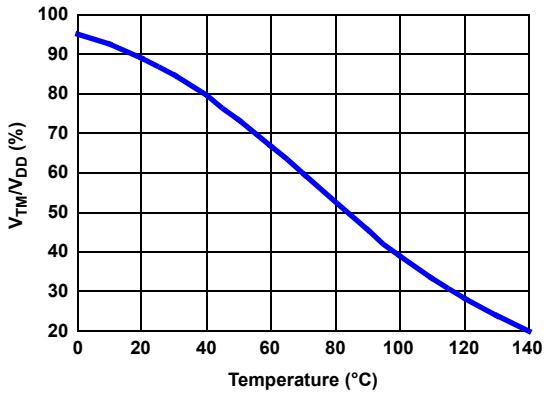


Figure 44. Ratio of TM Voltage to NTC Temperature with Recommended Parts

Because the voltage across the inductor DCR is sensed for the output current information, the sensed current has the same positive temperature coefficient as the inductor DCR, which is about +0.385%/°C. To obtain the correct current information, the ISL8210M uses the voltage at the NTC pin and TCOMP register to compensate the temperature impact on the sensed current. The block diagram of this function is shown in Figure 45.

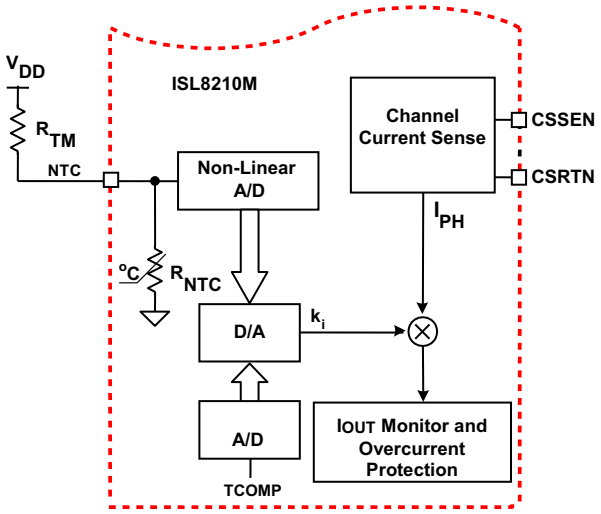


Figure 45. Block Diagram of Integrated Temperature Compensation

Based on the V_{DD} voltage, the ISL8210M converts the NTC pin voltage to a digital signal for temperature compensation. With the nonlinear A/D converter of the ISL8210M, the NTC digital signal is linearly proportional to the NTC temperature.

Because the NTC is not directly attached to the current sensing component, it inherits high thermal impedance between the NTC and the current sensing element. The TCOMP can be used to correct the temperature difference between NTC and the current sense component.

The ISL8210M multiplexes the TCOMP value with the NTC digital signal to obtain the adjustment gain to compensate the temperature impact on the sensed channel current. The compensated current signal is used for I_{OUT} and overcurrent protection functions. The four different TCOMP options that can be set by resistor dividers connected to the SET2 pin are:

- +5°C
- +15°C
- +30°C
- OFF

Renesas recommends using +5°C as the TCOMP.

4.7 Fault Protection

The ISL8210M provides high system reliability with many fault protections, as summarized in Table 9.

Table 9. Fault Protection Summary

Fault	Description	Fault Action
Input UVLO	VIN pin UVLO; or set by the EN pin with an external divider for higher level. See Figures 39 and 40.	Shut down and recover when V_{IN} > UVLO
Bias UVLO	VDD, PVCC, 7VLDO UVLO	Shut down and recover when Bias > UVLO
Start-Up OVP	Higher than V_{OUT}. See "Electrical Specifications" on page 10.	Latch OFF, reset by VDD or toggling EN pin
Output OVP	Rising = 116%; Falling = 100%	
Output UVP	74% of V_{OUT}, Latch OFF	
Short-Circuit and OCP Protection	Peak load current = 14.3A typical	Latch OFF (reset by VDD or toggling EN pin), or retry every 9ms
OTP	Rising = 22.31%V_{DD} (~+136°C) Falling = 27.79%V_{DD} (~+122°C)	Shut down above +136°C and recover when temperature drops below +122°C

Input UVLO and OTP faults respond to the current state with hysteresis, while output OVP and output UVP faults are latch events. Output OCP and output short-circuit faults can be latch or retry events depending on the SET3 setting. All fault latch events can be reset by VDD cycling or toggling the EN pin. The OCP retry event has a hiccup time of 9ms and the module can be recovered when the fault is removed.

4.7.1 Overvoltage Protection

The Overvoltage Protection (OVP) fault detection circuit triggers when the voltage between V_{SEN+} and V_{SEN-} is above the rising overvoltage threshold. When an OVP fault is declared, the module is latched off and PGOOD is be asserted low. The fault remains latched and can be reset by VDD cycling or toggling the EN pin.

Although the module has latched off in response to an OVP fault, the Low-Side Gate Driver (LGATE) retains the ability to toggle the low-side MOSFET on and off in response to the output voltage transversing the OVP rising and falling thresholds. The LGATE turns on the low-side MOSFET to discharge the output voltage, protecting the load. The LGATE turns off the low-side MOSFET when the sensed output voltage is lower than the falling overvoltage threshold (typically 100%). If the output voltage rises again, the LGATE turns on the low-side MOSFET again when the output voltage is above the rising overvoltage threshold (typically 120%). By doing so, the IC protects the load when there is a consistent overvoltage condition.

In addition to normal operation OVP, 5.5ms (typical, worst 6.5ms) after all rails (VDD, PVCC, 7VLDO, VIN) POR and before the end of soft-start, the start-up OVP circuits are enabled to protect against OVP event. See "Electrical Specifications" on page 10.

4.7.2 Undervoltage Protection

The Undervoltage Protection (UVP) fault detection circuit triggers if the output voltage is below the undervoltage threshold (typically 74% of DAC). When an UVP fault is declared, the module is latched off, forcing the LGATE and High-Side Gate Driver (UGATE) outputs low, and the PGOOD pin is asserted low. The fault remains latched and can be reset by VDD cycling or toggling the EN pin.

4.7.3 Overcurrent and Short-Circuit Protection

Inductor DCR sensing is used for current sense and senses current continuously for fast response. The current sense amplifier uses the CSEN and CSRTN inputs to reproduce a signal proportional to the inductor current, I_L. The sense current is proportional to the inductor current and is used for overcurrent protection.

The Overcurrent Protection (OCP) is triggered when the load current is 14.3A typically. OCP protects inductor saturation from a short-circuit event and provides a more robust power train and system protection. When an OCP or short-circuit fault is declared, the module is latched off, forcing both the high-side and low-side gate driver outputs low, or it retries with a hiccup time of 9ms. The fault response is programmable by SET3. However, the latched off event can be reset by VDD cycling or toggling the EN pin.

4.7.4 Over-Temperature Protection

An NTC inside the module senses the inductor temperature for both over-temperature and current sense temperature compensation. The NTC is connected to the NTC pin and SGND pad, and it results in lower NTC pin voltage at higher temperature. A comparator with hysteresis compares the NTC pin voltage to the threshold set. At +136°C (typical), Over-Temperature Protection (OTP) is triggered, and ISL8210M operation is disabled. When the sensed temperature is around +122.4°C, the ISL8210M resumes normal operation. When an OTP fault is declared, the module forces the LGATE and UGATE outputs low.

4.8 PGOOD Monitor

The PGOOD pin indicates when the module is capable of supplying regulated voltage. If there is a fault condition of a rail's (VDD, PVCC, 7VLDO, or VIN) UVLO, output Overcurrent (OCP), output Overvoltage (OVP), output Undervoltage (UVP), or Over-Temperature (OTP), PGOOD is asserted low. Note that the PGOOD pin is an undefined impedance with insufficient V_{DD} (typically <2.5V).

4.9 PFM Mode Operation

In PFM mode, programmable by SET2, the switching frequency is dramatically reduced to minimize the switching loss and significantly improve light-load efficiency. The ISL8210M can enter and exit PFM mode seamlessly as load changes. For high V_{OUT} applications, the LGATE might not turn on long enough to charge the boot capacitor in PFM mode with 0A load. Reneas recommends enabling the ISL8210M's ultrasonic PFM feature (by SET3), which maintains the LGATE switching frequency above 20kHz and keeps the boot capacitor charged for immediate load apply events. Alternatively, maintaining a minimum load can enhance the boot capacitor charge.

5. Layout Guidelines

Careful attention to layout requirements is necessary for a successful implementation of the ISL8210M power module. The ISL8210M switches at a very high frequency. Therefore, the switching times are very short. At these switching frequencies, even the shortest trace has significant impedance. The peak gate drive current also rises significantly in an extremely short time. Current transition from one MOSFET to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. The voltage spikes can degrade efficiency, generate EMI, and increase MOSFET voltage stress and ringing. Careful component selection and proper PCB layout minimize the magnitude of these voltage spikes. Use the ISL8210MEVAL1Z as a example and reference for the PCB layout.

The following are layout considerations:

- Renesas recommends using a six-layer PCB board. Use the top and bottom layer to route VIN and VOUT. Use a full ground plane in the internal layers (underneath the module) with shared SGND and PGND to simplify the layout design. Use another full ground plane directly above the bottom layer. Use the other internal layers to route the remote sense and PGOOD signals.
- Place the input capacitors and high frequency decoupling ceramic capacitors between VIN and PGND, as close to the module as possible. The loop formed by the input capacitors, VIN, and PGND must be as small as possible to minimize high frequency noise. Place the output ceramic capacitors close to VOUT. Use a copper plane to connect the output ceramic capacitors to the load to avoid any parasitic inductances and resistances. An illustrative layout example is shown in Figures 46 and 47.
- Use large copper planes for power paths (VIN, VOUT, and PGND) to minimize conduction loss and thermal stress. Use multiple vias to connect the power planes in different layers.
- Do not oversize the copper planes for the PHASE planes. Because the PHASE planes are subjected to very high dv/dt, the parasitic capacitor formed between these planes and the surrounding circuitry tends to couple the switching noise. Ensure that none of the sensitive signal traces are routed close to the PHASE plane.
- Place the PVCC and VIN1 bypass capacitors underneath the PVCC and VIN1 pins and connect their grounds to the SGND. For the external pin-strap resistor dividers connected to SET1, SET2, SET3, and SET4, connect the low side dividers' ground to the SGND. If a local decoupling capacitor is used to bias these resistor dividers, place the decoupling capacitor close to the dividers and connect the capacitor's ground to the SGND. An illustrative layout example is shown in Figure 47.
- Connect remote sensing traces to the regulation point to achieve a tight output voltage regulation. Route the remote sensing traces in parallel underneath the PGND layer and avoid routing the sensing trace near noisy planes such as PHASE. Place 2Ω resistors close to VSEN and RGND, respectively, to dampen the noise on the traces.

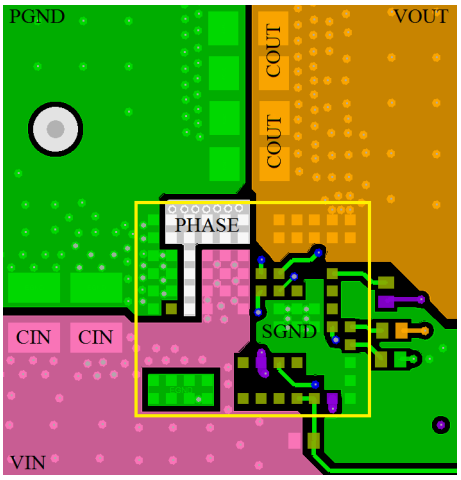


Figure 46. Layout Example - Top Layer

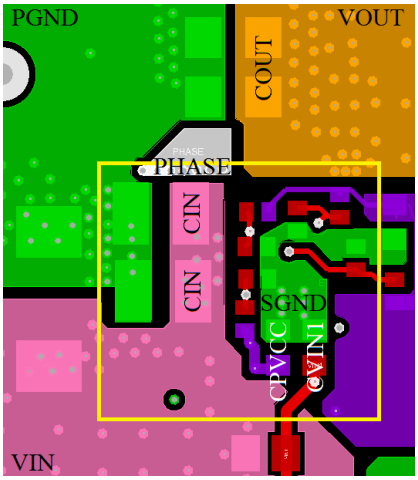


Figure 47. Layout Example - Bottom Layer

6. Thermal Considerations

Use the experimental power loss and θ_{JA} from the thermal modeling analysis to evaluate the thermal consideration for the module. The derating curves are derived from the maximum power allowed while maintaining the temperature below the maximum junction temperature of +125°C. The derating curves are derived based on tests of the ISL8210M evaluation board, which is a 6-layer board 3 x 3 inches in size with 2oz Cu on all layers and multiple via interconnects. In the actual application, other heat sources and design margins should be considered.

7. Package Description

The structure of the ISL8210M belongs to the High Density Array (HDA) no-lead package. The HDA package has advantages such as good thermal and electrical conductivity, low weight, and small size and is applicable for surface mounting technology that is being more readily used in the industry. The ISL8210M contains several types of devices, including resistors, capacitors, inductors, and control ICs. The ISL8210M is a copper leadframe based package with exposed copper thermal pads that have good electrical and thermal conductivity. The copper leadframe and multicomponent assembly is overmolded with a polymer mold compound to protect these devices.

The package outline, typical Printed Circuit Board (PCB) layout pattern design, and typical stencil pattern design are shown in "Package Outline Drawing" on page 40. The module has a small size of 12mm x 11mm x 5.3mm.

7.1 PCB Layout Pattern Design

The bottom of the ISL8210M is a leadframe footprint attached to the PCB by surface mounting process. The PCB layout pattern is shown in "Package Outline Drawing" on page 40. The PCB layout pattern is an array of solder mask defined PCB lands that align with the perimeters of the HDA exposed pads and I/O termination dimensions. The thermal lands on the PCB layout also feature an array of solder mask defined lands and should match 1:1 with the package exposed die pad perimeters. The exposed solder mask defined PCB land area should be 50-80% of the available module I/O area.

7.2 Thermal Vias

A grid of 1.0mm to 1.2mm pitch thermal vias drops down and connects to buried copper plane(s). Place the grid under the thermal land. The vias should be about 0.3mm to 0.33mm in diameter with the barrel plated to about 1.0 oz. of copper. Although adding more vias (by decreasing via pitch) improves the thermal performance, increasing the number of vias eventually yields diminishing returns. Use as many vias as practical for the thermal land size and your board design rules allow.

7.3 Stencil Pattern Design

Reflowed solder joints on the perimeter I/O lands should have about a 50µm to 75µm (2mil to 3mil) standoff height. The solder paste stencil design is the first step in developing optimized, reliable solder joints. The stencil aperture size to solder mask defined PCB land size ratio should typically be 1:1. The aperture width can be reduced slightly to help prevent solder bridging between adjacent I/O lands A typical solder stencil pattern is shown in the "Package Outline Drawing" on page 40. Consider the symmetry of the whole stencil pattern when designing its pads. A laser cut, stainless steel stencil with electropolished trapezoidal walls is recommended. Electropolishing "smooths" the aperture walls resulting in reduced surface friction and better paste release, which reduces voids. Using a Trapezoidal Section Aperture (TSA) also promotes paste release and forms a "brick like" paste deposit that assists in firm component placement. A 0.1mm to 0.15mm stencil thickness is recommended for this large pitch HDA.

7.4 Reflow Parameters

Due to the low mount height of the HDA, “No-Clean” Type 3 solder paste per ANSI/J-STD-005 is recommended. A nitrogen purge is also recommended during reflow. A system board reflow profile depends on the thermal mass of the entire populated board, so it is not practical to define a specific soldering profile just for the HDA. The profile given in Figure 48 is provided as a guideline, which can be adapted for varying manufacturing practices and applications.

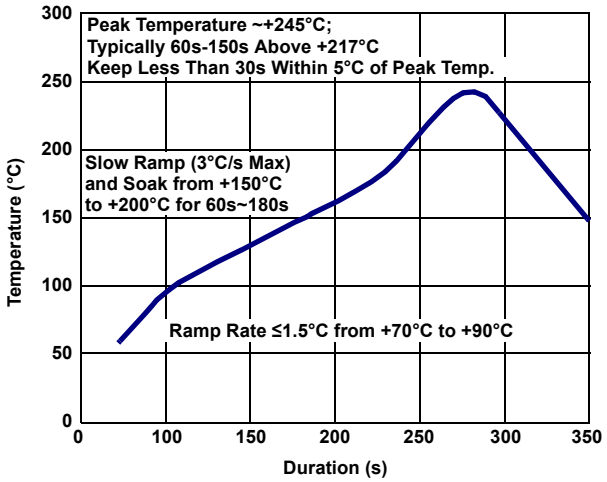


Figure 48. Typical Reflow Profile

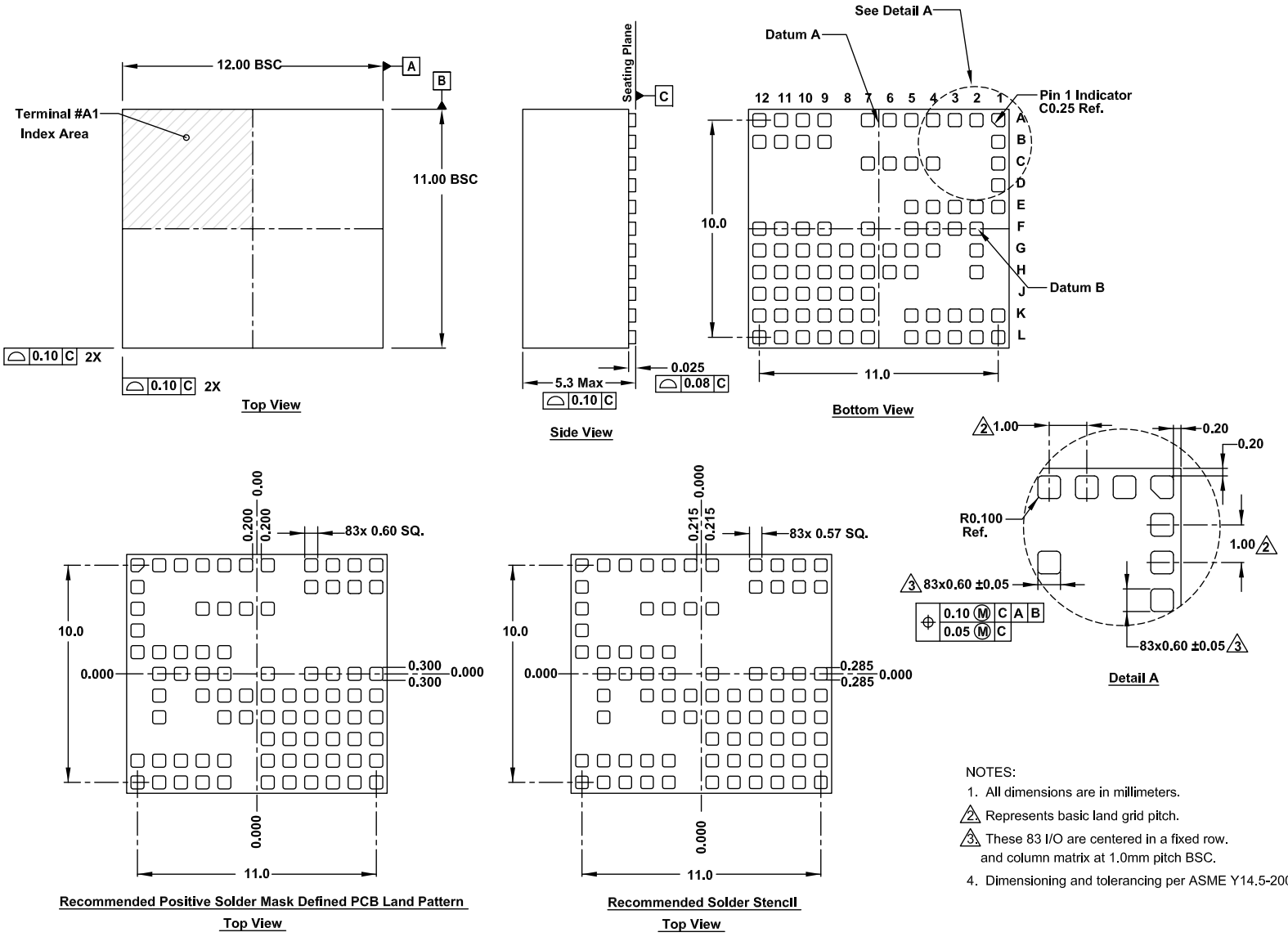
8. Revision History

Rev.	Date	Description
1.01	Feb 15, 2019	Updated third paragraph on page 1. Updated Figure 1. Updated Note 5 on page 9. Updated Figure 26 on page 17. Updated Figure 41 on page 21. Updated second paragraph in “Thermal Monitoring and Compensation” on page 31. Updated the Layout Guidelines section by removing “Layout Consideration” section title and updating first and 5th bullets. Updated Figures 46 and 47 on page 35. Updated board size on page 36. Updated disclaimer.
1.00	Dec 14, 2018	Initial release.

9. Package Outline Drawing

For the most recent package outline drawing, see Y83.12x11.

Y83.12x11
83 I/O 12mmx11mmx5.3mm HDA Module
Rev 0, 3/18



NOTES:

1. All dimensions are in millimeters.
2. Represents basic land grid pitch.
3. These 83 I/O are centered in a fixed row. and column matrix at 1.0mm pitch BSC.
4. Dimensioning and tolerancing per ASME Y14.5-2009.

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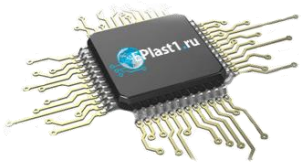

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