# NB7VQ572M

# 1.8V / 2.5V /3.3V Differential 4:1 Mux w/Input Equalizer to 1:2 CML Clock/Data Fanout / Translator

## Multi−Level Inputs w/ Internal Termination

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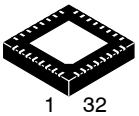


**QFN32**
**MN SUFFIX**
**CASE 488AM**

**MARKING DIAGRAM**

| | |
|---|---|
| A | = Assembly Location |
| WL | = Wafer Lot |
| YY | = Year |
| WW | = Work Week |
| ▪ | = Pb−Free Package |

(Note: Microdot may be in either location)

**ORDERING INFORMATION**

See detailed ordering and shipping information on page 10 of this data sheet.

### Description

The NB7VQ572M is a high performance differential 4:1 Clock / Data input multiplexer and a 1:2 CML Clock / Data fanout buffer that operates up to 7 GHz / 10 Gbps respectively with a 1.8 V, 2.5 V, or 3.3 V power supply.

Each INx / $\overline{\text{INx}}$ input pair incorporates a fixed Equalizer Receiver, which when placed in series with a Data path, will enhance the degraded signal transmitted across an FR4 backplane or cable interconnect. For applications that do not require Equalization, consider the NB7V572M, which is pin−compatible to the NB7VQ572M.

The differential Clock / Data inputs have internal 50 Ω termination resistors and will accept differential LVPECL, CML, or LVDS logic levels. The NB7VQ572M incorporates a pair of Select pins that will choose one of four differential inputs and will produce two identical CML output copies of Clock or Data.

As such, the NB7VQ572M is ideal for SONET, GigE, Fiber Channel, Backplane and other Clock/Data distribution applications. The two differential CML outputs will swing 400 mV when externally loaded and terminated with a 50 Ω resistor to $V_{CC}$ and are optimized for low skew and minimal jitter.

The NB7VQ572M is offered in a low profile 5x5 mm 32−pin QFN Pb−Free package. Application notes, models, and support documentation are available at www.onsemi.com. The NB7VQ572M is a member of the GigaComm™ family of high performance clock products.

### Features

- Input Data Rate > 10 Gb/s Typical
- Data Dependent Jitter < 10 ps
- Maximum Input Clock Frequency > 6 GHz Typical
- Random Clock Jitter < 0.8 ps RMS
- Low Skew 1:2 CML Outputs, < 15 ps max
- 4:1 Multi−Level Mux Inputs, accepts LVPECL, CML, LVDS
- 175 ps Typical Propagation Delay
- 45 ps Typical Rise and Fall Times
- Differential CML Outputs, 400 mV Peak−to−Peak, Typical
- Operating Range: $V_{CC}$ = 1.71 V to 3.6 V with GND = 0 V
- Internal 50 Ω Input Termination Resistors
- VREFAC Reference Output
- QFN−32 Package, 5mm x 5mm, Pb−Free
- −40°C to +85°C Ambient Operating Temperature
- These are Pb−Free Devices

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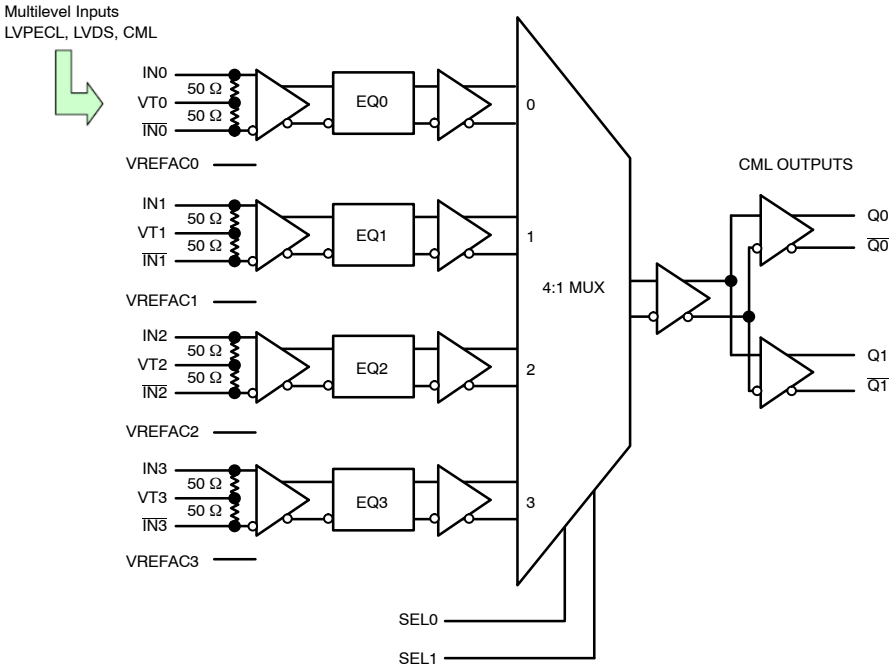



**Figure 1. Simplified Block Diagram**

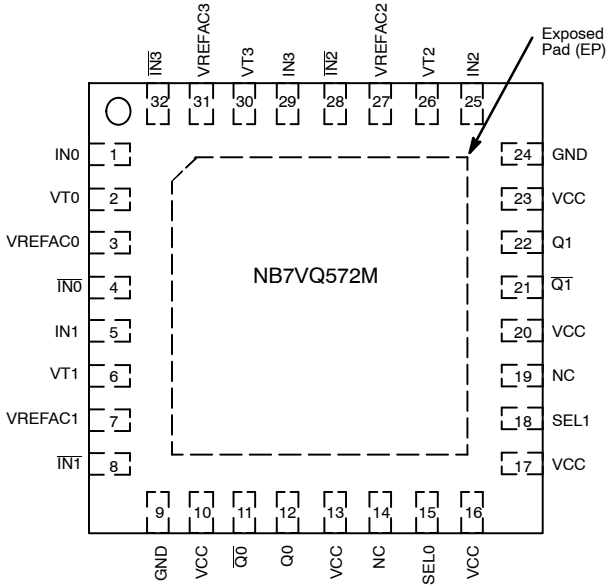



**Figure 2. Pinout: QFN−32 (Top View)**

**Table 1. INPUT SELECT FUNCTION TABLE**

| SEL1* | SEL0* | Clock / Data Input Selected |
|---|---|---|
| 0 | 0 | IN0 Input Selected |
| 0 | 1 | IN1 Input Selected |
| 1 | 0 | IN2 Input Selected |
| 1 | 1 | IN3 Input Selected |

*Defaults HIGH when left open.

**Table 2. PIN DESCRIPTION**

| Pin Number | Pin Name | I/O | Pin Description |
|---|---|---|---|
| 1, 4<br>5, 8<br>25, 28<br>29, 32 | IN0, $\overline{IN0}$<br>IN1, $\overline{IN1}$<br>IN2, $\overline{IN2}$<br>IN3, $\overline{IN3}$ | LVPECL, CML, LVDS Input | Noninverted, Inverted, Differential Clock or Data Inputs |
| 2, 6<br>26, 30 | VT0, VT1<br>VT2, VT3 | | Internal 100 Ω Center−tapped Termination Pin for INx / $\overline{INx}$ |
| 15<br>18 | SEL0<br>SEL1 | LVTTL/LVCMOS Input | Input Select pins, default HIGH when left open through a 94 kΩ pullup resistor. Input logic threshold is $V_{CC}$/2. See Select Function, Table 1. |
| 14, 19 | NC | − | No Connect |
| 10, 13, 16<br>17, 20, 23 | $V_{CC}$ | − | Positive Supply Voltage. |
| 11, 12<br>21, 22 | $\overline{Q0}$, Q0<br>$\overline{Q1}$, Q1 | CML Output | Inverted, Non−inverted Differential Outputs. |
| 9, 24 | GND | | Negative Supply Voltage |
| 3<br>7<br>27<br>31 | VREFAC0<br>VREFAC1<br>VREFAC2<br>VREFAC3 | − | Output Voltage Reference for Capacitor−Coupled Inputs |
| − | EP | − | The Exposed Pad (EP) on the QFN−32 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat−sinking conduit. The pad is electrically connected to the die, and must be electrically connected to GND. |

1. In the differential configuration when the input termination pins (VT0, VT1, VT2, VT3) are connected to a common termination voltage or left open, and if no signal is applied on INx/$\overline{INx}$ input, then the device will be susceptible to self−oscillation.
2. All $V_{CC}$, and GND pins must be externally connected to a power supply for proper operation.

**Table 3. ATTRIBUTES**

| Characteristics | | Value |
|---|---|---|
| ESD Protection | Human Body Model<br>Machine Model | > 2 kV<br>> 200 V |
| $R_{PU}$ – SELx Input Pullup Resistor | | 28 kΩ |
| Moisture Sensitivity (Note 3) | QFN−32 | Level 1 |
| Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V−0 @ 0.125 in |
| Transistor Count | | 252 |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | |

3. For additional information, see Application Note AND8003/D.

**Table 4. MAXIMUM RATINGS**

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Positive Power Supply | GND = 0 V | | 4.0 | V |
| $V_{IN}$ | Positive Input Voltage | GND = 0 V | | −0.5 to $V_{CC}$ +0.5 | V |
| $V_{INPP}$ | Differential Input Voltage \|IN − $\overline{IN}$\| | | | 1.89 | V |
| $I_{out}$ | Output Current Through $R_T$ (50 Ω Resistor) | | | ±40 | mA |
| $I_{IN}$ | Input current Through RT (50 Ω Resistor) | | | ±40 | mA |
| $I_{VREFAC}$ | $V_{REFAC}$ Sink or Source Current | | | ±1.5 | mA |
| $T_A$ | Operating Temperature Range | | | −40 to +85 | °C |
| $T_{stg}$ | Storage Temperature Range | | | −65 to +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Junction−to−Ambient) (Note 4) | 0 lfpm<br>500 lfpm | QFN−32<br>QFN−32 | 31<br>27 | °C/W<br>°C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction−to−Case) (Note 4) | | QFN−32 | 12 | °C/W |
| $T_{sol}$ | Wave Solder | ≤ 20 sec | | 265 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

4. JEDEC standard multilayer board − 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

**Table 5. DC CHARACTERISTICS CML OUTPUT** $V_{CC}$ = 1.71 V to 3.6 V , GND = 0 V, $T_A$ = −40°C to +85°C (Note 5)

| Symbol | Characteristic | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| $V_{CC}$ | Power Supply Voltage | $V_{CC}$ = 3.3 V<br>$V_{CC}$ = 2.5 V<br>$V_{CC}$ = 1.8 V | 3.0<br>2.375<br>1.71 | 3.3<br>2.5<br>1.8 | 3.6<br>2.625<br>1.89 | V |
| $I_{CC}$ | Power Supply Current for $V_{CC}$ (Inputs and Outputs Open) | $V_{CC}$ = 3.3 V<br>$V_{CC}$ = 2.5 V<br>$V_{CC}$ = 1.8 V | | 130<br>120<br>100 | 160<br>145<br>120 | mA |
| **CML OUTPUTS** (Note 6) | | | | | | |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = 3.3 V<br>$V_{CC}$ = 2.5 V<br>$V_{CC}$ = 1.8 V | $V_{CC}$ − 30<br>3270<br>2470<br>1770 | $V_{CC}$ − 5<br>3295<br>2495<br>1795 | $V_{CC}$<br>3300<br>2500<br>1800 | mV |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = 3.3 V<br>$V_{CC}$ = 2.5 V<br>$V_{CC}$ =1.8 V | $V_{CC}$ − 550<br>2675<br>1875 | $V_{CC}$ − 450<br>2825<br>2025<br>1325 | $V_{CC}$ − 350<br>2975<br>2175<br>1475 | mV |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = 3.3 V<br>$V_{CC}$ = 2.5 V<br>$V_{CC}$ =1.8 V | VCC − 625<br>2675<br>VCC − 600<br>1900<br>VCC − 550<br>1250 | VCC − 475<br>2825<br>VCC − 475<br>2025<br>VCC − 450<br>1350 | VCC − 325<br>2975<br>VCC − 350<br>2150<br>VCC − 350<br>1450 | mV |
| **DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE−ENDED** (Figures 7 and 8) (Note 7) | | | | | | |
| $V_{IH}$ | Single−ended Input HIGH Voltage | | $V_{th}$ + 100 | | $V_{CC}$ | mV |
| $V_{IL}$ | Single−ended Input LOW Voltage | | GND | | $V_{th}$ − 100 | mV |
| $V_{th}$ | Input Threshold Reference Voltage Range (Note 8) | | 1100 | | $V_{CC}$ − 100 | mV |
| $V_{ISE}$ | Single−ended Input Voltage ($V_{IH}$ − $V_{IL}$) | | 200 | | 1200 | mV |
| **VREFAC** | | | | | | |
| $V_{REFAC}$ | Output Reference Voltage (100 μA Load) | $V_{CC}$ = 3.3 V<br>$V_{CC}$ = 2.5 V<br>$V_{CC}$ = 1.8 V | $V_{CC}$ − 800<br>$V_{CC}$ − 750<br>1050 | $V_{CC}$ − 625<br>$V_{CC}$ − 575<br>$V_{CC}$ − 525 | $V_{CC}$ − 500<br>$V_{CC}$ − 450<br>$V_{CC}$ − 400 | mV |
| **DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY** (Figures 9 and 10) (Note 9) | | | | | | |
| $V_{IHD}$ | Differential Input HIGH Voltage (IN, $\overline{IN}$) | | 1200 | | $V_{CC}$ | mV |
| $V_{ILD}$ | Differential Input LOW Voltage (IN, $\overline{IN}$) | | 0 | | $V_{IHD}$ − 100 | mV |
| $V_{ID}$ | Differential Input Voltage (IN, $\overline{IN}$) ($V_{IHD}$ − $V_{ILD}$) | | 100 | | 1200 | mV |
| $V_{CMR}$ | Input Common Mode Range (Differential Configuration, Note 10) (Figure 11) | | 1150 | | $V_{CC}$ − 50 | mV |
| $I_{IH}$ | Input HIGH Current IN / $\overline{IN}$ (VTIN/$\overline{VTIN}$ Open) | | −150 | | 150 | μA |
| $I_{IL}$ | Input LOW Current IN / $\overline{IN}$ (VTIN/$\overline{VTIN}$ Open) | | −150 | | 150 | μA |
| **CONTROL INPUT** (SELx Pin) | | | | | | |
| $V_{IH}$ | Input HIGH Voltage for Control Pin | | $V_{CC}$ x 0.65 | | $V_{CC}$ | V |
| $V_{IL}$ | Input LOW Voltage for Control Pin | | GND | | $V_{CC}$ x 0.35 | V |
| $I_{IH}$ | Input HIGH Current | | −150 | | 150 | μA |
| $I_{IL}$ | Input LOW Current | | −150 | | 150 | μA |
| **TERMINATION RESISTORS** | | | | | | |
| $R_{TIN}$ | Internal Input Termination Resistor (Measured from INx to VTx) | | 45 | 50 | 55 | Ω |
| $R_{TOUT}$ | Internal Output Termination Resistor | | 45 | 50 | 55 | Ω |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Input and Output parameters vary 1:1 with $V_{CC}$.
6. CML outputs loaded with 50 Ω to $V_{CC}$ for proper operation.
7. $V_{th}$, $V_{IH}$, $V_{IL,}$ and $V_{ISE}$ parameters must be complied with simultaneously.
8. $V_{th}$ is applied to the complementary input when operating in single−ended mode.
9. $V_{IHD}$, $V_{ILD,}$ $V_{ID}$ and $V_{CMR}$ parameters must be complied with simultaneously.
10. $V_{CMR}$ min varies 1:1 with GND, $V_{CMR}$ max varies 1:1 with $V_{CC}$. The $V_{CMR}$ range is referenced to the most positive side of the differential input signal.

**Table 6. AC CHARACTERISTICS** $V_{CC}$ = 1.71 V to 3.6 V, GND = 0 V, $T_A$ = −40°C to +85°C (Note 11)

| Symbol | Characteristic | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Input Clock Frequency $V_{OUT} \geq$ 200 mV | | 6 | 7 | | GHz |
| $f_{DATAMAX}$ | Maximum Operating Data Rate NRZ, (PRBS23) | | 10 | 11 | | Gbps |
| $f_{SEL}$ | Maximum Toggle Frequency, SELx | | 4 | 10 | | MHz |
| $V_{OUTPP}$ | Output Voltage Amplitude (@ $V_{INPPmin}$) (Note 12) (Figure 12) $f_{in} \leq$ 5 GHz | | 250 | 400 | | mV |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay to Differential Outputs Measured at Differential Crosspoint | @ 1 GHz INx/$\overline{INx}$ to Qx/$\overline{Qx}$<br>@ 50 MHz SELx to Qx | 100 | 175<br>7 | 250<br>20 | ps<br>ns |
| $t_{PD\ Tempco}$ | Differential Propagation Delay Temperature Coefficient | | | 50 | | Δfs/°C |
| $t_{skew}$ | Output − Output skew (within device) (Note 13)<br>Device − Device skew ($t_{pdmax} - t_{pdmin}$) | | | 0<br>30 | 15<br>100 | ps |
| $t_{DC}$ | Output Clock Duty Cycle (Reference Duty Cycle = 50%) $f_{IN} \leq$ 5 GHz | | 45 | 50 | 55 | % |
| $\Phi_N$ | Phase Noise, $f_{in}$ = 1 GHz | 10 kHz<br>100 kHz<br>1 MHz<br>10 MHz<br>20 MHz<br>40 MHz | | −134<br>−136<br>−149<br>−149<br>−149<br>−149 | | dBc |
| $t_{\int\Phi N}$ | Integrated Phase Jitter (Figure TBD) $f_{in}$ = 1 GHz, 12 kHz − 20 MHz Offset (RMS) | | | 35 | | fs |
| $t_{JITTER}$ | Random Clock Jitter, RJ (Note 14) $f_{in} \leq$ 6 GHz | | | 0.2 | 0.8 | ps RMS |
| | Deterministic Jitter, DJ (Note 15) $f_{in} \leq$ 10 Gbps (12" FR4) | | | | 10 | ps pk−pk |
| | Crosstalk Induced Jitter (Adjacent Channel) (Note 17) | | | | 0.7 | ps RMS |
| $V_{INPP}$ | Input Voltage Swing (Differential Configuration) (Note 16) | | 100 | | 1200 | mV |
| $t_r$, $t_f$ | Output Rise/Falltimes @ 1 GHz; (20% − 80%), $V_{IN}$ = 400 mV Qx, $\overline{Qx}$ | | 25 | 45 | 65 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

11. Measured using a 150 mVpk−pk source, 50% duty cycle clock source. All output loading with external 50 Ω to $V_{CC}$. Input edge rates 40 ps (20% − 80%).
12. Output voltage swing is a single−ended measurement operating in differential mode.
13. Skew is measured between outputs under identical transitions and conditions. Duty cycle skew is defined only for differential operation when the delays are measured from crosspoint of the inputs to the crosspoint of the outputs.
14. Additive RMS jitter with 50% duty cycle clock signal.
15. Additive Peak−to−Peak data dependent jitter with input NRZ data at PRBS23.
16. Input voltage swing is a single−ended measurement operating in differential mode.
17. Crosstalk is measured at the output while applying two similar clock frequencies that are asynchronous with respect to each other at the inputs.

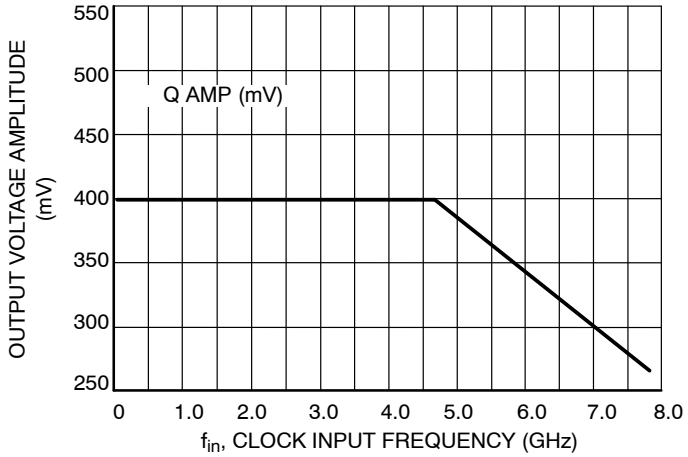



**Figure 3. Clock Output Voltage Amplitude ($V_{OUTPP}$) vs. Input Frequency ($f_{in}$) at Ambient Temperature (Typical)**

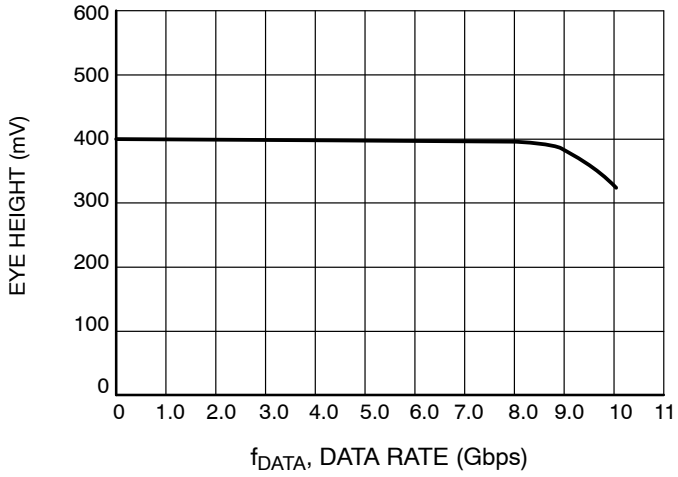



**Figure 4. Inside Eye Height vs. Input Data Rate (Gbps) at Ambient Temperature (typical), FR4 = 12”**

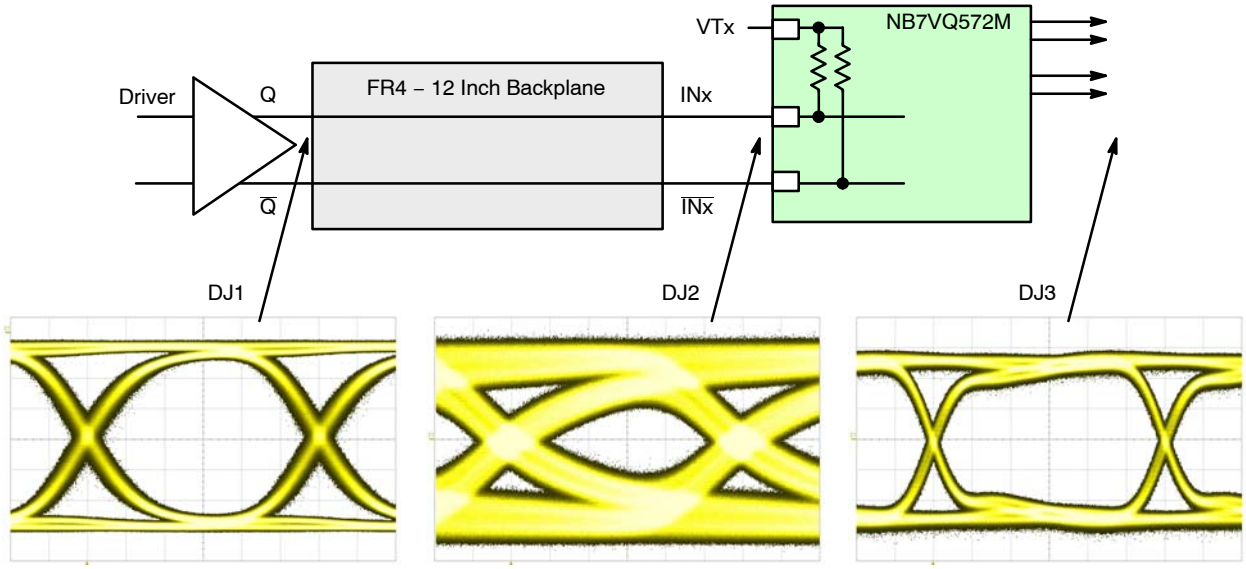



**Figure 5. Typical NB7VQ572M Equalizer Application and Interconnect with PRBS23 Pattern at 10 Gbps**

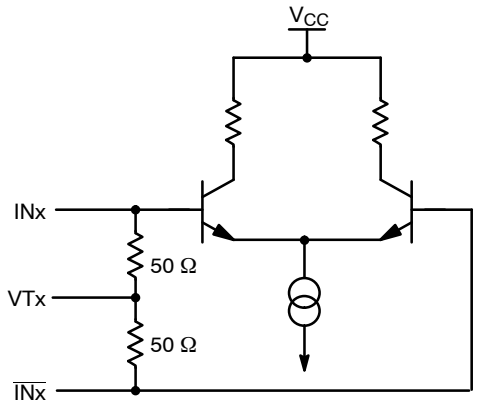



Figure 6. Input Structure

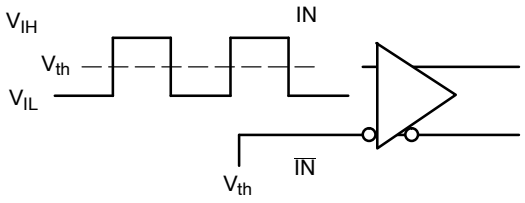



Figure 7. Differential Input Driven Single−Ended

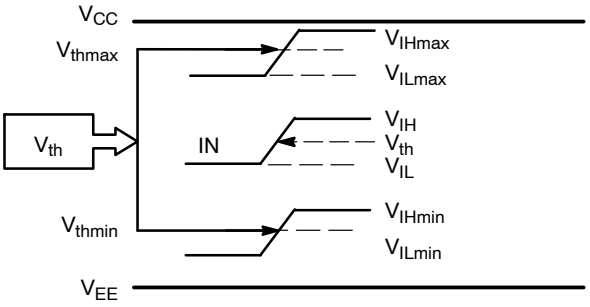



Figure 8. $V_{th}$ Diagram

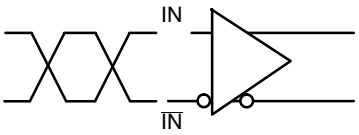



Figure 9. Differential Inputs Driven Differentially

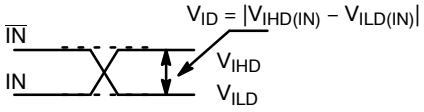



Figure 10. Differential Inputs Driven Differentially

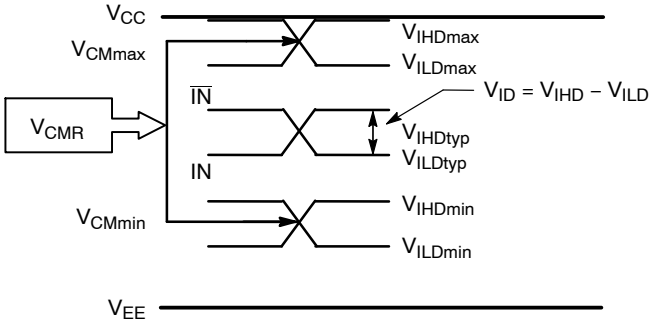



Figure 11. VCMR Diagram

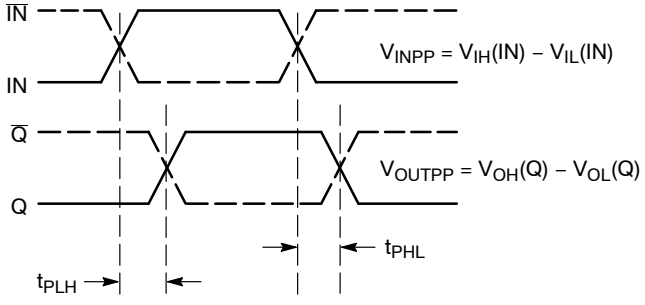



Figure 12. AC Reference Measurement

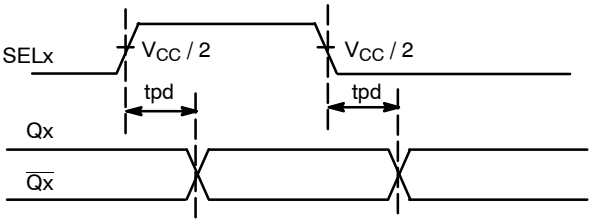



Figure 13. SELx to Qx Timing Diagram

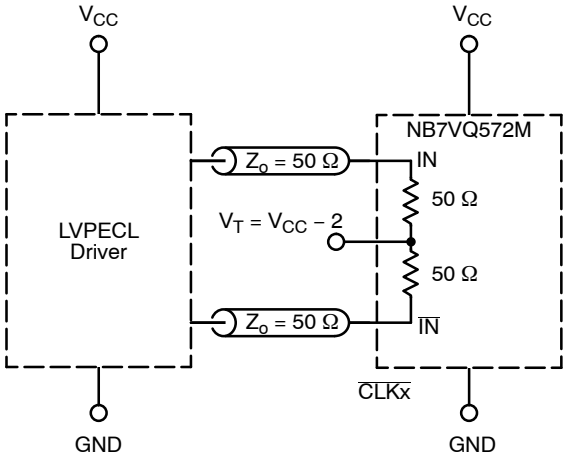



**Figure 14. LVPECL Interface**

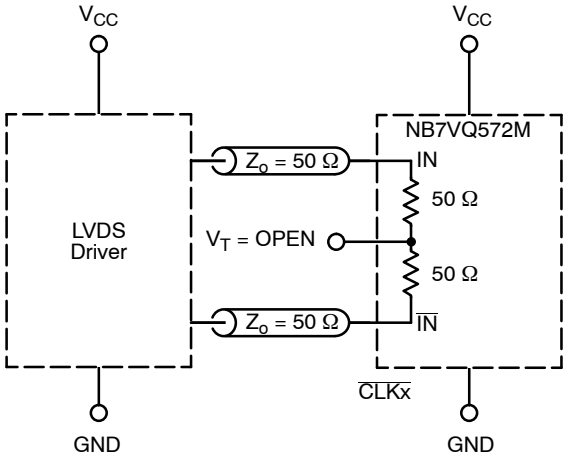



**Figure 15. LVDS Interface**

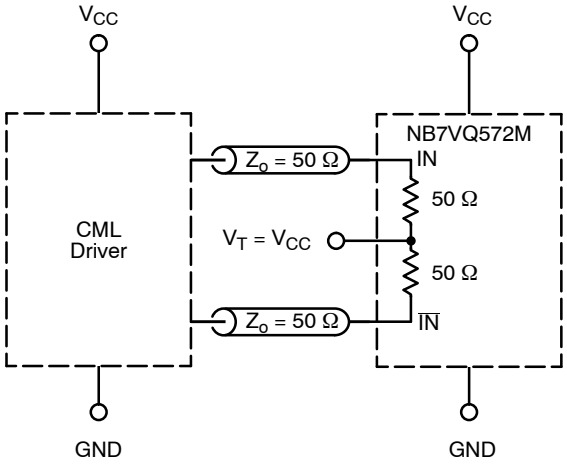



**Figure 16. Standard 50 Ω Load CML Interface**

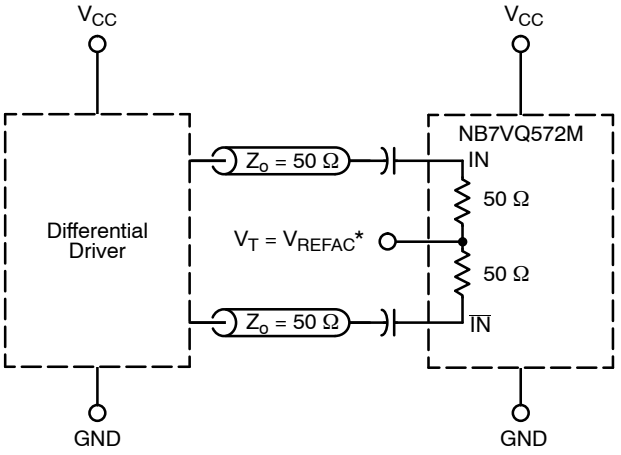



**Figure 17. Capacitor−Coupled Differential Interface ($V_T$ Connected to $V_{REFAC}$)**

*$V_{REFAC}$ bypassed to ground with a 0.01 μF capacitor.

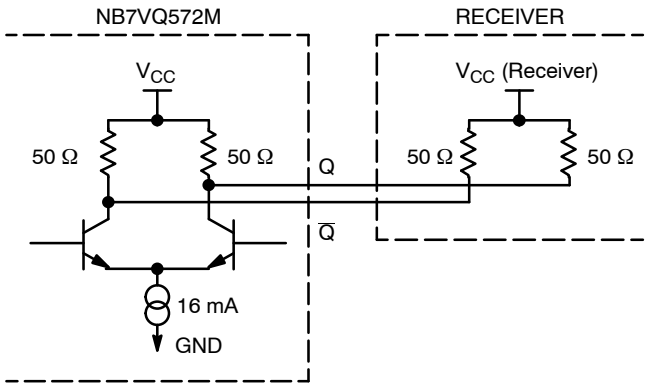



**Figure 18. Typical CML Output Structure and Termination**

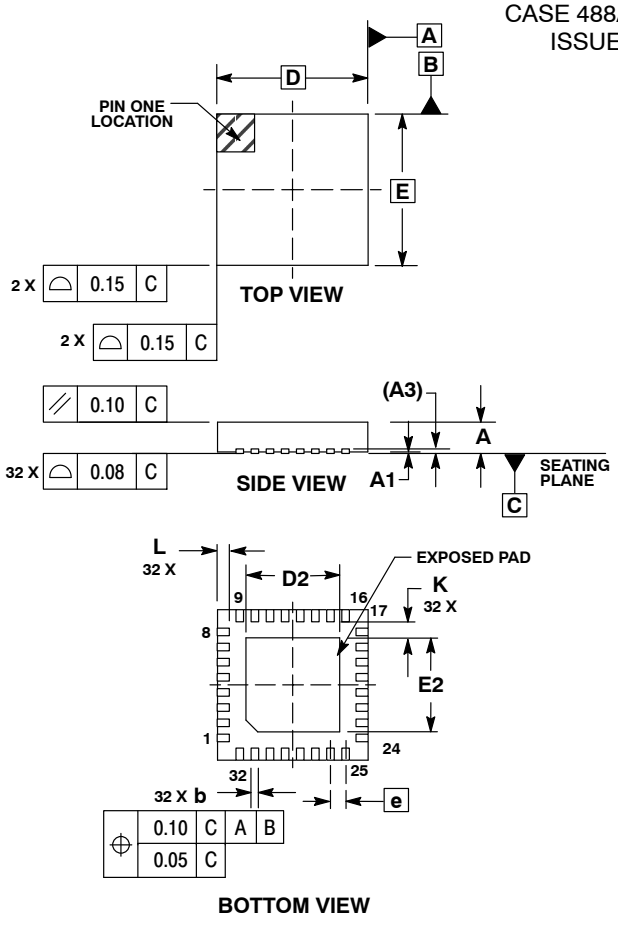
## DEVICE ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NB7VQ572MMNG | QFN−32<br>(Pb−free) | 74 Units / Rail |
| NB7VQ572MMNR4G | QFN−32<br>(Pb−free) | 1000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## PACKAGE DIMENSIONS

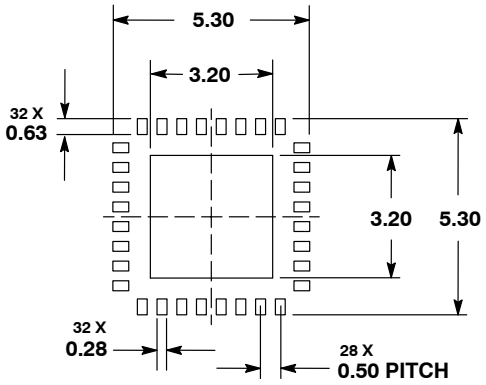
**QFN32 5*5*1 0.5 P**
CASE 488AM−01
ISSUE O




NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 0.800 | 0.900 | 1.000 |
| A1 | 0.000 | 0.025 | 0.050 |
| A3 | | 0.200 REF | |
| b | 0.180 | 0.250 | 0.300 |
| D | | 5.00 BSC | |
| D2 | 2.950 | 3.100 | 3.250 |
| E | | 5.00 BSC | |
| E2 | 2.950 | 3.100 | 3.250 |
| e | | 0.500 BSC | |
| K | 0.200 | −−− | −−− |
| L | 0.300 | 0.400 | 0.500 |

### SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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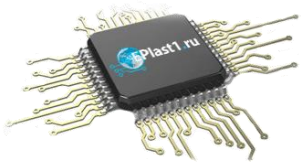


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