

## IRS2052MPbF 2 CH Digital Audio Amplifier

### Features

- 2 channel integrated analog input Class D audio amplifier driver
- Versatile protection control enabling latched, non-latched, or host controlled shutdown function
- Integrated clock oscillator
- Clipping detection
- External thermal sensor input
- On-chip thermal shutdown with warning
- Programmable over current protection
- Programmable dead-time generation
- Start and stop click noise reduction
- Under voltage protection
- High noise immunity

### Note

The IRS2052M digital audio driver is a two channel version of IRS2092(S) with additional features, such as internal clock and over temperature protection. The IRS2052M features clipping detection outputs, on-chip over temperature detection, over temperature sensor inputs and a fault reporting output.

### Product Summary

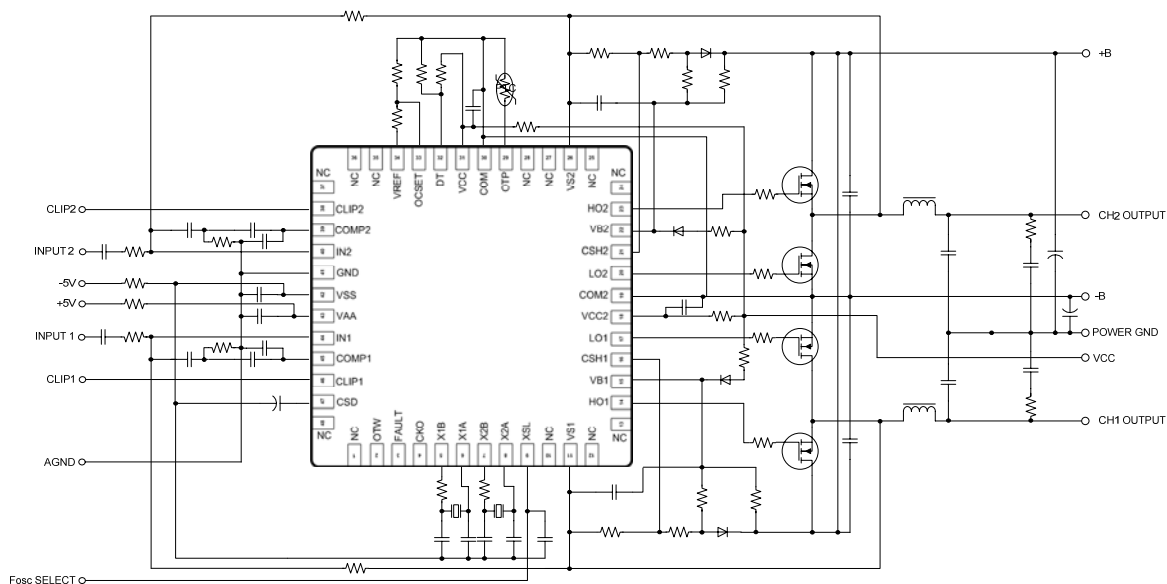
|  |                 |
|--|-----------------|
| Topology                                   | Half-Bridge     |
| $V_{\text{OFFSET (max)}}$                  | +/- 100 V       |
| $I_{\text{O+}} \& I_{\text{O-}}$ (typical) | 0.5 A & 0.6 A   |
| Selectable deadtime                        | 45/65/85/105 ns |
| DC offset                                  | <20 mV          |
| OC protection delay                        | 500 ns (max)    |
| Shutdown propagation delay                 | 250 ns (max)    |
| Error amplifier open loop gain             | >60 dB          |

### Package



MLPQ48 (7x7 mm, 0.50 mm pitch)

### Typical Connection



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**Description**

The IRS2052M integrates two channels of high voltage, high performance Class D audio amplifier drivers with PWM modulators and protections. In conjunction with external MOSFET and external components, a complete 2 channel Class D audio amplifier can be realized. The IRS2052M is designed with floating analog inputs and protection control interface pin especially for half bridge topology. High and low side MOSFET are protected from over current conditions by a programmable bi-directional current sensing. Essential elements of PWM modulator section allow flexible system design. A small MLPQ48 package enhances the benefit of smaller size of Class D topology. The IRS2052M is a lead-free, ROHS compliant.

**Qualification Information<sup>†</sup>**

|                                   |                         |   |
|-----------------------------------|-------------------------|---|
| <b>Qualification Level</b>        |                         | Industrial <sup>††</sup>  |
|                                   |                         | Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level. |
| <b>Moisture Sensitivity Level</b> |                         | MSL2 <sup>†††</sup> , 260°C<br>(per IPC/JEDEC J-STD-020)  |
| <b>ESD</b>                        | <b>Machine Model</b>    | Class B<br>(per JEDEC standard EIA/JESD22-A115)   |
|                                   | <b>Human Body Model</b> | Class 1B<br>(per EIA/JEDEC standard JESD22-A114)  |
| <b>IC Latch-Up Test</b>           |                         | Class I, Level A<br>(per JESD78)  |
| <b>RoHS Compliant</b>             |                         | Yes   |

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

**Absolute Maximum Ratings**

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM; all currents are defined positive into any lead. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

| Symbol       | Definition   | Min.                   | Max.            | Units |
|--------------|--|------------------------|-----------------|-------|
| $V_{Bn}$     | High side floating supply voltage                                | -0.3                   | 215             | V     |
| $V_{Sn}$     | High side floating supply voltage <sup>††</sup> , n=1-2          | $V_{Bn} - 15$          | $V_{Bn} + 0.3$  | V     |
| $V_{Hon}$    | High side floating output voltage, n=1-2                         | $V_{Sn} - 0.3$         | $V_{Bn} + 0.3$  | V     |
| $V_{CSHn}$   | CSH pin input voltage, n=1-2                                     | $V_{Sn} - 0.3$         | $V_{Bn} + 0.3$  | V     |
| $V_{CC}$     | $V_{CC}$ low side fixed supply voltage <sup>††</sup>             | -0.3                   | 20              | V     |
| $V_{CC2}$    | $V_{CC2}$ low side fixed supply voltage <sup>††</sup>            | -0.3                   | 20              | V     |
| $V_{Lon}$    | Low side output voltage, n=1-2                                   | -0.3                   | $V_{CC2} + 0.3$ | V     |
| $V_{AA}$     | Floating input positive supply voltage <sup>††</sup>             | (See $I_{AAZ}$ )       | 220             | V     |
| $V_{SS}$     | Floating input negative supply voltage <sup>††</sup>             | -1<br>(See $I_{SSZ}$ ) | $V_{AA} + 0.3$  | V     |
| $V_{GND}$    | Floating input supply ground voltage                             | $V_{SS} - 0.3$         | $V_{AA} + 0.3$  | V     |
| $I_{IN-n}$   | Inverting input current <sup>†</sup> , n=1-2                     | -                      | ±3              | mA    |
| $V_{CSD}$    | SD pin input voltage   | $V_{SS} - 0.3$         | $V_{AA} + 0.3$  | V     |
| $V_{COMPn}$  | COMP pin input voltage, n=1-2                                    | $V_{SS} - 0.3$         | $V_{AA} + 0.3$  | V     |
| $V_{CLIPn}$  | CLIP pin input voltage   | GND - 0.3              | $V_{AA} + 0.3$  | V     |
| $I_{CLIPn}$  | CLIP pin sinking current   | -                      | 5               | mA    |
| $V_{FAULT}$  | FAULT pin input voltage  | GND - 0.3              | $V_{AA} + 0.3$  | V     |
| $I_{FAULT}$  | FAULT pin sinking current  | -                      | 5               | mA    |
| $V_{OTW}$    | OTW pin input voltage  | GND - 0.3              | $V_{AA} + 0.3$  | V     |
| $I_{OTW}$    | OTW pin sinking current  | -                      | 5               | mA    |
| $V_{DT}$     | DT pin input voltage   | -0.3                   | $V_{CC} + 0.3$  | V     |
| $V_{OCSET}$  | OCSET pin input voltage  | -0.3                   | $V_{CC} + 0.3$  | V     |
| $V_{OTPn}$   | OTP pin input voltage  | -0.3                   | $V_{CC} + 0.3$  | V     |
| $I_{AAZ}$    | Floating input positive supply zener clamp current <sup>††</sup> | -                      | 10              | mA    |
| $I_{CCZ}$    | Low side $V_{CC}$ supply zener clamp current <sup>††</sup>       | -                      | 10              | mA    |
| $I_{CC2Z}$   | Low side $V_{CC2}$ supply zener clamp current <sup>††</sup>      | -                      | 10              | mA    |
| $I_{OTPZ}$   | OTP pin zener clamping current                                   | -                      | 1               | mA    |
| $I_{BSZn}$   | Floating supply zener clamp current <sup>††</sup> , n=1-2        | -                      | 10              | mA    |
| $I_{OREF}$   | Reference output current   | -                      | 5               | mA    |
| $dV_{Sn}/dt$ | Allowable $V_s$ voltage slew rate, n=1-2                         | -                      | 50              | V/ns  |
| $dV_{SS}/dt$ | Allowable $V_{ss}$ voltage slew rate <sup>†††</sup>              | -                      | 50              | V/ms  |

**Absolute Maximum Ratings (Cont'd)**

| Symbol         | Definition   | Min. | Max. | Units |
|----------------|--|------|------|-------|
| Pd             | Maximum power dissipation @ $T_A \leq +25^\circ\text{C}^{\dagger\dagger\dagger}$ | -    | 6    | W     |
| RthJA          | Thermal resistance, Junction to ambient <sup>††††</sup>                          | -    | 20   | °C/W  |
| T <sub>J</sub> | Junction Temperature   | -    | 150  | °C    |
| T <sub>S</sub> | Storage Temperature  | -55  | 150  | °C    |
| T <sub>L</sub> | Lead temperature (Soldering, 10 seconds)   | -    | 300  | °C    |

† IN-1 and IN-2 contain clamping diode to GND.

†† VAA-VSS, VCC-COM, VCC2-COM2, VB1-VS1 and VB2-VS2 contain internal shunt zener diodes. Note that the voltage ratings of these can be limited by the clamping current.

††† For the rising and falling edges of step signal of 10V. VSS=15V to 200V.

†††† According to JESD51-5. JEDEC still air chamber.

**Recommended Operating Conditions**

For proper operation, the device should be used within the recommended conditions below. The Vs and COM offset ratings are tested with supplies biased at  $V_{AA}-V_{SS}=10V$ ,  $V_{CC}=V_{CC2}=12V$ ,  $COM2=COM$  and  $V_B-V_S=12V$ . All voltage parameters are absolute voltages referenced to COM; all currents are defined positive into any lead.

| Symbol                | Definition   | Min.                  | Max.                  | Units |
|-----------------------|--|-----------------------|-----------------------|-------|
| $V_{Bn}$              | High side floating supply absolute voltage, n=1-2                  | $V_{Sn} + 10$         | $V_{Sn} + 14$         | V     |
| $V_{Sn}$              | High side floating supply offset voltage                           | †                     | 200                   | V     |
| $V_{AA}$              | Floating input supply voltage                                      | $V_{SS} + 4.5$        | $V_{SS} + 15$         | V     |
| $I_{AAZ}$             | Floating input positive supply zener clamp current                 | 1                     | 11                    | mA    |
| $V_{SS}$              | Floating input supply absolute voltage                             | 0                     | 200                   | V     |
| $V_{Hon}$             | High side floating output voltage, n=1-2                           | $V_S$                 | $V_B$                 | V     |
| $V_{CC}$              | Low side fixed supply voltage                                      | 10                    | 15                    | V     |
| $V_{CC2}$             | Low side fixed supply voltage                                      | 10                    | 15                    | V     |
| $ V_{CC-} - V_{CC2} $ | Low side voltages difference                                       | -                     | 1.2                   | V     |
| $V_{Lon}$             | Low side output voltage, n=1-2                                     | 0                     | $V_{CC2}$             | V     |
| $V_{GND}$             | GND pin input voltage  | $V_{SS}^{+++}$        | $V_{AA}^{+++}$        | V     |
| $V_{IN-n}$            | Inverting input voltage, n=1-2                                     | $V_{GND} - 0.5^{+++}$ | $V_{GND} + 0.5^{+++}$ | V     |
| $V_{CSD}$             | CSD pin input voltage  | $V_{SS}$              | $V_{AA}$              | V     |
| $V_{COMPn}$           | COMP pin input voltage, n=1-2                                      | $V_{SS}$              | $V_{AA}$              | V     |
| $C_{COMPn}$           | COMP pin phase compensation capacitor to GND, n=1-2                | 1                     | -                     | nF    |
| $V_{DT}$              | DT pin input voltage   | 0                     | $V_{CC}$              | V     |
| $I_{OREF}$            | Reference output current to COM <sup>††</sup>                      | 0.3                   | 0.8                   | mA    |
| $V_{OCSET}$           | OCSET pin input voltage  | 0.5                   | 5                     | V     |
| $V_{CSHn}$            | CSH pin input voltage, n=1-2                                       | $V_{Sn}$              | $V_{Bn}$              | V     |
| $dV_{SS}/dt$          | Allowable $V_{SS}$ voltage slew rate upon power-up <sup>++++</sup> | -                     | 50                    | V/ms  |
| $f_{SW}$              | Switching Frequency  | -                     | 800                   | kHz   |
| $T_A$                 | Ambient Temperature  | -40                   | 125                   | °C    |

† Logic operational for  $V_{sn}$  equal to  $-5V$  to  $+200V$ . Logic state held for  $V_{sn}$  equal to  $-5V$  to  $-V_{BSn}$ .

†† Nominal voltage for  $V_{REF}$  is 5.1V.  $I_{OREF}$  of 0.3 – 0.8mA dictates total external resistor value on  $V_{REF}$  to be 6.3k to 16.7k ohm.

††† GND input voltage is limited by  $I_{IN-n}$ .

++++  $V_{ss}$  ramps up from 0V to 200V.

**Electrical Characteristics**

$V_{CC}=V_{CC2}=V_{BS1}=V_{BS2}=V_{BS3}=V_{BS4}=12V$ ,  $V_{SS}=V_{S1}=V_{S2}=COM=COM2=0V$ ,  $V_{GND}=5V$ ,  $V_{AA}=10V$ ,  $C_L=1nF$  and  $T_A=25^{\circ}C$  unless otherwise specified.

| Symbol                            | Definition   | Min  | Typ  | Max  | Units | Test Conditions  |
|-----------------------------------|--|------|------|------|-------|--|
| <b>Low Side Supply 1</b>          |  |      |      |      |       |  |
| UV <sub>CC+</sub>                 | V <sub>CC</sub> supply UVLO positive threshold                               | 8.4  | 8.9  | 9.4  | V     |  |
| UV <sub>CC-</sub>                 | V <sub>CC</sub> supply UVLO negative threshold                               | 8.2  | 8.7  | 9.2  | V     |  |
| UV <sub>CC</sub> HYS              | UV <sub>CC</sub> hysteresis  | -    | 0.2  | -    | V     |  |
| I <sub>QCC</sub>                  | Low side quiescent current   | -    | -    | 5    | mA    | V <sub>DT</sub> =V <sub>CC</sub>                         |
| V <sub>CLAMPL1</sub>              | Low side zener diode clamp voltage   | 19.6 | 20.4 | 21.6 | V     | I <sub>CC</sub> =10mA                                    |
| <b>Low Side Supply 2</b>          |  |      |      |      |       |  |
| I <sub>QCC2</sub>                 | Low side quiescent current   | -    | -    | 4    | mA    |  |
| V <sub>CLAMPL2</sub>              | Low side zener diode clamp voltage   | 19.6 | 20.4 | 21.6 | V     | I <sub>CC2</sub> =10mA                                   |
| <b>High Side Floating Supply</b>  |  |      |      |      |       |  |
| UV <sub>BS+n</sub>                | High side well UVLO positive threshold, n=1-2                                | 8.0  | 8.5  | 9.0  | V     |  |
| UV <sub>BS-n</sub>                | High side well UVLO negative threshold, n=1-2                                | 7.8  | 8.3  | 8.8  | V     |  |
| UV <sub>BS</sub> HYS <sub>n</sub> | UV <sub>BS</sub> hysteresis, n=1-2   | -    | 0.2  | -    | V     |  |
| I <sub>QBSn</sub>                 | High side quiescent current, n=1-2   | -    | -    | 1    | mA    |  |
| I <sub>LKHn</sub>                 | High to Low side leakage current, n=1-2                                      | -    | -    | 50   | μA    | V <sub>Bn</sub> =V <sub>Sn</sub> =200V                   |
| V <sub>CLAMP<sub>Hn</sub></sub>   | High side zener diode clamp voltage, n=1-2                                   | 14.7 | 15.3 | 16.2 | V     | I <sub>BSn</sub> =5mA                                    |
| <b>Floating Input Supply</b>      |  |      |      |      |       |  |
| UV <sub>AA+</sub>                 | V <sub>AA</sub> floating supply UVLO positive threshold from V <sub>SS</sub> | 8.2  | 8.7  | 9.2  | V     | GND pin floating   |
| UV <sub>AA-</sub>                 | V <sub>AA</sub> floating supply UVLO negative threshold from V <sub>SS</sub> | 7.7  | 8.2  | 8.7  | V     | GND pin floating   |
| UV <sub>AA</sub> HYS              | UV <sub>AA</sub> hysteresis  | -    | 0.5  | -    | V     | GND pin floating   |
| I <sub>QAASD</sub>                | Floating Input positive quiescent supply current in shutdown mode            | -    | 1.5  | 3    | mA    | V <sub>CSD</sub> =V <sub>SS</sub>                        |
| I <sub>QAA10</sub>                | Floating Input positive quiescent supply current, positive input             | -    | 7    | 10   | mA    | V <sub>IN</sub> =V <sub>SS</sub> +5.2V                   |
| I <sub>QAA11</sub>                | Floating Input positive quiescent supply current, negative input             | -    | 5    | 8    | mA    | V <sub>IN</sub> =V <sub>SS</sub> +4.8V                   |
| I <sub>QAAST</sub>                | Floating Input positive quiescent supply current in start-up mode            | -    | 8    | 12   | mA    | V <sub>CSD</sub> =V <sub>SS</sub> +5.0V                  |
| I <sub>LKM</sub>                  | Floating input side to Low side leakage current                              | -    | -    | 50   | μA    | V <sub>AA</sub> =V <sub>SS</sub> =V <sub>GND</sub> =100V |
| V <sub>CLAMP<sub>M</sub></sub>    | Floating supply zener diode clamp voltage                                    | 19.6 | 20.4 | 22.6 | V     | I <sub>AA</sub> =5mA, V <sub>CSD</sub> =V <sub>SS</sub>  |

**Electrical Characteristics (Cont'd)**

| Symbol   | Definition  | Min                  | Typ                                    | Max                  | Units | Test Conditions                             |
|--|---|----------------------|--|----------------------|-------|---|
| <b>Audio Input</b> (GND=0V, V <sub>AA</sub> =5V, V <sub>SS</sub> =-5V, COM=COM2=V <sub>CC</sub> =V <sub>CC2</sub> =-5V, V <sub>S1</sub> =V <sub>S2</sub> =CSH1=CSH2=-5V, DT=OCSET=-5V) |   |                      |  |                      |       |   |
| V <sub>Osn</sub>   | CHn input offset voltage, n=1-2                         | -15                  | 0                                      | 15                   | mV    |   |
| I <sub>BINn</sub>  | CHn input bias current, n=1-2                           | -                    | -                                      | 40                   | nA    |   |
| GBWn   | CHn small signal bandwidth, n=1-2                       | -                    | 9                                      | -                    | MHz   | C <sub>COMPn</sub> =1nF, R <sub>fn</sub> =0 |
| V <sub>COMPn</sub>   | CHn OTA Output voltage, n=1-2                           | V <sub>AA</sub> -1   | -                                      | V <sub>SS</sub> +1   | V     |   |
| g <sub>mn</sub>  | CHn OTA transconductance, n=1-2                         | -                    | 100                                    | -                    | mS    | V <sub>IN-n</sub> =10mV                     |
| G <sub>Vn</sub>  | CHn OTA gain, n=1-2                                     | 60                   | -                                      | -                    | dB    |   |
| V <sub>Nrmsn</sub>   | CHn OTA input noise voltage, n=1-2                      | -                    | 250                                    | -                    | mVrms | BW=20kHz, Resolution BW=22Hz Fig.5          |
| SRn  | CHn slew rate, n=1-2                                    | -                    | ±5                                     | -                    | V/us  | C <sub>COMPn</sub> =1nF                     |
| CMRRn  | CHn common-mode rejection ratio, n=1-2                  | -                    | 60                                     | -                    | dB    |   |
| PSRRn  | CHn supply voltage rejection ratio, n=1-2               | -                    | 65                                     | -                    | dB    |   |
| V <sub>th+CLIPn</sub>  | CHn clip detection positive threshold, n=1-2            | 0.85xV <sub>AA</sub> | 0.90xV <sub>AA</sub>                   | 0.95xV <sub>AA</sub> | V     |   |
| V <sub>th-CLIPn</sub>  | CHn clip detection negative threshold, n=1-2            | 0.05xV <sub>AA</sub> | 0.10xV <sub>AA</sub>                   | 0.15xV <sub>AA</sub> | V     |   |
| t <sub>CLIPn</sub>   | CHn clipping detection propagation delay, n=1-2         | -                    | 40                                     | -                    | ns    | Note 1                                      |
| t <sub>CLIPmin</sub>   | CHn clipping detection minimum output duration          | -                    | 3                                      | -                    | us    | Note 1                                      |
| <b>PWM comparator</b>  |   |                      |  |                      |       |   |
| V <sub>thPWM</sub>   | PWM comparator threshold in COMP                        | -                    | (V <sub>AA</sub> - V <sub>SS</sub> )/2 | -                    | V     |   |
| f <sub>OTAn</sub>  | CHn COMP pin star-up local oscillation frequency, n=1-3 | 0.6                  | 1.0                                    | 1.5                  | MHz   | V <sub>CSD</sub> =VSS+5V                    |



**Electrical Characteristics (Cont'd)**

| Symbol   | Definition  | Min           | Typ           | Max           | Units | Test Conditions |
|--|---|---------------|---------------|---------------|-------|-----------------|
| <b>Clock Oscillator</b>                        |   |               |               |               |       |                 |
| $I_{CK1SINK}, I_{CK2SINK}$                     | X1B, X2B pins output sink current at $V_{X1B}, V_{X2B} = 0.5V$            | -             | -             | 20            | mA    |                 |
| $I_{CK1SOURCE}, I_{CK2SOURCE}$                 | X1B, X2B pins output source current at $V_{X1B}, V_{X2B} = V_{AA} - 0.5V$ | -             | -             | -20           | mA    |                 |
| $V_{OLCK1}, V_{OLCK2}$                         | X1B, X2B pins low level output voltage                                    | -             | -             | 0.07          | V     |                 |
| $V_{OHCK1}, V_{OHCK2}$                         | X1B, X2B pins high level output voltage                                   | -             | -             | 9.95          | V     |                 |
| $V_{ILCK1}, V_{ILCK2}$                         | X1A, X2A pins input low voltage   | -             | -             | 2             | V     |                 |
| $V_{IHCK1}, V_{IHCK2}$                         | X1A, X2A pins input high voltage  | 8             | -             | -             | V     |                 |
| $I_{IN1}, I_{IN2}$                             | X1A, X2A pins input current   | -             | -             | +/- 20        | uA    |                 |
| $C_{IN1}, C_{IN2}$                             | X1A, X2A pins input capacitance at X1A, X2A pins                          | -             | 1             | -             | pF    | Note 1          |
| $t_{ONCK1}, t_{OFFCK1}, t_{ONCK2}, t_{OFFCK2}$ | Propagation delay time from X1A to X1B, X2A to X2B                        | -             | 40            | -             | ns    |                 |
| $V_{thCKSL1}$                                  | CKSL pin threshold 1  | $0.61xV_{AA}$ | $0.67xV_{AA}$ | $0.74xV_{AA}$ | V     |                 |
| $V_{thCKSL2}$                                  | CKSL pin threshold 2  | $0.29xV_{AA}$ | $0.33xV_{AA}$ | $0.37xV_{AA}$ | V     |                 |

**Electrical Characteristics (Cont'd)**

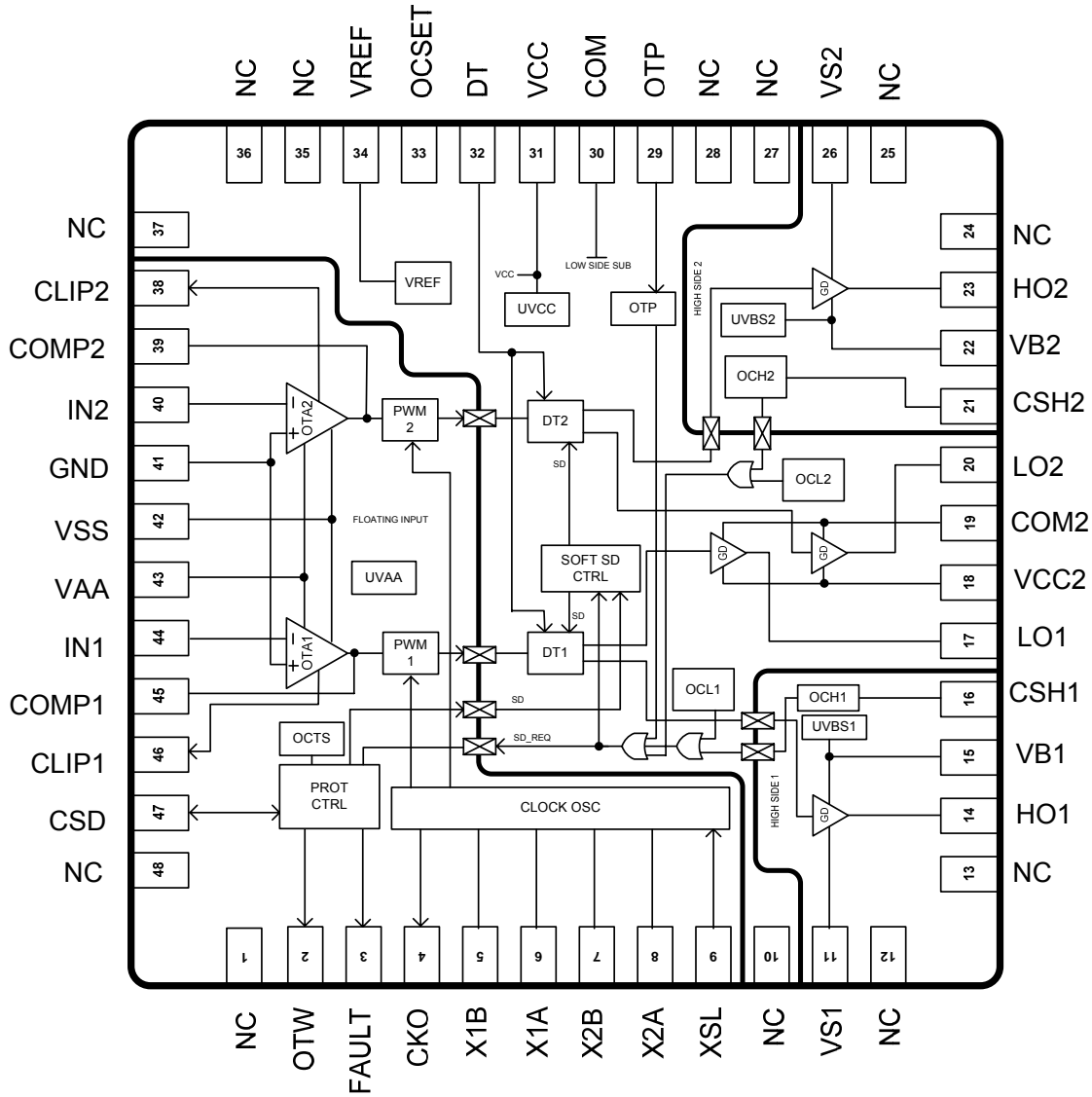
| Symbol            | Definition  | Min           | Typ             | Max           | Units | Test Conditions                           |
|-------------------|---|---------------|-----------------|---------------|-------|---|
| <b>Protection</b> |   |               |                 |               |       |   |
| $V_{REF}$         | Reference output voltage  | 4.8           | 5.1             | 5.4           | V     | $I_{OREF} = 0.5mA$                        |
| $V_{th_{OCLn}}$   | CHn low side OC threshold in $V_{sn}$ , n=1-2                                     | 1.1           | 1.2             | 1.3           | V     | OCSET=1.2V                                |
| $V_{th_{OCHn}}$   | CHn high side OC threshold in $V_{CSHn}$ , n=1-2                                  | 1.1+ $V_s$    | 1.2+ $V_s$      | 1.3+ $V_s$    | V     | $V_s=200V$ ,                              |
| $V_{ETO}$         | External OTP pin open circuit voltage   | 4.8           | 5.1             | 5.4           | V     |   |
| $V_{ETW}$         | External OTP pin warning threshold  | 1.1           | 1.4             | 1.6           | V     |   |
| $V_{ETSD}$        | External OTP pin shutdown threshold   | 2.3           | 2.8             | 3.3           | V     |   |
| $I_{ET}$          | External OTP bias sourcing current  | 0.43          | 0.65            | 0.87          | mA    | OTP=0V                                    |
| $T_W$             | On-chip thermal warning   | -             | $T_{SD}$<br>-20 | -             | °C    | Note 1                                    |
| $T_{SD}$          | ON-chip thermal shutdown  | -             | 150             | -             | °C    |   |
| $T_{WHYT}$        | On-chip thermal warning hysteresis  | -             | 15              | -             | °C    |   |
| $T_{SDHYT}$       | ON-chip thermal shutdown hysteresis   | -             | 15              | -             | °C    |   |
| $V_{th1}$         | CSD pin shutdown release threshold  | $0.62xV_{AA}$ | $0.70xV_{AA}$   | $0.78xV_{AA}$ | V     |   |
| $V_{th2}$         | CSD pin self reset threshold  | $0.26xV_{AA}$ | $0.30xV_{AA}$   | $0.34xV_{AA}$ | V     |   |
| $I_{CSD+}$        | CSD pin discharge current   | 70            | 100             | 130           | μA    | $V_{CSD} = V_{SS} + 7.5V$                 |
| $I_{CSD-}$        | CSD pin charge current  | 70            | 100             | 130           | μA    | $V_{CSD} = V_{SS} + 7.5V$                 |
| $V_{FAULT}$       | FAULT pin warning output voltage  | -             | GND             | GND<br>+0.1   | V     | $R_{PULL-UP} = 10k$                       |
| $V_{OTW}$         | OTW pin warning output voltage  | -             | GND             | GND<br>+0.1   | V     | $R_{PULL-UP} = 10k$                       |
| $t_{SSDn}$        | CHn soft shutdown propagation delay from $V_{CSD} < V_{SS} + V_{th1}$ to Shutdown | -             | -               | 1.4           | us    | $f_{PWM}=400kHz$ ,<br>Fig.2               |
| $t_{OCHn}$        | CHn propagation delay time from $V_{CSHn} > V_{th_{OCHn}}$ to Shutdown, n=1-2     | -             | -               | 800           | ns    | Fig.4                                     |
| $t_{OCLn}$        | CHn propagation delay time from $V_{sn} > V_{th_{OCL}}$ to Shutdown, n=1-2        | -             | -               | 700           | ns    | Fig.3                                     |
| $P_{SD}$          | Shutdown timing   | -             | 40              | -             | %     | $f_{PWM}=400kHz$ ,<br>Duty= 50%,<br>Fig.2 |

**Electrical Characteristics (Cont'd)**

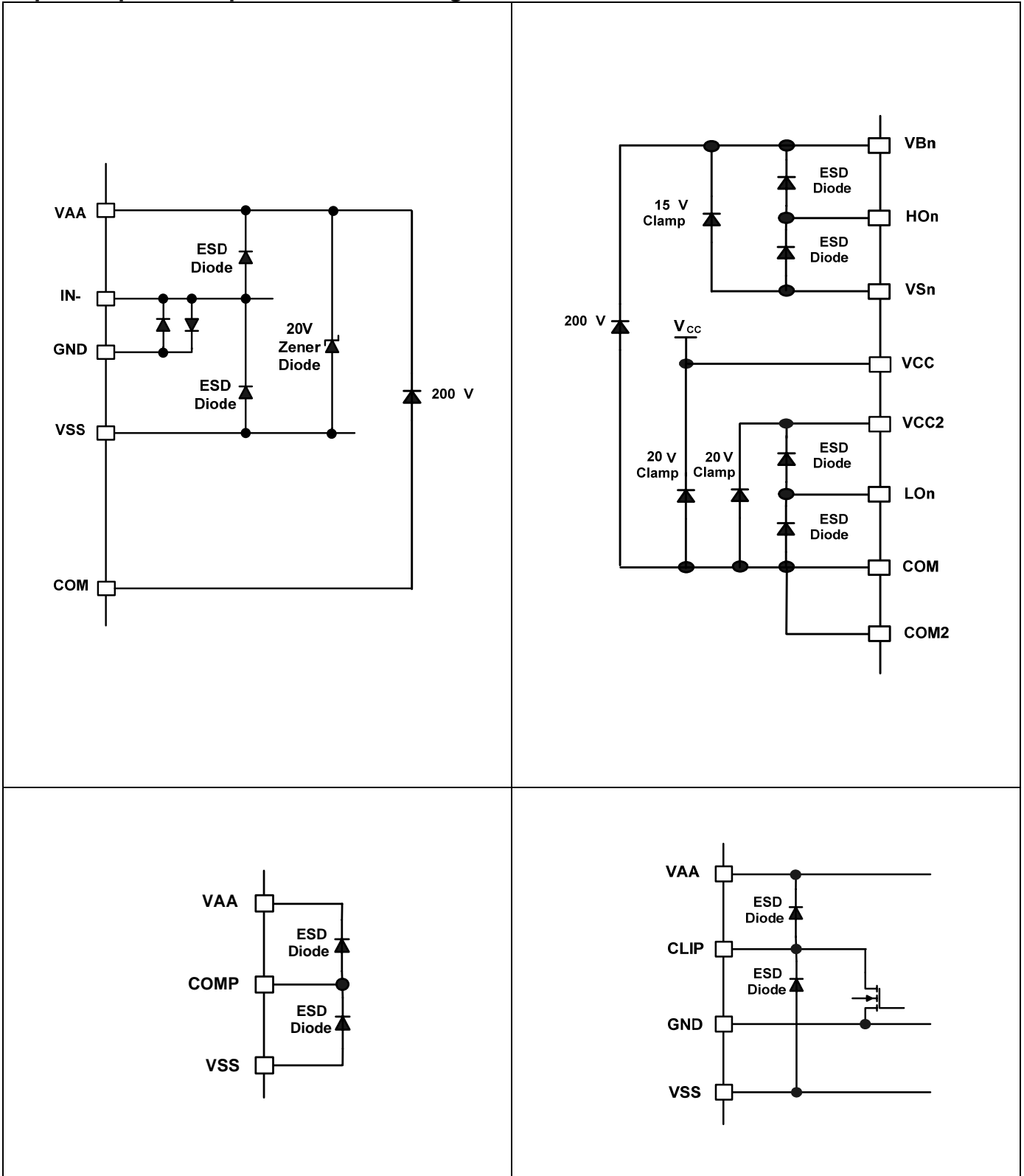
| Symbol             | Definition   | Min      | Typ      | Max      | Units | Test Conditions  |
|--------------------|--|----------|----------|----------|-------|--|
| <b>Gate Driver</b> |  |          |          |          |       |  |
| Io+n               | CHn output high short circuit current (Source) , n=1-2   | -        | 0.5      | -        | A     | Vo=0V,<br>PW≤10μS,<br>Note 1                           |
| Io-n               | CHn output low short circuit current (Sink) , n=1-2  | -        | 0.6      | -        | A     | Vo=12V,<br>PW≤10μS,<br>Note 1                          |
| VOLn               | CHn low level out put voltage LO – COM, HO - VS, n=1-2   | -        | -        | 0.1      | V     | Io=0A  |
| VOHn               | CHn high level out put voltage VCC – LO, VB - HO, n=1-2  | -        | -        | 1.4      | V     |  |
| Ton0n              | CHn high and low side turn-on propagation delay, n=1-2   | -        | 350      | -        | ns    | V <sub>DT</sub> = V <sub>CC</sub>                      |
| Toff0n             | CHn high and low side turn-off propagation delay, n=1-2  | -        | 325      | -        | ns    |  |
| tr                 | Turn-on rise time  | -        | 25       | 50       | ns    |  |
| tf                 | Turn-off fall time   | -        | 20       | 40       | ns    |  |
| DT1n               | CHn deadtime: LOn turn-off to HOn turn-on (DT <sub>LO-HO</sub> ) & HOn turn-off to LnO turn-on (DT <sub>HO-LO</sub> )                                  | 30       | 45       | 60       | ns    | V <sub>DT</sub> >V <sub>DT1</sub> ,                    |
| DT2n               | CHn deadtime: LOn turn-off to HOn turn-on (DT <sub>LO-HO</sub> ) & HOn turn-off to LOn turn-on (DT <sub>HO-LO</sub> )                                  | 45       | 65       | 85       | ns    | V <sub>DT1</sub> >V <sub>DT</sub> > V <sub>DT2</sub> , |
| DT3n               | CHn deadtime: LOn turn-off to HOn turn-on (DT <sub>LO-HO</sub> ) & HOn turn-off to LOn turn-on (DT <sub>HO-LO</sub> )                                  | 60       | 85       | 110      | ns    | V <sub>DT2</sub> >V <sub>DT</sub> > V <sub>DT3</sub> , |
| DT4n               | CHn deadtime: LOn turn-off to HOn turn-on (DT <sub>LO-HO</sub> ) & HO turn-off to LOn turn-on (DT <sub>HO-LO</sub> )V <sub>DT</sub> = V <sub>DT4</sub> | 80       | 105      | 145      | ns    | V <sub>DT</sub> <V <sub>DT3</sub>                      |
| V <sub>DT1</sub>   | DT mode select threshold 1   | 0.51xVcc | 0.57xVcc | 0.63xVcc | V     |  |
| V <sub>DT2</sub>   | DT mode select threshold 2   | 0.32xVcc | 0.36xVcc | 0.40xVcc | V     |  |
| V <sub>DT3</sub>   | DT mode select threshold 3   | 0.21xVcc | 0.23xVcc | 0.25xVcc | V     |  |

Note 1 Guaranteed by design, but not tested in production.

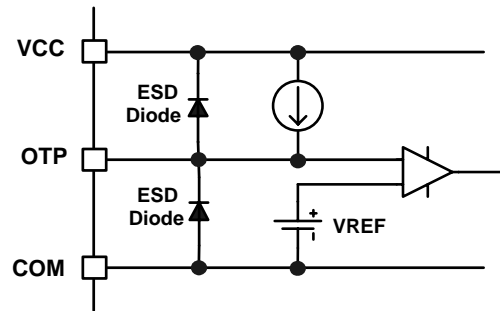
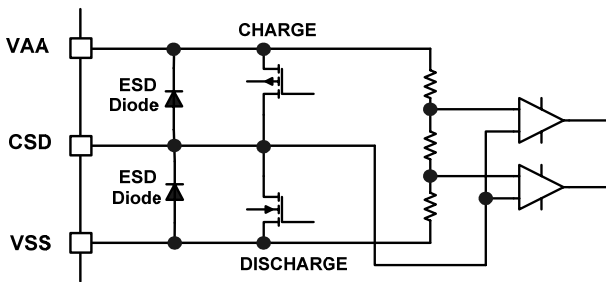
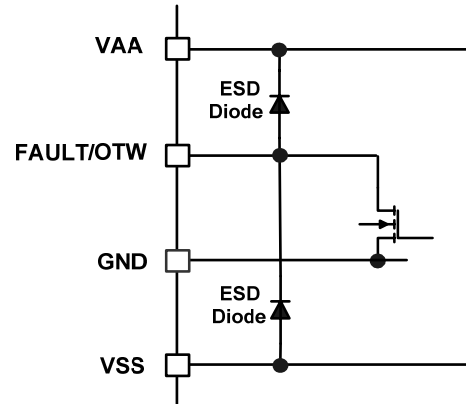
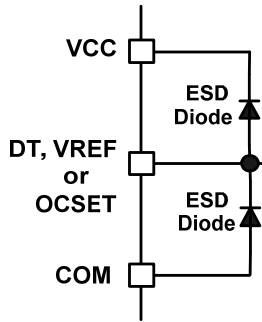
**Functional Block Diagram**



**Input/Output Pin Equivalent Circuit Diagrams**



**Input/Output Pin Equivalent Circuit Diagrams (Cont'd)**



**Lead Definitions**

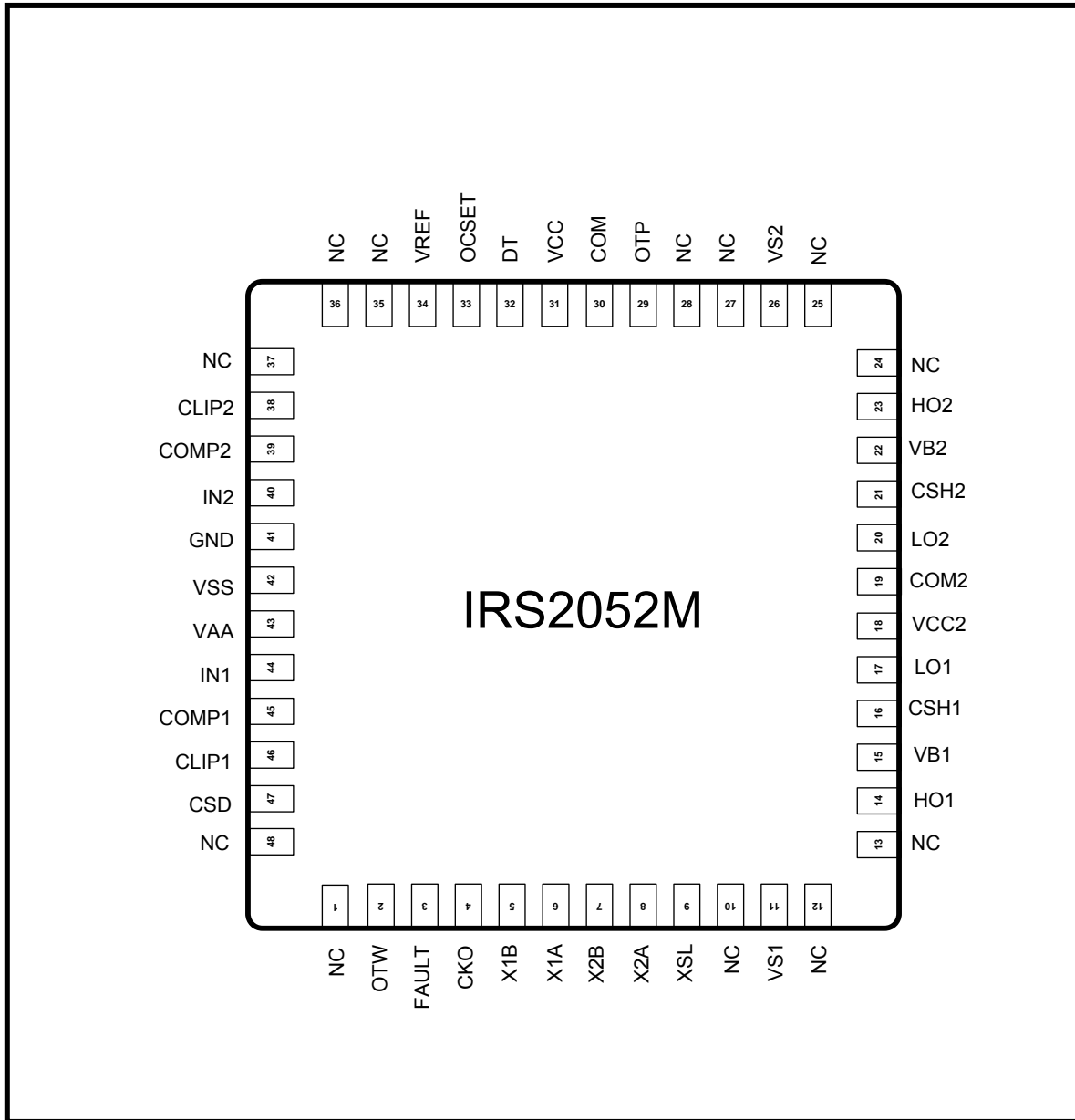
| Pin # | Symbol | I/O | Description  |
|-------|--------|-----|--|
| 1     | NC     |     |  |
| 2     | OTW    | O   | On-chip over temperature warning output                        |
| 3     | FAULT  | O   | Fault reporting output   |
| 4     | CKO    | O   | Clock output   |
| 5     | X1B    | O   | Clock oscillator output 1                                      |
| 6     | X1A    | I   | Clock oscillator input 1                                       |
| 7     | X2B    | O   | Clock oscillator output 2                                      |
| 8     | X2A    | I   | Clock oscillator input 2                                       |
| 9     | XSL    | I   | Clock oscillator select (VAA: osc 1, GND: osc 2, VSS: No sync) |
| 10    | NC     |     |  |
| 11    | VS1    | I   | CH1 High side floating supply return                           |
| 12    | NC     |     |  |
| 13    | NC     |     |  |
| 14    | HO1    | O   | CH1 High side output   |
| 15    | VB1    | I   | CH1 High side floating supply                                  |
| 16    | CSH1   | I   | CH1 High side over current sensing input, referenced to VS1    |
| 17    | LO1    | O   | CH1 Low side output  |
| 18    | VCC2   | I   | Low side gate drive supply                                     |
| 19    | COM2   | I   | Low side gate drive supply return                              |
| 20    | LO2    | O   | CH2 Low side output  |
| 21    | CSH2   | I   | CH2 High side over current sensing input, referenced to VS2    |
| 22    | VB2    | I   | CH2 High side floating supply                                  |
| 23    | HO2    | O   | CH2 High side output   |
| 24    | NC     |     |  |

**Lead Definitions (Cont'd)**

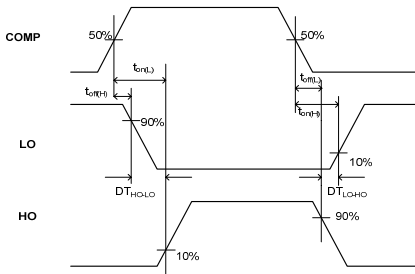
| Pin # | Symbol | I/O | Description  |
|-------|--------|-----|--|
| 25    | NC     |     |  |
| 26    | VS2    | I   | CH2 High side floating supply return                         |
| 27    | NC     |     |  |
| 28    | NC     |     |  |
| 29    | OTP    | I   | Over temperature sensor input, referenced to COM             |
| 30    | COM    | I   | Low side gate drive supply return                            |
| 31    | VCC    | I   | Low side gate drive supply                                   |
| 32    | DT     | I   | Deadtime program, reference to COM                           |
| 33    | OCSET  | I   | Low side OCP threshold, referenced to COM                    |
| 34    | VREF   | O   | 5.1V reference voltage output for OCSET                      |
| 35    | NC     |     |  |
| 36    | NC     |     |  |
| 37    | NC     |     |  |
| 38    | CLIP2  | O   | Clipping detection output CH2, open drain, referenced to GND |
| 39    | COMP2  | O   | CH2 PWM comparator input                                     |
| 40    | IN2    | I   | CH2 inverting audio input                                    |
| 41    | GND    | I   | Input reference GND  |
| 42    | VSS    | I   | Floating input negative supply                               |
| 43    | VAA    | I   | Floating input positive supply                               |
| 44    | IN1    | I   | CH1 inverting audio input                                    |
| 45    | COMP1  | O   | CH1 PWM comparator input                                     |
| 46    | CLIP1  | O   | Clipping detection output CH1, open drain, referenced to GND |
| 47    | CSD    | I/O | Protection control   |
| 48    | NC     |     |  |



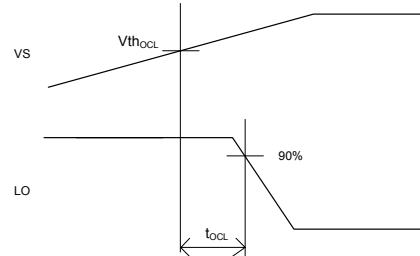
**Lead Assignments (MLPQ48\_7x7mm)**



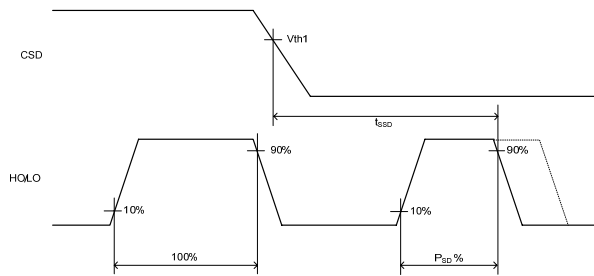
**Application Information and Additional Details**



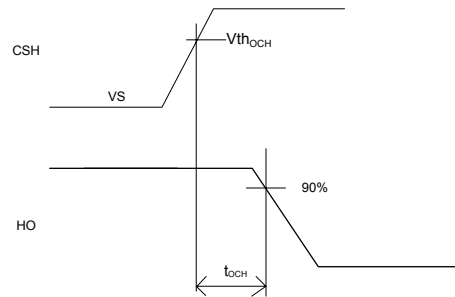
**Figure 1 Switching Time Waveform Definitions**



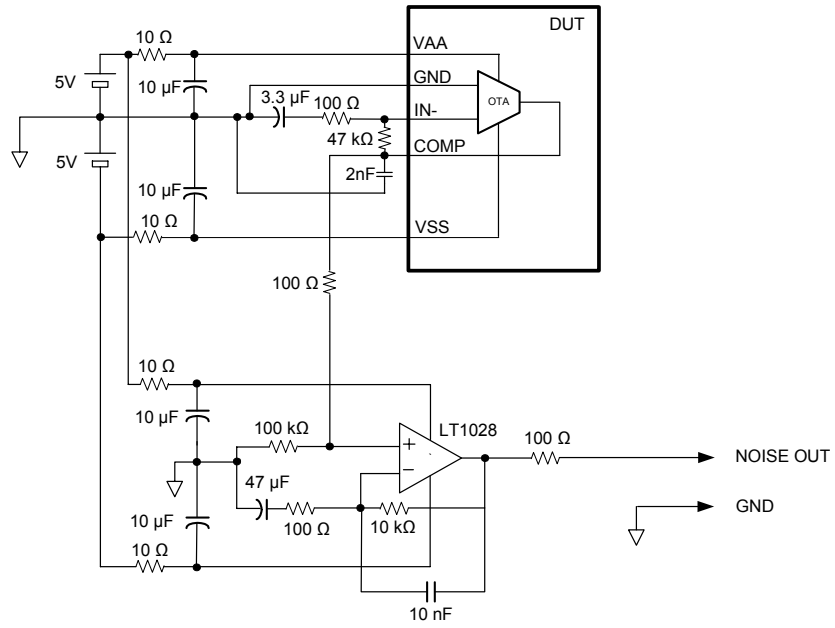
**Figure 3  $V_s > V_{th_{OCL}}$  to Shutdown Waveform**



**Figure 2 CSD to Shutdown Waveform Definitions**

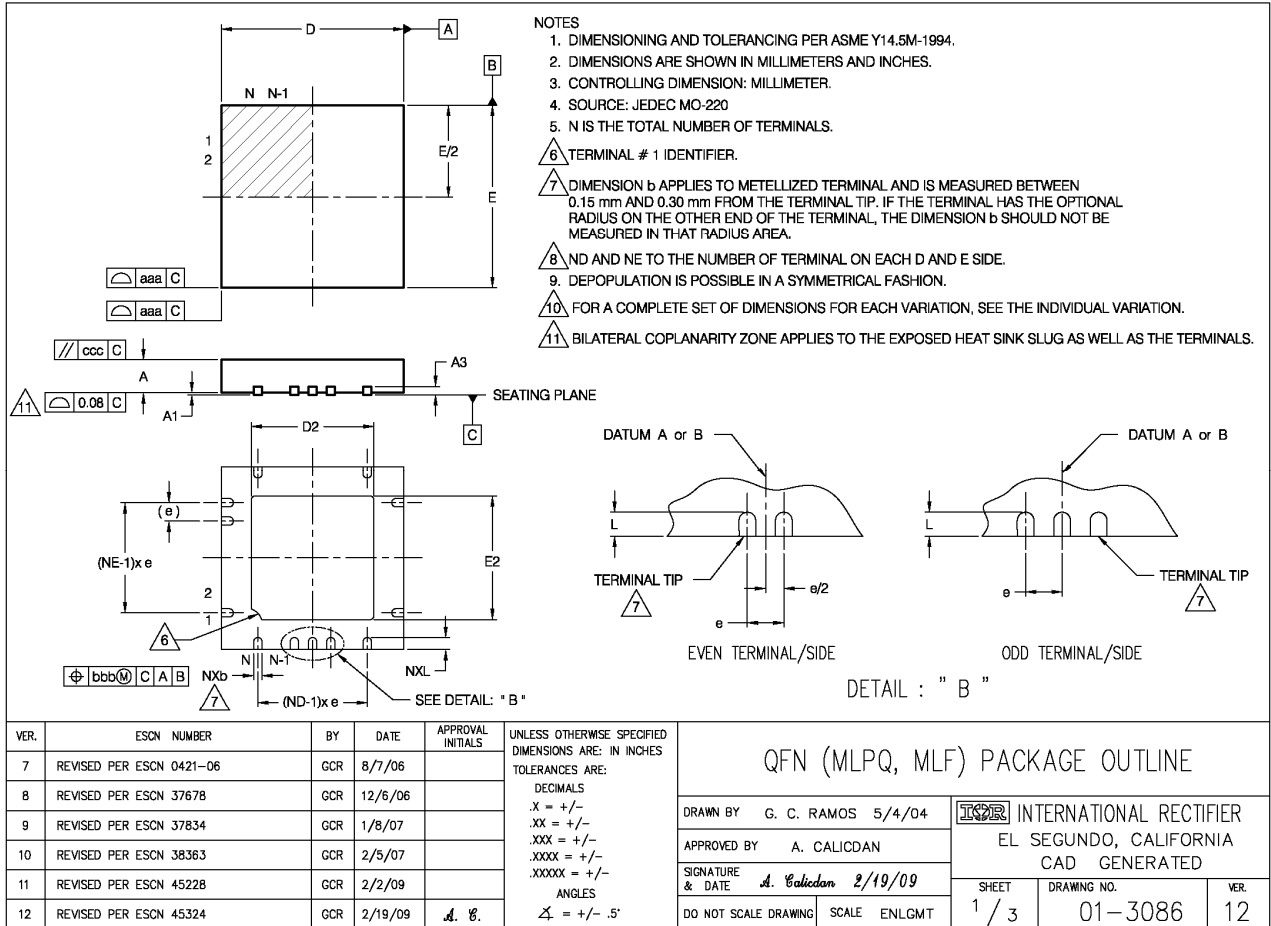


**Figure 4  $V_{C_{SH}} > V_{th_{OCH}}$  to Shutdown Waveform**



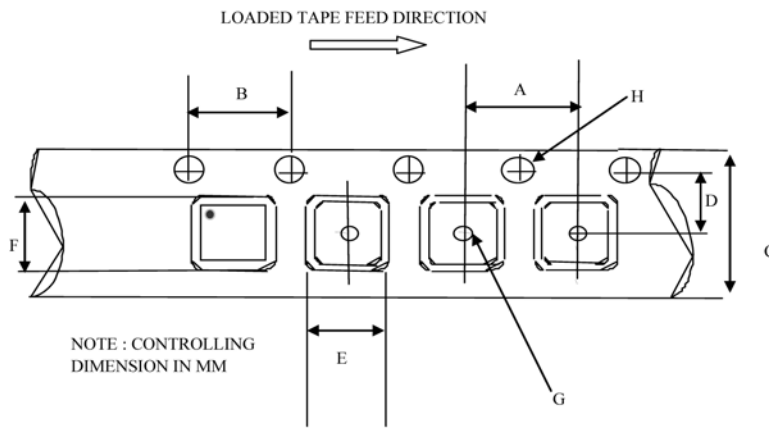
**Figure 5: OTA input noise voltage mesurent circuit**

Package Details: MLPQ 7X7



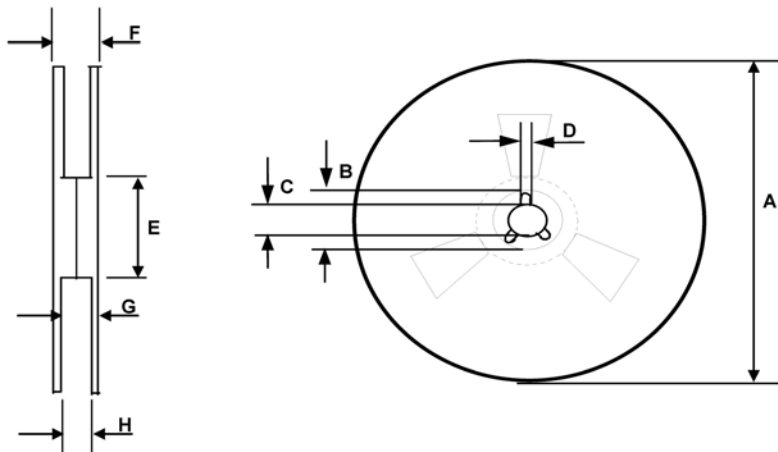
| SYMBOL | VKKD-4NJ1   |      |      |            |       |       |
|--------|-------------|------|------|------------|-------|-------|
|        | MILLIMETERS |      |      | INCHES     |       |       |
|        | MIN         | NOM  | MAX  | MIN        | NOM   | MAX   |
| A      | 0.80        | 0.90 | 1.00 | .032       | .035  | .039  |
| A1     | 0.00        | 0.02 | 0.05 | .000       | .0008 | .0019 |
| A3     | 0.20 REF    |      |      | .008 REF   |       |       |
| b      | 0.18        | 0.25 | 0.30 | .0071      | .0098 | .0118 |
| D2     | 5.40        | 5.55 | 5.65 | .213       | .219  | .222  |
| D      | 7.00 BSC    |      |      | .276 BSC   |       |       |
| E      | 7.00 BSC    |      |      | .276 BSC   |       |       |
| E2     | 5.40        | 5.55 | 5.65 | .213       | .219  | .222  |
| L      | 0.30        | 0.40 | 0.50 | .012       | .016  | .020  |
| e      | 0.50 PITCH  |      |      | .020 PITCH |       |       |
| N      | 48          |      |      | 48         |       |       |
| ND     | 12          |      |      | 12         |       |       |
| NE     | 12          |      |      | 12         |       |       |
| aaa    | 0.15        |      |      | .0059      |       |       |
| bbb    | 0.10        |      |      | .0039      |       |       |
| ccc    | 0.10        |      |      | .0039      |       |       |
| ddd    | 0.05        |      |      | .0019      |       |       |

**Tape and Reel Details: MLPQ 7X7**



CARRIER TAPE DIMENSION FOR 48MLPQ7X7

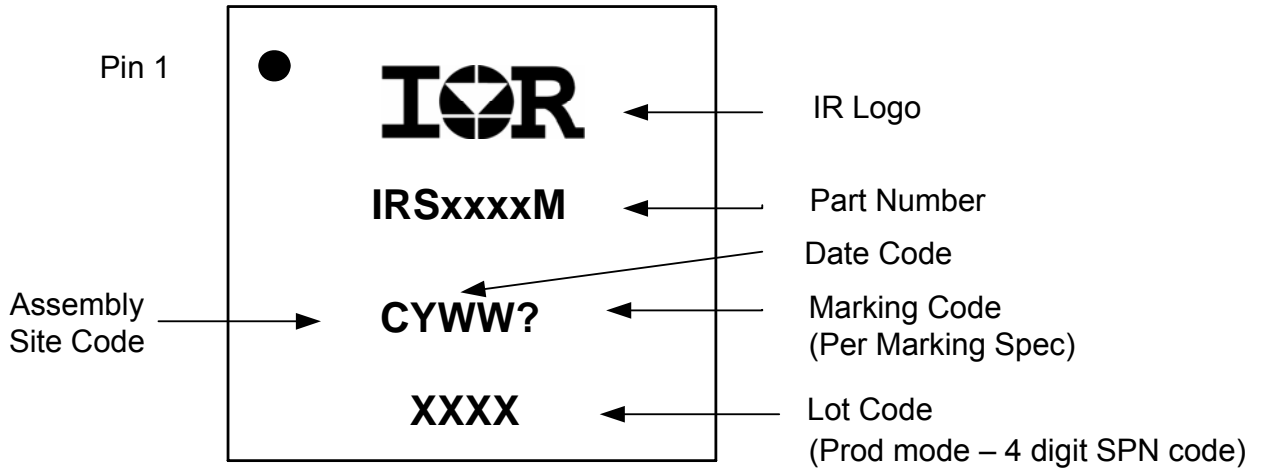
| Code | Metric |       | Imperial |       |
|------|--------|-------|----------|-------|
|      | Min    | Max   | Min      | Max   |
| A    | 11.90  | 12.10 | 0.474    | 0.476 |
| B    | 3.90   | 4.10  | 0.153    | 0.161 |
| C    | 15.70  | 16.30 | 0.618    | 0.641 |
| D    | 7.40   | 7.60  | 0.291    | 0.299 |
| E    | 7.15   | 7.35  | 0.281    | 0.289 |
| F    | 7.15   | 7.35  | 0.281    | 0.289 |
| G    | 1.50   | n/a   | 0.059    | n/a   |
| H    | 1.50   | 1.60  | 0.059    | 0.062 |



REEL DIMENSIONS FOR 48MLPQ7X7

| Code | Metric |        | Imperial |        |
|------|--------|--------|----------|--------|
|      | Min    | Max    | Min      | Max    |
| A    | 329.60 | 330.25 | 12.976   | 13.001 |
| B    | 20.95  | 21.45  | 0.824    | 0.844  |
| C    | 12.80  | 13.20  | 0.503    | 0.519  |
| D    | 1.95   | 2.45   | 0.767    | 0.096  |
| E    | 98.00  | 102.00 | 3.858    | 4.015  |
| F    | n/a    | 22.4   | n/a      | 0.881  |
| G    | 18.5   | 21.1   | 0.728    | 0.83   |
| H    | 16.4   | 18.4   | 0.645    | 0.724  |

**Part Marking Information**



**Ordering Information**

| Base Part Number | Package Type | Standard Pack |          | Complete Part Number |
|------------------|--------------|---------------|----------|----------------------|
|                  |              | Form          | Quantity |                      |
| IRS2052M         | MLPQ 48 7x7  | Tape and Reel | 3000     | IRS2052MTRPBF        |

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