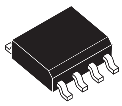
LCP1521S/LCP152DEE

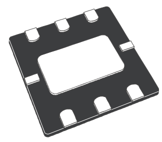
ASD (Application Specific Devices)
Programmable transient voltage suppressor for SLIC protection

Features

- Dual programmable transient suppressor
- Wide negative firing voltage range:
  V_{MGL} = -150 V max.
- Low dynamic switching voltages:
  V_{FP} and V_{DGL}
- Low gate triggering current: I_{GT} = 5 mA max
- Peak pulse current: I_{PP} = 30 A (10/1000 µs)
- Holding current: I_H = 150 mA min
- Low space consuming package



SO-8
LCP1521S



QFN 3x3 6 leads
LCP152DEE

Order codes

Part Number	Marking
LCP1521S	CP152S
LCP1521SRL	CP152S
LCP152DEERL	LCP152

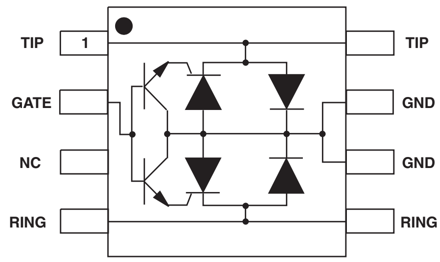
Description

These devices have been especially designed to protect new high voltage, as well as classical SLICs, against transient overvoltages.

Positive overvoltages are clamped by 2 diodes. Negative surges are suppressed by 2 thyristors, their breakdown voltage being referenced to -V_{BAT} through the gate.

These components present a very low gate triggering current (I_{GT}) in order to reduce the current consumption on printed circuit board during the firing phase.

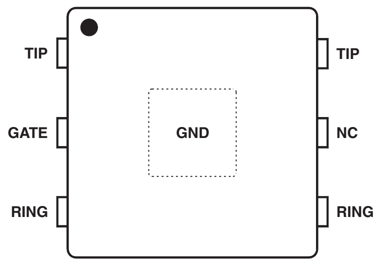
Figure 1. LCP1521S Functional diagram



Benefits

TRISILs™ are not subject to ageing and provide a fail safe mode in short circuit for a better level of protection. Trisils are used to ensure equipment meets various standards such as UL60950, IEC950 / CSA C22.2, UL1459 and FCC part 68. Trisils have UL94 V0 approved resin (Trisils are UL497B approved [file: E136224]).

Figure 2. LCP152DEE Functional diagram



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1 Characteristics

Table 1. Standards compliance

Standard	Peak surge voltage (V)	Voltage waveform	Required peak current (A)	Current waveform	Minimum serial resistor to meet standard (Ω)
GR-1089 Core First level	2500 1000	2/10 µs 10/1000 µs	500 100	2/10 µs 10/1000 µs	12 24
GR-1089 Core Second level	5000	2/10 µs	500	2/10 µs	24
GR-1089 Core Intra-building	1500	2/10 µs	100	2/10 µs	0
ITU-T-K20/K21	6000 1500	10/700 µs	150 37.5	5/310 µs	110 0
ITU-T-K20 (IEC 61000-4-2)	8000 15000	1/60 ns	ESD contact discharge ESD air discharge		0 0
VDE0433	4000 2000	10/700 µs	100 50	5/310 µs	60 10
VDE0878	4000 2000	1.2/50 µs	100 50	1/20 µs	0 0
IEC61000-4-5	4000 4000	10/700 µs 1.2/50 µs	100 100	5/310 µs 8/20 µs	60 0
FCC Part 68, lightning surge type A	1500 800	10/160 µs 10/560 µs	200 100	10/160 µs 10/560 µs	22.5 15
FCC Part 68, lightning surge type B	1000	9/720 µs	25	5/320 µs	0

Table 2. Thermal resistances

Symbol	Parameter		Value	Unit
$R_{th(j-a)}$	Junction to ambient	SO-8	120	° C/W
		QFN	140	

Table 3. Electrical characteristics (T_{amb} = 25° C)

Symbol	Parameter
I_{GT}	Gate triggering current
I_H	Holding current
I_{RM}	Reverse leakage current LINE / GND
I_{RG}	Reverse leakage current GATE / LINE
V_{RM}	Reverse voltage LINE / GND
V_{GT}	Gate triggering voltage
V_F	Forward drop voltage LINE / GND
V_{FP}	Peak forward voltage LINE / GND
V_{DGL}	Dynamic switching voltage GATE / LINE
V_{RG}	Reverse voltage GATE / LINE
C	Capacitance LINE / GND

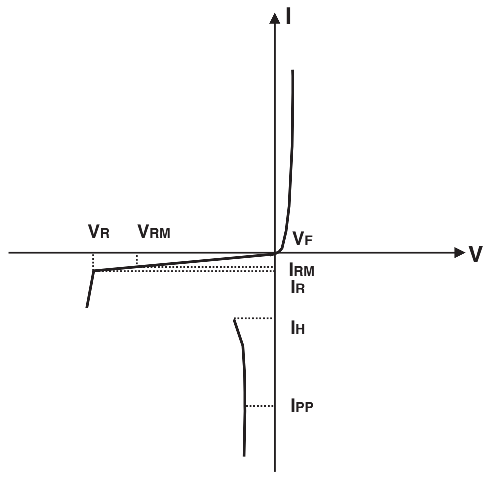


Table 4. Absolute ratings (T_{amb} = 25° C, unless otherwise specified)

Symbol	Parameter		Value	Unit
I_{PP}	Peak pulse current	10/1000 µs 8/20 µs 10/560 µs 5/310 µs 10/160 µs 1/20 µs 2/10 µs	30 100 35 40 50 100 150	A
I_{TSM}	Non repetitive surge peak on-state current (50Hz sinusoidal)	t = 20 ms t = 200 ms t = 1 s	18 10 7	A
I_{GSM}	Maximum gate current (50Hz sinusoidal)	t = 10 ms	2	A
V_{MLG} V_{MGL}	Maximum voltage LINE/GND Maximum voltage GATE/LINE	-40° C < Tamb < +85° C -40° C < Tamb < +85° C	-150 -150	V
T_{stg} T_j	Storage temperature range Maximum junction temperature		-55 to +150 150	° C
T_L	Maximum lead temperature for soldering during 10 s.		260	° C

Table 5. Repetitive peak pulse current

Symbol	Definition	Example
t_r	Rise time (µs)	Pulse waveform 10/1000 µs: t_r = 10 µs t_p = 1000 µs
t_p	Pulse duration (µs)	

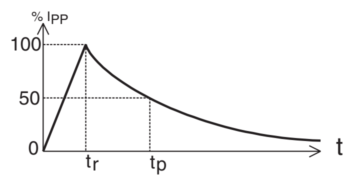


Table 6. Parameters related to the diode LINE / GND (T_{amb} = 25° C)

Symbol	Test conditions			Max	Unit
V_F	I_F = 5A		t = 500 µs	3	V
V_{FP}(1)	10/700 µs 1.2/50 µs 2/10 µs	1.5 kV 1.5 kV 2.5 kV	R_S = 10 Ω R_S = 10 Ω R_S = 62 Ω	5 9 30	V

1. See test circuit for V_{FP} (*Figure 4.*): R_S is the protection resistor located on the line card.

Table 7. Parameters related to the protection Thyristors (T_{amb} = 25° C, unless otherwise specified)

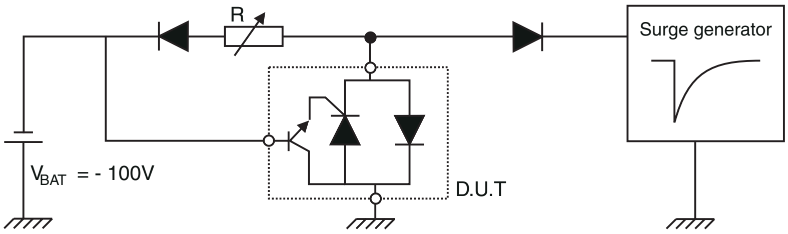
Symbol	Test conditions				Typ	Max	Unit
I_{GT}	$V_{GND / LINE}$ = -48 V				0.1	5	mA
I_H	V_{GATE} = -48 V(1)				150		mA
V_{GT}	at I_{GT}					2.5	V
I_{RG}	V_{RG} = -150 V V_{RG} = -150 V			T_j = 25° C T_j = 85° C		5 50	µA
V_{DGL}	V_{GATE} = -48 V(2) 10/700 µs 1.2/50 µs 2/10 µs	1.5 kV 1.5 kV 2.5 kV	R_S = 10 Ω R_S = 10 Ω R_S = 62 Ω	I_{PP} = 30 A I_{PP} = 30 A I_{PP} = 38 A		7 10 25	V

1. see functional holding current (I_H) test circuit
2. see test circuit for V_{DG} The oscillations with a time duration lower than 50ns are not taken into account.

Table 8. Parameters related to diode and protection Thyristors (Tamb = 25° C, unless otherwise specified)

Symbol	Test conditions			Typ	Max	Unit
I_{RM}	$V_{GATE / LINE}$ = -1 V $V_{GATE / LINE}$ = -1 V	V_{RM} = -150 V V_{RM} = -150 V	T_j = 25° C T_j = 85° C		5 50	µA
C	V_R = 50 V bias, V_{RMS} = 1 V, F = 1 MHz V_R = 2 V bias, V_{RMS} = 1 V, F = 1 MHz			15 35		pF

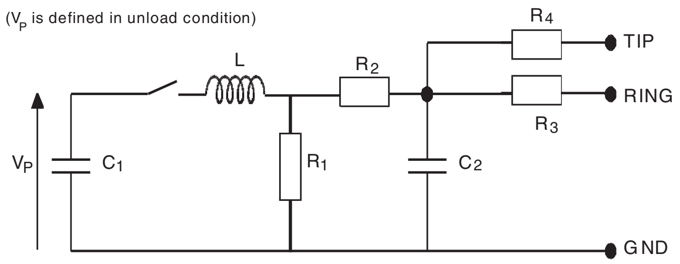
Figure 3. Functional Holding Current (I_H) test circuit: GO-NO GO test



This is a GO-NO GO test which allows to confirm the holding current (I_H) level in a functional test circuit.

TEST PROCEDURE:
- Adjust the current level at the I_H value by short circuiting the D.U.T.
- Fire the D.U.T. with a surge current: I_{PP} = 10A, 10/1000µs
- The D.U.T. will come back to the off-state within a duration of 50ms max.

Figure 4. Test circuit for V_{FP} and V_{DGL} parameters



Pulse (µs)		V_p (V)	C_1 (µF)	C_2 (nF)	L (µH)	R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	R_4 (Ω)	I_{PP} (A)	R_s (Ω)
t_r	t_p										
10	700	1500	20	200	0	50	15	25	25	30	10
1.2	50	1500	1	33	0	76	13	25	25	30	10
2	10	2500	10	0	1.1	1.3	0	3	3	38	62

2 Technical information

Figure 5. LCP152 concept behavior

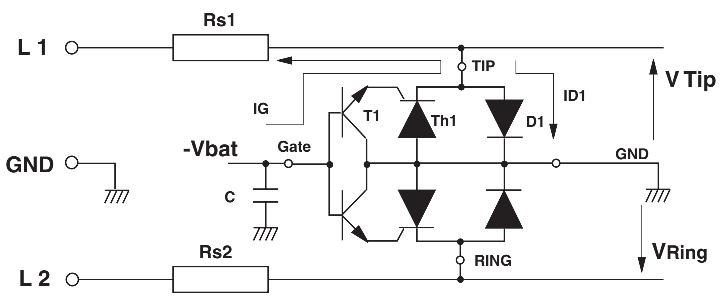


Figure 5. shows the classical protection circuit using the LCP152 crowbar concept. This topology has been developed to protect the new high voltage SLICs. It allows to program the negative firing threshold while the positive clamping value is fixed at GND.

When a negative surge occurs on one wire (L1 for example) a current IG flows through the base of the transistor T1 and then injects a current in the gate of the thyristor Th1. Th1 fires and all the surge current flows through the ground. After the surge when the current flowing through Th1 becomes less negative than the holding current IH, then Th1 switches off.

When a positive surge occurs on one wire (L1 for example) the diode D1 conducts and the surge current flows through the ground.

Figure 6. Example of PCB layout based on LCP152S protection

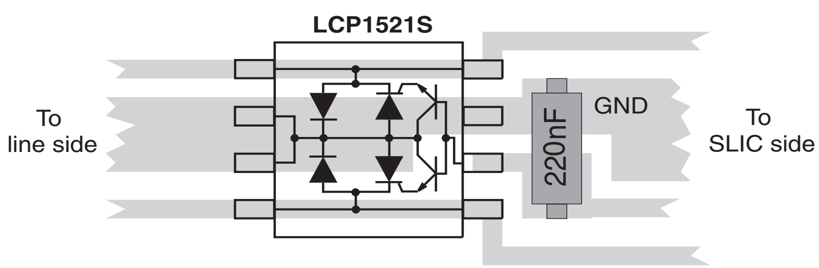


Figure 6. shows the classical PCB layout used to optimize line protection.

The capacitor C is used to speed up the crowbar structure firing during the fast surge edges.

This allows to minimize the dynamical breakover voltage at the SLIC Tip and Ring inputs during fast strikes. Note that this capacitor is generally present around the SLIC - Vbat pin.

So to be efficient it has to be as close as possible from the LCP152 Gate pin and from the reference ground track (or plan) (see *Figure 6.*). The optimized value for C is 220 nF.

The series resitors Rs1 and Rs2 designed in *Figure 5.* represent the fuse resistors or the PTC which are mandatory to withstand the power contact or the power induction tests imposed by the various country standards. Taking into account this fact the actual lightning surge current flowing through the LCP is equal to:

$I_{surge} = V_{surge} / (R_g + R_s)$

With:

V_{surge} = peak surge voltage imposed by the standard.

R_g = series resistor of the surge generator

R_s = series resistor of the line card (e.g. PTC)

e.g. For a line card with 30 Ω of series resistors which has to be qualified under GR1089 Core 1000V 10/1000 µs surge, the actual current through the LCP152 is equal to:

I_{surge} = 1000 / (10 + 30) = **25 A**

The LCP152 is particularly optimized for the new telecom applications such as the fiber in the loop, the WLL, the remote central office. In this case, the operating voltages are smaller than in the classical system. This makes the high voltage SLICs particularly suitable.

The schematics of *Figure 7.* give the most frequent topology used for these applications.

Figure 7. Protection of high voltage SLIC

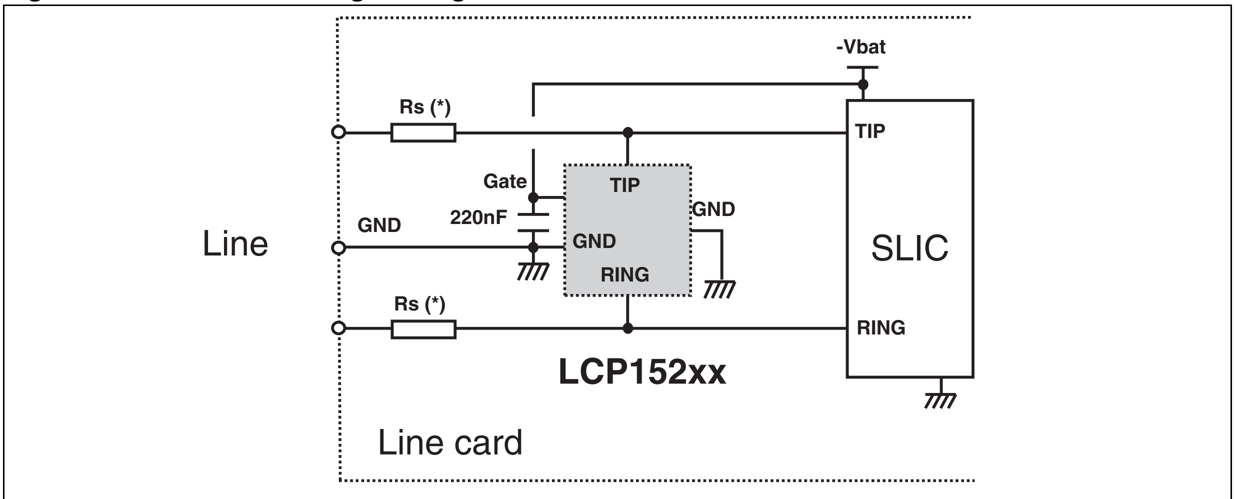


Figure 8. Surge peak current versus overload duration

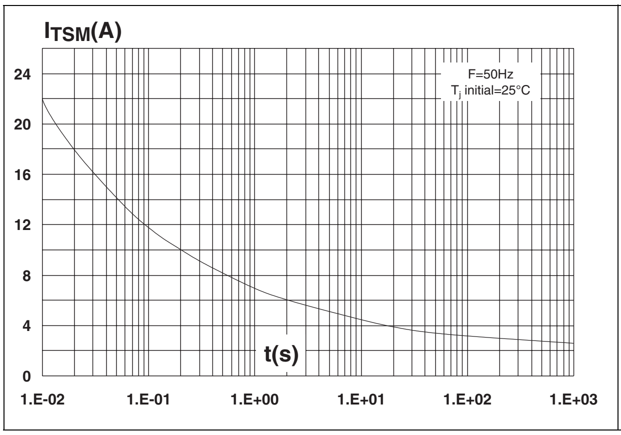
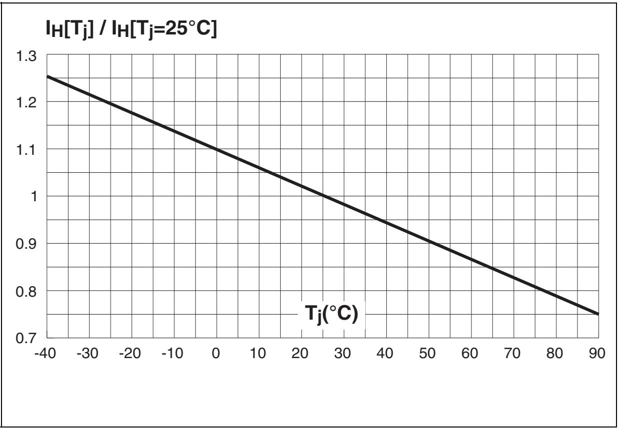
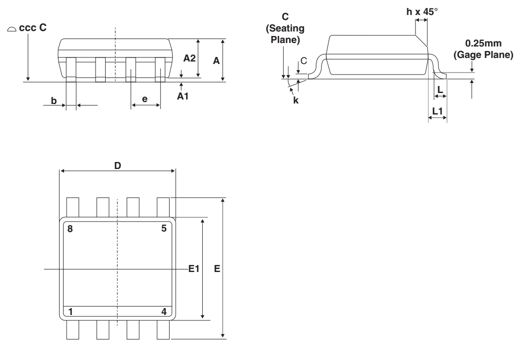


Figure 9. Relative variation of holding current versus junction temperature



3 Package information

Table 9. SO-8 Dimensions



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.1		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
C	0.17		0.23	0.007		0.009
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.041	
k°	0		8	0		8
ccc			0.10			0.004

Figure 10. Footprint (dimensions in mm)

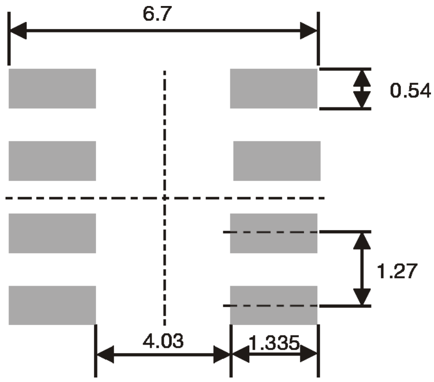
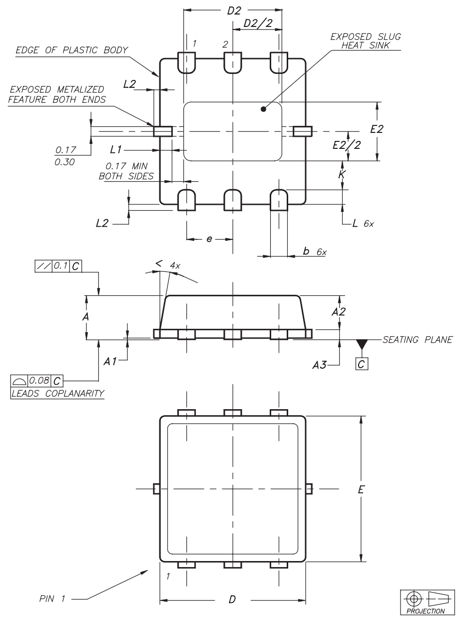
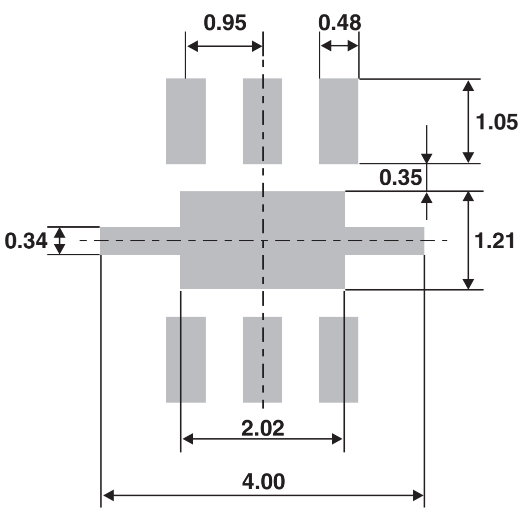


Table 10. QFN 3x3 6 Leads Package dimensions



REF.	DIMENSIONS					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80		1	0.031		0.040
A1	0		0.05	0		0.002
A2	0.65		0.75	0.026		0.030
A3		20			0.787	
b	0.33		0.43	0.013		0.017
D	2.90	3	3.10	0.114	0.118	0.122
D2	1.92		2.12	0.076		0.083
E	2.90	3	3.10	0.114	0.118	0.122
E2	1.11		1.31	0.044		0.051
e		0.95			0.037	
L	0.20		0.45	0.008		0.018
L1		0.24			0.009	
L2			0.13			0.005
K	0.20			0.008		
<	0°		12°	0°		12°

Figure 11. QFN 3x3 6 Leads Footprint dimensions (in mm)



4 Ordering information

Part Number	Marking	Package	Weight	Base qty	Delivery mode
LCP1521S	CP152S	SO-8	0.11 g	100	Tube
LCP1521SRL(1)	CP152S			2500	Tape and reel
LCP152DEERL(1)	LCP152	QFN 3x3 6L	0.022 g	3000	Tape and reel

1. Preferred device

5 Revision history

Date	Revision	Description of Changes
Sep-2003	1A	First issue.
08-Dec-2004	2	1/ Page 2 table 3: Thermal resistances changed from 130° C/W (SO-8) to 120° C/W and from 170° C/W (QFN) to 140° C/W. 2/ SO-8 and QFN footprint dimensions added.
17-Feb-2005	3	Table 9 on page 4: correction of typo on capacitance unit.
03-May-2005	4	Table 5 on page 3: I_{TSM} value @ t= 1s from 4 A to 4.5 A.
07-Jul-2006	5	Replaced QFN package illustration on page 1. Reformatted document to current layout standard. Values of I_{TSM} modified in Table 4. SO-8 package dimensions updated in Table 9.

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