CS5320/21/22

24-Bit Variable Bandwidth A/D Converter Chipset

Features

- CMOS A/D Converter Chipset
- Dynamic Range
  - 130 dB @ 25 Hz Bandwidth
  - 121 dB @ 411 Hz Bandwidth
- Delta-Sigma Architecture
  - Fourth-Order Modulator
  - Variable Oversampling: 64X to 4096X
  - Internal Track-and-Hold Amplifier
- CS5321 Signal-to-Distortion: 115 dB
- Clock Jitter Tolerant Architecture
- Input Voltage Range: ±4.5 V
- Flexible Filter Chip
  - Hardware or Software Selectable Options
  - Seven Selectable Filter Corners (-3 dB) Frequencies: 25, 51, 102, 205, 411, 824 and 1650 Hz
- Low Power Dissipation: <100 mW

Description

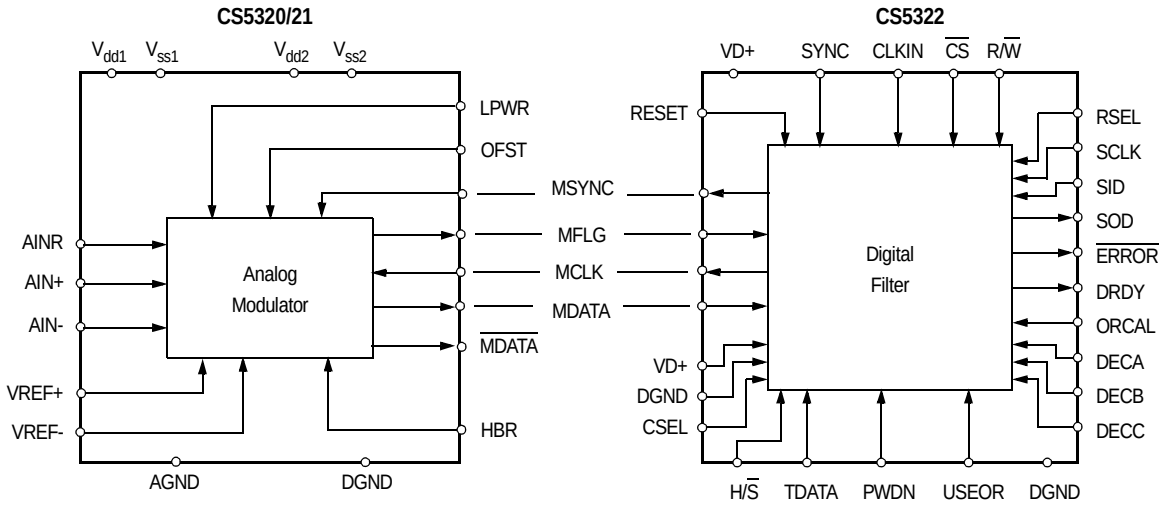
The CK5320 and CK5321 Chipsets function as a unique A/D converter intended for very high resolution measurement of signals below 1500 Hz. The CK5320 Chipset is a cost effective commercial grade solution for applications which require a high dynamic range A/D converter. The chipsets perform sampling, A/D conversion, and anti-alias filtering.

The CS5320 and CS5321 use Delta-Sigma modulation to produce highly accurate conversions. The ΔΣ modulator oversamples, virtually eliminating the need for external analog anti-alias filters. The CS5322 linear-phase FIR digital filter decimates the output to any one of seven selectable update periods: 16, 8, 4, 2, 1, 0.5 and 0.25 milliseconds. Data is output from the digital filter in a 24-bit serial format.

ORDERING INFORMATION*

Chip Sets	Kits
CS5320-KL & CS5322-KL	CK5320-KL1
CS5321-BL & CS5322-KL	CK5321-KL1
CS5321-BL & CS5322-BL	CK5321-BL1

* Refer to Table 5



Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

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1. CHARACTERISTICS AND SPECIFICATIONS

CS5320 AND CS5321 ANALOG CHARACTERISTICS (T_A = (See Note 1); V_{ss1}, V_{ss2} = -5V; V_{dd1}, V_{dd2} = +5V; VD+ = 5V; AGND = DGND = 0V; HBR = V_{dd} LPWR = 0, MCLK = 1.024 MHz; Device connected as shown in Figure 20, CS5322 used for filtering; Logic 1 = VD+, Logic 0 = 0V; unless otherwise specified.)

Parameter*		Symbol	CS5320 Min	CS5320 Typ	CS5320 Max	CS5321 Min	CS5321 Typ	CS5321 Max	Unit
Dynamic Performance									
Dynamic Range	(Note 2)	DR							
HBR = 1	f_O = 4000 Hz		-	103	-	-	103	-	dB
OFST = 1	f_O = 2000 Hz		-	118	-	-	118	-	dB
	f_O = 1000 Hz		113	121	-	116	121	-	dB
	f_O = 500 Hz		-	124	-	-	124	-	dB
	f_O = 250 Hz		-	127	-	-	127	-	dB
	f_O = 125 Hz		-	129	-	-	129	-	dB
	f_O = 62.5 Hz		-	130	-	-	130	-	dB
HBR = 0	f_O = 4000 Hz		-	99	-	-	99	-	dB
OFST = 1	f_O = 2000 Hz		-	115	-	-	115	-	dB
	f_O = 1000 Hz		-	118	-	-	118	-	dB
	f_O = 500 Hz		-	121	-	-	121	-	dB
	f_O = 250 Hz		-	124	-	-	124	-	dB
	f_O = 125 Hz		-	126	-	-	126	-	dB
	f_O = 62.5 Hz		-	127	-	-	127	-	dB
Signal-to-Distortion	(Note 3)	SDR							
	HBR = 1		100	110	-	100	115	-	dB
	HBR = 0		-	120	-	110	120	-	dB
Intermodulation Distortion	(Note 4)	IMD	-	105	-	-	110	-	dB
dc Accuracy									
Full Scale Error	(Note 5)	FSE	-	1	-	-	1	-	%
Full Scale Drift	(Note 5,6)	TC_{FS}	-	5	-	-	5	-	ppm/°C
Offset	(Note 5)	V_{ZSE}	-	10	-	-	10	-	mV
Offset after Calibration	(Note 7)		-	±100	-	-	±100	-	µV
Offset Calibration Range	(Note 8)		-	100	-	-	100	-	%F.S.
Offset Drift	(Note 5,6)	TC_{ZSE}	-	60	-	-	60	-	µV/°C

Notes:
1. CS5320-KL and CS5322-KL are guaranteed from 0^o to 70^o C. CS5322-BL is guaranteed from -40^o to $+85^o$ C. CS5321-BL is guaranteed from -55^o to $+85^o$ C.
2. f_O = CS5322 output word rate. Refer to "CS5322 FILTER CHARACTERISTICS" on page 8 for details on the FIR Filter.
3. Characterized with full scale input signal of 50 Hz; fo = 500 Hz.
4. Characterized with input signals of 30 Hz and 50 Hz, each 6 dB down from full scale with fo = 1000 Hz.
5. Specification is for the parameter over the specified temperature range and is for the CS5320/21 device only (VREF = +4.5 V). It does not include the effects of external components; OFST = 0.
6. Drift specifications are guaranteed by design and/or characterization.
7. The offset after calibration specification applies to the effective offset voltage for a ±4.5 volt input to the CS5320/21 modulator, but is relative to the output digital codes from the CS5322 after ORCAL and USEOR have been made active.
8. The CS5322 offset calibration is performed digitally and includes ± full scale (±4.5 volts into CS5320/21). Calibration of offsets greater than ±5% of full scale will begin to subtract from the dynamic range.

CS5320 AND CS5321 ANALOG CHARACTERISTICS (Continued)

Parameter*	Symbol	CS5320/21 Min	CS5320/21 Typ	CS5320/21 Max	Unit
Input Characteristics					
Input Signal Frequencies (Note 9)	BW	dc	-	1500	Hz
Input Voltage Range (Note 10)	V_{IN}	-4.5	-	+4.5	V
Input Overrange Voltage (Note 10)	I_{OVR}	-	-	5	%F.S.
Power Supplies					
DC Power Supply Currents (Note 11)					
LPWR = 0 Positive Supplies		-	5.5	7.5	mA
Negative Supplies		-	5.5	7.5	mA
LPWR = 1 Positive Supplies			3.0	4.5	mA
Negative Supplies			3.0	4.5	mA
Power Consumption (Note 11)					
Normal Operating Mode (Note12)	P_{DN}	-	55	75	mW
Lower Power Mode (Note 13)	P_{DL}	-	30	45	mW
Power Down	P_D	-	2	-	mW
Power Supply Rejection (dc to 128 kHz) (Note 14)	PSR	-	60	-	dB

Notes:
9. The upper bandwidth limit is determined by the CS5322 digital filter.
10. This input voltage range is for the configuration shown in Figure 20, the System Connection Diagram, and applies to signal from dc to f3 Hz. Refer to CS5322 Filter Characteristics for the values of f3.
11. All outputs unloaded. All logic inputs forced to V_{dd} or GND respectively.
12. LPWR = 0.
13. The CS5321 power dissipation can be reduced under the following conditions:
    a) LPWR=1; MCLK=512kHz, HBR=1
    b) LWPR=1; MCLK=1.024MHz, HBR=0
14. Characterized with a 100 mVp-p sine wave applied separately to each supply.

* Refer to Parameter Definitions (immediately following pin descriptions at the end of this data sheet).

Specifications are subject to change without notice.

CS5320 AND CS5321 SWITCHING CHARACTERISTICS (T_A = (See Note 1); V_{dd1}, V_{dd2} = 5V ± 5%; V_{ss1}, V_{ss2} = -5V ± 5%; Inputs: Logic 0 = 0V Logic 1 = V+; C_L = 50 pF (Note 15))

Parameter			Symbol	Min	Typ	Max	Units
MCLK Frequency		(Note 16)	f_c	0.250	1.024	1.2	MHz
MCLK Duty Cycle				40	-	60	%
MCLK Jitter (In-band)				-	-	300	ps
Rise Times:	Any Digital Input	(Note 17)	t_{risein}	-	-	100	ns
	Any Digital Output		$t_{riseout}$	-	50	200	ns
Fall Times:	Any Digital Input	(Note 17)	t_{fallin}	-	-	100	ns
	Any Digital Output		$t_{fallout}$	-	50	200	ns
MSYNC Setup Time to MCLK rising			t_{mss}	20	-	-	ns
MSYNC Hold Time after MCLK rising			t_{msh}	20	-	-	ns
MCLK rising to Valid MFLG			t_{mfh}	-	140	255	ns
MCLK rising to Valid MDATA			t_{mdv}	-	170	300	ns

Notes: 15. Guaranteed by design, characterization, or test.
16. If MCLK is removed, the modulator will enter the power down mode.
17. Excludes MCLK input. MCLK should be driven with a signal having rise and fall times of 25 ns or faster.

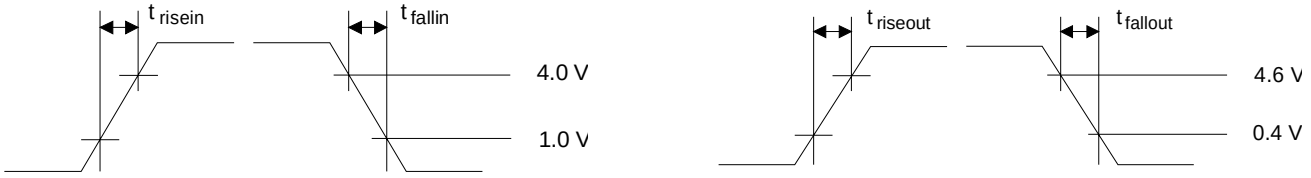


Figure 1. Rise and Fall Times

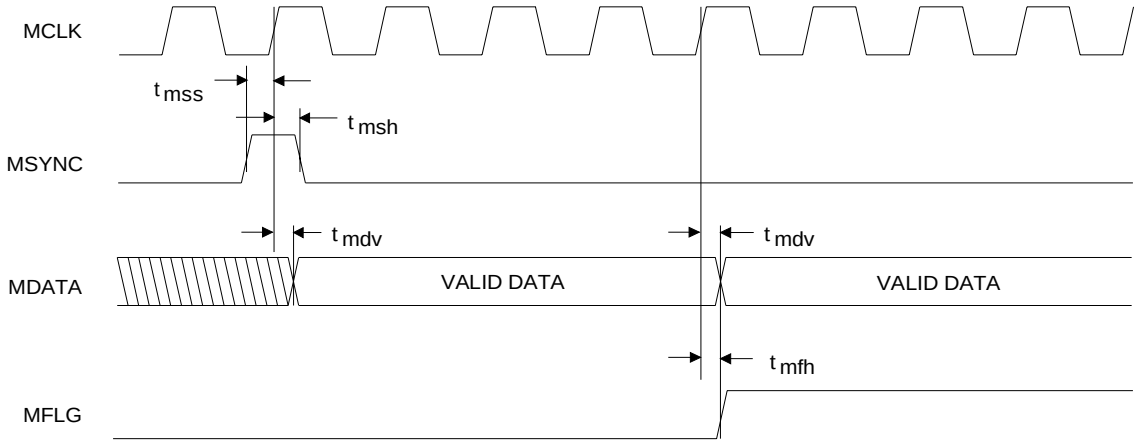


Figure 2. CS5320 and CS5321 Interface Timing, HBR=1

CS5320 AND CS5321 DIGITAL CHARACTERISTICS (T_A = (See Note 1); V_{dd1} = V_{dd2} = 5.0V ± 5%; GND = 0V; measurements performed under static conditions)

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Drive Voltage	(Note 18)	V_{IH}	(V_{dd})-0.6	-	-	V
Low-Level Input Drive Voltage	(Note 18)	V_{IL}	-	-	1.0	V
High-Level Output Voltage IOUT = -40 µA	(Note 19)	V_{OH}	(V_{dd})-0.3	-	-	V
Low-Level Output Voltage IOUT = +40 µA	(Note 19)	V_{OL}	-	-	0.3	V
Input Leakage Current		I_{LKG}	-	-	±10	µA
Digital Input Capacitance		C_{IN}	-	9	-	pF
Digital Output Capacitance		C_{OUT}	-	9	-	pF

Notes: 18. Device is intended to be driven with CMOS logic levels.
19. Device is intended to be interfaced to CMOS logic. Resistive loads are not recommended on these pins.

CS5320 AND CS5321 RECOMMENDED OPERATION CONDITIONS (Voltages with respect to GND = 0V, See Note 20)

Parameter		Symbol	Min	Typ	Max	Units
DC Supply:	Positive	$V_{dd1,}V_{dd2}$	4.75	5.0	5.25	V
	Negative	V_{ss1},V_{ss2}	-4.75	-5.0	-5.25	V
Ambient Operating Temperature	-KL	T_A	0	-	+70	°C
	-BL	T_A	-55	-	+85	°C

Notes: 20. The maximum voltage differential between the Positive Supply of the CS5320/21 and the Positive Digital Supply of the CS5322 must be less than 0.25V.

CS5320 AND CS5321 ABSOLUTE MAXIMUM RATINGS * (Voltages with respect to GND = 0V)

Parameter		Symbol	Min	Max	Units
DC Supply:	Positive	$V_{dd1,}V_{dd2}$	-0.3	6.0	V
	Negative	V_{ss1},V_{ss2}	+0.3	-6.0	V
Input Current, Any Pin Except Supplies	(Note 21)	I_{in}	-	±10	mA
Output Current		I_{out}	-	25	mA
Total Power (all supplies and outputs)		P_t	-	1	W
Digital Input Voltage		V_{IND}	-0.3	(V_{dd})+0.3	V
Storage Temperature		T_{stg}	-65	150	°C

Notes: 21. Transient currents of up to 100 mA will not cause SCR latch up.

*WARNING: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

CS5322 FILTER CHARACTERISTICS (T_A = (See Note 1); VD+ = 5.0V; GND = 0V; CLKIN = 1.024 MHz; transfer function shown in Figure 3; unless otherwise specified.)

Output Word Rate f_0 (Hz)	Passband f1 (Hz)	Passband Flatness R_{PB} (dB)	-3dB Freq. f2 (Hz)	Stopband f3 (Hz) (Note 22)	Group Delay (ms)
4000	1500	0.2	1652.5	2000	7.25
2000	750	0.04	824.3	1000	14.5
1000	375	0.08	411.9	500	29
500	187.5	0.1	205.9	250	58
250	93.8	0.1	102.9	125	116
125	46.9	0.1	51.5	62.5	232
62.5	23.4	0.1	25.7	31.25	464

Notes: 22. G_{SB} = -130 dB for all Output Word Rates.

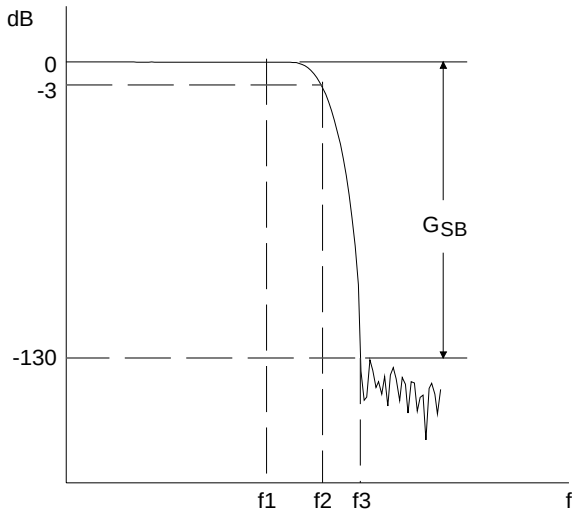


Figure 3. CS5322 Filter Response

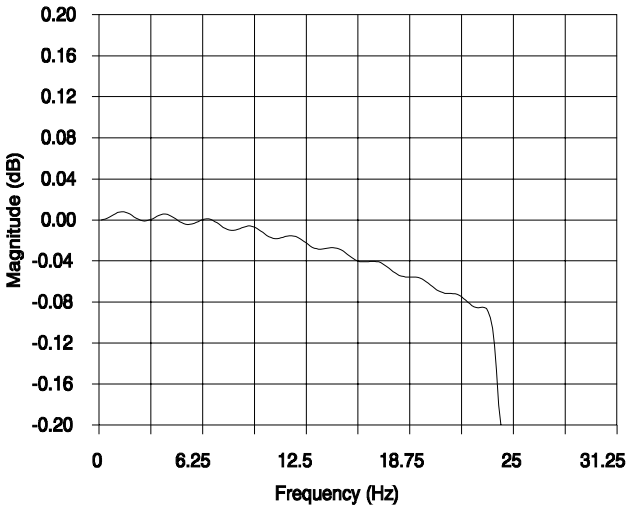


Figure 4. CS5322 Digital Filter Passband Ripple f_0 = 62.5 Hz

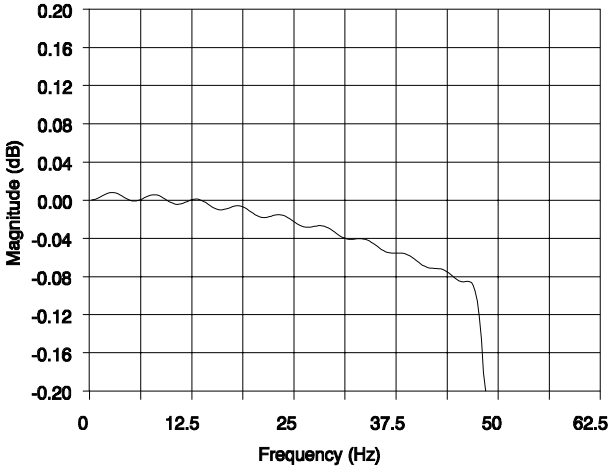


Figure 5. CS5322 Digital Filter Passband Ripple f_0 = 125 Hz

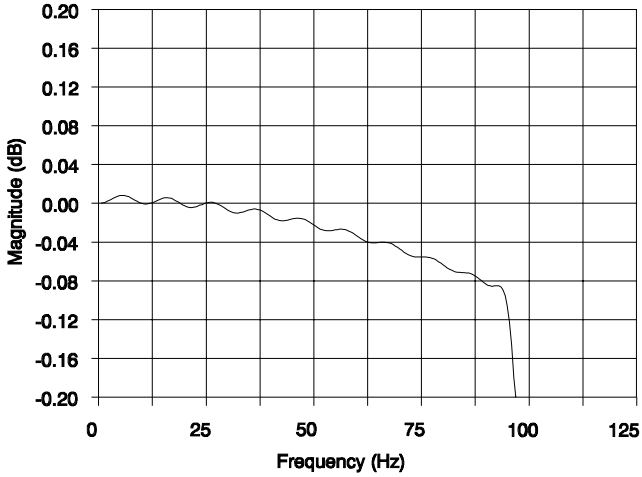


Figure 6. CS5322 Digital Filter Passband Ripple f_0 = 250 Hz

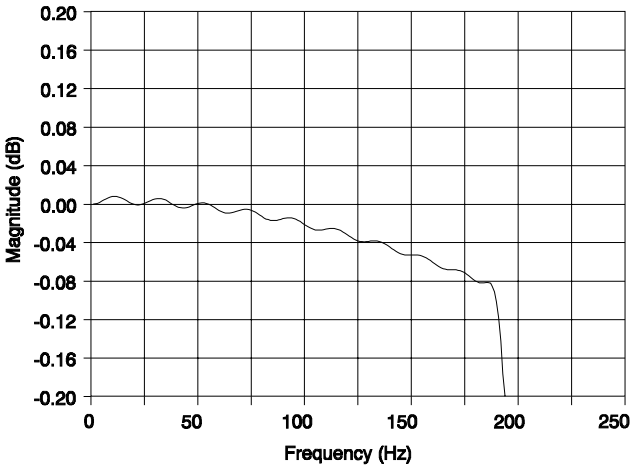


Figure 7. CS5322 Digital Filter Passband Ripple f_0 = 500 Hz

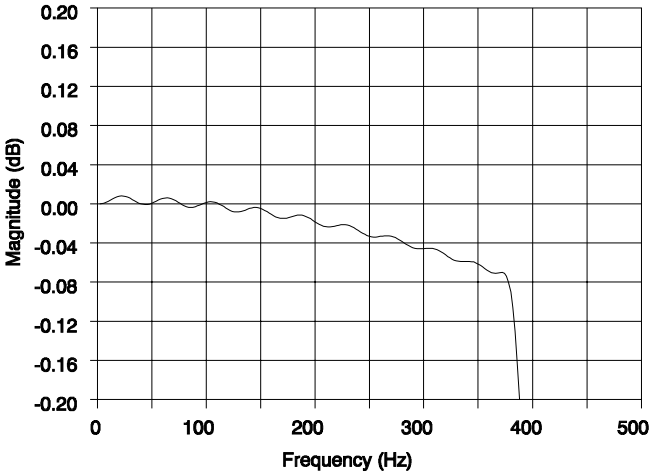


Figure 8. CS5322 Digital Filter Passband Ripple f_0 = 1000 Hz

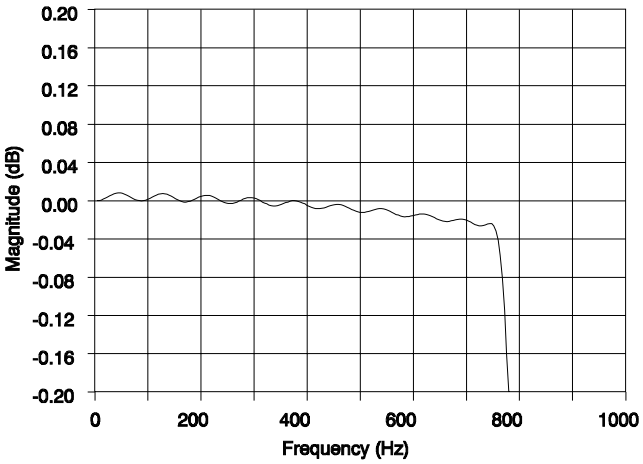


Figure 9. CS5322 Digital Filter Passband Ripple f_0 = 2000 Hz

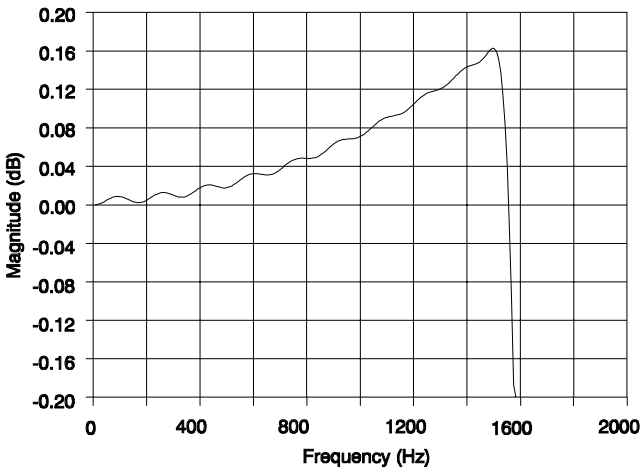


Figure 10. CS5322 Digital Filter Passband Ripple f_0 = 4000 Hz

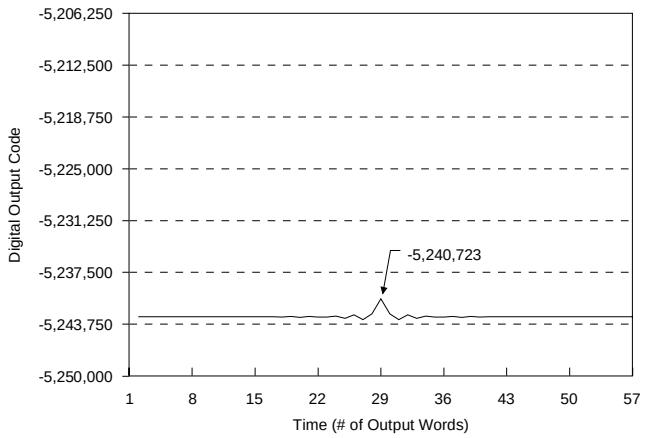


Figure 11. CS5322 Impulse Response, f_0 = 62.5 Hz

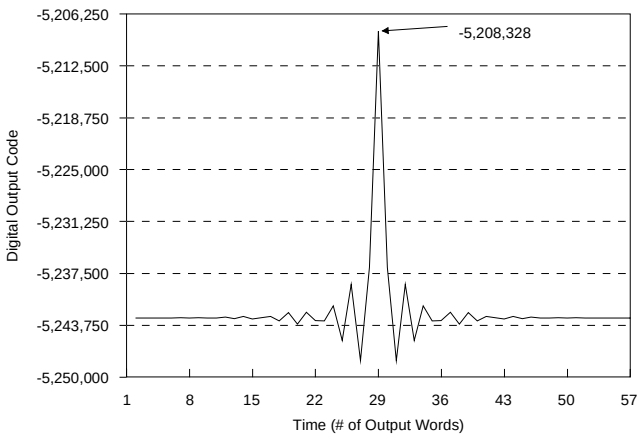


Figure 12. CS5322 Impulse Response, f_0 = 1000 Hz

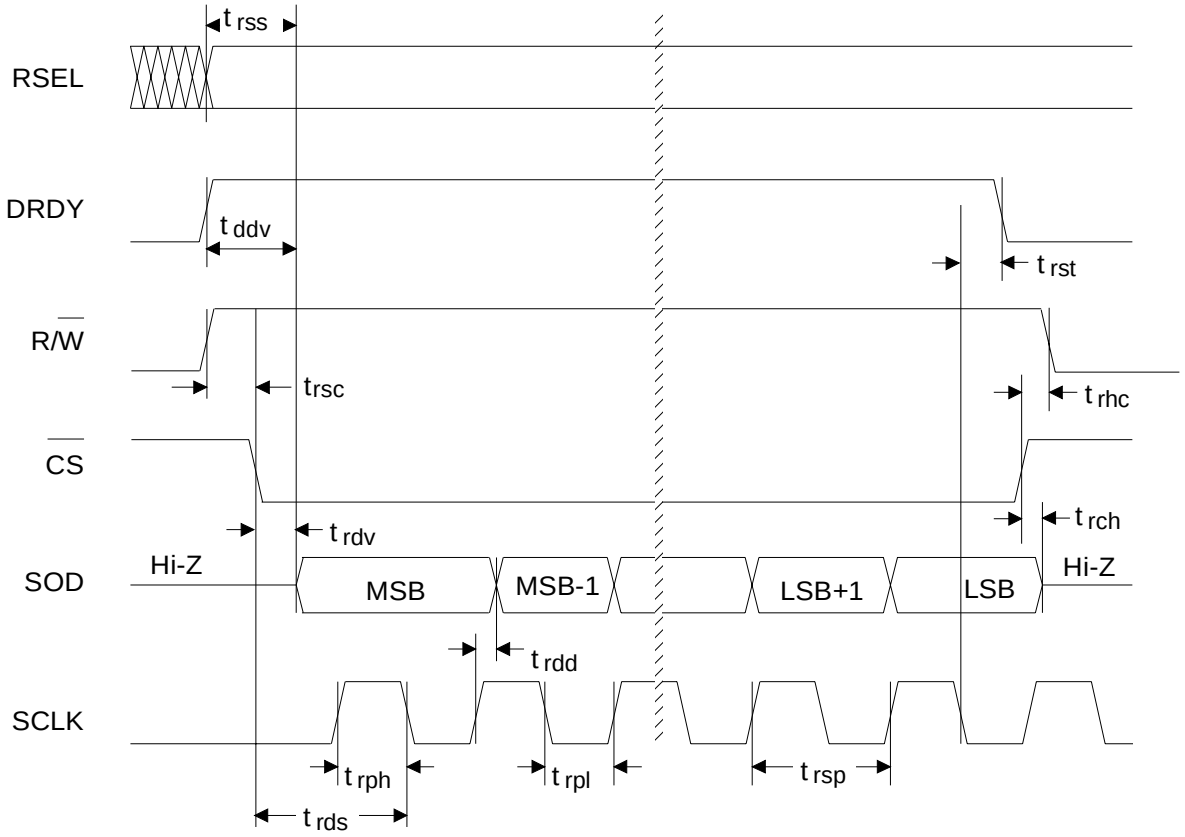
CS5322 POWER SUPPLY (T_A = (See Note 1); VD+ = 5V; CLKIN = 1.024 MHz)

Parameter			CS5322-K Min	CS5322-K Typ	CS5322-K Max	CS5322-B Min	CS5322-B Typ	CS5322-B Max	Unit
Power Supply Current:	ID+	(Note 11)	-	2.2	4	-	2.2	4	mA
Power Dissipation:		(Note 11)							
		PWDN Low	-	11	20	-	11	20	mW
		PWDN High	-	0.6	2.5	-	0.6	2.5	mW

CS5322 SWITCHING CHARACTERISTICS (T_A = (See Note 1); VD+ = 5V ± 5%; DGND = 0V; Inputs: Logic 0 = 0V Logic 1 = VD+; C_L = 50 pF (Note 23)

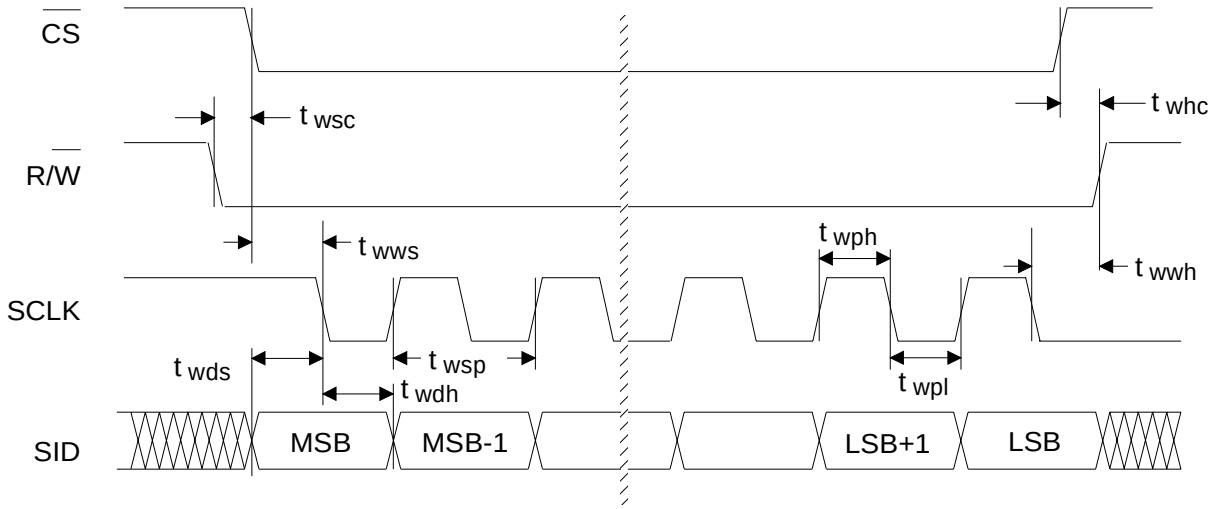
Parameter		Symbol	Min	Typ	Max	Units
CLKIN Frequency		f_c	0.512	1.024	1.2	MHz
CLKIN Duty Cycle			40	-	60	%
Rise Times:	Any Digital Input	t_{rise}	-	-	100	ns
	Any Digital Output		-	50	100	ns
Fall Times:	Any Digital Input	t_{fall}	-	-	100	ns
	Any Digital Output		-	50	100	ns
Serial Port Read Timing						
DRDY to Data Valid		t_{ddv}	-	-	25	ns
RSEL Setup Time before Data Valid		t_{rss}	50	-	-	ns
Read Setup before $\overline{CS}$ Active		t_{rsc}	20	-	-	ns
Read Active to Data Valid		t_{rdv}	-	-	50	ns
SCLK rising to New SOD bit		t_{rdd}	-	-	50	ns
SCLK Pulse Width High		t_{rph}	30	-	-	ns
SCLK Pulse Width Low		t_{rpl}	30	-	-	ns
SCLK Period		t_{rsp}	100	-	-	ns
SCLK falling to DRDY falling		t_{rst}	-	-	50	ns
$\overline{CS}$ High to Output Hi-Z		t_{rch}	-	-	20	ns
Read Hold Time after $\overline{CS}$ Inactive		t_{rhc}	20	-	-	ns
Read Select Setup to SCLK falling		t_{rds}	20	-	-	ns
Serial Port Write Timing						
Write Setup Before $\overline{CS}$ Active		t_{wsc}	20	-	-	ns
SCLK Pulse Width Low		t_{wpl}	30	-	-	ns
SCLK Pulse Width High		t_{wph}	30	-	-	ns
SCLK Period		t_{wsp}	100	-	-	ns
Write Setup Time to First SCLK falling		t_{wws}	20	-	-	ns
Data Setup Time to First SCLK falling		t_{wds}	20	-	-	ns
Write Select Hold Time after SCLK falling		t_{wwh}	20	-	-	ns
Write Hold Time after $\overline{CS}$ Inactive		t_{whc}	20	-	-	ns
Data Hold Time after SCLK falling		t_{wdh}	20	-	-	ns

23. Guaranteed by design, characterization and/or test.



Serial Port Read Timing

(R/$\overline{W}$ = 1, CS = 0, RSEL = 1 DRDY Does not toggle if reading status, RSEL = 0)



Serial Port Write Timing

Figure 13. CS5322 Serial Port Timing

CS5322 SWITCHING CHARACTERISTICS (continued)

Parameter	Symbol	Min	Typ	Max	Units
Test Data (TDATA) Timing					
SYNC Setup Time to CLKIN rising	t_{ss}	20	-	-	ns
SYNC Hold Time after CLKIN rising	t_{sh}	20	-	-	ns
TDATA Setup Time to CLKIN rising after SYNC	t_{tds}	-	20	-	ns
TDATA Hold Time after CLKIN rising	t_{tdh}	-	150	-	ns
ORCAL Setup Time to CLKIN rising	t_{os}	20	-	-	ns
ORCAL Hold Time after CLKIN rising	t_{oh}	20	-	-	ns
DRDY Timing					
CLKIN rising to DRDY falling	t_{df}	-	140	-	ns
CLKIN falling to DRDY rising	t_{dr}	-	150	-	ns
CLKIN rising to ERROR change	t_{ec}	-	140	-	ns
RESET Timing					
RESET Setup Time to CLKIN rising	t_{rs}	20	-	-	ns
RESET Hold Time after CLKIN rising	t_{rh}	20	-	-	ns
SYNC Setup Time to CLKIN rising	t_{ss}	20	-	-	ns
SYNC Hold Time after CLKIN rising	t_{sh}	20	-	-	ns

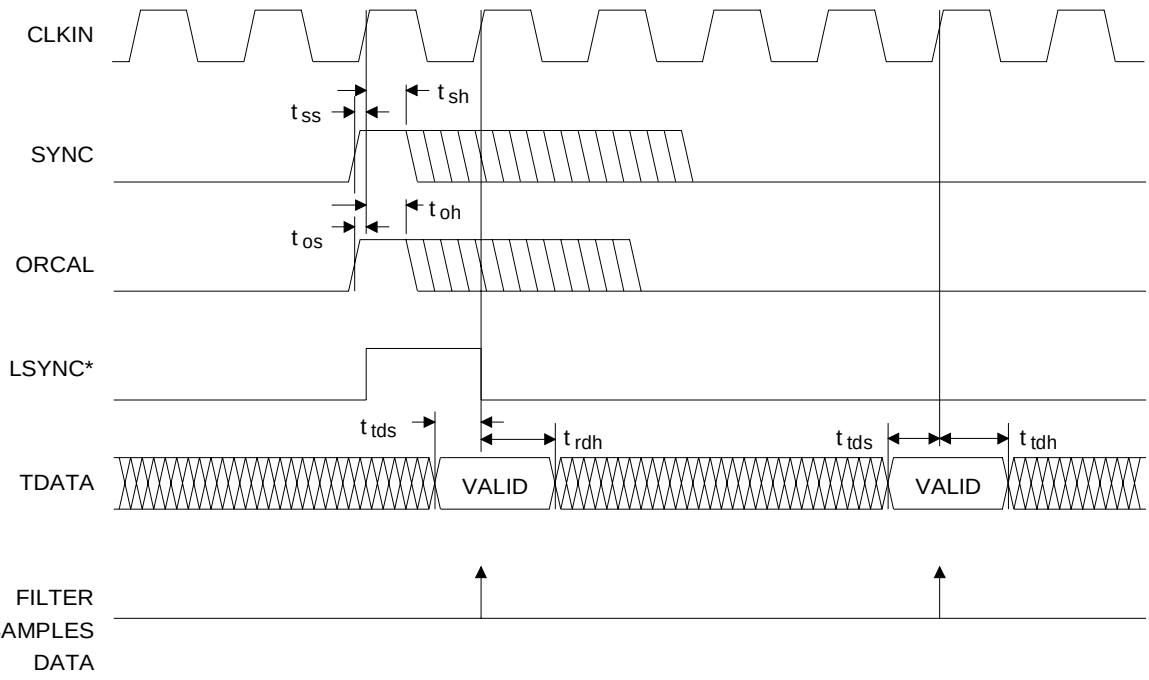
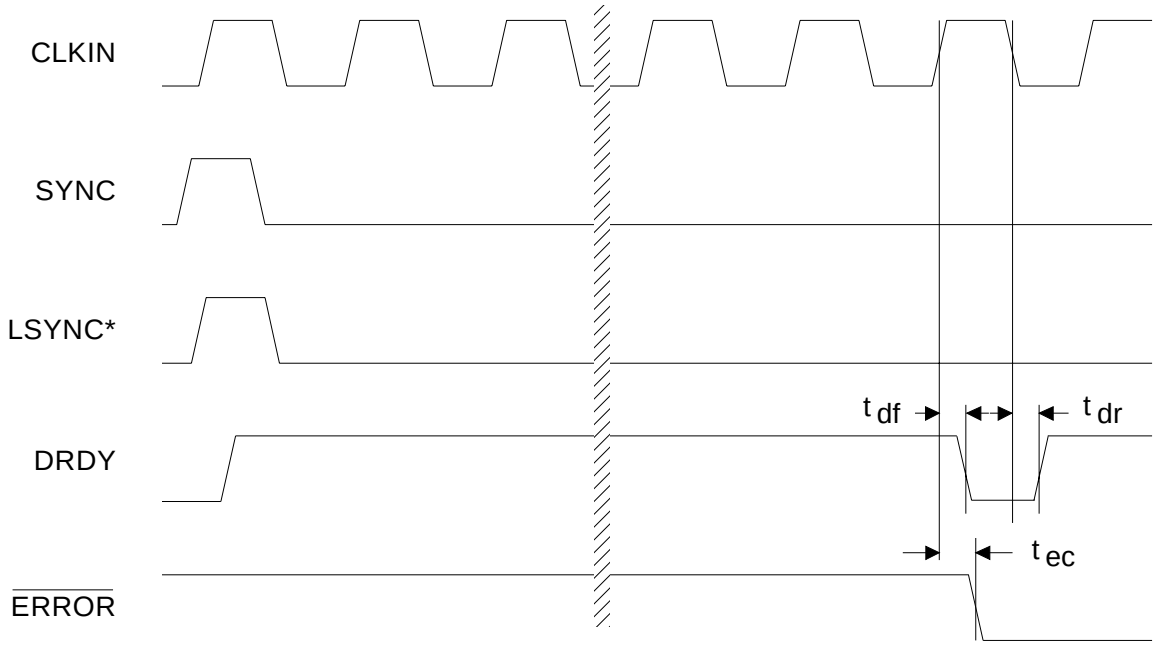


Figure 14. TDATA Setup/Hold Timing



*Note: For overwrite case, DRDY will remain high.

Figure 15. DRDY Timing

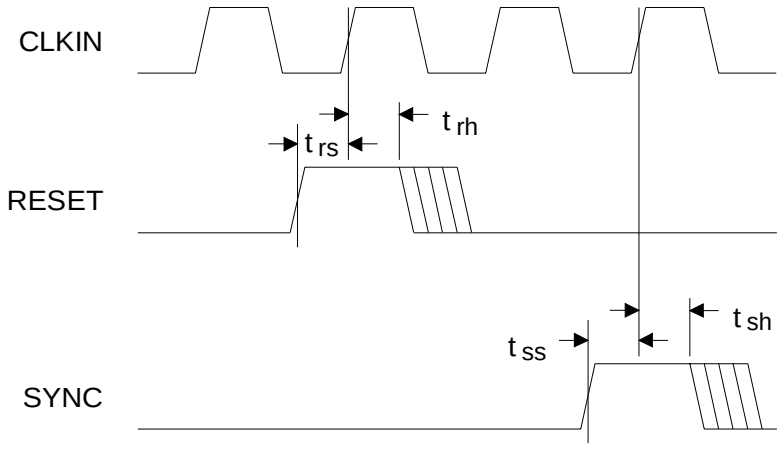
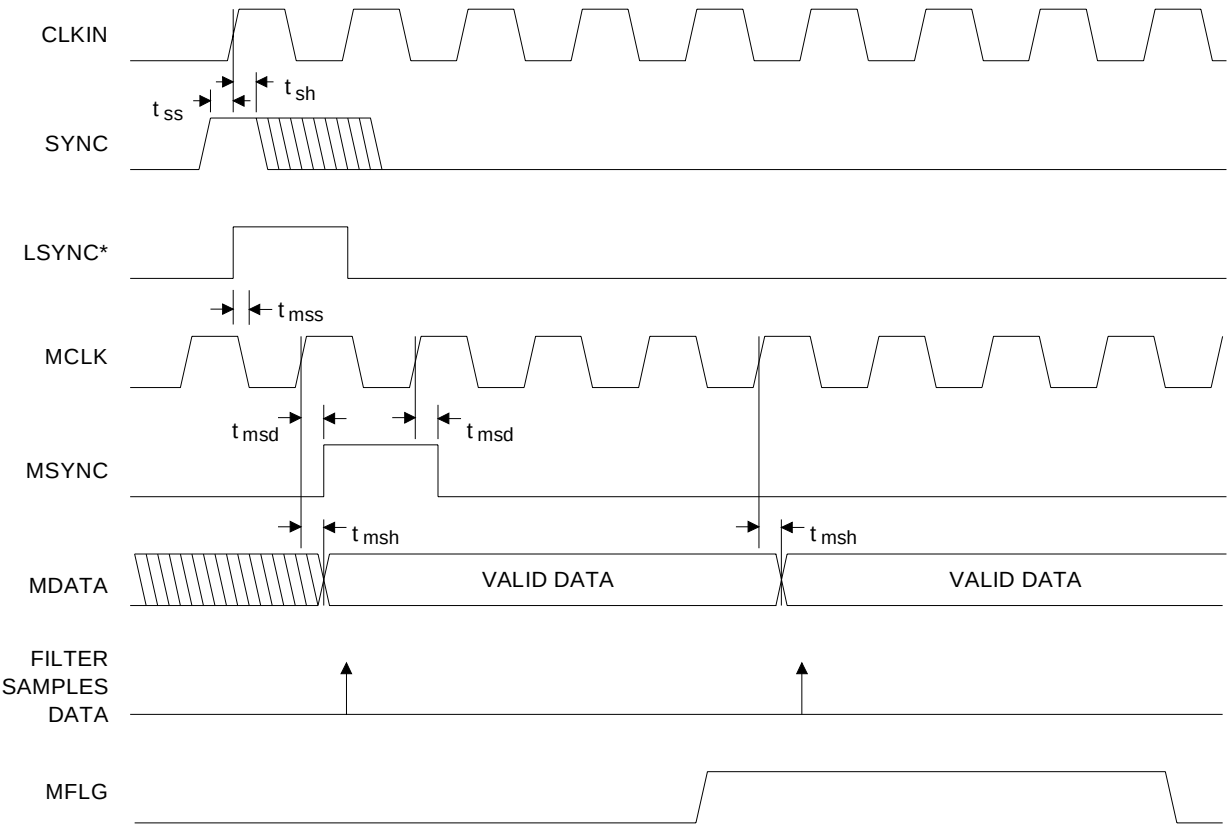


Figure 16. RESET Timing

CS5322 SWITCHING CHARACTERISTICS (continued)

Parameter			Symbol	Min	Typ	Max	Units
MCLK Frequency		(Note 24)	f_c	0.512	1.024	1.1	MHz
MCLK Duty Cycle				40	-	60	%
Rise Times:	Any Digital Input	(Note 25)	t_{rise}	-	-	100	ns
	Any Digital Output			-	50	200	ns
Fall Times:	Any Digital Input	(Note 25)	t_{fall}	-	-	100	ns
	Any Digital Output			-	50	200	ns
SYNC Setup Time to CLKIN rising			t_{ss}	20	-	-	ns
SYNC Hold Time after CLKIN rising			t_{sh}	20	-	-	ns
CLKIN edge to MCLK edge			t_{mss}	-	30	-	ns
MCLK rising to Valid MDATA			t_{msh}	-	50	-	ns
MSYNC Delay from MCLK rising		(Note 26)	t_{msd}	-	90	-	ns

Notes: 24. If MCLK is removed, the modulator will enter the power down mode.
25. Excludes MCLK input. MCLK should be driven with a signal having rise and fall times of 25 ns or faster.
26. Only the rising edge of MSYNC relative to MCLK is used to synchronize the device. MSYNC can return low at any time as long as it remains high for at least one MCLK cycle.



* Internal timing signal generated in the CS5322

Figure 17. CS5320/21/CS5322 Interface Timing

CS5322 DIGITAL CHARACTERISTICS (T_A = (See Note 1); VD+ = 5.0V ± 5%; GND = 0V; measurements performed under static conditions)

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Drive Voltage		V_{IH}	(VD+)-0.3	-	-	V
Low-Level Input Drive Voltage		V_{IL}	-	-	0.3	V
High-Level Input Threshold	(Note 27)		(VD+)-1.0	-	-	V
Low-Level Input Threshold	(Note 27)		-	-	1.0	V
High-Level Output Voltage IOUT = -40µA	(Note 28)	V_{OH}	(VD+)-0.6	-	-	V
Low-Level Output Voltage IOUT = +1.6 mA	(Note 28)	V_{OL}	-	-	0.4	V
Input Leakage Current All pins except MFLG, SOD		I_{LKG}	-	-	±10	µA
Three-State Leakage Current		I_{OZ}	-	-	±10	µA
Digital Input Capacitance		C_{IN}	-	9	-	pF
Digital Output Capacitance		C_{OUT}	-	9	-	pF

Notes: 27. Device is intended to be driven with CMOS logic levels.
28. Device is intended to be interfaced to CMOS logic. Resistive loads are not recommended on these pins.

CS5322 RECOMMENDED OPERATION CONDITIONS (Voltages with respect to GND = 0V)

Parameter		Symbol	Min	Typ	Max	Units
DC Supply:	(Note 29)					
Positive		VD+	4.75	5.0	5.25	V
Negative		VD-	-4.75	-5.0	-5.25	V
Ambient Operating Temperature	-KL	T_A	0	-	+70	°C
	-BL	T_A	-40	-	+85	°C

Notes: 29. The maximum voltage differential between the Positive Supply of the CS5320/21 and the Positive Digital Supply of the CS5322 must be less than 0.25V.

CS5322 ABSOLUTE MAXIMUM RATINGS * (Voltages with respect to GND = 0V)

Parameter		Symbol	Min	Typ	Max	Units
DC Supply:	(Note 29)					
Positive		VD+	-0.3	-	(VD+)+0.3	V
Negative		VD-	0.3	-	-6.0	V
Input Current, Any Pin Except Supplies	(Note 30)	I_{in}	-	-	±10	mA
Digital Input Voltage		VIND	-0.3	-	(VD+)+0.3	V
Storage Temperature		T_{stg}	-65	-	150	°C

Notes: 30. Transient currents of up to 100 mA will not cause SCR latch up.

*WARNING: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

2. GENERAL DESCRIPTION

The CS5320 and CS5321 are fourth-order CMOS monolithic analog modulators designed specifically for very high resolution measurement of signals between dc and 1500 Hz. Configuring the CS5320 or CS5321 with the CS5322 FIR filter results in a high resolution A/D converter system that performs sampling and A/D conversion with dynamic range exceeding 120 dB .

The CS5320 and CS5321 use a fourth-order oversampling architecture to achieve high resolution A/D conversion. The modulator consists of a 1-bit A/D converter embedded in a negative feedback loop. The modulator provides an oversampled serial bit stream at 256 kbits per second (HBR=1) and 128 kbits per second (HBR=0) operating with a clock rate of 1.024 MHz. Figure 18 illustrates the CS5320/CS5321 Block Diagram.

The CS5322 is a monolithic digital Finite Impulse Response (FIR) filter with programmable decimation. The CS5322 and CS5320/CS5321 are intended to be used together to form a unique high dynamic range ADC chipset. The CS5322 provides the digital anti-alias filter for the CS5320/CS5321 modulator output. The CS5322 consists of: a multistage FIR filter, four registers (status, data, offset, and configuration), a flexible serial input and output port, and a 2-channel input data multiplexer that selects data from the CS5320/CS5321 (MDATA) or user test data (TDATA). The CS5322 decimates (64x to 4096x) the output to any of seven selectable up-date periods: 16, 8, 4, 2, 1, 0.5 and 0.25 milliseconds. Data is output from the digital filter in a 24-bit serial format. Figure 19 illustrates the CS5322 Block Diagram.

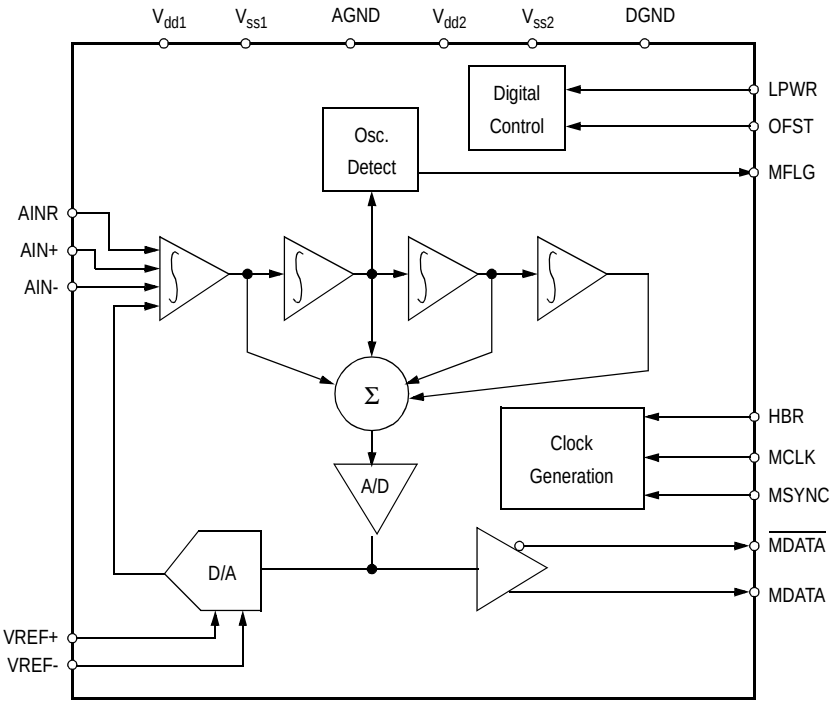


Figure 18. CS5320/21 Block Diagram

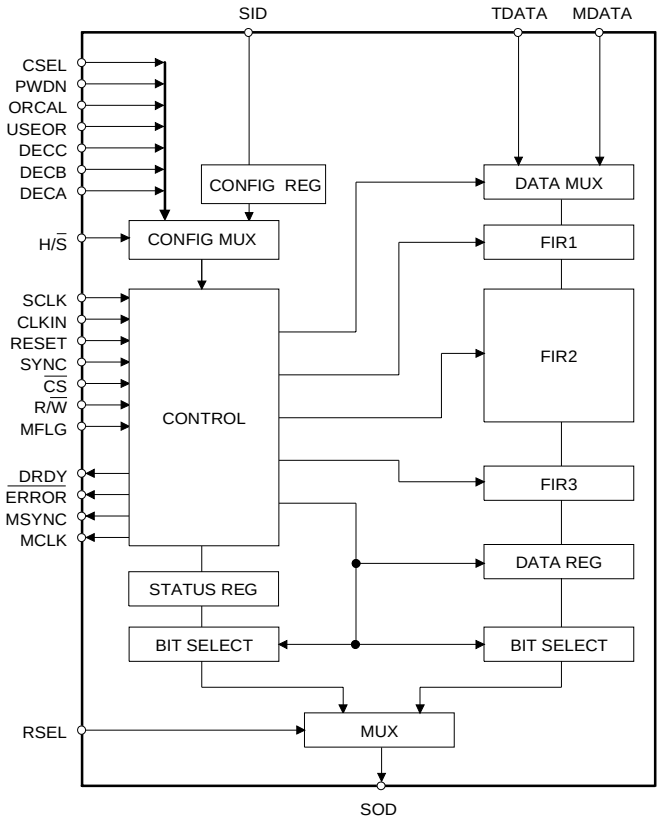


Figure 19. CS5322 Block Diagram

2.1 Analog Input

The CS5320 and CS5321 modulators use a switched capacitor architecture for its signal and voltage reference inputs. The signal input uses three pins; AINR, AIN+, and AIN-. The AIN- pin acts as the return pin for the AINR and AIN+ pins. The AINR pin is a switched capacitor "rough charge" input for the AIN+ pin. The input impedance for the rough charge pin (AINR) is 1/fC where f is two times the modulator sampling clock rate and C is the internal sampling capacitor (about 40 pF). Using a 1.024 MHz master clock (HBR = 1) yields an input impedance of about 1/(512 kHz)X(40 pF) or about 50 kΩ. Internal to the chip the rough charge input pre-charges the sampling capacitor used on the AIN+ input, therefore the effective input impedance on the AIN+ pin is orders of magnitude above the impedance seen on the AINR pin.

The analog input structure inside the VREF+ pin is very similar to the AINR pin but includes additional circuitry whose operating current can change over temperature and from device to device. Therefore, if gain accuracy is important, the VREF+ pin should be driven from a low source impedance. The current demand of the VREF+ pin will produce a voltage drop of approximately 45 mV across the 200 Ω source resistor of Figure 20 and Figure 21 Option A with MCLK = 1.024 MHz, HBR = 1, and temperature = 25°C.

When the CS5320/21 modulator is operated with a 4.5 V reference it will accept a 9 V p-p input signal, but modulator loop stability can be adversely affected by high frequency out-of-band signals. Therefore, input signals must be band-limited by an input filter. The -3 dB corner of the input filter must be equal to the modulator sampling clock divided by 64. The modulator sampling clock is MCLK/4 when HBR = 1 or MCLK/8 when HBR = 0. With MCLK = 1.024 MHz, HBR = 1, the modulator sampling clock is 256 kHz which requires an input filter with a -3 dB corner of 4 kHz. The bandlimiting may be accomplished in an amplifier stage ahead of the CS5320/21 modulator or with the RC input filter at the AIN+ and AINR input pins. The RC filter at the AIN+ and AINR pins is recommended to reduce the "charge kick" that the driving amplifier sees as the switched capacitor sampling is performed.

Figure 20 illustrates the CS5320/21 and CS5322 system connections. The input components on AINR and AIN+ should be identical values for optimum performance. In choosing the components the capacitor should be a minimum of 0.1 µF (C0G dielectric ceramic preferred). For minimum board space, the RC components on the AINR input can be removed, but this will force the driving amplifier to source the full dynamic charging current of the AINR input. This can increase distortion in the driving amplifier and reduce system performance. In choosing the RC filter components, increasing C and minimizing R is preferred. Increasing C reduces the instantaneous voltage change on the pin, but may require paralleling capacitors to maintain smaller size (the recommended 0.1 µF C0G ceramic capacitor is larger than other similar-valued capacitors with different dielectrics). Larger resistor values will increase the voltage drop across the resistor as the recharging current charges the switched capacitor input.

2.2 The OFST Pin

The CS5320/21 modulator can produce "idle tones" which occur in the passband when the input signal is steady state dc signal within about
±50 mV of bipolar zero. In the CS5320/21 these tones are about 135 dB down from full scale. The user can force these idle tones "out-of-band" by adding 100 mV of dc offset to the signal at the AIN input. Alternately, if the user circuitry has a low offset voltage such that the input signal is within ±50 mV of bipolar zero when no AC signal is present, the OFST pin on the CS5320/21 can be activated. When OFST = 1, +100 mV of input re-

ferred offset will be added internal to the CS5320/21 and guarantee that any idle tones present will lie out-of-band. The user should be certain that when OFST is active (OFST =1) that the offset voltage generated by the user circuitry does not negate the offset added by the OFST pin.

2.3 Input Range and Overrange Conditions

The analog input is applied to the AIN+ and AINR pins with the AIN- pin connected to GND. The input is fully differential but for proper operation the AIN- pin must remain at GND potential.

The analog input span is defined by the voltage applied between the VREF+ and VREF- input pins. See the Voltage Reference section of this data sheet for voltage reference requirements.

The modulator is a fourth order delta-sigma and is therefore conditionally stable. The modulator may go into an oscillatory condition if the analog input is overranged. Input signals which exceed either plus or minus full scale by more than 5 % can introduce instability in the modulator. If an unstable condition is detected, the modulator will be reduced to a first order system until loop stability is achieved. If this occurs the MFLG pin will transition from a low to a high will result in an error bit being set in the CS5322. The input signal must be reduced to within the full scale range of the converter for at least 32 MCLK cycles for the modulator to recover from this error condition.

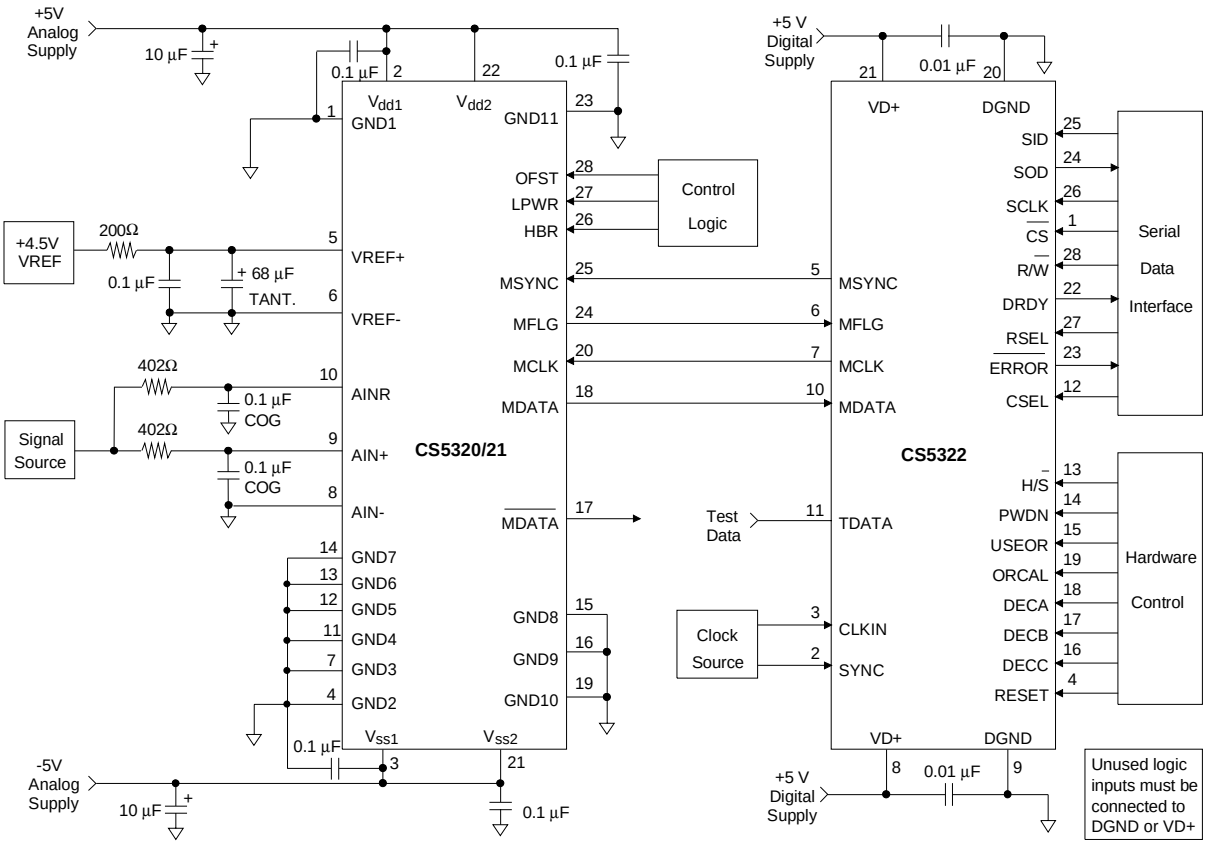


Figure 20. System Connection Diagram

2.4 Voltage Reference

The CS5320/21 is designed to operate with a voltage reference in the range of 4.0 to 4.5 volts. The voltage reference is applied to the VREF+ pin with the VREF- pin connected to the GND. A 4.5 V reference will result in the best S/N performance but most 4.5 V references require a power supply voltage greater than 5.0 V for operation. A 4.0 V reference can be used for those applications which must operate from only 5.0 V supplies, but will yield a S/N slightly lower (1-2 dB) than when using a 4.5 V reference. The voltage reference should be designed to yield less than 2 µV rms of noise in band at the VREF+ pin of the CS5320/21. The CS5322 filter selection will determine the bandwidth over which the voltage reference noise will affect the CS5320/21/22 dynamic range.

For a 4.5 V reference, the LT1019-4.5 voltage reference yields low enough noise if the output is filtered with a low pass RC filter as shown in Figure 21 Option A. The filter in Figure 21 Option A is acceptable for most spectral measurement applications, but a buffered version with lower source impedance (Figure 21 Option B) may be preferred for dc-measurement applications. Due to its dynamic (switched-capacitor) input the input impedance of the +VREF pin of the CS5320/21 will change any time MCLK or HBR is changed. Therefore the current required from the voltage reference will change any time MCLK or HBR is changed. This can affect gain accuracy due to the high source impedance of the filter resistor in Figure 20 and Figure 21 Option A. If gain error is to be minimized, especially when MCLK or HBR is changed, the voltage reference should have lower output impedance. The buffer of Figure 21 Option B offers lower output impedance and will exhibit better system gain stability.

2.5 Clock Source

For proper operation, the CS5320/21 must be provided with a CMOS-compatible clock on the MCLK pin. The MCLK for the CS5320/21 is usually provided by the CS5322 filter. MCLK is usually 1.024 MHz to set the seven selectable output word rates from the CS5322. The MCLK frequency can be as low as 250 kHz and as high as 1.2 MHz. The choice of clock frequency can affect performance; see the Performance section of the data

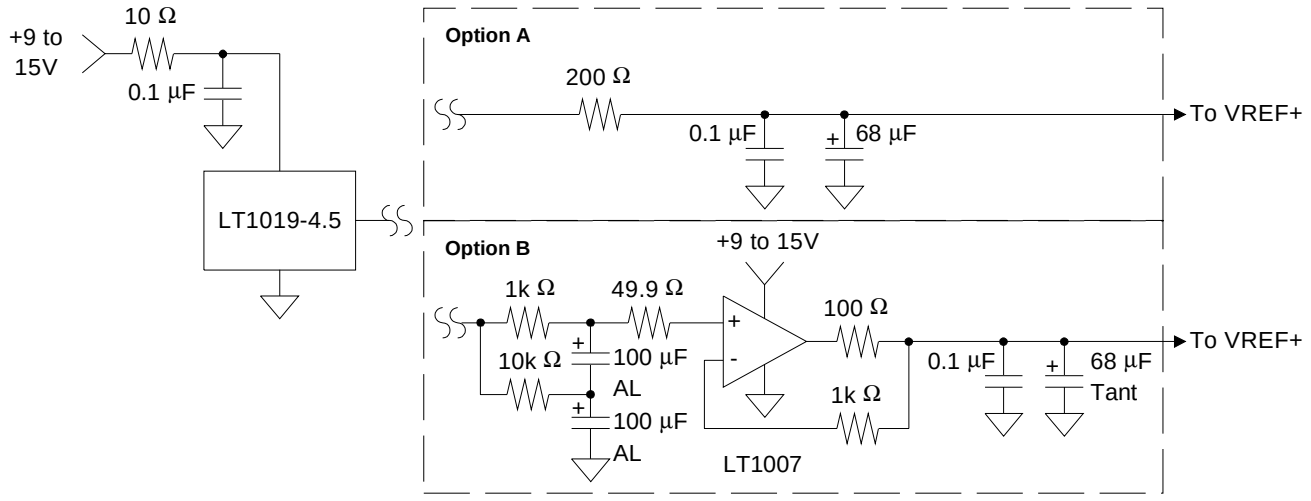


Figure 21. 4.5 Voltage Reference with two filter options

sheet. The clock must have less than 300 ps jitter to maintain data sheet performance from the device. The CS5320/21 is equipped with loss of clock detection circuitry which will cause the CS5320/21 to enter a powered-down state if the MCLK is removed or reduced to a very low frequency. The HBR pin on the CS5320/21 modifies the sampling clock rate of the modulator. When HBR = 1, the modulator sampling clock will be at MCLK/4; with HBR = 0 the modulator sampling clock will be at MCLK/8. The chip set will exhibit about 3 dB less S/N performance when the HBR pin is changed from a logic "1" to a logic "0" for the same output word rate from the CS5322.

2.6 Low Power Mode

The CS5320/21 includes a low power operating mode (LPWR =1). When operated with LPWR = 1, the CS5320/21 modulator sampling clock must be restricted to rates of 128 kHz or less. Operating in low power mode with modulator sample rates greater than 128 kHz will greatly degrade performance.

2.7 Digital Interface and Data Format

The MCLK signal (normally 1.024 MHz) is divided by four, or by eight inside the CS5320/21 to generate the modulator oversampling clock. The HBR pin determines whether the clock divider inside the CS5320/21 divides by four (HBR =1) or by eight (HBR = 0). The modulator outputs a ones density bit stream from its MDATA and $\overline{\text{MDATA}}$ pins proportional to the analog input signal, but at a bit rate determined by the modulator over sampling clock. For proper synchronization of the bitstream, the CS5320/21 must be furnished with an MSYNC signal prior to data conversion. The MSYNC signal, generated by the CS5322, resets the MCLK counter-divider in the CS5320/21 to the correct phase so that the bitstream can be properly sampled by the CS5322 digital filter.

When operated with the CS5322 digital filter the output codes from the CS5320/21/22 will range from approximately decimal -5,242,880 to +5,242,879 for an input to the CS5320/21 of ±4.5 V. Table 1 illustrates the output coding for various input signal amplitudes. Note that with a signal input defined as a full scale signal (4.5 V with VREF+ = 4.5 V) the CS5320/22 and CS5321/22 chipsets does not output a full scale digital code of 8,388,607 but is scaled to a lower value to allow some overrange capability. Input signals can exceed the defined full scale by up to 5% and still be converted properly.

Modulator Input Signal	CS5322 Filter Output Code	
	HEX	Decimal
> (+VREF + 5%)	Error Flag Possible	
≈ (+VREF + 5%)	53FFFF(H)	+5505023
+VREF	4FFFFF(H)	+5242879
0V	000000(H)	0
-VREF	B00000(H)	-5242880
≈ - (+VREF +5%)	AC0000(H)	-5505024
> - (+VREF +5%)	Error Flag Possible	

Table 1. Output Coding for the CS5320/21 and CS5322 Combination

2.8 Performance

Figure 22, 23 and 24 illustrate the spectral performance of the CS5321/22 and CS5320/22 chipsets when operating from a 1.024 MHz master clock. Ten 1024 point FFTs were averaged to produce the plots.

Figure 22 illustrates the chip set with a 100 Hz, -20 dB input signal. The sample rate was set at 1 kHz. Dynamic range is 122 dB.

The dynamic range calculated by the test soft-ware is reduced somewhat in Figures 23 and 24 because of jitter in the signal test oscillator. Jitter in the 100 Hz signal source is interpreted by the signal processing software to be increased noise.

The choice of master clock frequency will affect performance. The CS5320/21 will exhibit the best Signal/ Distortion performance with slower modulator sampling clock rates as slower sample rates allow more time for amplifier settling.

For lowest offset drift, the CS5320/21 should be operated with MCLK = 1.024 MHz and HBR = 1. Slower modulator sampling clock rates will exhibit more offset drift. Changing MCLK to 512 kHz (HBR = 1) or changing HBR to zero (MCLK = 1.024 MHz) will cause the drift rate to double. Offset drift is not linear over temperature so it is difficult to specify an exact drift rate. Offset drift characteristics vary from part to part and will vary as the power supply voltages vary. Therefore, if the CS5320/21 is to be used in precision dc measurement applications where offset drift is to be minimized, the power supplies should be well regulated. The CS5320/21 will exhibit about 6 ppm/°C of offset drift with MCLK = 1 and HBR = 1.

Gain drift of the CS5320/21 itself is about 5 ppm/°C and is not affected by either modulator sample rate or by power supply variation.

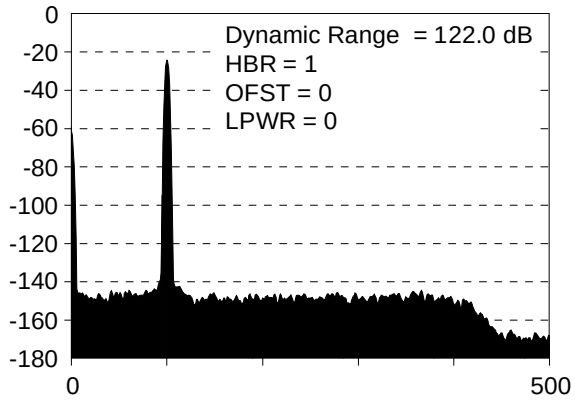


Figure 22. 1024 Point FFT Plot with -20 dB Input, 100 Hz Input, ten averages

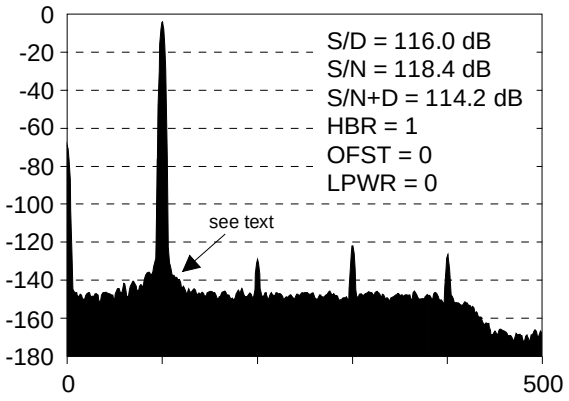


Figure 23. 1024 Point FFT Plot with Full Scale Input, 100 Hz Input, HBR = 1, ten averages

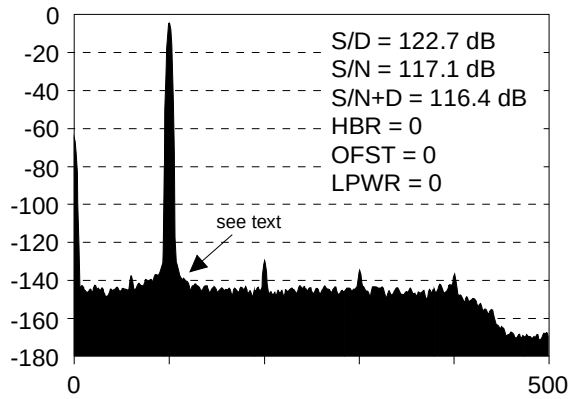


Figure 24. 1024 Point FFT Plot with Full Scale Input, 100 Hz Input, HBR = 0, ten averages

2.9 Power Supply Considerations

The system connection diagram, Figure 20, illustrates the recommended power supply arrangements. There are two positive power supply pins for the CS5320/21 and two negative power supply pins. Power must be supplied to all four pins and each of the supply pins should be de-coupled with a 0.1 µF capacitor to the nearest ground pin on the device.

When used with the CS5322 digital filter, the maximum voltage differential between the positive supplies of the CS5320/21 and the positive digital supply of the CS5322 must be less than 0.25 V. Operation beyond this constraint may result in loss of analog performance in the CS5320/22 and CS5321/22 system performance.

Many seismic or portable data acquisition systems are battery powered and utilize dc-dc converters to generate the necessary supply voltages for the system. To minimize the effects of power supply interference, it is desirable to operate the dc-dc converter at a frequency which is rejected by the digital filter, or locked to the modulator sample clock rate.

A synchronous dc-dc converter, whose operating frequency is derived from the 1.024 MHz clock used to drive the CS5322, will minimize the potential for "beat frequencies" appearing in the passband between dc and the corner frequency of the digital filter.

2.10 Power Supply Rejection Ratio

The PSRR of the CS5320/21 is frequency dependent. The CS5322 digital filter attenuation will aid in rejection of power supply noise for frequencies above the corner frequency setting of the CS5322. For frequencies between dc and the corner frequency of the digital filter, the PSRR is nearly constant at about 60 dB.

2.11 RESET Operation

The RESET pin puts the CS5322 into a known initialized state. RESET is recognized on the next CLKIN rising edge after the RESET pin has been brought high (RESET=1). All internal logic is initialized when RESET is active.

Normal device operation begins on the second CLKIN rising edge after RESET is brought low. The CS5322 will remain in an idle state, not performing convolutions, until triggered by a SYNC event.

A RESET operation clears memory, sets the data output register, offset register, and status flags to all zeroes, and sets the configuration register to the state of the corresponding hardware pins (PWDN, ORCAL, DECC, DECB, DECA, USEOR, and CSEL). The reset state is entered on power on, independent of the RESET pin. If RESET is low, the first CLKIN will exit the power on reset state.

2.12 Power-down Operation

The PWDN pin puts the CS5322 into the power-down state. The power-down state is entered on the first CLKIN rising edge after the PWDN pin is brought high. While in the power-down state, the MCLK and MSYNC signals to the CS5320/21 analog modulator are held low. The loss of the MCLK signal to the modulator causes it to power-down. The signals on the MDATA and MFLG pins are ignored. The serial interface of the CS5322 remains active allowing read and write operations. Information in the data register, offset register, configuration register, and convolution data memory are maintained during power-down. The internal controller requires 64 clock cycles after PWDN is asserted before CLKIN stops.

The CS5322 exits the power-down state on the first CLKIN rising edge after the PWDN pin is brought low. The CS5322 then enters an idle state until triggered by a SYNC event.

To avoid possible high current states while in the power down state, the following conditions apply:

1) CLKIN must be active for at least 64 clock cycles after PWDN entry.
2) CSEL and TDATA must not both be asserted high.

2.13 SYNC Operation

The SYNC pin is used to start convolutions and synchronize the CS5322 and CS5320/21 to an external sampling source or timing reference. The SYNC event is recognized on the first CLKIN rising edge after the SYNC pin goes high. SYNC may remain high indefinitely. Only the sequence of SYNC rising followed by CLKIN rising generates a SYNC event.

The SYNC event aligns the output sample and causes the filter to begin convolutions. The first SYNC event causes an immediate DRDY provided DRDY is low. Subsequent data ready events will occur at a rate determined by the decimation rate inputs DECC, DECB, and DECA. Multiple SYNC events can be applied with no effect on operation if they are perfectly timed according to the decimation rate. Any SYNC event not in step with the decimation rate will cause a realignment and loss of data.

2.14 Serial Read Operation

Serial read is used to obtain status or conversion data. The $\overline{CS}$, R/$\overline{W}$, SCLK, RSEL, and SOD pins control the read operation. The serial read operation is activated when $\overline{CS}$ goes low ($\overline{CS}$=0) with the R/$\overline{W}$ pin high (R/$\overline{W}$=1). The RSEL pin selects between conversion data (data register) or status information (status register). The selected serial bit stream is output on the SOD (Serial Output Data) pin.

On read select, SCLK can either be high or low, the first bit appears on the SOD pin and should be latched on the falling edge of SCLK. After the first SCLK falling edge, each SCLK rising edge shifts out a new bit. Status reads are 16 bits, and data reads are 24 bits. Both streams are supplied as MSB first, LSB last.

In the event more SCLK pulses are supplied than necessary to clock out the requested information, trailing zeroes will be output for data reads and trailing LSB's for status reads. If the read operation is terminated before all the bits are read, the internal bit pointer is reset to the MSB so that a re-read will give the same data as the first read, with one exception. The status error flags are cleared on read and will not be available on a re-read.

The status error flags must be read before entering the power-down state. If an error has occurred before entering powerdown and the status bit (ER-ROR) has not been read, the status bits (ER-ROR, OVERWRITE, MFLG, ACC1 and ACC2) may not be cleared on status reads. Upon exiting the power-down state and entering normal operation, the user may be flagged that an error is still present.

The SOD pin floats when read operation is deactivated (R/$\overline{W}$=1, $\overline{CS}$=1). This enables the SID and SOD pins to be tied together to form a bi-directional serial data bus. There is an internal nominal 100 kΩ pull-up resistor on the SOD pin.

2.15 Serial Write Operation

Serial write is used to write data to the configuration register. The $\overline{CS}$, R/$\overline{W}$, SCLK and SID pins control the serial write operation. The serial write operation is activated when $\overline{CS}$ goes low ($\overline{CS}$=0) with R/$\overline{W}$ pin low (R/$\overline{W}$=0).

Serial input data on the SID pin is sampled on the falling edge of SCLK. The input bits are stored in a temporary buffer until either the write operation is terminated or 8 bits have been received. The data is then parallel loaded into the configuration register. If fewer than 8 bits are input before the write termination, the other bits may be indeterminate.

Note that a write will occur when $\overline{CS}$ = 0 and R/$\overline{W}$ = 0 even if SCLK is not toggled. Failure to clock in data with the appropriate number of SCLKs can leave the configuration register in an indeterminate condition.

The serial bit stream is received MSB first, LSB last. The order of the input control data is PWDN first, followed by ORCAL, USEOR, CSEL, Reserved, DECC, DECB, and DECA. The configuration data bits are defined in Table 2. The configuration data controls device operation only when in the software mode, i.e., the H/S pin is low (H/S = 0). The Reserved configuration data bit must always be written low.

2.16 Offset Calibration Operation

The offset calibration routine computes the offset produced by the CS5320/21 modulator and stores this value in the offset register. The USEOR pin or bit determines if the offset register data is to be used to correct output words.

After power is applied to the chip set the CS5322 must be RESET. To begin an offset calibration, the CS5320/21 analog input must represent the offset value. Then in software mode (H/S = 0) the ORCAL bit must be toggled from a low to a high. In hardware mode the ORCAL pin must be toggled low for at least one CLKIN cycle, then taken high (except when ORCAL = 1 and the CS5322 is RESET as this toggles the ORCAL internally). After ORCAL has been toggled, the SYNC signal must be applied to the CS5322. The filter settles on the input value in 56 output words. The output word rate is determined by the state of the decimation rate control pins, DECC, DECB, and DECA. On the 57th output word, the CS5322 issues the ORCALD status flag, outputs the offset data sample, and internally loads the offset register. During calibration, the offset register value is not used.

If USEOR is high (USEOR=1), subsequent samples will have the offset subtracted from the output. The state of USEOR must remain high for the complete duration of the convolution cycle. If USEOR is low (USEOR=0), the output word is not corrected, but the offset register retains its value for later use. The results of the last calibration will be held in the offset register until the end of a new calibration, or until the CS5322 is reset using the RESET pin. USEOR does not alter the offset register value, only its usage.

To restart a calibration, ORCAL and SYNC must be taken low for at least one CLKIN cycle. ORCAL must then be taken high. The calibration will restart on the next SYNC event. If the ORCAL pin remains in a high state, only a single calibration will start on the first SYNC signal.

Input Bit #	Equivalent Hardware Function	Description
1 (MSB)	PWDN	Standby mode
2	ORCAL	Self-offset calibration
3	USEOR	Use Offset Register
4	CSEL	Channel Select
5	Reserved	Factory use only
6	DECC	Filter BW selection
7	DECB	Filter BW selection
8 (LSB)	DECA	Filter BW selection

Table 2. Configuration Data Bits

2.17 Status Bits

The Status Register is a 16-bit register which allows the user to read the flags and configuration settings of the CS5322. Table 3 documents the data bits of the Status Register.

The ERROR flag, $\overline{\text{ERROR}}$, is the OR'ed result of OVERWRITE, MFLG, ACC1, and ACC2. The ERROR bit is active high whenever any of the four error bits are set due to a fault condition. The $\overline{\text{ERROR}}$ output has a nominal 100 KΩ internal pull-up resistor.

The OVERWRITE bit is set when new conversion data is ready to be loaded into the data register, but the previous data was not completely read out. This can occur on either of two conditions: a read operation is in progress or a read operation was started, then aborted, and not completed. These two conditions are data read attempts. The attempt is identified by the first SCLK low edge (MSB read) of a data register read. If a data register read is not attempted, the CS5322 assumes that data is not wanted and does not assert OVERWRITE, and the old data is over-written by the new data. On an OVERWRITE condition, the old partially read data is preserved, and the new data word is lost.

Status reads have no effect on OVERWRITE assert operations. The OVERWRITE bit is cleared on a status register read or RESET.

The MFLG error bit reflects the CS5320/21 MFLG signal. Any high level on the CS5322 MFLG pin will set the MFLG status bit. The bit is cleared on a status register read or RESET operation, only if the MFLG pin on the CS5322 has returned low. A internal nominal 100 KΩ pulldown resistor is on the MFLG pin.

The accumulator error bits, ACC1 and ACC2, indicate that an underflow or overflow has occurred in the FIR1 filter for ACC1, or the FIR2 and FIR3 filters for ACC2. Both errors are cleared on a status read, provided the error conditions are no longer

Output Bit #	Function	Description
1 (MSB)	Error	Detects one of the errors below
2	OVERWRITE Error	Overwrite Error
3	MFLG Error	Modulator Flag Error
4	ACC1 Error	Accumulator 1 Error
5	ACC2 Error	Accumulator Error
6	DRDY	Data Ready
7	1SYNC	First sample after SYNC
8	ORCALD	Offset calibration done
9	PWDN	Standby mode
10	ORCAL	Self-offset Calibration
11	USEOR	Use Offset Register
12	CSEL	Channel Select
13	Reserved	Factory use only
14	DECC	Bandwidth Selection Status
15	DECB	Bandwidth Selection Status
16	DECA	Bandwidth Selection Status

Table 3. Status Data (from the SOD Pin)

present. In normal operation the ACC1 error will only occur when the input data stream to FIR1 is all 1's for more than 32 bits. The ACC2 error cannot occur in normal operation.

The DRDY bit reflects the state of the DRDY pin. DRDY rising edge indicates that a new data word has been loaded into the data register and is available for reading. DRDY will fall after the SCLK falling edge that reads the data register LSB. If no-data read attempt is made, DRDY will pulse low for 1/2 CLKIN cycle, providing a positive edge on the new data availability. In the OVERWRITE case, DRDY remains high because new data is not loaded at the normal end of conversion time.

The 1SYNC status bit provides an indication of the filter group delay. It goes high on the second output sample after SYNC and is valid for only that sample. For repetitive SYNC operations, SYNC must run at one fourth the output word rate or slower to avoid interfering with the 1SYNC operation. With these slower repetitive SYNC's or non-periodic SYNC's separated by at least three output words, 1SYNC will occur on the second output sample after SYNC.

ORCALD indicates that calibration of the offset register is complete and the offset sample is available in the output register. This flag is high only during that sample and is otherwise low.

The remaining five status bits (PWDN, ORCAL, USEOR, CSEL, Reserved, DECC, DECB, and DECA) provide configuration readback for the user. These bits echo the control source for the CS5322 such that in the hardware mode ($H/\overline{S}$=1), they follow the corresponding input pins. In host mode ($H/\overline{S}$=0) they follow the corresponding configuration bits.

A brief explanation of the eight bits are as follows:

PWDN - When high, indicates that the CS5322 is in the power-down state.

ORCAL - When high, indicates a potential calibration start.

USEOR - When high, indicates the Offset Register is used. During calibration, this bit will read zero indicating the offset register is not being used during calibration.

CSEL- When high, TDATA is selected as the filter source. When low, the MDATA output signal from the CS5320/21 is selected as the input source to the filter.

Reserved - Always read low.

DECC, DECB, and DECA - Indicate the decimation rate of the filter and are defined in Table 4.

DECC	DECB	DECA	Output Word Rate (Hz)	Clocks Filter Output
0	0	0	62.5	16384
0	0	1	125	8192
0	1	0	250	4096
0	1	1	500	2048
1	0	0	1000	1024
1	0	1	2000	512
1	1	0	4000	256
1	1	1	Reserved	-

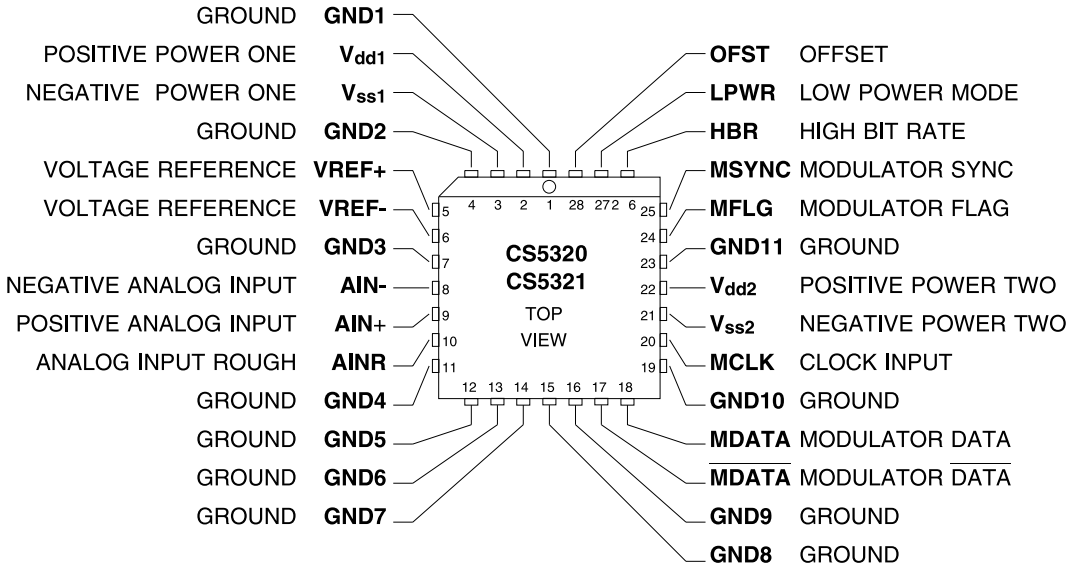
Table 4. Bandwidth Selection: Truth Table

2.18 Board Layout Considerations

All of the 0.1 µF filter capacitors on the power supplies, AIN+, and AINR, should be placed very close to the chip and connect to the nearest ground pin on the device. The capacitors between VREF+ and VREF- should be located as close to the chip as possible. The 0.l µF capacitors on the AIN+ and AINR pins should be placed with their leads on the same axis, not side-by-side. If these capacitors are placed side-by-side their electric fields can interact and cause increased distortion. The chip should be surrounded with a ground plane. Trace fill should be used around the analog input components.

See *AN18: Layout and Design Rules for Data Converters* for further information.

3. CS5320/21 PIN DESCRIPTIONS



Power Supplies

V_{dd1} – Positive Power One, PIN 2

Positive supply voltage. Nominally +5 Volts.

V_{dd2} – Positive Power Two, PIN 22

Positive supply voltage. Nominally +5 Volts.

V_{ss1} – Negative Power One, PIN 3

Negative supply voltage. Nominally -5 Volts.

V_{ss2} – Negative Power Two, PIN 21

Negative supply voltage. Nominally -5 Volts.

GND1 through GND11 – Ground, PINS 1, 4, 7, 11, 12, 13, 14, 15, 16, 19, 23.

Ground reference.

Analog Inputs

AIN+ - Positive Analog Input, PIN 9

Nominally ± 4.5V

AIN- - Negative Analog Input, PIN 8

This pin is tied to ground.

AINR - Analog Input Rough, PIN 10

Allows a non-linear current to bypass the main external anti-aliasing filter which if allowed to happen, would cause harmonic distortion in the modulator. Please refer to the System Connection Diagram and the Analog Input and Voltage Reference section of the data sheet for recommended use of this pin.

VREF+ – Positive Voltage Reference Input, PIN 5

This pin accepts an external +4.5 V voltage reference.

VREF- – Negative Voltage Reference Input, PIN 6

This pin is tied to ground.

Digital Inputs

MCLK – Clock Input, PIN 20

A CMOS-compatible clock input to this pin (nominally 1.024 MHz) provides the necessary clock for operation of the modulator and data output portions of the A/D converter. MCLK is normally supplied by the CS5322

MSYNC – Modulator Sync, PIN 25

A transition from a low to high level on this input will re-initialize the CS5320/21. MSYNC resets a divider-counter to align the MDATA output bit stream from the CS5320/21 with the timing inside the CS5322.

OFST - Offset, PIN 28

When high, adds approximately 100 mV of input referred offset to guarantee that any zero input limit cycles are out of band if present. When low, zero offset is added.

LPWR - Low Power Mode, PIN 27

The CS5320/21 power dissipation can be reduced from its nominal value of 55 mW to 30 mW under the following conditions:

LPWR=1; MCLK = 512 kHz, HBR=1; or LPWR=1; MCLK = 1.024 MHz, HBR=0

HBR – High Bit Rate, Pin 26

Selects either 1/4 MCLK (HBR=1) or 1/8MCLK (HBR=0) for the modulator sampling clock.

Digital Outputs

MDATA – Modulator Data Output, PIN 18

Data will be presented in a one-bit serial data stream at a bit rate of 256 kHz (HBR=1) or 128 kHz (HBR=0) with MCLK operating at 1.024 MHz.

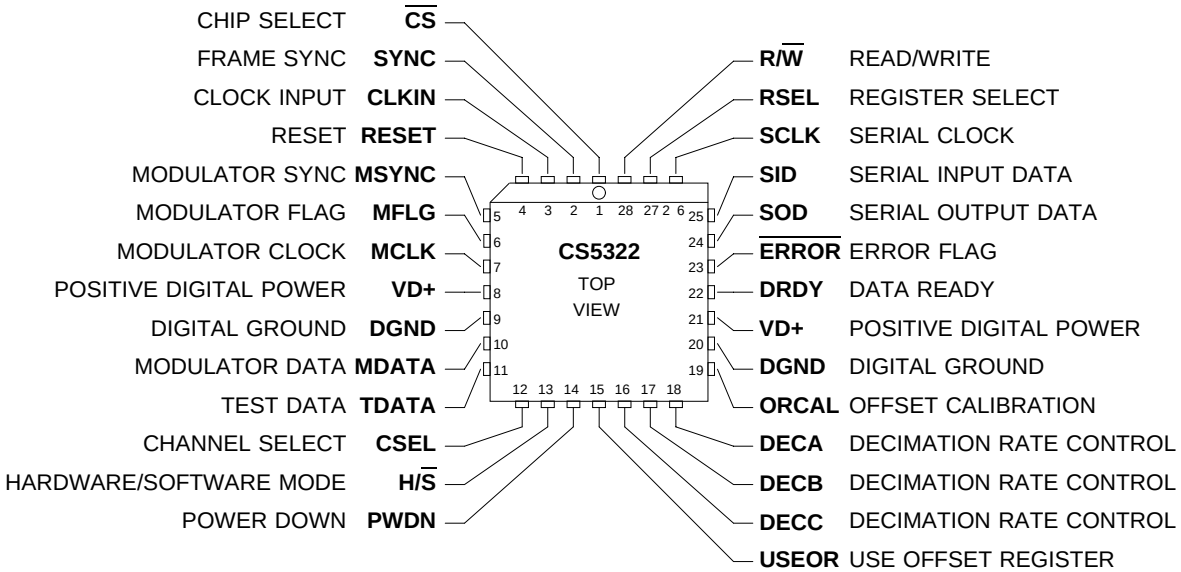
$\overline{\text{MDATA}}$ – Modulator Data Output, PIN 17

Inverse of the MDATA output.

MFLG – Modulator Flag, PIN 24

A transition from a low to high level signals that the CS5320/21 modulator is unstable due to an over-range on the analog input

4. CS5322 PIN DESCRIPTIONS



Power Supplies

VD+ – Positive Digital Power, Pin 8, 21

Positive digital supply voltage. Nominally +5 volts.

DGND – Digital Ground, Pin 9, 20

Digital ground reference.

Digital Outputs

MCLK – Modulator Clock Output, Pin 7

A CMOS-compatible clock output (nominally 1.024 MHz) that provides the necessary clock for operation of the modulator.

MSYNC – Modulator Sync, Pin 5

The transition from a low to high level on this output will re-initialize the CS5320/21.

$\overline{\text{ERROR}}$ - Error Flag, Pin 23

This signal is the output of an open pull-up NOR gate with a nominal 100 kΩ pull-up resistor to which the error status data (OVERWRITE error, MFLG error, ACC1 error and ACC2 error) are inputs. When low, it notifies the host processor that an error condition exists. The $\overline{\text{ERROR}}$ signal can be wire OR'd together with other filters' outputs. The value of the internal pull-up resistor is 100 kΩ.

DRDY - Data Ready, Pin 22

When high, data is ready to be shifted out of the serial port data register.

SOD - Serial Output Data, Pin 24

The output coding is 2's complement with the data bits presented MSB first, LSB last. Data changes on the rising edge of SCLK. An internal nominal 100 kΩ pull-up resistor is included.

Digital Inputs

MDATA – Modulator Data, Pin 10

Data will be presented in a one-bit serial data stream at a bit rate of 256 KHz; (CLKIN = 1.024 MHz).

TDATA - Test Data, Pin 11

Input for user test data.

MFLG – Modulator Flag, Pin 6

A transition from a low to high level signals that the CS5320/21 modulator is unstable due to an over-range on the analog input. A Status Bit will be set in the digital filter indicating an error condition. An internal nominal 100 kΩ pull-down resistor included on the input pin.

RESET - Filter Reset, Pin 4

Performs a hard reset on the chip, all registers and accumulators are cleared. All signals to the device are locked out except CLKIN. The error flags in the Status Register are set to zero and the Data Register and Offset Register are set to zero. The configuration register is set to the values of the corresponding input pins. SYNC must be applied to resume convolutions after RESET deasserts.

CLKIN - Clock Input, Pin 3

A CMOS-Compatible clock input to this pin (nominally 1.024 MHz) provides the necessary clock for operation the modulator and filter.

SYNC - Frame Sync, Pin 2

Conversion synchronization input. This signal synchronizes the start of the filter convolution. More than one SYNC signal can occur with no effect on filter performance, providing the SYNC signals are perfectly timed at intervals equal to the output sample period.

CSEL - Channel Select, Pin 12

When high, information on the TDATA pin is presented to the digital filter. A low causes data on the MDATA input to be presented to the digital filter.

PWDN - Powerdown, Pin 14

Powers down the filter when taken high. Convolution cycles in the digital filter and the MCLK signal are stopped. The registers maintain their data and the serial port remains active. SYNC must be applied to resume convolutions after PWDN deasserts.

DECA - Decimation Rate Control, Pin 18

See Table 4.

DECB - Decimation Rate Control, Pin 17

See Table 4.

DECC - Decimation Rate Control, Pin 16

See Table 4.

H/$\overline{S}$ - Hardware/Software Mode Select, Pin 13

When high, the device pins control device operation; when low, the value entered by a prior configuration write controls device operation.

$\overline{CS}$ - Chip Select, Pin 1

When high, all signal activity on the SID, R/$\overline{W}$ and SCLK pins is ignored. The DRDY and $\overline{ERROR}$ signals indicate the status of the chip's internal operation.

R/$\overline{W}$ - Read/Write, Pin 28

Used in conjunction with $\overline{CS}$ such that when both signals are low, the filter inputs data from the SID pin on the falling edge of SCLK. If $\overline{CS}$ is low and R/$\overline{W}$ is high, the filter outputs data on the SOD pin on the rising edge of SCLK. R/$\overline{W}$ low floats the SOD pin allowing SID and SOD to be tied together, forming a bidirectional serial data bus.

SCLK - Serial Clock, Pin 26

Clock signal generated by host processor to either input data on the SID input pin, or output data on the SOD output pin. For write, data must be valid on the SID pin on the falling edge of SCLK. Data changes on the SOD pin on the rising edge of SCLK.

SID - Serial Data Input, Pin 25

Data bits are presented MSB first, LSB last. Data is latched on the falling edge of SCLK.

RSEL - Register Select, Pin 27

Selects conversion data when high, or status data when low.

USEOR - Use Offset Register, Pin 15

Use offset register value to correct output words when high. Output words will not be offset corrected when low.

ORCAL - Offset Register Calibrate, Pin 19

Initiates an offset calibration cycle when SYNC goes high after ORCAL has been toggled from low to high. The offset value is output on the 57th word following SYNC. Subsequent words will have their offset correction controlled by USEOR.

5. ORDERING INFORMATION

Kits	Analog Modulator			Digital Filter		
Part Number	Part Number	Temperature	Package	Part Number	Temperature	Package
CK5320-KL1	CS5320-KL	0^{o} to $+70^{o}$ C	28-pin PLCC	CS5322-KL	0^{o} to $+70^{o}$ C	28-pin PLCC
CK5321-KL1	CS5321-BL	-55^{o} to $+85^{o}$ C	28-pin PLCC	CS5322-KL	0^{o} to $+70^{o}$ C	28-pin PLCC
CK5321-BL1	CS5321-BL	-55^{o} to $+85^{o}$ C	28-pin PLCC	CS5322-BL	-40^{o} to $+85^{o}$ C	28-pin PLCC

Table 5. Detailed Ordering Information

6. PARAMETER DEFINITIONS

Dynamic Range

The ratio of the full-scale (rms) signal to the broadband (rms) noise signal. Broadband noise is measured with the input grounded within the bandwidth of 1 Hz to f3 Hz (See "CS5322 FILTER CHARACTERISTICS" on page 8). Units in dB.

Signal-to-Distortion

The ratio of the full-scale (rms) signal to the rms sum of all harmonics up to f3 Hz.
Units in dB.

Intermodulation Distortion

The ratio of the rms sum of the two test frequencies (30 and 50 Hz) which are each 6 dB down from full-scale to the rms sum of all intermodulation components within the bandwidth of dc to f3 Hz. Units in dB.

Full Scale Error

The ratio of the difference between the value of the voltage reference and analog input voltage to the full scale span (two times the voltage reference value). This ratio is calculated after the effects of offset and the external bias components are removed and the analog input voltage is adjusted. Measurement of this parameter uses the circuitry illustrated in the System Connection Diagram. Units in %.

Full Scale Drift

The change in the Full Scale value with temperature. Units in %/°C.

Offset

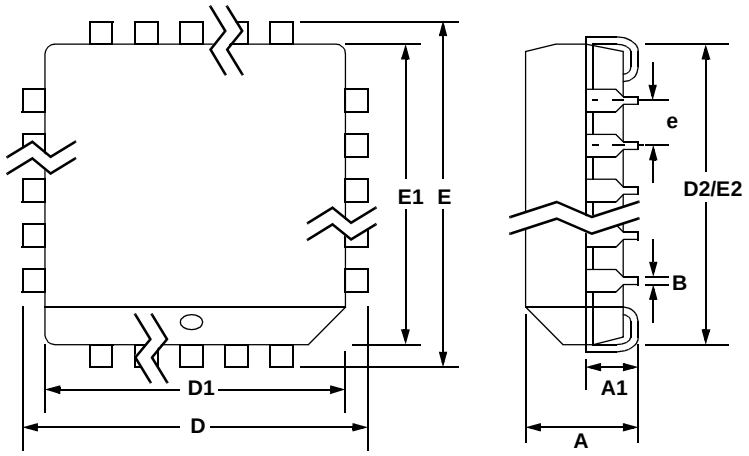
The difference between the analog ground and the analog voltage necessary to yield an output code from the CS5320/22 or CS5321/22 of 000000(H). Measurement of this parameter uses the circuit configuration illustrated in the System Connection Diagram. Units in mV.

Offset Drift

The change in the Offset value with temperature. Measurement of this parameter uses the circuit configuration illustrated in the System Connection Diagram. Units in µV/°C.

7. PACKAGE DIMENSIONS

28L PLCC PACKAGE DRAWING



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.165	0.180	4.043	4.572
A1	0.090	0.120	2.205	3.048
B	0.013	0.021	0.319	0.533
D	0.485	0.495	11.883	12.573
D1	0.450	0.456	11.025	11.582
D2	0.390	0.430	9.555	10.922
E	0.485	0.495	11.883	12.573
E1	0.450	0.456	11.025	11.582
E2	0.390	0.430	9.555	10.922
e	0.040	0.060	0.980	1.524

JEDEC #: MS-018

• Notes •


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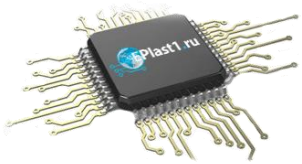
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- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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