REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add two packages, C-5 and C-4. Make changes to table I, and throughout. For case X, the dimensions have been changed and figure 2 has been replaced with D-10 configuration. Inactivate devices 01XX and 02XX for new design. Use M38510 device. Add a truth table.	90-01-24	M. A. Frye
B	Add device types 05, 06, 07, and 08. Add vendors CAGES 1ES66, OH9K9, and 33256. Editorial changes throughout.	93-03-15	M. A. Frye
C	Add class V devices. Add Z package. Editorial changes throughout.	97-04-15	R. Monnin
D	Changes in accordance with NOR 5962-R368-97. – drw	97-06-23	Raymond Monnin
E	Change descriptive designator for case outline Z from GDFP2-F28 to CDFP3-F28. Editorial changes throughout. Redrawn. - drw	99-12-30	Raymond Monnin
F	Sheet 7, table I, V_{IL} test, change max limit from –0.8 V to 0.8 V. - drw	00-03-01	Raymond Monnin
G	Add radiation features and post irradiation limits. - drw	01-05-16	Raymond Monnin
H	Add device type 01 to the post irradiation limits in table I. - drw	02-07-10	Raymond Monnin
J	Sheet 6, table I, Integral linearity error test (ILE), post irradiation limits for device types 01 and 02, subgroup 1, change from -1.0 LSB min to -1.5 LSB min and from 1.0 LSB max to 1.5 LSB max.	03-04-25	Raymond Monnin

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED

REV																				
SHEET																				
REV	H	H	H	H	H	H														
SHEET	15	16	17	18	19	20														

REV STATUS	REV	J	H	H	H	H	J	H	H	H	H	H	H	H	H
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Sandra B. Rooney	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43216** **http://www.dscc.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Charles E. Besore	
	APPROVED BY Michael A. Frye	MICROCIRCUIT, LINEAR, MICROPROCESSOR COMPATIBLE, 12-BIT ANALOG-TO-DIGITAL CONVERTERS, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 86-07-10	
	REVISION LEVEL J	SIZE A CAGE CODE **67268** **5962-85127** SHEET 1 OF 20

DSCC FORM 2233
APR 97

5962-E297-03

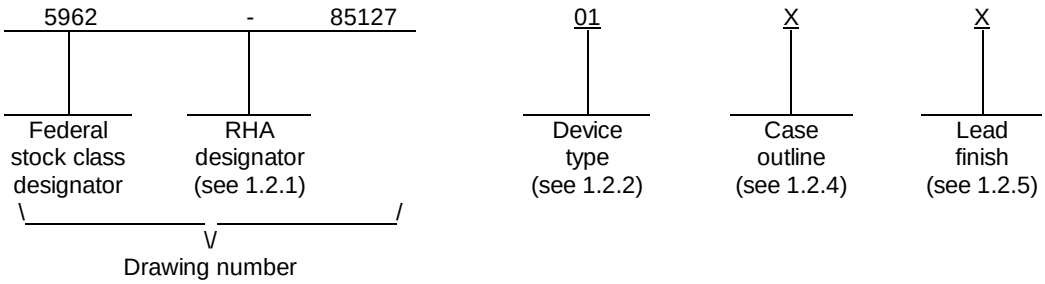
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1. SCOPE

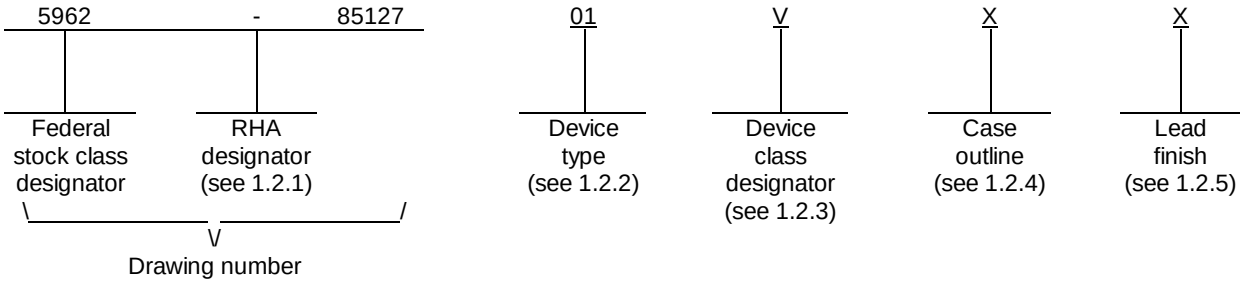
1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following examples.

For device classes M and Q:



For device class V:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function
01	574AU	Monolithic, high performance, 12-bit A/D converter with microprocessor interface
02	574AT	Monolithic, medium performance, 12-bit A/D converter with microprocessor interface
03	574AU	Multi-chip, high performance, 12-bit A/D converter with microprocessor interface
04	574AT	Multi-chip, medium performance, 12-bit A/D converter with microprocessor interface
05	574ZA	Monolithic, high performance, low power, 12-bit A/D converter with microprocessor interface
06	574ZB	Monolithic, medium performance, low power, 12-bit A/D converter with microprocessor interface
07	574AU	Monolithic, high performance, low power, 12-bit A/D converter with microprocessor interface
08	574AT	Monolithic, medium performance, low power, 12-bit A/D converter with microprocessor interface

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as listed below. Since the device class designator has been added after the original issuance of this drawing, device classes M and Q designators will not be included in the PIN and will not be marked on the device.

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	dual-in-line
Y	CQCC1-N44	44	square leadless chip carrier
Z	CDFP3-F28	28	flat pack
3	CQCC1-N28	28	square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

V_{CC} to digital common	0 to +16.5 V dc
V_{EE} to digital common	0 to -16.5 V dc
V_{LOG} to digital common	0 to +7 V dc
Analog to digital common:	
Device types 01, 02, 03, 04	$\pm$1 V dc
Device types 05, 06, 07, 08	-0.5 V dc to +1 V dc
Control inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to digital common	-0.5 V dc to V_{LOG} +0.5 V dc
Analog inputs (REF IN, BIP OFF, 10 V_{IN}) to analog common	V_{EE} to V_{CC}
20 V_{IN} analog input voltage to analog common	$\pm$24 V dc
$V_{REF\ OUT}$	Indefinite short to common, 10 ms short to V_{CC}
Power dissipation at 75°C:	
Device types 01, 02, 05, 06, 07, 08	1,000 mW 2/
Device types 03, 04	2,080 mW 2/
Lead temperature (soldering, 10 seconds)	+300°C
Storage temperature	-65°C to +150°C
Thermal resistance, junction-to-ambient (θ_{JA}):	
Cases X and 3	70°C/W
Case Y	38°C/W
Case Z	60°C/W
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ For cases X and 3, derate linearly above T_A = +75°C at 20.8 mW/°C.
For cases Y, derate linearly above T_A = +75°C at 22.7 mW/°C.
For cases Z, derate linearly above T_A = +115°C at 17 mW/°C.

1.4 Recommended operating conditions.

Power supply
Operating voltage range:
Positive supply (V_{LOG}) ..... +4.5 V dc to +5.5 V dc
Positive supply (V_{CC}) ..... +11.4 V dc to +16.5 V dc
Negative supply (V_{EE}) ..... -11.4 V dc to -16.5 V dc
Ambient operating temperature range ..... -55°C to +125°C

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rad(Si)/s) ..... ≤100 Krads (Si)

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Block or logic diagrams. The block or logic diagrams shall be as specified on figure 3.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 81 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ V_{CC} = +15 V, V_{LOG} = +5 V, V_{EE} = -15 V 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power supply current From V_{LOG}	I_{LOG}		1, 2, 3	01, 02, 03, 04		40	mA
		M, D, P, L, R	1	01, 02		40	
			1, 2, 3	05, 06, 07, 08		1	
Power supply current From V_{CC}	I_{CC}		1, 2, 3	01, 02		5	mA
		M, D, P, L, R	1	01, 02		5	
			1, 2, 3	03, 04		15	
				05, 06, 07, 08		9	
Power supply current From V_{EE}	I_{EE}		1, 2, 3	01, 02, 03, 04	-30		mA
		M, D, P, L, R	1	01, 02	-30		
			1, 2, 3	05, 06, 07, 08	0		
Resolution			1, 2, 3	All	12		Bits
Integral linearity error	ILE		1	All	-0.5	0.5	LSB
			2, 3		-1.0	1.0	
		M, D, P, L, R	1	01, 02	-1.5	1.5	
Differential linearity error (minimum resolution for which no missing codes guaranteed) 2/	DLE		1	All	12		Bits
			2, 3		12		
Unipolar offset voltage error	V_{IO}	T_A = +25°C	1	All	-2.0	2.0	LSB
		M, D, P, L, R	1	01, 02	-3.0	3.0	
			12	01	-1.0	1.0	
Unipolar offset drift 2/	$\frac{\Delta V_{IO}}{\Delta T}$	Using internal reference	1, 2, 3 3/	01, 02	-1.0	1.0	LSB
			2, 3	03, 04 05, 06 07, 08			
Bipolar offset voltage error	B_Z	T_A = +25°C	1	All	-4.0	4.0	LSB
		M, D, P, L, R	1	01, 02	-5.0	5.0	
			12	01	-2.0	2.0	
Bipolar zero offset drift 2/	$\frac{\Delta B_Z}{T}$	Using internal reference	1, 2, 3 3/	01	-1.0	1.0	LSB
			2, 3	03, 05, 07			
			1, 2, 3 3/	02	-2.0	2.0	
			2, 3	04, 06, 08			

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ V_{CC} = +15 V, V_{LOG} = +5 V, V_{EE} = -15 V 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Gain error	ΔA_E	T_A = +25°C	1	01, 02		0.25	% of F.S.
		M, D, P, L, R	1	01, 02		0.35	
		With 50Ω resistor from REF OUT to REF IN	1	03, 04, 05, 06, 07, 08		0.30	
			12	01		0.125	
Gain error drift 2/	$\frac{\Delta A_E}{\Delta T}$	Using internal reference	1, 2, 3 3/	01	-12.5	12.5	ppm/°C
			2, 3	03, 05, 07			
			1, 2, 3 3/	02	-25.0	25.0	
			2, 3	04, 06, 08			
Power supply sensitivity (Maximum change in full scale calibration) 2/	$+P_{SS1}$	+13.5 V ≤ V_{CC} ≤ +16.5 V T_A = +25°C	1	All	-1.0	1.0	LSB
	$+P_{SS2}$	+11.4 V ≤ V_{CC} ≤ +12.6 V T_A = +25°C					
	$+P_{SS3}$	+4.5 V ≤ V_{LOG} ≤ +5.5 V T_A = +25°C	1	All	-0.5	0.5	
	$-P_{SS1}$	-16.5 V ≤ V_{EE} ≤ -13.5 V T_A = +25°C	1	All	-1.0	1.0	
	$-P_{SS2}$	-12.6 V ≤ V_{EE} ≤ -11.4 V T_A = +25°C					
Input Impedance 2/	Z_{IN}	10 V span, T_A = +25°C	4	All	3	7	kΩ
		20 V span, T_A = +25°C	4	01, 02, 03, 04	6	14	
				05, 06, 07, 08	15	25	
Internal reference voltage	V_{REF}	T_A = +25°C 4/	1	01, 02	9.98	10.02	V
		M, D, P, L, R	1	01, 02	9.95	10.05	
			1	03, 04 07, 08	9.90	10.10	
				05, 06	9.97	10.03	
			12	01	9.99	10.01	
Output current 2/, 5/	I_O	Available for external loads T_A = +25°C	1	01, 02, 03, 04		1.5	mA
				05, 06, 07, 08		2.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ V_{CC} = +15 V, V_{LOG} = +5 V, V_{EE} = -15 V 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input voltage (CE, $\overline{CS}$, 12/8, R/$\overline{C}$, A_O) 2/, 6/	V_{IH}	Logic "1", T_A = +25°C	1	01, 02, 05, 06, 07, 08	2.0	5.5	V
				03, 04	2.4	5.5	
	V_{IL}	Logic "0", T_A = +25°C	1	All	-0.5	0.8	
Input current 2/	I_{IN}	T_A = +25°C	1	01, 02, 03, 04, 07, 08	-20	+20	µA
				05,06	-1	1	
Output voltage (DB11-DB0, STS) 2/	V_{OL}	Logic "0", T_A = +25°C, I_{SINK} = +1.6 mA	1	All		0.4	V
Output voltage (DB11-DB0) 2/	V_{OH}	Logic "1", T_A = +25°C, I_{SOURCE} = +500 µA	1 1	All	2.4		V
High impedance state output current 2/	I_Z	High-Z state, T_A = +25°C, DB11 – DB0 only	1	01, 02, 03, 04, 07, 08	-20	+20	µA
				05, 06	-5	+5	
Functional tests		See 4.4.1b, T_A = +25°C	7	All			
Low R/$\overline{C}$ pulse width 2/, 7/	t_{HRL}	See figure 4	9, 10, 11	01, 02	250		ns
				03, 04	350		
				05, 06, 07, 08	50		
STS delay from R/$\overline{C}$ 2/, 7/	t_{DS}	See figure 4	9, 10, 11	01, 02, 03, 04		600	ns
				05, 06, 07, 08		200	
Data valid after R/$\overline{C}$ low 2/, 7/	t_{HDR}	See figure 4	9, 10, 11	01, 02, 05, 06, 07, 08	25		ns
				03, 04	15		
STS delay after valid data 2/,7/	t_{HS}	See figure 4	9, 10, 11	01, 02, 05, 06, 07, 08	300	1000	ns
				03, 04	300	1200	
High R/$\overline{C}$ pulse width 2/, 8/	t_{HRH}	See figure 4	9, 10, 11	01, 02, 03, 04	300		ns
				05, 06, 07, 08	150		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ V_{CC} = +15 V, V_{LOG} = +5 V, V_{EE} = -15 V 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data access time 2/,8/	t_{DDR}	See figure 4	9, 10, 11	01, 02, 03, 04		250	ns
				05, 06, 07, 08		150	
STS delay from CE 2/, 8/	t_{DSC}	See figure 4	9, 10, 11	01, 02, 03, 04		350	ns
				05, 06, 07, 08		200	
CE pulse width 2/, 8/	t_{HEC}	See figure 5	9, 10, 11	01, 02, 03, 04	300		ns
				05, 06, 07, 08	50		
Conversion time 2/, 9/	t_C	8-bit cycle See figure 5	9, 10, 11	01,02 5/	10	24	µs
				03, 04, 05, 06, 07, 08	10	17	
		12-bit cycle See figure 5	9, 10, 11	01,02 5/	15	35	
				03, 04, 05, 06, 07, 08	15	25	
Access time (from CE) 2/, 7/	t_{DD}	See figure 6	9, 10, 11	01, 02		200	ns
				03, 04		250	
				05, 06, 07, 08		150	
Data valid after CE low 2/, 7/	t_{HD}	See figure 6	9, 10, 11	01, 02, 05, 06, 07, 08	25		ns
				03, 04	15		
Output float delay 2/, 7/	t_{HL}	See figure 6	9, 10, 11	01, 02		100	ns
				03, 04, 05, 06, 07, 08		150	

1/ Devices supplied to this drawing have been characterized through all levels M, D, P, L, and R of irradiation. However, this device is only tested at the "R" level. Pre and post irradiation values are identical unless otherwise specified in table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.
2/ This parameter is not tested post irradiation.
3/ Guaranteed to the limits specified, if not tested for subgroup 1.
4/ The reference voltage external load current shall be a constant dc and shall not exceed 1.5 mA.
5/ Reference should be buffered for operation on ±12 V supplies. External load should not change during conversion.
6/ For devices 01 and 02, 12/$\overline{8}$ is not TTL compatible and must be hard wired to V_{LOG} or digital ground.
7/ Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits.
8/ Parameters t_{HRH}, t_{DDR}, t_{DSC}, and t_{HEC}, if not tested, shall be guaranteed to the specified limits.
9/ For devices 03 and 04, time measured from 50 percent level of digital transitions, tested with 50 pF and 3.0 kΩ load.

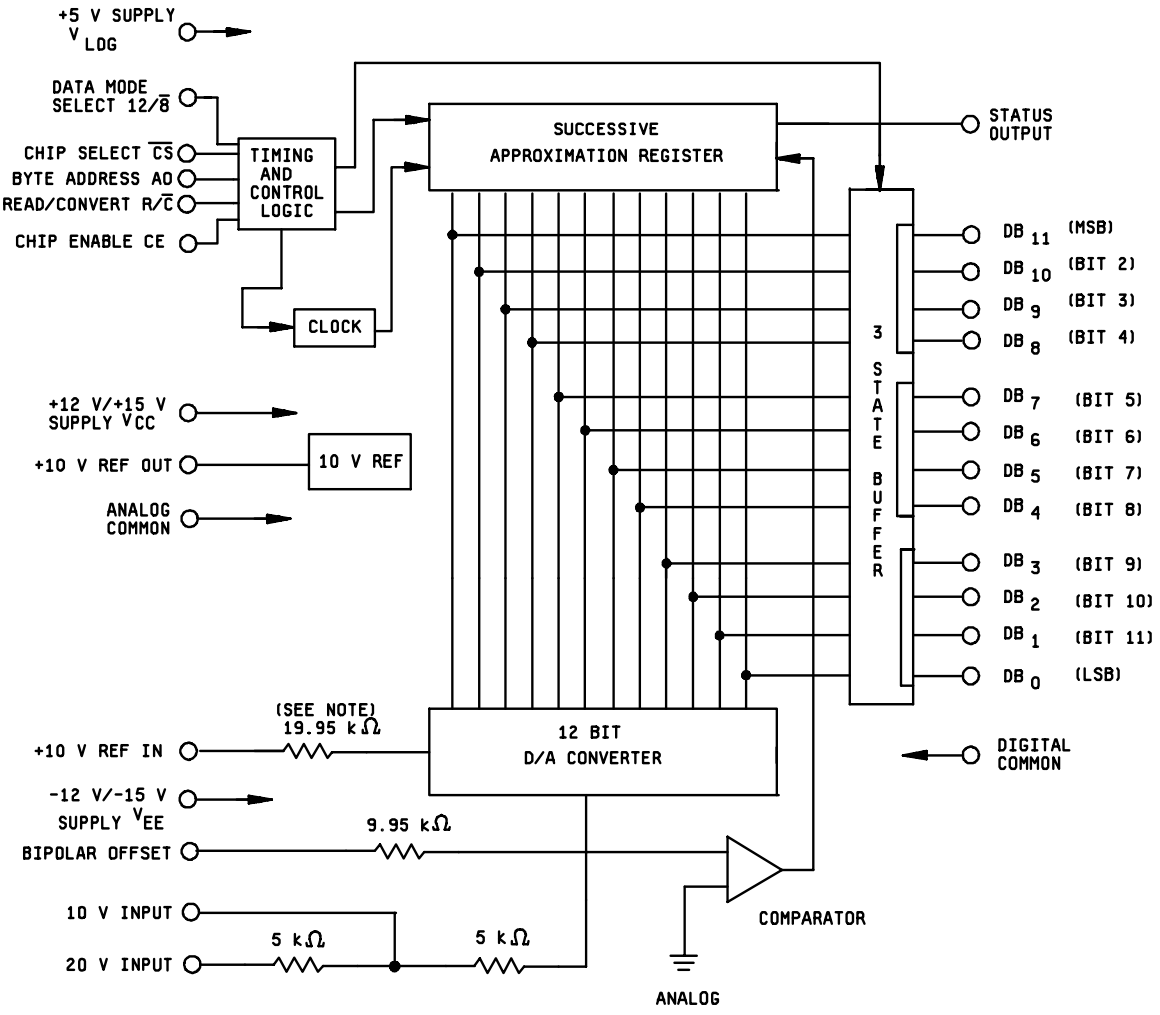
Device types	All	01, 02	01, 02, 05, 06, 07, 08	03, 04
Case outlines	X	Z	3	Y
Terminal number	Terminal symbol			Terminal symbol
1	V_{LOG}			V_{LOG}
2	12/$\overline{8}$			12/$\overline{8}$
3	$\overline{CS}$			$\overline{CS}$
4	AO			AO
5	R/$\overline{C}$			NC
6	CE			NC
7	V_{CC}			NC
8	REF OUT			NC
9	AGND			R/$\overline{C}$
10	REF IN			CE
11	V_{EE}			V_{CC}
12	BIP OFF			REF OUT
13	10 V_{IN}			AGND
14	20 V_{IN}			REF IN
15	DGND			V_{EE}
16	DB0			NC
17	DB1			BIP OFF
18	DB2			10 V_{IN}
19	DB3			20 V_{IN}
20	DB4			NC
21	DB5			NC
22	DB6			NC
23	DB7			NC
24	DB8			DGND
25	DB9			NC
26	DB10			NC
27	DB11 (MSB)			DB0
28	STS			DB1
29				DB2
30				NC
31				DB3
32				DB4
33				DB5
34				DB6
35				DB7
36				DB8
37				DB9
38				NC
39				NC
40				NC
41				NC
42				DB10
43				DB11 (MSB)
44				STS

FIGURE 1. Terminal connections.

CE	$\overline{CS}$	$\overline{R/C}$	$\overline{12/8}$	A_O	Operation
0	X	X	X	X	None
X	1	X	X	X	None
1	0	0	X	0	Initiate 12-bit conversion
1	0	0	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit parallel output
1	0	1	0	0	Enable 8 most significant bits
1	0	1	0	1	Enable 4 LSBs + 4 trailing zeros

FIGURE 2. Truth table.

Device types 01, 02, 03, and 04



NOTE: For device types 03 and 04, the resistor value is 9.95 kΩ.

FIGURE 3. Block diagram.

Device types 05, 06, 07, and 08

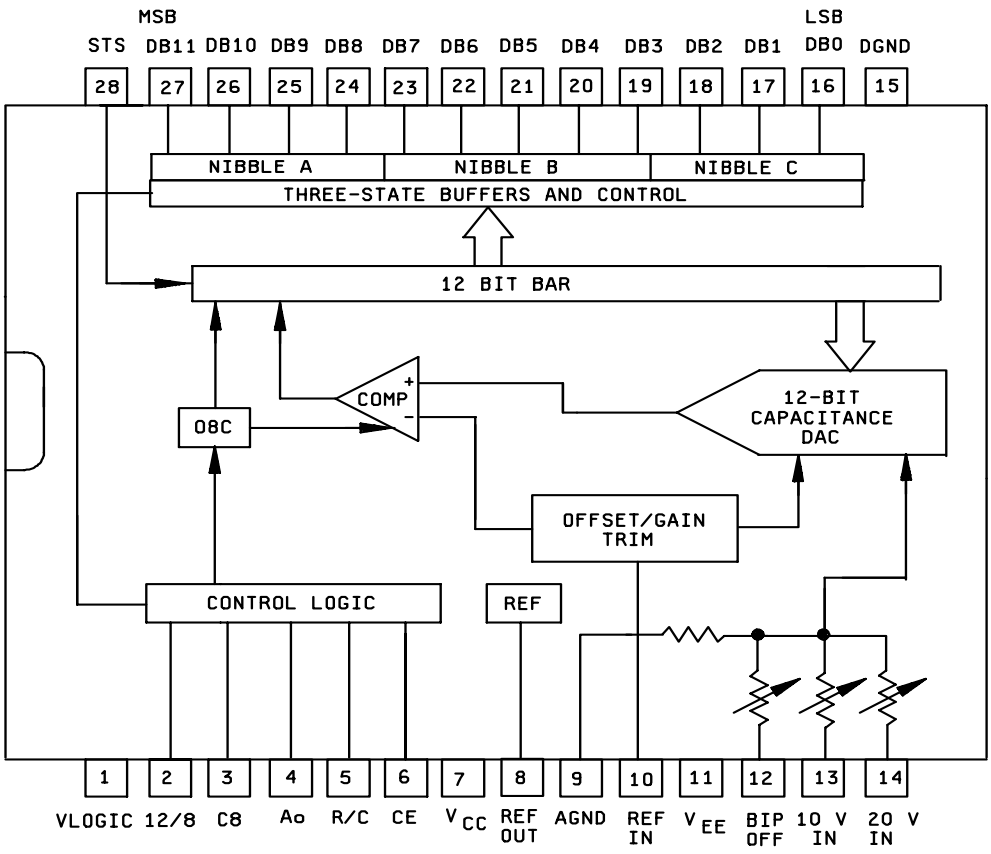
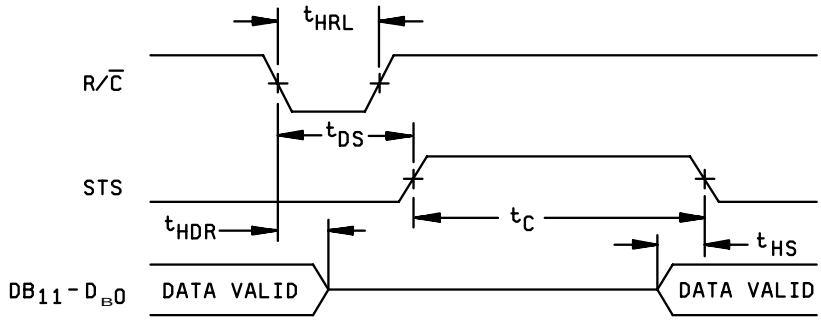
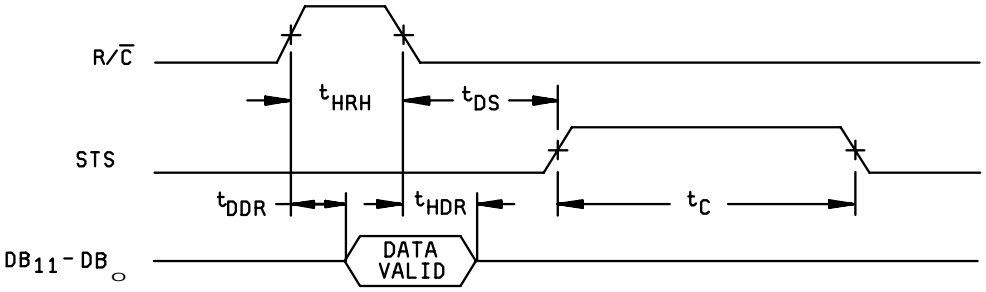


FIGURE 3. Block diagram - continued.



LOW PULSE FOR R/$\overline{C}$ - OUTPUTS ENABLED AFTER CONVERSION



HIGH PULSE FOR R/$\overline{C}$ - OUTPUTS ENABLED WHILE R/$\overline{C}$ HIGH, OTHERWISE HIGH-Z

FIGURE 4. High/low pulse for R/$\overline{C}$ outputs.

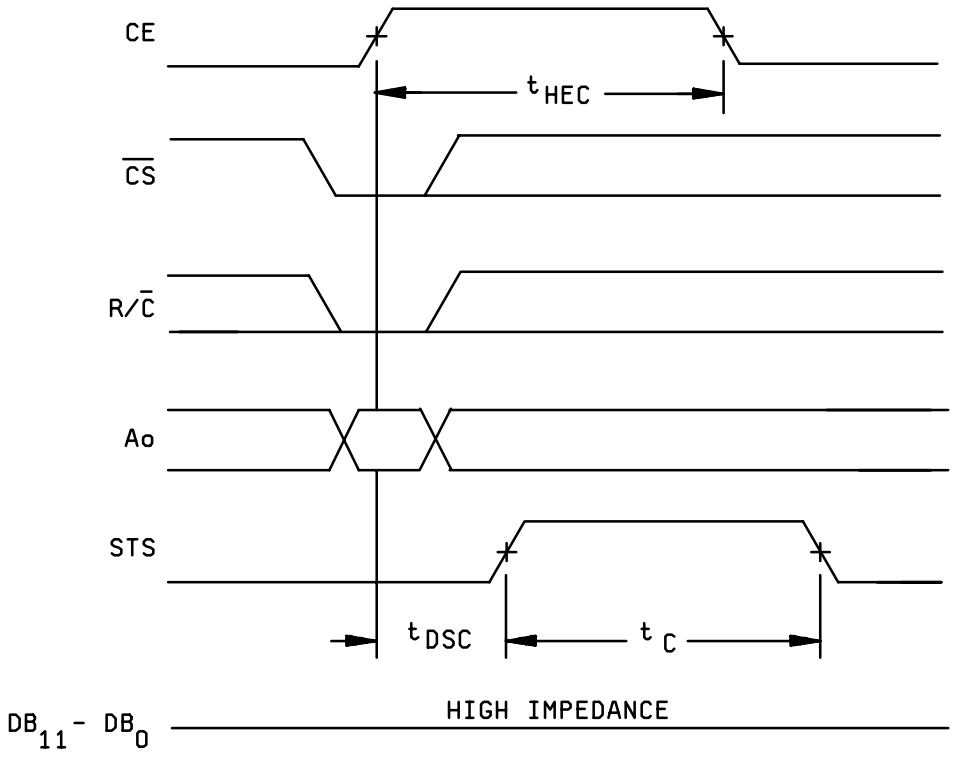


FIGURE 5. Convert start diagram.

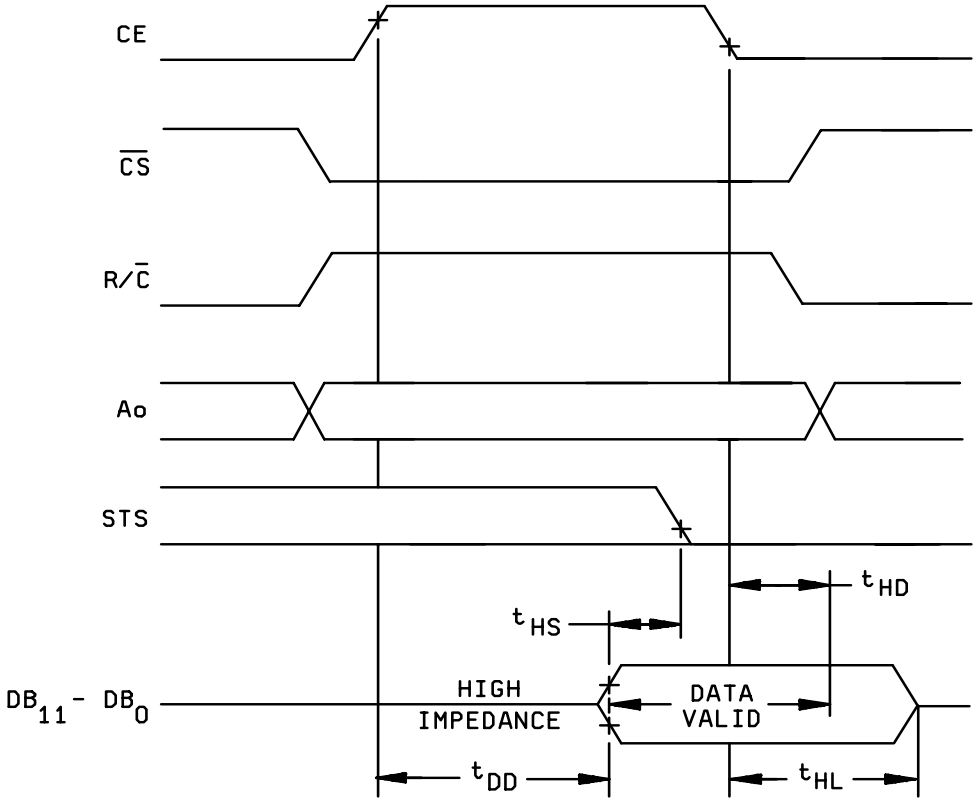


FIGURE 6. Read cycle timing.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Optional subgroup 12, for device 01, is used for grading the part selection at 25°C.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 4, 12	1/ 1, 2, 3, 4, 12	1/, 2/ 1, 2, 3, 4, 12
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 9, 10, 11, 12	1, 2, 3, 4, 7, 9, 10, 11, 12	1, 2, 3, 4, 7, 9, 10, 11, 12
Group C end-point electrical parameters (see 4.4)	1, 4	1, 4	2/ 1, 4
Group D end-point electrical parameters (see 4.4)	1, 4	1, 4	1, 4
Group E end-point electrical parameters (see 4.4)	- - -	- - -	1

1/ PDA applies to subgroup 1.
2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the previous interim electrical parameters.

TABLE IIB. 240 hour burn-in and group C end-point electrical parameters.

Test title	Endpoint limits		Delta limits	Units
	Min	Max		
Uni Vio	-1	2	±0.5	LSB
Bpze	-5.5	4.5	±1	LSB
Ae	-0.35	0.35	±.10	%FSR

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 shall include verifying the functionality of the device.

c. Subgroups 5, 6, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

d. Optional subgroup 12, for device type 01, is used for grading the part selection at 25°C.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

V_{LOG}	Logic supply
$\overline{12/8}$	Data mode select input
CS	Chip select input
$A\overline{0}$	Byte address/short cycle input
R/C	Read/convert input
CE	Chip enable input
V_{CC}	Positive power supply
REF OUT	Reference output
AGND	Analog ground
REF IN	Reference input
V_{EE}	Negative power supply
BIP OFF	Bipolar offset input
V_{IN}	Span input
DGND	Digital ground
D0-D11	Tree-state data outputs
STS	Status output
NC	No connection

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 03-04-25

Approved sources of supply for SMD 5962-85127 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-85127013A	24355	AD574AUE/883B
5962-8512701XA	24355	AD574AUD/883B
5962-8512701XC	1ES66	MX574AUD/883B
5962-8512701VXA	24355	AD574AUD/QMLV
5962-8512701VZA	24355	AD574AUF/QMLV
5962R8512701VXA	24355	AD574AUD/QMLR
5962R8512701VZA	24355	AD574AUF/QMLR
5962-85127023A	24355	AD574ATE/883B
5962-85127023C	1ES66	MX574ATE/883B
5962-8512702XA	24355	AD574ATD/883B
	1ES66	MX574ATQ/883B
5962-8512702XC	1ES66	MX574ATD/883B
5962-8512702VXA	24355	AD574ATD/QMLV
5962-8512702VZA	24355	AD574ATF/QMLV
5962R8512702VXA	24355	AD574ATD/QMLR
5962R8512702VZA	24355	AD574ATF/QMLR
5962-8512703XA	34371	HI1-574AUD/883
5962-8512703YA	3/	HI4-574AUE/883
5962-8512704XA	34371	HI1-574ATD/883
5962-8512704YA	3/	HI4-574ATE/883
5962-85127053A	3/	HADC574ZAMC/883
5962-8512705XC	3/	HADC574ZAMJ/883
5962-85127063A	3/	HADC574ZBMC/883
5962-8512706XC	3/	HADC574ZBMJ/883
5962-85127073C	3/	HS574AU/B-LCC
5962-8512707XC	3/	HS574AU/B
5962-85127083C	3/	HS574AT/B-LCC
5962-8512708XC	3/	HS574AT/B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Incorporated Route 1 Industrial Park PO Box 9106 Norwood, MA 02062-9106 Point of contact: 1500 Space Park Drive PO Box 58020 Santa Clara, CA 95050-8020
1ES66	Maxim Integrated Products 120 San Gabriel Drive Sunnyvale, CA 94086-5126
34371	Intersil Corporation 2401 Palm Bay Blvd PO Box 883 Melbourne, FL 32902-0883

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.

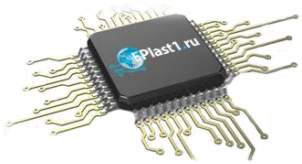
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Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.