

### Features

- 32768x8 bit static CMOS RAM
- Access times 70 ns, 100 ns
- Common data inputs and data outputs
- Three-state outputs
- Typ. operating supply current
  - 70 ns: 50 mA
  - 100 ns: 40 mA
- TTL/CMOS-compatible
- Automatical reduction of power dissipation in long Read Cycles
- Power supply voltage  $5\text{ V} \pm 10\%$
- Operating temperature ranges
  - 0 to 70 °C
  - 40 to 85 °C
  - 40 to 125 °C
- QS 9000 Quality Standard
- ESD protection > 2000 V (MIL STD 883C M3015.7)
- Latch-up immunity >100 mA
- Packages: PDIP28 (600 mil)  
SOP28 (330 mil)

### Description

The U62256A is a static RAM manufactured using a CMOS process technology with the following operating modes:

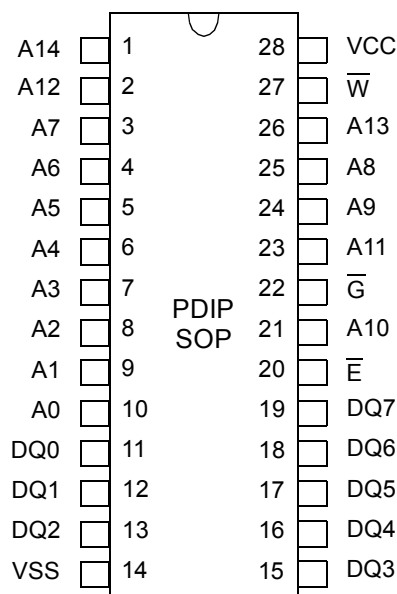
- Read
- Standby
- Write
- Data Retention

The memory array is based on a 6-transistor cell.

The circuit is activated by the falling edge of  $\overline{E}$ . The address and control inputs open simultaneously. According to the information of  $\overline{W}$  and  $\overline{G}$ , the data inputs, or outputs, are active. In a Read cycle, the data outputs are activated by the falling edge of  $\overline{G}$ , afterwards the data word read will be available at the outputs DQ0-DQ7. After the address change, the data outputs go High-Z until the new information read is available. The data outputs have not preferred state. The Read cycle is finished by the

falling edge of  $\overline{W}$ , or by the rising edge of  $\overline{E}$ , respectively. Data retention is guaranteed down to 2 V. With the exception of  $\overline{E}$ , all inputs consist of NOR gates, so that no pull-up/pull-down resistors are required.

### Pin Configuration



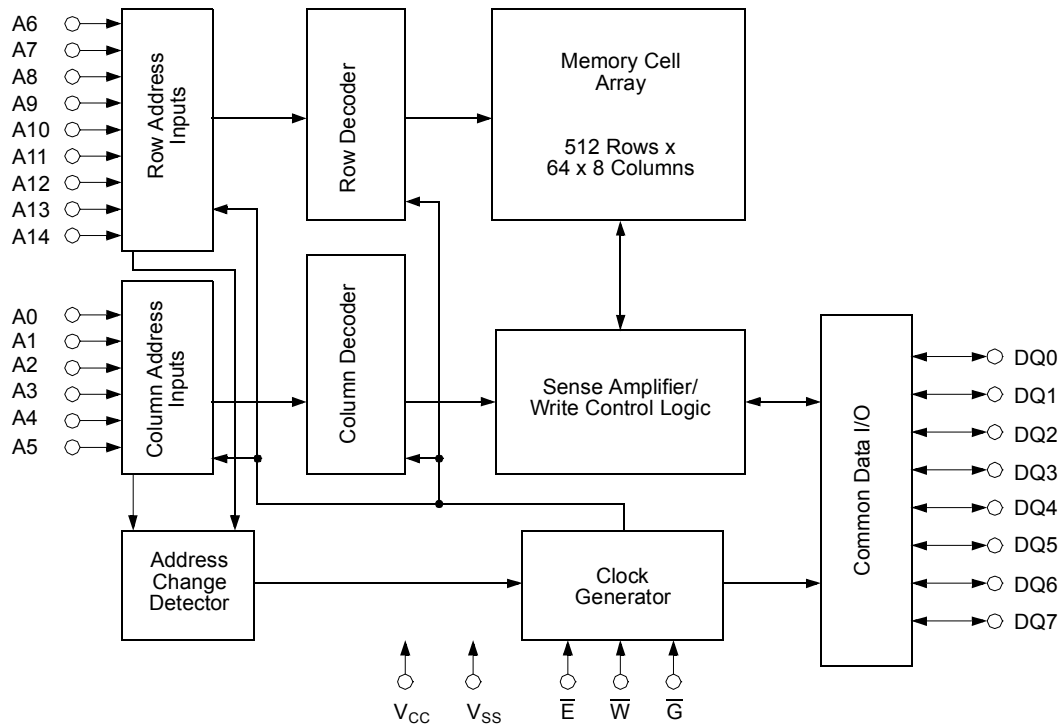
Top View

### Pin Description

Signal Name	Signal Description
A0 - A14	Address Inputs
DQ0 - DQ7	Data In/Out
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
VCC	Power Supply Voltage
VSS	Ground

# U62256A

## Block Diagram



## Truth Table

Operating Mode	$\bar{E}$	$\bar{W}$	$\bar{G}$	DQ0 - DQ7
Standby/not selected	H	*	*	High-Z
Internal Read	L	H	H	High-Z
Read	L	H	L	Data Outputs Low-Z
Write	L	L	*	Data Inputs High-Z

\* H or L

## Characteristics

All voltages are referenced to  $V_{SS} = 0$  V (ground).

All characteristics are valid in the power supply voltage range and in the operating temperature range specified.

Dynamic measurements are based on a rise and fall time of  $\leq 5$  ns, measured between 10 % and 90 % of  $V_i$ , as well as input levels of  $V_{iL} = 0$  V and  $V_{iH} = 3$  V. The timing reference level of all input and output signals is 1.5 V, with the exception of the  $t_{dis}$ -times and  $t_{en}$ -times, in which cases transition is measured  $\pm 200$  mV from steady-state voltage.

Absolute Maximum Ratings <sup>a</sup>		Symbol	Min.	Max.	Unit
Power Supply Voltage		$V_{CC}$	-0.5	7	V
Input Voltage		$V_I$	-0.5	$V_{CC} + 0.5$ <sup>b</sup>	V
Output Voltage		$V_O$	-0.5	$V_{CC} + 0.5$ <sup>b</sup>	V
Power Dissipation		$P_D$	-	1	W
Operating Temperature	C-Type	$T_a$	0	70	°C
	K-Type		-40	85	
	A-Type		-40	125	
Storage Temperature	C/K-Type	$T_{stg}$	-65	125	°C
	A-Type		-65	150	
Output Short-Circuit Current at $V_{CC} = 5$ V and $V_O = 0$ V <sup>c</sup>		$ I_{OS} $		200	mA

<sup>a</sup> Stresses greater than those listed under „Absolute Maximum Ratings“ may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

<sup>b</sup> Maximum voltage is 7 V

<sup>c</sup> Not more than 1 output should be shorted at the same time. Duration of the short circuit should not exceed 30 s.

Recommended Operating Conditions	Symbol	Conditions	Min.	Max.	Unit
Power Supply Voltage	$V_{CC}$		4.5	5.5	V
Input Low Voltage <sup>d</sup>	$V_{iL}$		-0.3	0.8	V
Input High Voltage	$V_{iH}$		2.2	$V_{CC} + 0.3$	V

<sup>d</sup> -2 V at Pulse Width 10 ns

# U62256A

Electrical Characteristics	Symbol	Conditions	Min.	Max.	Unit
Supply Current - Operating Mode	$I_{CC(OP)}$	$V_{CC} = 5.5\text{ V}$ $V_{IL} = 0.8\text{ V}$ $V_{IH} = 2.2\text{ V}$ $t_{cW} = 70\text{ ns}$ $t_{cW} = 100\text{ ns}$		70 65	mA mA
Supply Current - Standby Mode (CMOS level)	$I_{CC(SB)}$	$V_{CC} = 5.5\text{ V}$ $V_{\bar{E}} = V_{CC} - 0.2\text{ V}$ C-Type K-Type A-Type		5 10 50	$\mu\text{A}$ $\mu\text{A}$ $\mu\text{A}$
Supply Current - Standby Mode (TTL level)	$I_{CC(SB)1}$	$V_{CC} = 5.5\text{ V}$ $V_{\bar{E}} = 2.2\text{ V}$		1	mA
Output High Voltage	$V_{OH}$	$V_{CC} = 4.5\text{ V}$ $I_{OH} = -1.0\text{ mA}$	2.4		V
Output Low Voltage	$V_{OL}$	$V_{CC} = 4.5\text{ V}$ $I_{OL} = 3.2\text{ mA}$		0.4	V
Input High Leakage Current	$I_{IH}$	$V_{CC} = 5.5\text{ V}$ $V_{IH} = 5.5\text{ V}$		2	$\mu\text{A}$
Input Low Leakage Current	$I_{IL}$	$V_{CC} = 5.5\text{ V}$ $V_{IL} = 0\text{ V}$	-2		$\mu\text{A}$
Output High Current	$I_{OH}$	$V_{CC} = 4.5\text{ V}$ $V_{OH} = 2.4\text{ V}$		-1	mA
Output Low Current	$I_{OL}$	$V_{CC} = 4.5\text{ V}$ $V_{OL} = 0.4\text{ V}$	3,2		mA
Output Leakage Current High at Three-State Outputs	$I_{OHZ}$	$V_{CC} = 5.5\text{ V}$ $V_{OH} = 5.5\text{ V}$		1	$\mu\text{A}$
Low at Three-State Outputs	$I_{OLZ}$	$V_{CC} = 5.5\text{ V}$ $V_{OL} = 0\text{ V}$	-1		$\mu\text{A}$

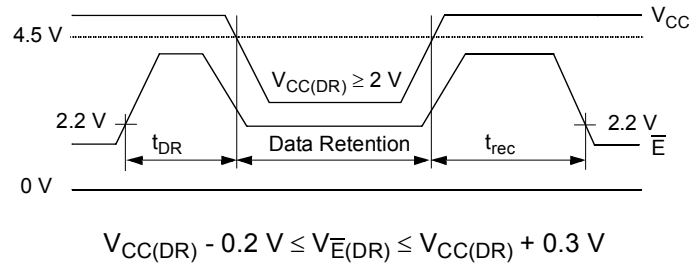
Switching Characteristics Read Cycle	Symbol		07		10		Unit
	Alt.	IEC	Min.	Max.	Min.	Max.	
Read Cycle Time	$t_{RC}$	$t_{cR}$	70		100		ns
Address Access Time to Data Valid	$t_{AA}$	$t_{a(A)}$		70		100	ns
Chip Enable Access Time to Data Valid	$t_{ACE}$	$t_{a(E)}$		70		100	ns
Output Enable Access Time to Data Valid	$t_{OE}$	$t_{a(G)}$		35		45	ns
$\bar{E}$ HIGH to Output in High-Z	$t_{HZCE}$	$t_{dis(E)}$		25		35	ns
$\bar{G}$ HIGH to Output in High-Z	$t_{HZOE}$	$t_{dis(G)}$		25		35	ns
$\bar{E}$ LOW to Output in Low-Z	$t_{LZCE}$	$t_{en(E)}$	5		5		ns
$\bar{G}$ LOW to Output in Low-Z	$t_{LZOE}$	$t_{en(G)}$	0		0		ns
Output Hold Time from Address Change	$t_{OH}$	$t_{v(A)}$	5		5		ns

Switching Characteristics Write Cycle	Symbol		07		10		Unit
	Alt.	IEC	Min.	Max.	Min.	Max.	
Write Cycle Time	$t_{WC}$	$t_{cW}$	70		100		ns
Write Pulse Width	$t_{WP}$	$t_{w(W)}$	55		70		ns
Write Pulse Width Setup Time	$t_{WP}$	$t_{su(W)}$	55		70		ns
Address Setup Time	$t_{AS}$	$t_{su(A)}$	0		0		ns
Address Valid to End of Write	$t_{AW}$	$t_{su(A-WH)}$	65		80		ns
Chip Enable Setup Time	$t_{CW}$	$t_{su(E)}$	65		80		ns
Pulse Width Chip Enable to End of Write	$t_{CW}$	$t_{w(E)}$	65		80		ns
Data Setup Time	$t_{DS}$	$t_{su(D)}$	30		35		ns
Data Hold Time	$t_{DH}$	$t_{h(D)}$	0		0		ns
Address Hold from End of Write	$t_{AH}$	$t_{h(A)}$	0		0		ns
$\bar{W}$ LOW to Output in High-Z	$t_{HZWE}$	$t_{dis(W)}$		25		35	ns
$\bar{G}$ HIGH to Output in High-Z	$t_{HZOE}$	$t_{dis(G)}$		25		35	ns
$\bar{W}$ HIGH to Output in Low-Z	$t_{LZWE}$	$t_{en(W)}$	0		0		ns
$\bar{G}$ LOW to Output in Low-Z	$t_{LZOE}$	$t_{en(G)}$	0		0		ns

# U62256A

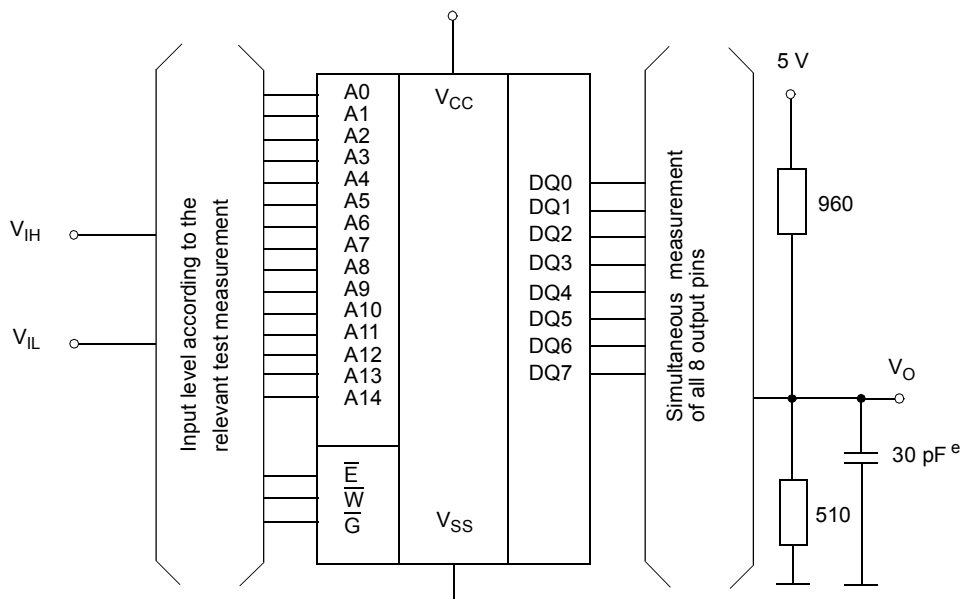
## Data Retention Mode

### $\bar{E}$ -Controlled



Data Retention Characteristics	Symbol Alt. IEC	Conditions	Min.	Typ.	Max.	Unit
Data Retention Supply Voltage	$V_{CC(DR)}$		2		5.5	V
Data Retention Supply Current	$I_{CC(DR)}$	$V_{CC(DR)} = 3 V$ $V_{\bar{E}} = V_{CC(DR)} - 0.2 V$ C-Type K-Type A-Type			3 6 30	$\mu A$ $\mu A$ $\mu A$
Data Retention Setup Time	$t_{CDR}$	$t_{su(DR)}$	0			ns
Operating Recovery Time	$t_R$	$t_{rec}$	$t_{cR}$			ns

### Test Configuration for Functional Check



<sup>e</sup> In measurement of  $t_{dis(E)}$ ,  $t_{dis(W)}$ ,  $t_{dis(G)}$ ,  $t_{en(E)}$ ,  $t_{en(W)}$ ,  $t_{en(G)}$  the capacitance is 5 pF.

Capacitance	Conditions	Symbol	Min.	Max.	Unit
Input Capacitance	$V_{CC} = 5.0\text{ V}$ $V_I = V_{SS}$	$C_I$	-	7	pF
Output Capacitance	$f = 1\text{ MHz}$ $T_a = 25\text{ °C}$	$C_O$	-	7	pF

All pins not under test must be connected with ground by capacitors.

## Ordering Code

Example

**U62256A S2 K 07 LL**

Type

Package

D = PDIP28 (600 mil, only C/K-Type and 70 ns)  
S2 = SOP28 (330 mil) Type 2

Operating Temperature Range

C = 0 to 70 °C  
K = -40 to 85 °C  
A = -40 to 125 °C

Access Time

07 = 70 ns  
10 = 100 ns (only C/K-Type)

Leadfree Option

blank = Standard Package

G1 = Leadfree Green Package <sup>f</sup>

Power Consumption

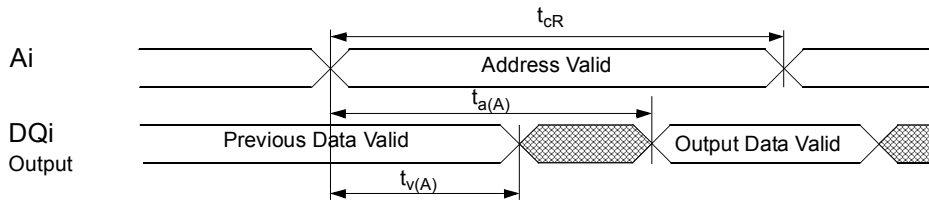
blank = Standard (only A-Type)

LL = Very Low Power (C/K-Type)

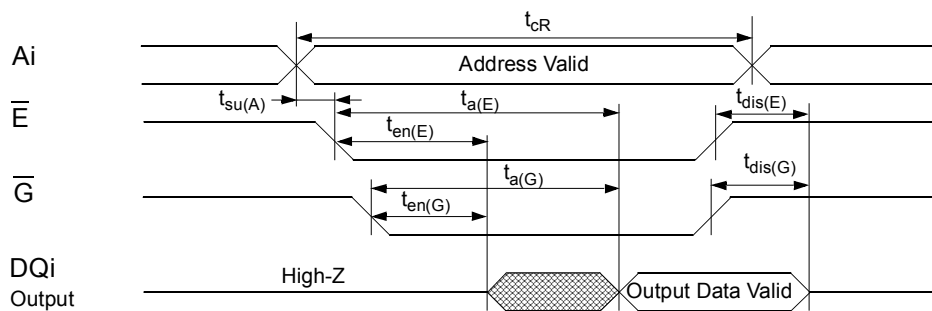
<sup>f</sup> on special request

# U62256A

Read Cycle 1: Ai-controlled (during Read Cycle :  $\bar{E} = \bar{G} = V_{IL}, \bar{W} = V_{IH}$ )

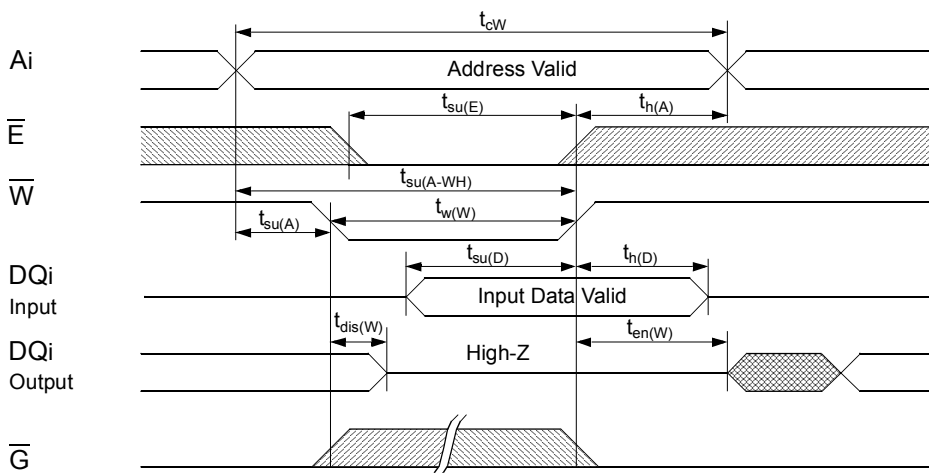


Read Cycle 2:  $\bar{G}$ -,  $\bar{E}$ -controlled (during Read Cycle:  $\bar{W} = V_{IH}$ )

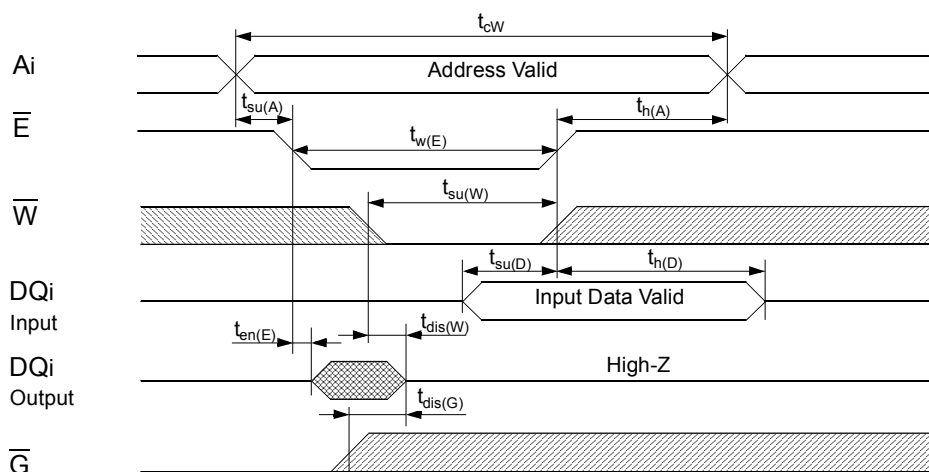




Write Cycle1:  $\overline{W}$ -controlled



Write Cycle 2:  $\overline{E}$ -controlled



undefined  L- to H-level  H- to L-level 

The information describes the type of component and shall not be considered as assured characteristics. Terms of delivery and rights to change design reserved.

## **LIFE SUPPORT POLICY**

ZMD products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the ZMD product could create a situation where personal injury or death may occur.

Components used in life-support devices or systems must be expressly authorized by ZMD for such purpose.

## **LIMITED WARRANTY**

The information in this document has been carefully checked and is believed to be reliable. However Zentrum Mikroelektronik Dresden AG (ZMD) makes no guarantee or warranty concerning the accuracy of said information and shall not be responsible for any loss or damage of whatever nature resulting from the use of, or reliance upon it. The information in this document describes the type of component and shall not be considered as assured characteristics.

ZMD does not guarantee that the use of any information contained herein will not infringe upon the patent, trademark, copyright, mask work right or other rights of third parties, and no patent or licence is implied hereby. This document does not in any way extend ZMD's warranty on any product beyond that set forth in its standard terms and conditions of sale.

ZMD reserves terms of delivery and reserves the right to make changes in the products or specifications, or both, presented in this publication at any time and without notice.



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



#### Как с нами связаться

**Телефон:** 8 (812) 309 58 32 (многоканальный)

**Факс:** 8 (812) 320-02-42

**Электронная почта:** [org@eplast1.ru](mailto:org@eplast1.ru)

**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.