

Features

- 32768x8 bit static CMOS RAM
- Access times 70 ns, 100 ns
- Common data inputs and data outputs
- Three-state outputs
- Typ. operating supply current
 - 70 ns: 50 mA
 - 100 ns: 40 mA
- TTL/CMOS-compatible
- Automatical reduction of power dissipation in long Read Cycles
- Power supply voltage $5\text{ V} \pm 10\%$
- Operating temperature ranges
 - 0 to 70 °C
 - 40 to 85 °C
 - 40 to 125 °C
- QS 9000 Quality Standard
- ESD protection > 2000 V (MIL STD 883C M3015.7)
- Latch-up immunity >100 mA
- Packages: PDIP28 (600 mil)
SOP28 (330 mil)

Description

The U62256A is a static RAM manufactured using a CMOS process technology with the following operating modes:

- Read
- Standby
- Write
- Data Retention

The memory array is based on a 6-transistor cell.

The circuit is activated by the falling edge of \bar{E} . The address and control inputs open simultaneously. According to the information of \bar{W} and \bar{G} , the data inputs, or outputs, are active. In a Read cycle, the data outputs are activated by the falling edge of \bar{G} , afterwards the data word read will be available at the outputs DQ0-DQ7. After the address change, the data outputs go High-Z until the new information read is available. The data outputs have not preferred state. The Read cycle is finished by the

falling edge of \bar{W} , or by the rising edge of \bar{E} , respectively. Data retention is guaranteed down to 2 V. With the exception of \bar{E} , all inputs consist of NOR gates, so that no pull-up/pull-down resistors are required.

Pin Configuration



Top View

Pin Description

| Signal Name | Signal Description |
|-------------|----------------------|
| A0 - A14 | Address Inputs |
| DQ0 - DQ7 | Data In/Out |
| \bar{E} | Chip Enable |
| \bar{G} | Output Enable |
| \bar{W} | Write Enable |
| VCC | Power Supply Voltage |
| VSS | Ground |

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Block Diagram



Truth Table

| Operating Mode | \bar{E} | \bar{W} | \bar{G} | DQ0 - DQ7 |
|----------------------|-----------|-----------|-----------|--------------------|
| Standby/not selected | H | * | * | High-Z |
| Internal Read | L | H | H | High-Z |
| Read | L | H | L | Data Outputs Low-Z |
| Write | L | L | * | Data Inputs High-Z |

* H or L

Characteristics

All voltages are referenced to $V_{SS} = 0\text{ V}$ (ground).

All characteristics are valid in the power supply voltage range and in the operating temperature range specified.

Dynamic measurements are based on a rise and fall time of $\leq 5\text{ ns}$, measured between 10 % and 90 % of V_i , as well as input levels of $V_{iL} = 0\text{ V}$ and $V_{iH} = 3\text{ V}$. The timing reference level of all input and output signals is 1.5 V, with the exception of the t_{dis} -times and t_{en} -times, in which cases transition is measured $\pm 200\text{ mV}$ from steady-state voltage.

| Absolute Maximum Ratings ^a | | Symbol | Min. | Max. | Unit |
|---|----------|------------|------|-----------------------------|------|
| Power Supply Voltage | | V_{CC} | -0.5 | 7 | V |
| Input Voltage | | V_I | -0.5 | $V_{CC} + 0.5$ ^b | V |
| Output Voltage | | V_O | -0.5 | $V_{CC} + 0.5$ ^b | V |
| Power Dissipation | | P_D | - | 1 | W |
| Operating Temperature | C-Type | T_a | 0 | 70 | °C |
| | K-Type | | -40 | 85 | |
| | A-Type | | -40 | 125 | |
| Storage Temperature | C/K-Type | T_{stg} | -65 | 125 | °C |
| | A-Type | | -65 | 150 | |
| Output Short-Circuit Current at $V_{CC} = 5\text{ V}$ and $V_O = 0\text{ V}$ ^c | | $ I_{OS} $ | | 200 | mA |

^a Stresses greater than those listed under „Absolute Maximum Ratings“ may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

^b Maximum voltage is 7 V

^c Not more than 1 output should be shorted at the same time. Duration of the short circuit should not exceed 30 s.

| Recommended Operating Conditions | Symbol | Conditions | Min. | Max. | Unit |
|----------------------------------|----------|------------|------|----------------|------|
| Power Supply Voltage | V_{CC} | | 4.5 | 5.5 | V |
| Input Low Voltage ^d | V_{iL} | | -0.3 | 0.8 | V |
| Input High Voltage | V_{iH} | | 2.2 | $V_{CC} + 0.3$ | V |

^d -2 V at Pulse Width 10 ns

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| Electrical Characteristics | Symbol | Conditions | Min. | Max. | Unit |
|---|---------------|--|------|---------------|---|
| Supply Current - Operating Mode | $I_{CC(OP)}$ | $V_{CC} = 5.5\text{ V}$ $V_{IL} = 0.8\text{ V}$ $V_{IH} = 2.2\text{ V}$ $t_{cW} = 70\text{ ns}$ $t_{cW} = 100\text{ ns}$ | | 70 65 | mA mA |
| Supply Current - Standby Mode (CMOS level) | $I_{CC(SB)}$ | $V_{CC} = 5.5\text{ V}$ $V_{\bar{E}} = V_{CC} - 0.2\text{ V}$ C-Type K-Type A-Type | | 5 10 50 | μA μA μA |
| Supply Current - Standby Mode (TTL level) | $I_{CC(SB)1}$ | $V_{CC} = 5.5\text{ V}$ $V_{\bar{E}} = 2.2\text{ V}$ | | 1 | mA |
| Output High Voltage | V_{OH} | $V_{CC} = 4.5\text{ V}$ $I_{OH} = -1.0\text{ mA}$ | 2.4 | | V |
| Output Low Voltage | V_{OL} | $V_{CC} = 4.5\text{ V}$ $I_{OL} = 3.2\text{ mA}$ | | 0.4 | V |
| Input High Leakage Current | I_{IH} | $V_{CC} = 5.5\text{ V}$ $V_{IH} = 5.5\text{ V}$ | | 2 | μA |
| Input Low Leakage Current | I_{IL} | $V_{CC} = 5.5\text{ V}$ $V_{IL} = 0\text{ V}$ | -2 | | μA |
| Output High Current | I_{OH} | $V_{CC} = 4.5\text{ V}$ $V_{OH} = 2.4\text{ V}$ | | -1 | mA |
| Output Low Current | I_{OL} | $V_{CC} = 4.5\text{ V}$ $V_{OL} = 0.4\text{ V}$ | 3,2 | | mA |
| Output Leakage Current High at Three-State Outputs | I_{OHZ} | $V_{CC} = 5.5\text{ V}$ $V_{OH} = 5.5\text{ V}$ | | 1 | μA |
| Low at Three-State Outputs | I_{OLZ} | $V_{CC} = 5.5\text{ V}$ $V_{OL} = 0\text{ V}$ | -1 | | μA |

| Switching Characteristics Read Cycle | Symbol | | 07 | | 10 | | Unit |
|---|------------|--------------|------|------|------|------|------|
| | Alt. | IEC | Min. | Max. | Min. | Max. | |
| Read Cycle Time | t_{RC} | t_{cR} | 70 | | 100 | | ns |
| Address Access Time to Data Valid | t_{AA} | $t_{a(A)}$ | | 70 | | 100 | ns |
| Chip Enable Access Time to Data Valid | t_{ACE} | $t_{a(E)}$ | | 70 | | 100 | ns |
| Output Enable Access Time to Data Valid | t_{OE} | $t_{a(G)}$ | | 35 | | 45 | ns |
| \bar{E} HIGH to Output in High-Z | t_{HZCE} | $t_{dis(E)}$ | | 25 | | 35 | ns |
| \bar{G} HIGH to Output in High-Z | t_{HZOE} | $t_{dis(G)}$ | | 25 | | 35 | ns |
| \bar{E} LOW to Output in Low-Z | t_{LZCE} | $t_{en(E)}$ | 5 | | 5 | | ns |
| \bar{G} LOW to Output in Low-Z | t_{LZOE} | $t_{en(G)}$ | 0 | | 0 | | ns |
| Output Hold Time from Address Change | t_{OH} | $t_{v(A)}$ | 5 | | 5 | | ns |

| Switching Characteristics Write Cycle | Symbol | | 07 | | 10 | | Unit |
|--|------------|----------------|------|------|------|------|------|
| | Alt. | IEC | Min. | Max. | Min. | Max. | |
| Write Cycle Time | t_{WC} | t_{cW} | 70 | | 100 | | ns |
| Write Pulse Width | t_{WP} | $t_{w(W)}$ | 55 | | 70 | | ns |
| Write Pulse Width Setup Time | t_{WP} | $t_{su(W)}$ | 55 | | 70 | | ns |
| Address Setup Time | t_{AS} | $t_{su(A)}$ | 0 | | 0 | | ns |
| Address Valid to End of Write | t_{AW} | $t_{su(A-WH)}$ | 65 | | 80 | | ns |
| Chip Enable Setup Time | t_{CW} | $t_{su(E)}$ | 65 | | 80 | | ns |
| Pulse Width Chip Enable to End of Write | t_{CW} | $t_{w(E)}$ | 65 | | 80 | | ns |
| Data Setup Time | t_{DS} | $t_{su(D)}$ | 30 | | 35 | | ns |
| Data Hold Time | t_{DH} | $t_{h(D)}$ | 0 | | 0 | | ns |
| Address Hold from End of Write | t_{AH} | $t_{h(A)}$ | 0 | | 0 | | ns |
| \bar{W} LOW to Output in High-Z | t_{HZWE} | $t_{dis(W)}$ | | 25 | | 35 | ns |
| \bar{G} HIGH to Output in High-Z | t_{HZOE} | $t_{dis(G)}$ | | 25 | | 35 | ns |
| \bar{W} HIGH to Output in Low-Z | t_{LZWE} | $t_{en(W)}$ | 0 | | 0 | | ns |
| \bar{G} LOW to Output in Low-Z | t_{LZOE} | $t_{en(G)}$ | 0 | | 0 | | ns |

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Data Retention Mode

\bar{E} -Controlled



$$V_{CC(DR)} - 0.2 \text{ V} \leq V_{\bar{E}(DR)} \leq V_{CC(DR)} + 0.3 \text{ V}$$

| Data Retention Characteristics | Symbol Alt. IEC | Conditions | Min. | Typ. | Max. | Unit |
|--------------------------------|--------------------|--|----------|------|--------------|---|
| Data Retention Supply Voltage | $V_{CC(DR)}$ | | 2 | | 5.5 | V |
| Data Retention Supply Current | $I_{CC(DR)}$ | $V_{CC(DR)} = 3 \text{ V}$ $V_{\bar{E}} = V_{CC(DR)} - 0.2 \text{ V}$ C-Type K-Type A-Type | | | 3 6 30 | μA μA μA |
| Data Retention Setup Time | t_{CDR} | $t_{su(DR)}$ | 0 | | | ns |
| Operating Recovery Time | t_R | t_{rec} | t_{cR} | | | ns |

Test Configuration for Functional Check



^e In measurement of $t_{dis(E)}$, $t_{dis(W)}$, $t_{dis(G)}$, $t_{en(E)}$, $t_{en(W)}$, $t_{en(G)}$ the capacitance is 5 pF.

| Capacitance | Conditions | Symbol | Min. | Max. | Unit |
|--------------------|--|--------|------|------|------|
| Input Capacitance | $V_{CC} = 5.0\text{ V}$ $V_I = V_{SS}$ | C_I | - | 7 | pF |
| Output Capacitance | $f = 1\text{ MHz}$ $T_a = 25\text{ °C}$ | C_O | - | 7 | pF |

All pins not under test must be connected with ground by capacitors.

Ordering Code

Example

U62256A S2 K 07 LL

Type

Package

D = PDIP28 (600 mil, only C/K-Type and 70 ns)
S2 = SOP28 (330 mil) Type 2

Operating Temperature Range

C = 0 to 70 °C
K = -40 to 85 °C
A = -40 to 125 °C

Access Time

07 = 70 ns
10 = 100 ns (only C/K-Type)

Leadfree Option

blank = Standard Package

G1 = Leadfree Green Package ^f

Power Consumption

blank = Standard (only A-Type)

LL = Very Low Power (C/K-Type)

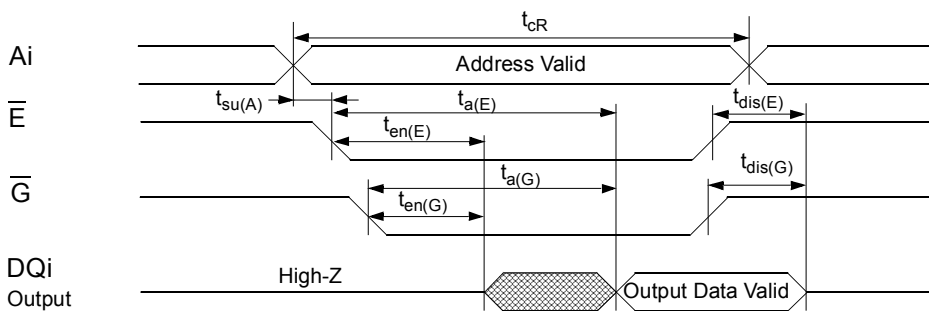
^f on special request

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Read Cycle 1: Ai-controlled (during Read Cycle : $\bar{E} = \bar{G} = V_{IL}, \bar{W} = V_{IH}$)



Read Cycle 2: \bar{G} -, \bar{E} -controlled (during Read Cycle: $\bar{W} = V_{IH}$)



Write Cycle1: \overline{W} -controlled



Write Cycle 2: \overline{E} -controlled



undefined  L- to H-level  H- to L-level 

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