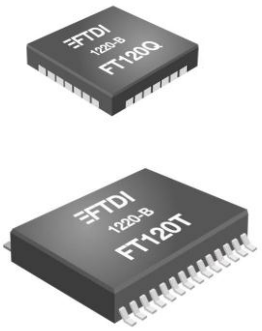
Future Technology Devices International Ltd.

FT120

(USB Device Controller with Parallel Bus IC)



The FT120 is a USB controller developed independently with close consideration of the industry classic, D12 chip. It communicates with a microcontroller over the generic parallel interface. The FT120 has the following advanced features:

- USB 2.0 Full Speed compatible.
- High performance USB device controller with integrated SIE, endpoint buffer, transceiver and voltage regulators.
- Supports 8-bit parallel interface to external microcontroller.
- Supports DMA operation
- Integrated 320 bytes of configurable endpoint buffer
- Ping-pong buffer scheme for primary endpoint increases data transfer throughput
- Multiple interrupt modes to facilitate both bulk and isochronous transfers.
- Dedicated clock output pin with programmable clock frequency (4 – 24 MHz)
- 30 kHz output clock provided during suspend.
- Integrated D+ pull-up resistor for USB connection
- USB connection indicator that toggles with USB transmit and receive activities.
- Supports bus powered or self powered application.
- Single power supply operation at 3.3V or 5V.
- Internal 1.8V and 3.3V LDO regulators
- Integrated power-on-reset circuit.
- UHCI/OHCI/EHCI host controller compatible.
- -40°C to 85°C extended operating temperature range.
- Available in Pb-free TSSOP-28 and QFN-28 packages (RoHS compliant).

1 Typical Applications

- Provide USB port to Microcontrollers
- USB Industrial Control
- Mass storage data transfers for multitude of embedded systems applications, including medical, industrial data-logger, power-metering, and test instrumentation
- Provide USB port to FPGA's
- Utilising USB to add system modularity
- Isochronous support for video applications in security, industrial control, and quality inspections

1.1 Part Numbers

Part Number	Package
FT120T-x	TSSOP-28
FT120Q-x	QFN-28

Note: Packaging codes for x is:

- R: Taped and Reel, (TSSOP is 2,500pcs per reel, QFN is 6,000pcs per reel).
- U: Tube packing, 50pcs per tube (TSSOP only)
- T: Tray packing, 490pcs per tray (QFN only)

For example: FT120T-R is 2,500pcs taped and reel packing

1.2 USB Compliant

At the time of writing this datasheet, the FT120 was in the process of completing USB compliance testing.

2 Block Diagrams

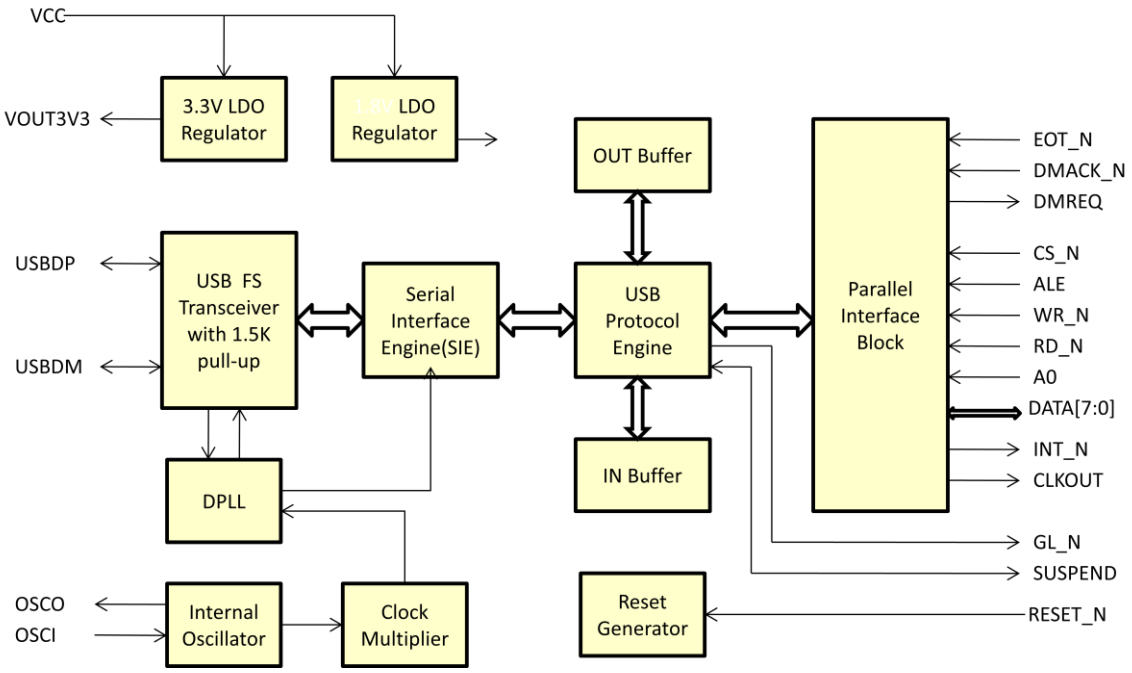


Figure 2-1 FT120 Block Diagram

For a description of each function please refer to Section 4.

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3 Device Pin Out and Signal Description

3.1 TSSOP-28 Package Pin Out

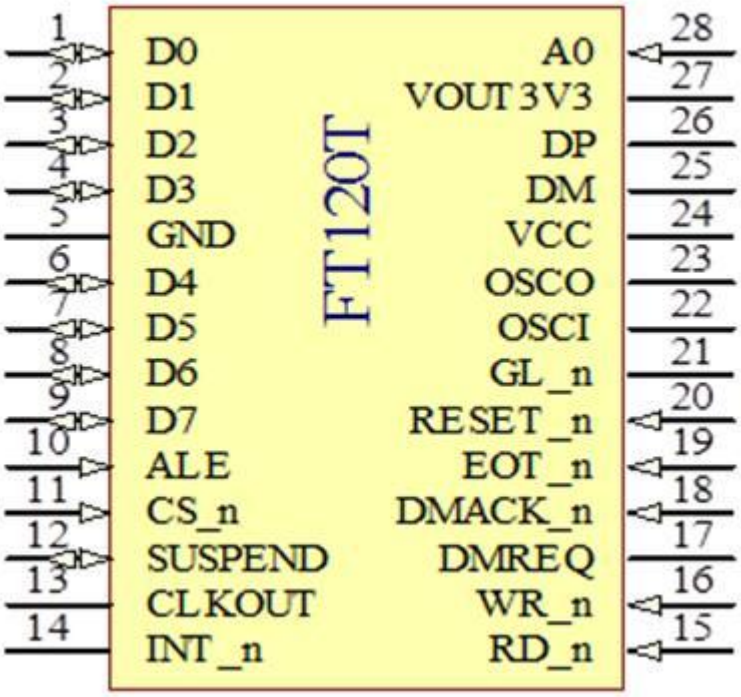


Figure 3-1 TSSOP-28 package schematic symbol

3.2 QFN-28 Package Pin Out

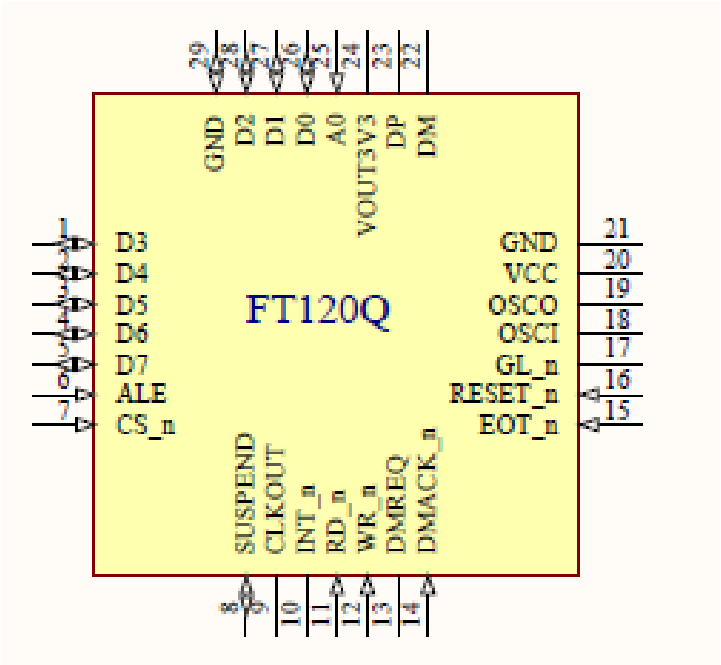


Figure 3-2 QFN-28 package schematic symbol

3.3 Pin Description

PIN No. (TSSOP-28)	PIN No. (QFN-28)	PIN NAME	TYPE	DESCRIPTION
1	26	DATA0	IO	Data bus bit 0.
2	27	DATA1	IO	Data bus bit 1.
3	28	DATA2	IO	Data bus bit 2.
4	1	DATA3	IO	Data bus bit 3.
5	21	GND	P	Ground.
6	2	DATA4	IO	Data bus bit 4.
7	3	DATA5	IO	Data bus bit 5.
8	4	DATA6	IO	Data bus bit 6.
9	5	DATA7	IO	Data bus bit 7.
10	6	ALE	I	Address latch enable for multiplexed address/data bus configuration. This pin must be pulled Low for non-multiplexed address/data bus configuration.
11	7	CS_n	I	Chip select (Active Low).
12	8	SUSPEND	I,OD	Device suspend (output) and wakeup (input).
13	9	CLKOUT	O	Programmable output clock.
14	10	INT_n	OD	Interrupt (Active Low).
15	11	RD_n	I	Read enable (Active Low).
16	12	WR_n	I	Write enable (Active Low).
17	13	DMREQ	O	DMA request.
18	14	DMACK_n	I	DMA acknowledge (Active Low).
19	15	EOT_n	I	End of DMA transfer (Active Low). Also function as Vbus sensing input for self-powered application. _n_n_n_n
20	16	RESET_n	I	Asynchronous reset (Active Low).
21	17	GL_n	OD	USB bus activity indicator (Active Low)
22	18	OSCI	I	Crystal connection input (6MHz); alternatively, a 1.8V square wave clock can be applied.
23	19	OSCO	O	Crystal connection output (6MHz) ; if the external clock signal is connected to OSCI, then OSCO

PIN No. (TSSOP-28)	PIN No. (QFN-28)	PIN NAME	TYPE	DESCRIPTION
				should be left unconnected
24	20	VCC	P	Power supply (3.3V or 5V)
25	22	USBDM	AIO	USB data signal minus
26	23	USBDP	AIO	USB data signal plus
27	24	VOUT3V3	P	3.3V regulator output for 5V operation; To operate the IC at 3.3 V, supply 3.3 V to both the VCC and VOUT3V3 pins
28	25	A0	I	Address bit for non-multiplexed address/data bus configuration. - A0=1 indicates command phase; - A0=0 indicates data phase. This pin must be pulled High for multiplexed address/data bus configuration.
-	29	GND	P	Ground. Die pad for QFN-28 package.

Table 3-1 FT120 Pin Description

Note, symbol used for pin TYPE:

OD : Open Drain Output

O : Output

IO : Bi-directional Input and Output

I : Plain input

AIO : Analog Input and Output

P : Power or ground

4 Function Description

The FT120 is a USB device controller which interfaces with microcontrollers via a generic 8-bit parallel bus.

4.1 Functional Block Descriptions

The following sections describe the function of each block. Please refer to the block diagram shown in **Figure 2-1**.

+1.8V LDO Regulator. The +1.8V LDO regulator generates the +1.8V reference voltage for the internal core of the IC with input capabilities from 3.3V or 5V.

+3.3V LDO Regulator. The +3.3V LDO regulator generates the +3.3V supply voltage for the USB transceiver. An external decoupling capacitor needs to be attached to the VOUT3V3 regulator output pin. The regulator also provides +3.3V power to the 1.5kΩ internal pull up resistor on USBDP pin. The allowable input voltages are 5V or 3.3V. When using 3.3V voltage as input voltage, the VCC and VOUT3V3 pins should be tied together. This will result in the regulator being by-passed.

USB Transceiver. The USB Transceiver cell provides the USB 1.1 / USB 2.0 full-speed physical interface. Output drivers provide +3.3V level slew rate control , while a differential input and two single ended input receivers provide data in, Single-Ended-0 (SE0) and USB reset detection conditions respectfully. A 1.5kΩ pull up resistor on USBDP is incorporated.

DPLL. The DPLL cell locks on to the incoming NRZI USB data and generates recovered clock and data signals..

Internal Oscillator. The Internal Oscillator cell generates a 6MHz reference clock from the 6MHz crystal. The Oscillator also has the capability of running from an external clock applied on the OSCI pin. This provides an input to the Clock Multiplier function.

Clock Multiplier. The 12MHz and 48MHz reference clock signals for various internal blocks can be generated from the 6 MHz via the oscillator functions and clock multiplier circuitry.

Serial Interface Engine (SIE). The Serial Interface Engine (SIE) block performs the parallel to serial and serial to parallel conversion of the USB data. In accordance with the USB 2.0 specification, it performs bit stuffing/un-stuffing and CRC5/CRC16 generation. It also checks the CRC on the USB data stream.

USB Protocol Engine. The USB Protocol Engine manages the data stream from the device USB control endpoint. It handles the low level USB protocol requests generated by the USB host controller. The Protocol Engine also includes a memory management unit which handles endpoint buffers.

OUT Buffer. Data sent from the USB host controller to FT120 via the USB data OUT endpoint is stored in the OUT buffer. Data is removed from the OUT buffer to system memory under control of the parallel interface block.

IN Buffer. Data from system memory is stored in the IN buffer. The USB host controller removes data from the IN buffer by sending a USB request for data from the device data IN endpoint.

RESET Generator. The integrated Reset Generator cell provides a reliable power-on reset to the device internal circuitry at power up. The RESET_n input pin allows an external device to reset the FT120.

Parallel Interface Block. The 8-bit parallel bus allows direct interface to a generic microcontroller (MCU), supporting both multiplexed and non-multiplexed address/data bus configurations. The FT120 also supports Direct Memory Access (DMA) operation. With DMA access data can be written to the IN buffer or read from the OUT buffer without MCU intervention. The DMA access can be done in single cycle or burst mode.

4.2 Interrupt Modes

The FT120 interrupt pin (INT_n) can be programmed to generate interrupt in different modes. The interrupt source can be any bit in Interrupt Register, or receiving SOF packet, or both. The interrupt modes are selectable by two register bits, one is the SOF-only Interrupt Mode bit (bit 7 of Clock Division Factor register), and the other is Interrupt Pin Mode bit (bit 5 of DMA Configuration register).

Interrupt mode	Bit SOF-only Interrupt Mode	Bit Interrupt Pin Mode	Interrupt source
0	0	0	Any bit in Interrupt register
1	0	1	Any bit in Interrupt register and SOF
2	1	X	SOF only

Table 4-1 Interrupt modes

5 Endpoint Buffer Management

The FT120 has 3 physical endpoints (EP0, EP1 and EP2) or 6 logic endpoints (EPI0-EPI5). EP0 is control endpoint, with 16 bytes maximum packet size for both control OUT (EPI0) and control IN (EPI1) endpoint. EP1 can be used as either bulk endpoint or interrupt endpoint, with 16 bytes maximum packet size for both OUT (EPI2) and IN (EPI3) endpoints. Table 5-1 shows the endpoint type and maximum packet size for EP0 and EP1.

Endpoint Number	Endpoint Index (EPI)	Endpoint Direction	Transfer Type	Max Packet Size
0	0	OUT	Control	16
	1	IN	Control	16
1	2	OUT	Bulk/Interrupt	16
	3	IN	Bulk/Interrupt	16

Table 5-1 Endpoint configuration for EP0 and EP1

EP2 is the primary endpoint. It can be configured as either bulk/interrupt or isochronous endpoint. The maximum packet size allowed for EP2 depends on the mode of configuration through Set Mode command. Table 5-2 shows all the 4 endpoint configuration modes for EP2.

Endpoint Configuration Mode (EP2)	Endpoint Index (EPI)	Endpoint Direction	Transfer Type	Max Packet Size
0 (default)	4	OUT	Bulk/Interrupt	64
	5	IN	Bulk/Interrupt	64
1	4	OUT	Isochronous	128
2	5	IN	Isochronous	128
3	4	OUT	Isochronous	64
	5	IN	Isochronous	64

Table 5-2 Endpoint configuration for EP2

As the primary endpoint, EP2 is suitable for transmitting or receiving relatively large data. To improve the data throughput, a pair of ping-pong buffer is implemented for EP2 buffer. This allows the concurrent operation between USB bus access and MCU or DMA local bus access. For example, for EP2 IN endpoint (EPI5), the USB host can read data from FT120 ping buffer while the local MCU is writing to the pong buffer at the same time. The USB host can subsequently read from FT120 pong buffer without waiting for it to be filled. Buffer switching is handled automatically by FT120.

The EP2 buffer also supports DMA operation. The MCU needs to initialize the DMA operation through Set DMA command. Once DMA operation is enabled, data will be moving between the system memory and FT120 endpoint buffer under the DMA controller. Buffer switching between ping buffer and pong buffer is handled automatically.

6 Commands and Registers

The FT120 supported commands are summarized in Table 6-1. These commands include initialization commands, data flow commands and generic commands, which are described in detail in sections 6.2, 6.3 and 6.4 respectively.

6.1 Command Summary

Command Name	Target	Code (hex)	Data phase
Initialization Commands			
Set Address Enable	Device	D0h	Write 1 byte
Set Endpoint Enable	Device	D8h	Write 1 byte
Set Mode	Device	F3h	Write 2 bytes
Set DMA	Device	FBh	Write/Read 1 byte
Data Flow Commands			
Read Interrupt Register	Device	F4h	Read 2 bytes
Select Endpoint	Endpoint 0 OUT	00h	Read 1 byte (optional)
	Endpoint 0 IN	01h	Read 1 byte (optional)
	Endpoint 1 OUT	02h	Read 1 byte (optional)
	Endpoint 1 IN	03h	Read 1 byte (optional)
	Endpoint 2 OUT	04h	Read 1 byte (optional)
	Endpoint 2 IN	05h	Read 1 byte (optional)
Read Last Transaction Status	Endpoint 0 OUT	40h	Read 1 byte
	Endpoint 0 IN	41h	Read 1 byte
	Endpoint 1 OUT	42h	Read 1 byte
	Endpoint 1 IN	43h	Read 1 byte
	Endpoint 2 OUT	44h	Read 1 byte
	Endpoint 2 IN	45h	Read 1 byte
Read Endpoint Status	Endpoint 0 OUT	80h	Read 1 byte
	Endpoint 0 IN	81h	Read 1 byte
	Endpoint 1 OUT	82h	Read 1 byte
	Endpoint 1 IN	83h	Read 1 byte
	Endpoint 2 OUT	84h	Read 1 byte

Command Name	Target	Code (hex)	Data phase
	Endpoint 2 IN	85h	Read 1 byte
Read Buffer	Selected Endpoint	F0h	Read multiple bytes
Write Buffer	Selected Endpoint	F0h	Write multiple bytes
Set Endpoint Status	Endpoint 0 OUT	40h	Write 1 byte
	Endpoint 0 IN	41h	Write 1 byte
	Endpoint 1 OUT	42h	Write 1 byte
	Endpoint 1 IN	43h	Write 1 byte
	Endpoint 2 OUT	44h	Write 1 byte
	Endpoint 2 IN	45h	Write 1 byte
Acknowledge Setup	Selected Endpoint	F1h	None
Clear Buffer	Selected Endpoint	F2h	None
Validate Buffer	Selected Endpoint	FAh	None
General Commands			
Read Current Frame Number	Device	F5h	Read 1 or 2 bytes
Send Resume	Device	F6h	None

Table 6-1 FT120 command set

6.2 Initialization Commands

6.2.1 Set Address Enable

Command : D0h

Data : Write 1 byte

Bit	Symbol	Reset	Description
6-0	Address	0b'0000000	USB assigned device address. A bus reset will reset all address bits to 0.
7	Enable	0	Function enable. A bus reset will automatically enable the function at default address 0.

Table 6-2 Address Enable Register

6.2.2 Set Endpoint Enable

Command : D8h

Data : Write 1 byte

Bit	Symbol	Reset	Description
0	EP_Enable	0	Enable EP1 and EP2 endpoints (Note EP0 is always enabled regardless the setting of EP_Enable bit). Endpoints can only be enabled when the function is enabled.
7-1	Reserved	0b'0000000	Reserved, write to 0

Table 6-3 Endpoint Enable Register

6.2.3 Set Mode

Command : F3h

Data : Write 2 bytes

Bit	Symbol	Reset	Description
0	Reserved	0	Reserved, write to 0
1	No Suspend Clock	1	0: CLKOUT switches to 30 KHz during USB suspend 1: CLKOUT remains unchanged during USB suspend Note: The programmed value will not be changed by a bus reset.
2	Clock Running	1	0: internal clocks stop during USB suspend 1: internal clocks continue running during USB suspend This bit must be set to '0' for bus powered application in order to meet the USB suspend current requirement. Note: The programmed value will not be changed by a bus reset.
3	Interrupt Mode	1	0: interrupt will not generate on NAK or Error transactions 1: interrupt will generate on NAK and Error transactions Note: The programmed value will not be changed by a bus reset.
4	DP_Pullup	0	0: Pullup resistor on USBDP pin disabled 1: Pullup resistor on USBDP pin enabled when Vbus is present Note: The programmed value will not be changed by a bus reset.
5	Reserved	0	Reserved, write to 0
7-6	Endpoint Configuration Mode	0b'00	Set the endpoint configuration mode for EP2. 00: Mode 0 (Non-ISO Mode) 01: Mode 1 (ISO-OUT Mode) 10: Mode 2 (ISO-IN Mode)

Bit	Symbol	Reset	Description
			11: Mode 3 (ISO-IO Mode)

Table 6-4 Configuration Register (Byte 1)

Bit	Symbol	Reset	Description
3-0	Clock Division Factor	0b'1011	The Clock Division Factor value (CDF) determines the output clock frequency on the CLKOUT pin. Frequency = 48 MHz / (CDF +1), where CDF ranges 1-12 or the allowed CLKOUT frequency is 4-24 MHz. Default CLKOUT is 4 MHz. When the CDF is programmed to 0b'1111, the CLKOUT will be turned off. It is recommended to turn off the CLKOUT if it not used, for power saving (about 3mA). Note: The programmed value will not be changed by a bus reset.
5-4	Reserved	0b'00	Reserved, write to 0
6	SET_TO_ONE	0	This bit must be set to 1
7	SOF-only Interrupt Mode	0	0: normal operation 1: interrupt will generate on receiving SOF packet only, regardless the value of the Interrupt Pin Mode bit in DMA configuration register.

Table 6-5 Clock Division Factor Register (Byte 2)

6.2.4 Set DMA

Command : FBh

Data : Read/Write 1 byte

Bit	Symbol	Reset	Description
1-0	DMA Burst	0b'00	Set the DMA burst size 00: Single cycle mode 01: 4 cycle burst mode 10: 8 cycle burst mode 11: 16 cycle burst mode
2	DMA Enable	0	Enable DMA operation 0: DMA operation is disabled 1: DMA operation is enabled FT120 will clear this bit upon EOT_n assertion.
3	DMA Direction	0	This bit indicates the DMA read or write operation. 0: DMA read. Data read from FT120 OUT buffer to system memory. 1: DMA write. Data write to FT120 IN buffer from system

Bit	Symbol	Reset	Description
			memory.
4	Auto Reload	0	Automatically restart the DMA operation. 0: DMA needs to restart by software 1: DMA will restart automatically after the previous DMA transfer finishes
5	Interrupt Pin Mode	0	0: normal operation. Interrupt will generate if any of the bit in the interrupt register is set. 1: interrupt will generate upon receiving SOF packet or if any of the bit in the interrupt register is set.
6	EPI4 Interrupt Enable	0	Interrupt Enable for endpoint index 4. During DMA operation, EPI4 interrupt should be turned off to avoid un-necessary interrupt service.
7	EPI5 Interrupt Enable	0	Interrupt Enable for endpoint index 5. During DMA operation, EPI5 interrupt should be turned off to avoid un-necessary interrupt service.

Table 6-6 DMA Configuration Register

6.3 Data Flow Commands

6.3.1 Read Interrupt Register

Command : F4h

Data : Read 1 or 2 bytes

Bit	Symbol	Reset	Description
0	Endpoint 0 Out	0	Interrupt for endpoint 0 OUT buffer. Cleared by Read Last Transaction Status command.
1	Endpoint 0 In	0	Interrupt for endpoint 0 IN buffer. Cleared by Read Last Transaction Status command.
2	Endpoint 1 Out	0	Interrupt for endpoint 1 OUT buffer. Cleared by Read Last Transaction Status command.
3	Endpoint 1 In	0	Interrupt for endpoint 1 IN buffer. Cleared by Read Last Transaction Status command.
4	Endpoint 2 Out	0	Interrupt for endpoint 2 OUT buffer. Cleared by Read Last Transaction Status command.
5	Endpoint 2 In	0	Interrupt for endpoint 2 IN buffer. Cleared by Read Last Transaction Status command.
6	Bus Reset	0	Interrupt for bus reset. This bit will be cleared after reading.
7	Suspend Change	0	Interrupt for USB bus suspend status change. This bit will be set to '1' when FT120 goes to suspend (missing 3 continuous SOFs) or resumes from suspend. This bit will be cleared after reading.

Table 6-7 Interrupt Register Byte 1

Bit	Symbol	Reset	Description
0	DMA EOT	0	Interrupt for end of DMA transfer. This bit will be cleared after reading.
1	Reserved	0b'xxxxxxx	Reserved

Table 6-8 Interrupt Register Byte 2

6.3.2 Select Endpoint

Command : 00-05h (0ih where 'i' is the index of logic endpoint number)

Data : Optional Read 1 byte

Bit	Symbol	Reset	Description
0	Full/Empty	0	0: selected endpoint buffer is empty 1: selected endpoint buffer is full
1	Stall	0	0: selected endpoint is not stalled 1: selected endpoint is stalled
7-2	Reserved	0b'xxxxxx	Reserved

Table 6-9 Endpoint Status Register

6.3.3 Read Last Transaction Status

Command : 40-45h (4ih where 'i' is the index of logic endpoint number)

Data : Read 1 byte

Bit	Symbol	Reset	Description
0	Data Receive/Transmit Success	0	0: indicate USB data receive or transmit not OK 1: indicate USB data receive or transmit OK
4-1	Error Code	0b'0000	Refer to Table 6-11
5	Setup Packet	0	0: indicate not a setup packet 1: indicate last received packet has a SETUP token
6	Data 0/1 Packet	0	0: packet has a DATA0 token 1: packet has a DATA1 token
7	Previous Status not Read	0	0: previous transaction status was read 0: previous transaction status was not read

Table 6-10 Endpoint Last Transaction Status Register

Error Code	Result
0000	No error
0001	PID encoding error

Error Code	Result
0010	PID unknown
0011	Unexpected packet
0100	Token CRC error
0101	Data CRC error
0110	Time out error
0111	Reserved
1000	Unexpected EOP
1001	Packet NAKed
1010	Sent stall
1011	Buffer overflow
1101	Bit stuff error
1111	Wrong DATA PID

Table 6-11 Transaction error code

6.3.4 Read Endpoint Status

Command : 80-85h (8ih where 'i' is the index of logic endpoint number)

Data : Read 1 byte

Bit	Symbol	Reset	Description
1-0	Reserved	0b'00	Reserved
2	Setup packet	0	0: indicate not a setup packet 1: indicate last received packet has a SETUP token
4-3	Reserved	0b'xx	Reserved
5	Buffer 0 Full	0	0: ping buffer is not filled up 1: ping buffer is filled up
6	Buffer 1 Full	0	0: pong buffer is not filled up 1: pong buffer is filled up Note: this bit only applicable to EP2 which supports ping-pong buffer

Bit	Symbol	Reset	Description
7	Endpoint Stalled	0	0: endpoint is not stalled 1: endpoint is stalled

Table 6-12 Endpoint Buffer Status Register

6.3.5 Read Buffer

Command : F0h
Data : Read multiple bytes

The Read Buffer command is used to read the received packet from the selected endpoint OUT buffer.

The data in the endpoint buffer is organized as follows:

- byte 0: reserved, don't care
- byte 1: length of payload packet
- byte 2: Payload packet byte 1
- byte 3: Payload packet byte 2
- …
- byte n: Payload packet byte n (n = packet length + 2)

For DMA read operation the first two bytes are skipped. Only the payload packet itself will be read and stored in system memory.

6.3.6 Write Buffer

Command : F0h
Data : Write multiple bytes

The Write Buffer command is used to write payload packet to the selected endpoint IN buffer.

The data must be organized in the same way as described in the Read Buffer command. Byte 0 should always be set to 00h.

For DMA write operation the first two bytes are skipped. Only the payload packet itself shall be written to the selected endpoint OUT buffer. Buffer is validated when the max packet size is reached, or when the DMA transfer is terminated by EOT_n (usually the last packet).

6.3.7 Clear Buffer

Command : F2h
Data : None

Followed by Read Buffer command, the Clear Buffer command should be issued after all data has been read out from the endpoint buffer. This is to free the buffer to receive next packet from USB host.

6.3.8 Validate Buffer

Command : FAh
Data : None

Followed by Write Buffer command, the Validate Buffer command should be issued after all data has been written to the endpoint buffer. This is to set the buffer full flag so that the packet can be sent to USB host when IN token arrives.

6.3.9 Set Endpoint Status

Command : 40-45h (4ih where 'i' is the index of logic endpoint number)
Data : Write 1 byte

Bit	Symbol	Reset	Description
0	Stall	0	0: Disable the endpoint STALL state. 1: Enable the endpoint STALL state. For EP0 OUT (control OUT endpoint) the STALL state will automatically be cleared by receiving a SETUP packet. When this bit is cleared, the endpoint will reinitialize. Any data in the endpoint buffer will be flushed away, and the PID for next packet will carry DATA0 flag.
7-1	Reserved	0b'xxxxxxx	Reserved

Table 6-13 Endpoint Control Register

6.3.10 Acknowledge Setup

Command : F1h
Data : None

When receiving a SETUP packet the FT120 will flush the IN buffer and disable the Validate Buffer and Clear Buffer commands for both IN and OUT endpoints. The MCU shall read and process the SETUP packet, and then issue the Acknowledge Setup command to re-enable the Validate Buffer and Clear Buffer commands. The Acknowledge Setup command must be sent to both IN and OUT endpoints.

6.4 General Commands

6.4.1 Read Current Frame Number

Command : F5h

Data : Read One or Two Bytes

Bit	Symbol	Reset	Description
7-0	Frame Number LSB	00h	Frame number for last received SOF, byte 1 (least significant byte)

Table 6-14 Frame Number LSB Register

Bit	Symbol	Reset	Description
2-0	Frame Number MSB	0b'000	Frame number for last received SOF, byte 2 (Most significant byte)
7-3	Reserved	0b'00000	Reserved

Table 6-15 Frame Number MSB Register

6.4.2 Send Resume

Command : F6h

Data : None

To perform remote-wakeup when suspended, the MCU needs to issue Send Resume command. The FT120 will send an upstream resume signal for a period of 10 ms. If the clock is not running during suspend, the MCU needs to wakeup FT120 by drive SUSPEND pin to LOW, followed by Send Resume command.

7 Reference Schematic

Figure 7-1 shows a reference schematic for a FT120 module which can be connected to a generic microcontroller to add USB device function. The reference design supports both bus-powered and self-powered application.

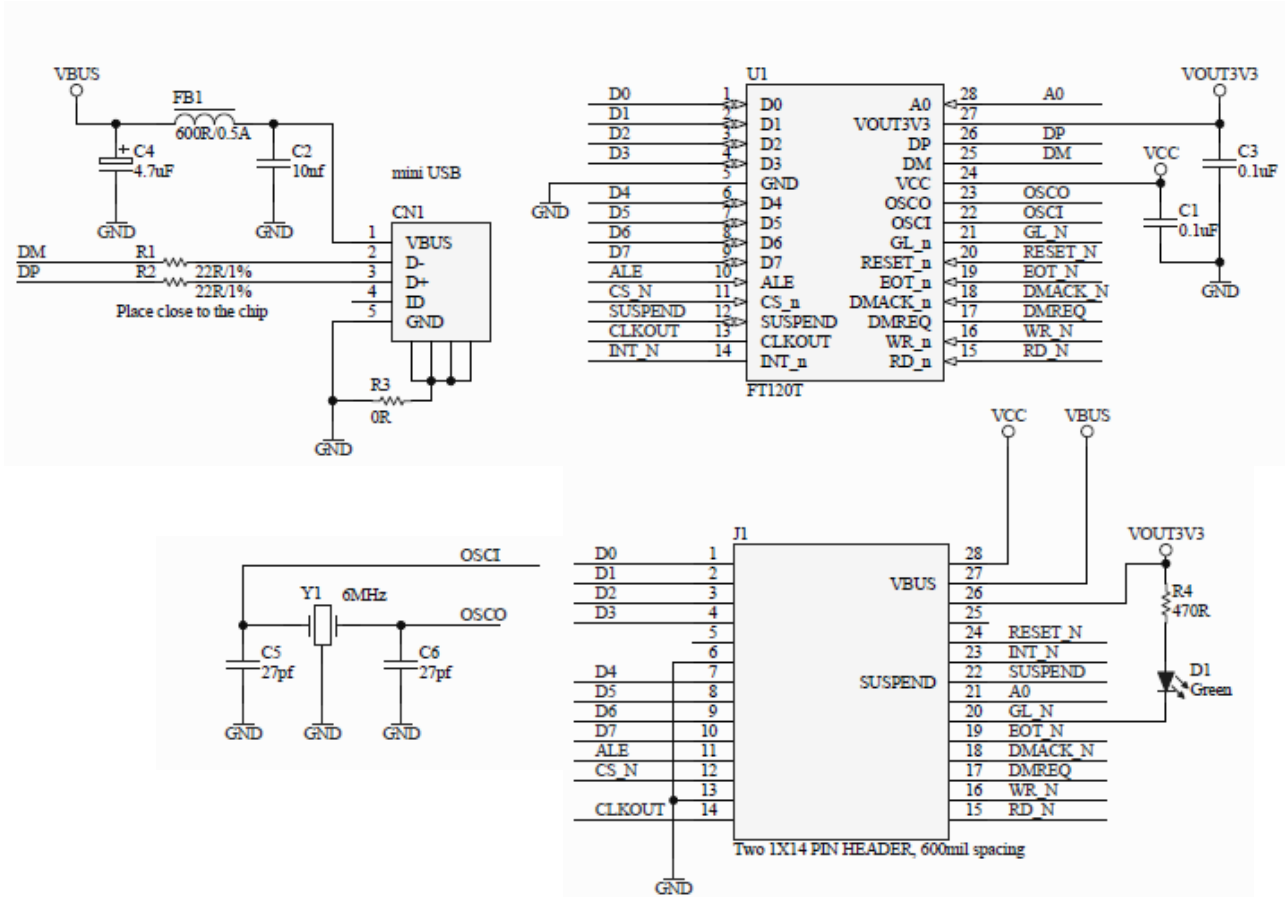


Figure 7-1 FT120 Reference schematics

8 Devices Characteristics and Ratings

8.1 Absolute Maximum Ratings

The absolute maximum ratings for the FT120 devices are as follows. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these may cause permanent damage to the device.

Parameter	Value	Unit
Storage Temperature	-65 to 150	°C
Floor Life (Out of Bag) At Factory Ambient (30°C / 60% Relative Humidity)	168 (IPC/JEDEC J-STD-033A MSL Level 3 Compliant)*	Hours
Ambient Temperature (Power Applied)	-40 to 85	°C
Latch-up current	TBD	mA
Electrostatic Discharge Voltage(ESD) human body model(HBM)	±2000	V
Electrostatic Discharge Voltage(ESD) machine model(MM)	±200	V
Electrostatic Discharge Voltage(ESD) charged device model(CDM)	±500	V
VCC Supply Voltage	-0.5 to +6.0	V
DC Input Voltage – USBDP and USBDM	-0.5 to +3.8	V
DC Input Voltage – High Impedance Bidirectional	-0.5 to + (VCC +0.5)	V
DC Input Voltage – All Other Inputs	-0.5 to + (VCC +0.5)	V
DC Output Current – Outputs	22	mA

Table 8-1 Absolute Maximum Ratings

* If devices are stored out of the packaging beyond this time limit the devices should be baked before use. The devices should be ramped up to a temperature of +125°C and baked for up to 17 hours.

8.2 DC Characteristics

DC Characteristics (Ambient Temperature = -40°C to +85°C)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
VCC1	VCC Operating Supply Voltage	4.0	5.0	5.5	V	Normal Operation
VCC2	VCC Operating Supply Voltage	3.0	3.3	3.6	V	Regulator by-pass mode Operation
Icc1	Operating Supply Current		5		mA	Normal Operation, USB bus transmit or receive, CLKOUT off
Icc2	Operating Supply Current		8		mA	Normal Operation, USB bus transmit or receive, CLKOUT = 12 MHz
Icc3	Operating Supply Current		84		µA	USB Suspend, Clock Running = '0', excluding the DP_Pullup current
VOUT3V3	3.3v regulator output	3.0	3.3	3.6	V	VCC=5V

Table 8-2 Operating Voltage and Current

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.4		3.6	V	I source = 4mA
Vol	Output Voltage Low			0.4	V	I sink = 4mA
Vih	Input Voltage High	2.0			V	
Vil	Input Voltage Low	-		0.8	V	

Table 8-3 digital I/O Pin Characteristics

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
UVoh	I/O Pins Static Output (High)	2.8		3.6	V	R_L = 1.5kΩ to 3.6 V
UVol	I/O Pins Static Output (Low)	-		0.3	V	R_L = 15kΩ to GND
UVse	Single Ended Rx Threshold	0.8		2.0	V	
UCom	Differential Common Mode	0.8		2.5	V	

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
UVDif	Differential Input Sensitivity	0.2			V	
UDrvZ	Driver Output Impedance	29	-	44	Ω	Including external 22 Ω ±1% series resistor

Table 8-4 USB I/O Pin (USBDP, USBDM) Characteristics

8.3 AC Characteristics

Parameter	Value			Unit
	Minimum	Typical	Maximum	
Frequency of Operation (see Note 1)	5.997	6.000	6.003	MHz
Duty Cycle	45	50	55	%

Table 8-5 Crystal or clock Characteristics (OSCI, OSCO pins)

Note 1: Equivalent to ±500ppm

Symbol	Parameter	Min	Max	Unit
	ALE Timings:			
tLH	ALE High Pulse Width	20		ns
tAVLL	Address Valid to ALE Low Time	10		ns
tLLAX	ALE Low to Address Transition Time		10	ns
	Write Timings:			
tCLWL	CS_n (DMACK_n) Low to WR_n Low Time	0		ns
tWHCH	WR_n High to CS_n (DMACK_n) High Time	5		ns
tAVWL	A0 Valid to WR_n Low Time	0		ns
tWHAX	WR_n High to A0 Transition Time	5		ns
tWL	WR_n Low Pulse Width	20		ns
tWDSU	Write Data Setup Time	30		ns
tWDH	Write Data Hold Time	10		ns
tWC	Write Cycle Time	500		ns

Symbol	Parameter	Min	Max	Unit
t(WC-WD)	Write command to write data	600		ns
	Read Timings:			
tCLRL	CS_n (DMACK_n) Low to RD_n Low Time	0		ns
tRHCH	RD_n High to CS_n (DMACK_n) High Time	5		ns
tAVRL	A0 Valid to RD_n Low Time	0		ns
tRL	RD_n Low Pulse Width	20		ns
tRLDD	RD_n Low to Data Valid Time		20	ns
tRHDZ	RD_n High to Data Hi-Z Time		20	ns
tRC	Read Cycle Time	500		ns
t(WC-RD)	Write command to read data	600		ns

Table 8-6 Parallel Interface IO timing

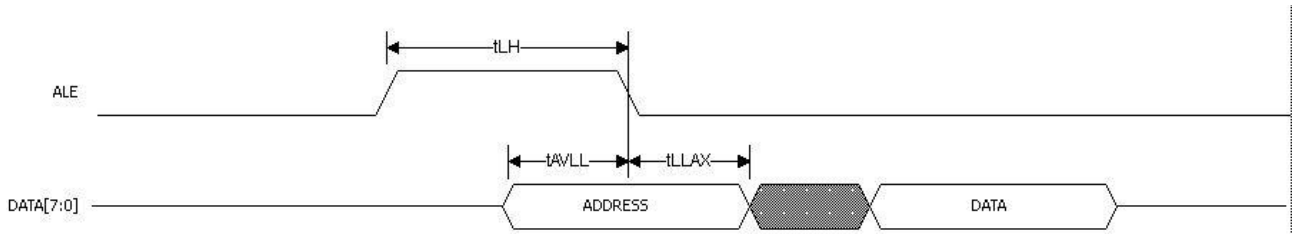


Figure 8-1 ALE Timing

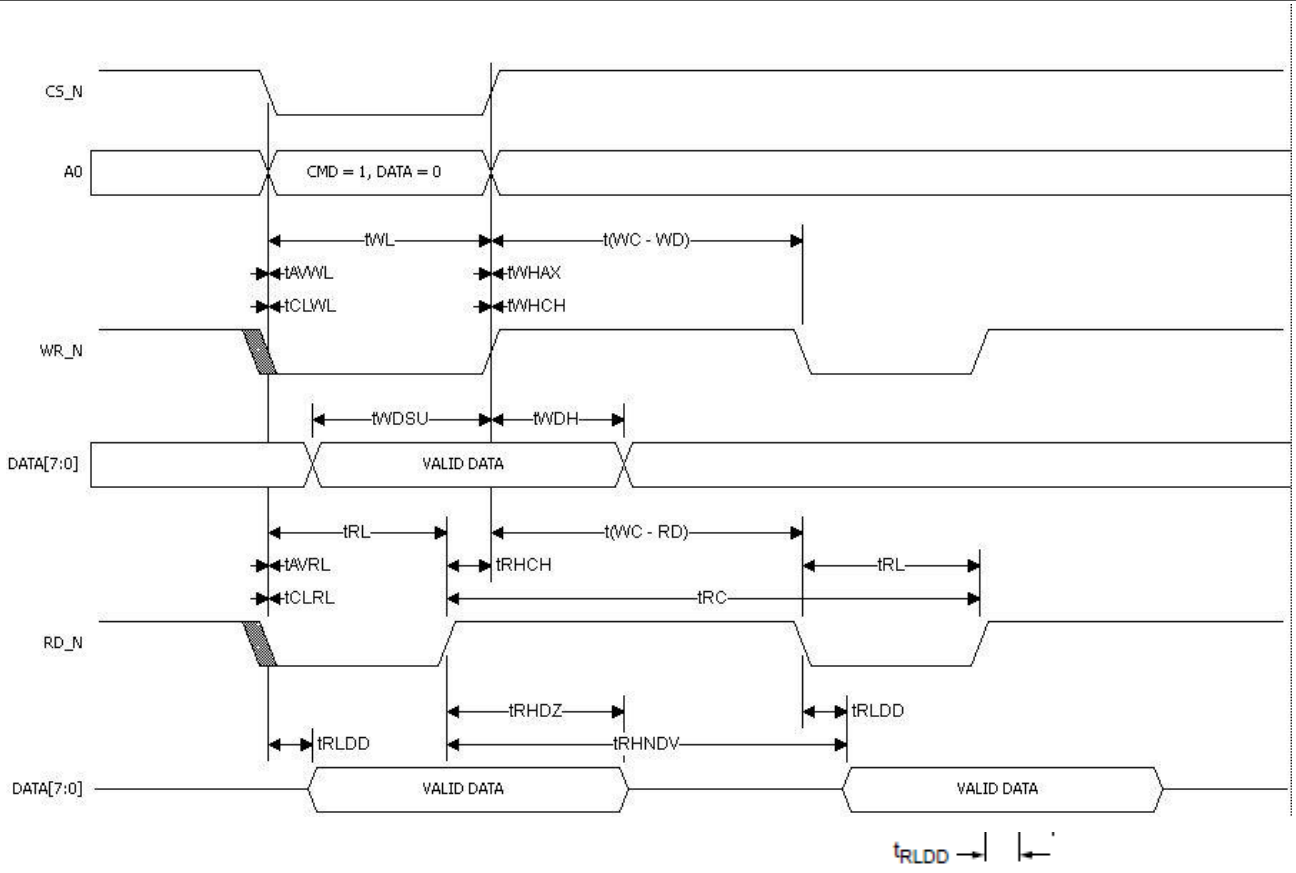


Figure 8-2 Parallel interface timing

Symbol	Parameter	Min	Max	Unit
	Single-cycle DMA Timings:			
tRHSH	DMREQ High to RD_n/WR_n High Time	120		ns
tAHRH	DMACK_n High to DMREQ High Time		330	ns
tSHAH	RD_n/WR_n High to DMACK_n High Time	130		ns
tEL	EOT_n Low Pulse Width (Simultaneous DMACK_n, RD_n/WR_n and EOT_n low time)	10		ns
	Burst DMA Timings:			
tSLRL	RD_n/WR_n Low to DMREQ Low Time		40	ns
tRHSH	DMREQ High to RD_n/WR_n High Time	120		ns
tSHAH	RD_n/WR_n High to DMACK_n High Time	130		ns
	EOT Timings:			
tELRL	EOT_n Low to DMREQ Low Time		40	ns

Table 8-7 DMA timing characteristics

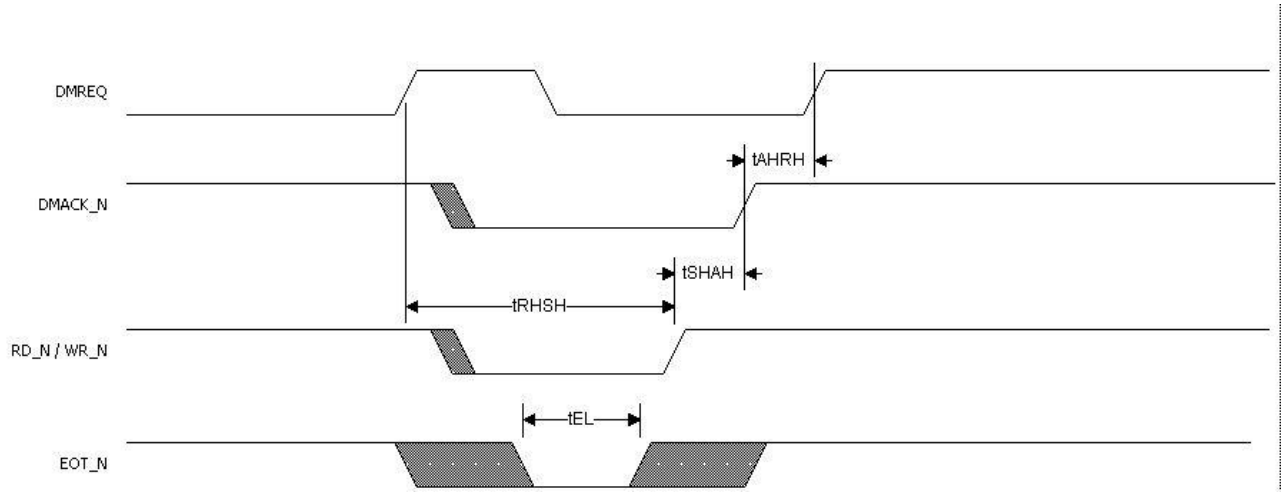


Figure 8-3 Single cycle DMA timing

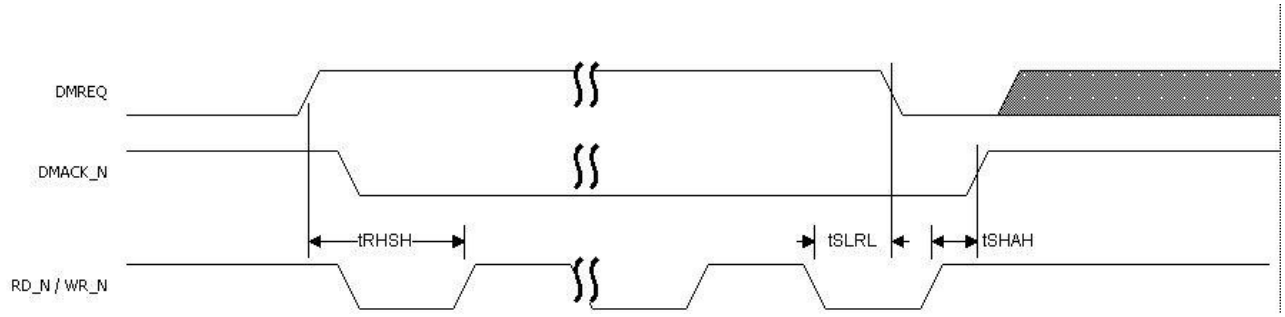


Figure 8-4 Burst mode DMA timing

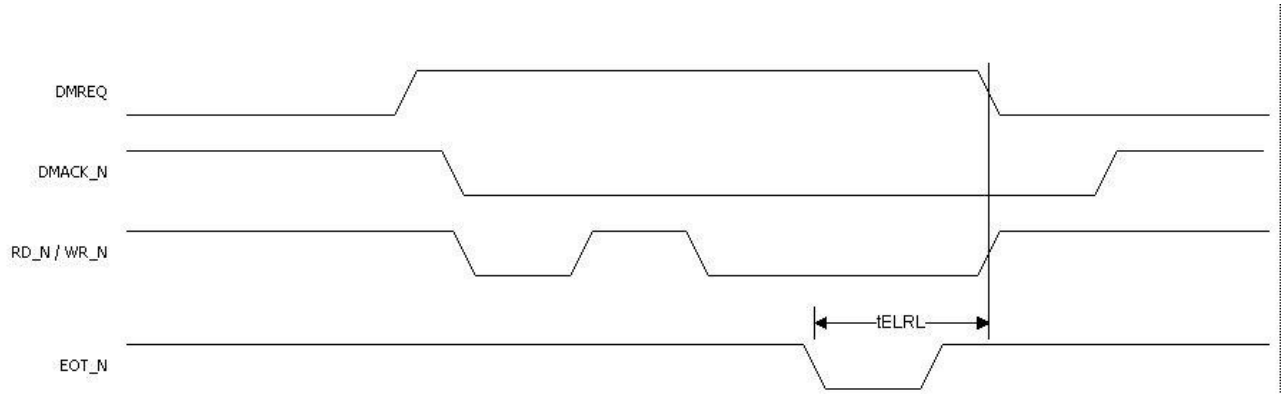
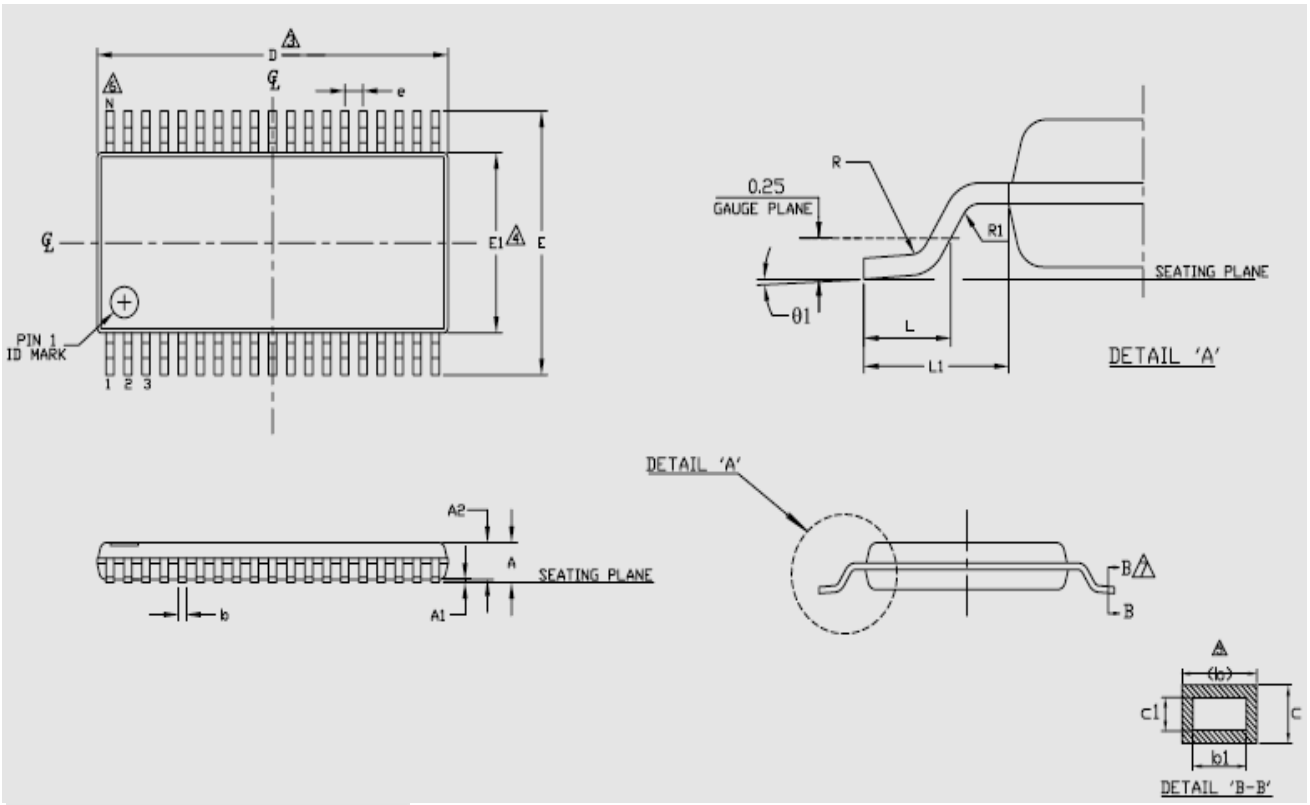


Figure 8-5 DMA terminated by EOT_n

9 Package Parameters

The FT120 is available in two different packages. The FT120T is the TSSOP-28 package option and the FT120Q is the QFN-28 package option. The solder reflow profile for both packages is described in Section 0.

9.1 TSSOP-28 Package Dimensions



SYMBOL	28L TSSOP		
	MIN	NOM.	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	0.90	1.05
D	9.6	9.7	9.8
E1	4.3	4.4	4.5
E	6.2	6.4	6.6
L	0.45	0.60	0.75
R	0.09	—	—
R1	0.09	—	—
b	0.19	—	0.30
b1	0.19	0.22	0.25
c	0.09	—	0.20
c1	0.09	—	0.16
θ1	0°	—	8°
L1	1.0 REF		
e	0.65 BSC		
N	28		
Ref.	Jedec MO-153 Issue C Variation AE		

Figure 9-1 TSSOP-28 Package Dimensions

The FT120T is supplied in a RoHS compliant 28 pin TSSOP package. The package is lead (Pb) free and uses a 'green' compound. The package is fully compliant with European Union directive 2002/95/EC.

This package is nominally 4.4mm x 9.7mm body (6.4mm x9.7mm including pins). The pins are on a 0.65 mm pitch. The above mechanical drawing shows the TSSOP-28 package.

All dimensions are in millimetres.

9.2 TSSOP-28 Package Markings

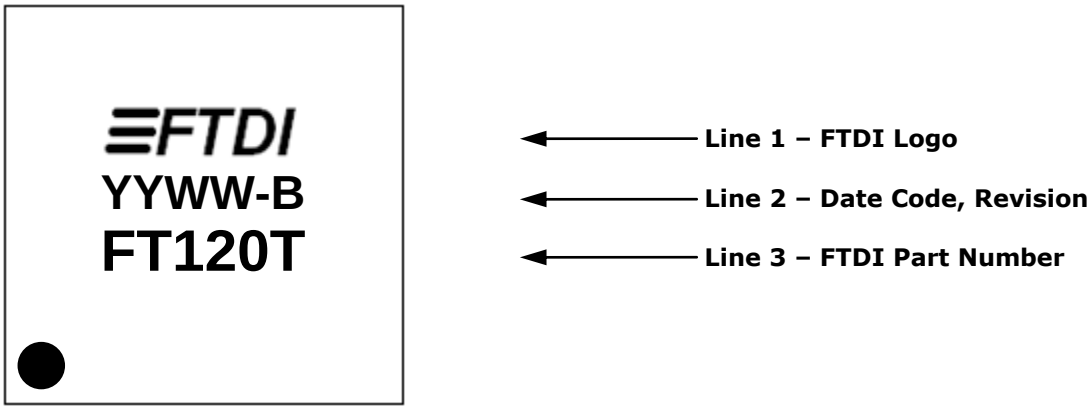
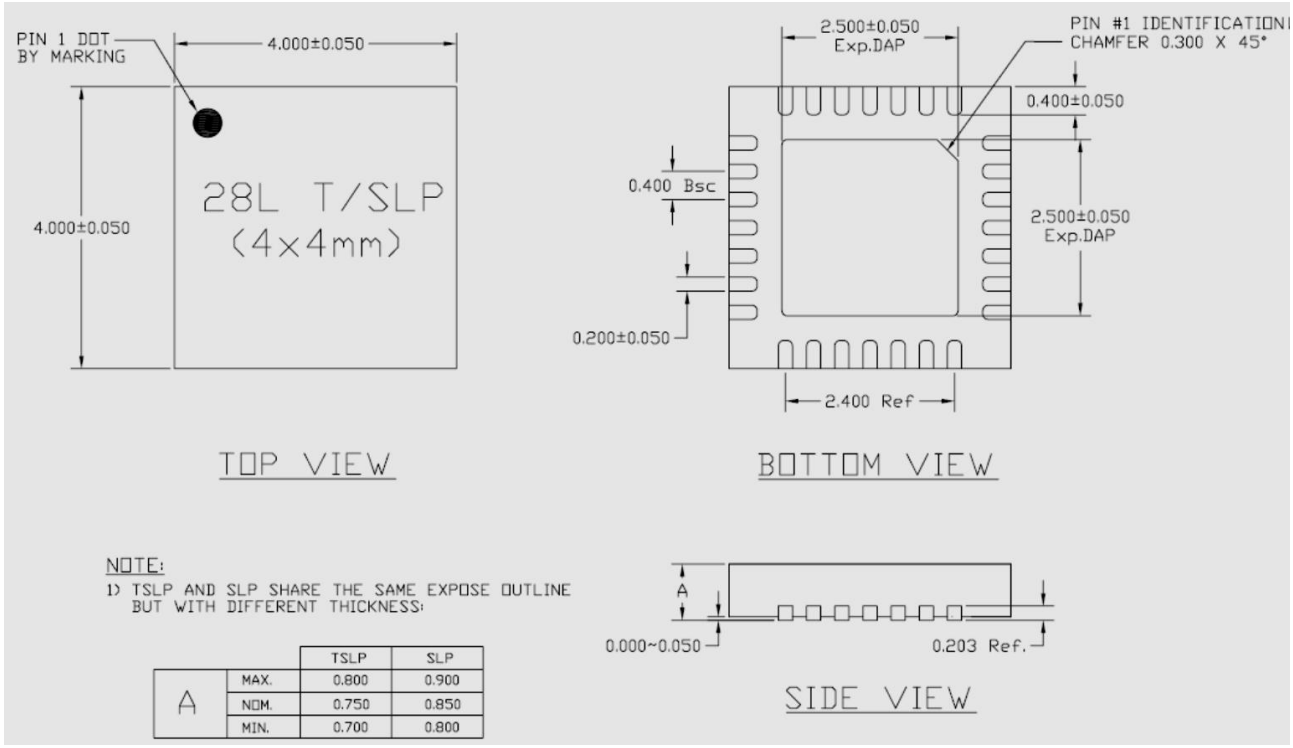


Figure 9-2 TSSOP-28 Package Markings

The date code format is **YYWW** where WW = 2 digit week number, YY = 2 digit year number.

9.3 QFN-28 Package Dimensions



		TSLP	SLP
A	MAX.	0.800	0.900
	NOM.	0.750	0.850
	MIN.	0.700	0.800

Figure 9-3 QFN-28 Package Dimensions

The FT120Q is supplied in a RoHS compliant leadless QFN-28 package. The package is lead (Pb) free, and uses a 'green' compound. The package is fully compliant with European Union directive 2002/95/EC.

This package is nominally 4.00mm x 4.00mm. The solder pads are on a 0.40mm pitch. The above mechanical drawing shows the QFN-28 package. All dimensions are in millimetres.

The centre pad on the base of the FT120Q is internally connected to GND pin, and can be left unconnected, or connected to ground (recommended).

9.4 QFN-28 Package Markings

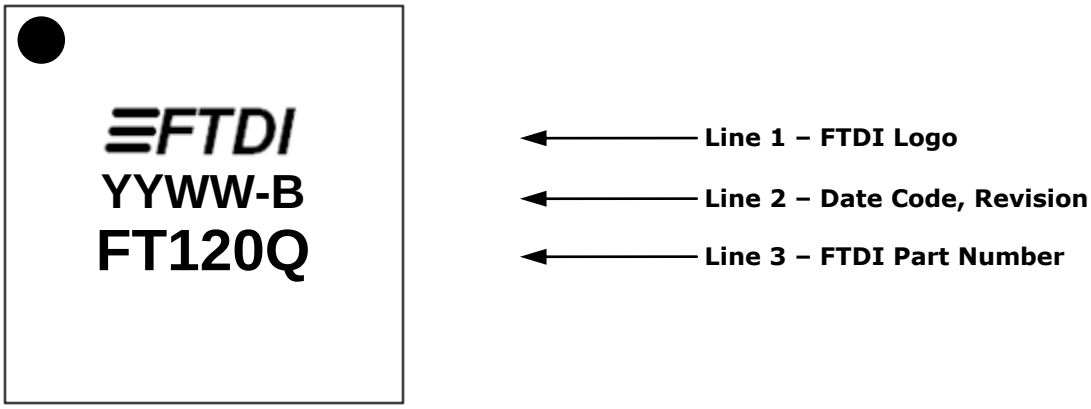


Figure 9-4 QFN-28 Package Markings

The date code format is **YYWW** where WW = 2 digit week number, YY = 2 digit year number.

9.5 Solder Reflow Profile

The FT120 is supplied in Pb free TSSOP-28 and QFN-28 packages. The recommended solder reflow profile for both package options is shown in Figure 9-5.

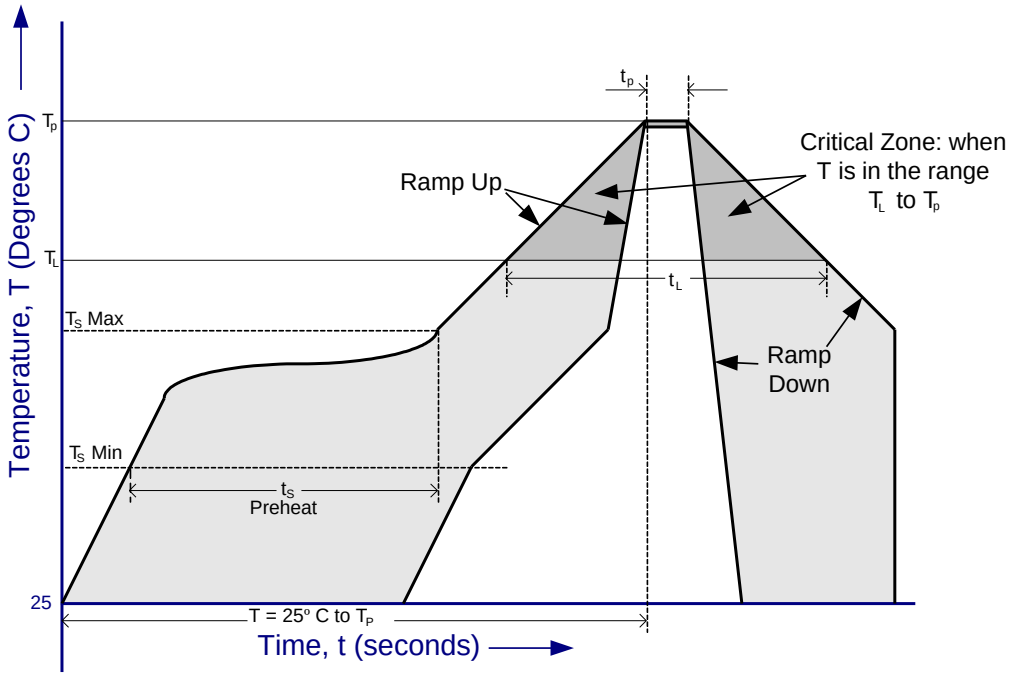


Figure 9-5 FT120 Solder Reflow Profile

The recommended values for the solder reflow profile are detailed in Table 9-1. Values are shown for both a completely Pb free solder process (i.e. the FT120 is used with Pb free solder), and for a non-Pb free solder process (i.e. the FT120 is used with non-Pb free solder).

Profile Feature	Pb Free Solder Process	Non-Pb Free Solder Process
Average Ramp Up Rate (T_s to T_p)	3°C / second Max.	3°C / Second Max.
Preheat - Temperature Min (T_s Min.) - Temperature Max (T_s Max.) - Time (t_s Min to t_s Max)	 150°C 200°C 60 to 120 seconds	 100°C 150°C 60 to 120 seconds
Time Maintained Above Critical Temperature T_L: - Temperature (T_L) - Time (t_L)	 217°C 60 to 150 seconds	 183°C 60 to 150 seconds
Peak Temperature (T_p)	260°C	240°C

Profile Feature	Pb Free Solder Process	Non-Pb Free Solder Process
Time within 5°C of actual Peak Temperature (t_p)	20 to 40 seconds	20 to 40 seconds
Ramp Down Rate	6°C / second Max.	6°C / second Max.
Time for T= 25°C to Peak Temperature, T_p	8 minutes Max.	6 minutes Max.

Table 9-1 Reflow Profile Parameter Values

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Appendix B - Revision History

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Document Feedback:	Send Feedback

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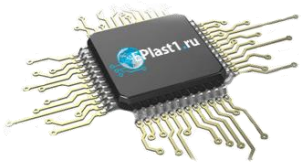

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