AAT4292

SmartSwitch™

Seven Channel High-Side I/O Expander

General Description

The AAT4292 SmartSwitch™ is a member of AnalogicTech's Application Specific Power MOSFET™ (ASPM™) product family. The AAT4292 has seven P-channel MOSFETs configured for use as a high side microprocessor GPIO expander powered from a common supply source. Operating over a 1.8V to 5.5V range, the AAT4292 is ideal for portable Li-Ion/Polymer powered products. The state of each output channel is controlled with a single GPIO line via the EN/SET pin using AnalogicTech's Simple Serial Control™ (AS²Cwire™) interface.

The switch states are controlled by AnalogicTech's Simple Serial Control (AS²Cwire) interface which permits ease of control and efficiency of size. The quiescent supply current is very low, typically 6.3µA. In shutdown mode, the supply current is reduced to less than 1µA.

The AAT4292 is offered in a Pb-free, 10-pin SC70JW package specified over the -40°C to +85°C temperature range.

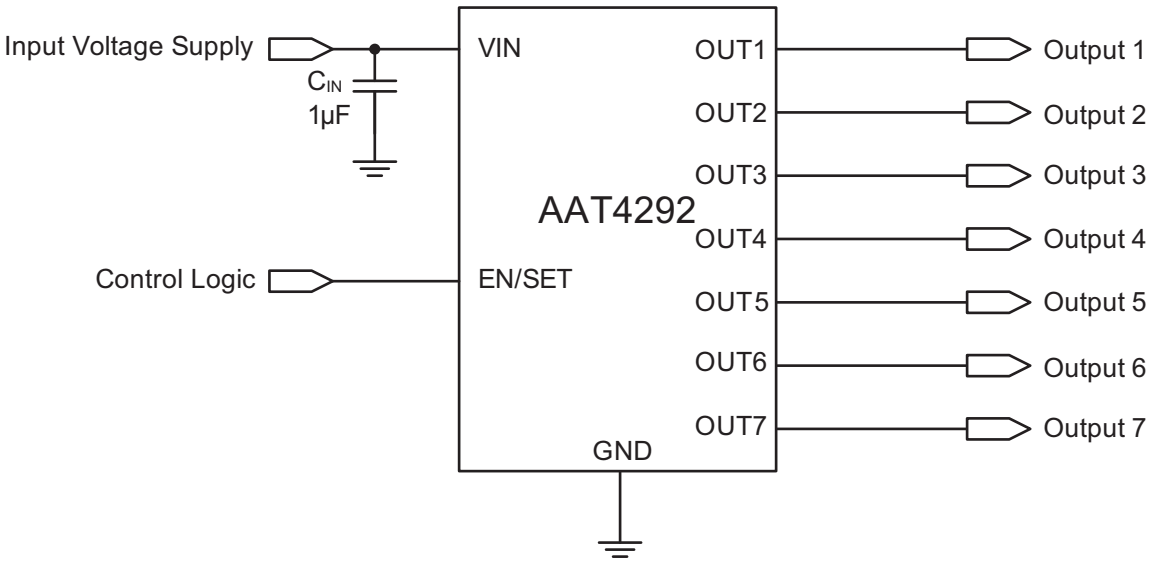
Features

- V_{IN} Range: 1.8V – 5.5V
- 7 Independent Output Channels
- 1.1Ω $R_{DS(ON)}$ per Channel
- User Programmable AS²Cwire Interface
- Low Quiescent Current
  - 6.3µA Operational
  - 0.1µA in shutdown
- -40°C to +85°C Temperature Range
- Available in SC70JW-10 Package

Applications

- Cell Phone Keypad, Backlight And Fashion Lighting Control
- I/O Expander
- Media Players
- Multiple Channel Low Power Switching
- Portable Electronic Devices

Typical Application

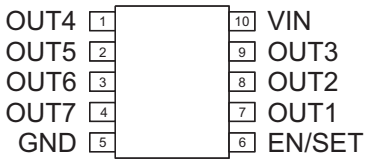


Pin Descriptions

Symbol	Pin #	Function
OUT4	1	P-channel MOSFET drain; Channel 4 output pin.
OUT5	2	P-channel MOSFET drain; Channel 5 output pin.
OUT6	3	P-channel MOSFET drain; Channel 6 output pin.
OUT7	4	P-channel MOSFET drain; Channel 7 output pin.
GND	5	Ground connection.
EN/SET	6	Input control pin using AS^{2}Cwire serial interface. The device records rising edges of the clock, and decodes them into 128 states controlling the ON/OFF states of the outputs. See Table 1 and Table 2 for output settings. In addition, a logic low forces the device into shutdown mode, reducing the supply current to less than 1µA. This pin should not be left floating.
OUT1	7	P-channel MOSFET drain; Channel 1 output pin.
OUT2	8	P-channel MOSFET drain, Channel 2 output pin.
OUT3	9	P-channel MOSFET drain, Channel 3 output pin.
VIN	10	Input supply voltage. VIN is connected to the P-channel MOSFET common sources. Connect a 1µF ceramic capacitor from VIN to GND.

Pin Configuration

SC70JW-10
(Top View)



Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
V_{IN}	VIN to GND	-0.3 to 6.0	V
V_{OUT}	OUT to GND	-0.3 to V_{IN} + 0.3	V
$V_{EN/SET}$	EN/SET to GND	-0.3 to 6.0	V
I_{MAX}	Maximum Continuous Switch Current	250	mA
T_J	Operating Junction Temperature Range	-40 to 150	°C
V_{ESD}	ESD Rating – HBM[2]	4000	V

Thermal Information

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance[3]	225	°C/W
P_D	Maximum Power Dissipation[4] (T_A = 25°C)	440	mW

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
2. Human body model is a 100pF capacitor discharged through a 1.5kΩ resistor to each pin.
3. Mounted on a FR4 board.
4. Derate 4.4mW/°C above 25°C.

Electrical Characteristics[1]

V_{IN} = 5.0V, T_A = -40°C to 85°C unless otherwise noted. Typical values are T_A = 25°C.

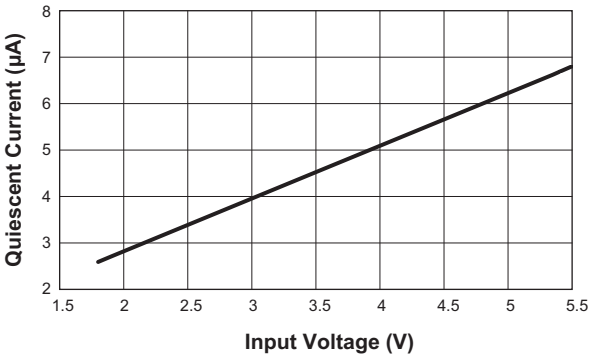
Symbol	Description	Conditions	Min	Typ	Max	Units
Power Supply and MOSFETs						
V_{IN}	Operation Voltage		1.8		5.5	V
I_Q	Quiescent Current	EN/SET = V_{IN} = 5V, I_{OUTn} = 0, All Switches ON		6.3	10	µA
$I_{SD(OFF)}$	Shutdown Current	EN/SET = GND, V_{IN} = 5V, OUTn = 0		0.1	1.0	µA
$R_{DS(ON)}$	P-Channel High-Side MOSFET On-State Resistance	V_{IN} = 5.0V, I_{OUTn} = 100mA, T_A = 25°C		1.1	1.7	Ω
		V_{IN} = 4.2V, I_{OUTn} = 100mA, T_A = 25°C		1.2	1.8	
		V_{IN} = 3.0V, I_{OUTn} = 100mA, T_A = 25°C		1.5	2.2	
		V_{IN} = 1.8V, I_{OUTn} = 100mA, T_A = 25°C		2.5	3.8	
T_{CRDS}	On-State Resistance Temperature Coefficient			2800		ppm/°C
Switch Timing						
$t_{D(ON)}$	Output Turn-On Delay Time[2]	V_{IN} = 5V, R_{LOAD} = 500Ω, C_{OUT} = 100nF		40		ns
t_R	Turn-On Rise Time	V_{IN} = 5V, R_{LOAD} = 500Ω, C_{OUT} = 100nF		270		
$t_{D(OFF)}$	Output Turn-Off Delay Time[3]	V_{IN} = 5V, R_{LOAD} = 500Ω		40		
Control Logic (EN/SET)						
$V_{EN(L)}$	Enable Threshold Low	V_{IN} = 1.8V			0.4	V
$V_{EN(H)}$	Enable Threshold High	V_{IN} = 5.5V	1.6			V
t_{LO}	EN/SET Low Time	$V_{EN/SET}$ < 0.4V	100			ns
t_{HI}	Minimum EN/SET High Time	$V_{IN} \leq$ 2.5V			500	ns
		V_{IN} > 2.5V			250	
t_{OFF}	EN/SET Off Timeout			1.3	4.0	µs
t_{LAT}	EN/SET Latch Timeout			1.15	4.0	µs
I_{SINK}	EN/SET Input Leakage Current	$V_{EN/SET}$ = 5.5V		0.01	1.0	µA

1. The AAT4292 is guaranteed to meet performance specification over the –40°C to +85°C operating temperature range, and is assured by design, characterization and correlation with statistical process controls.
2. $t_{D(ON)}$ is the time after latch timeout to 90% of the output voltage.
3. $t_{D(OFF)}$ is the time after off timeout to 10% of the output voltage.

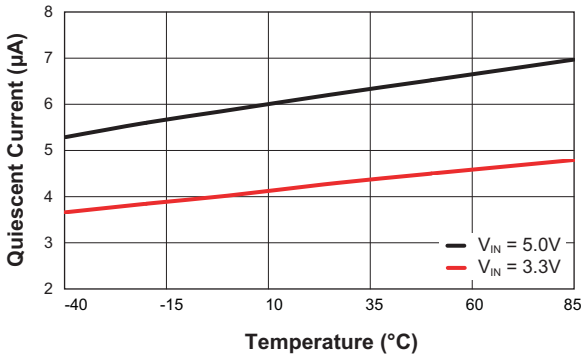
Typical Characteristics

Unless otherwise noted, V_{IN} = 5.0V, C_{IN} = 1µF, C_{OUTn} = 0.1µF, T_A = 25°C.

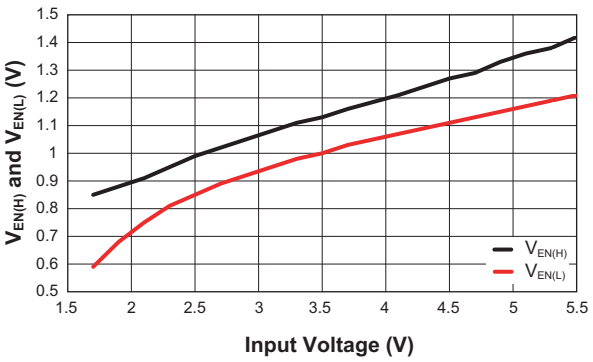
Quiescent Current vs. Input Voltage



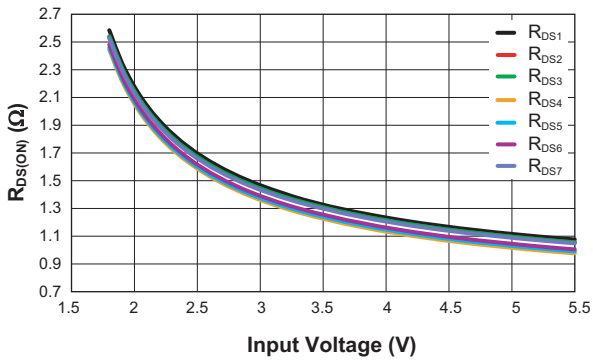
Quiescent Current vs. Temperature



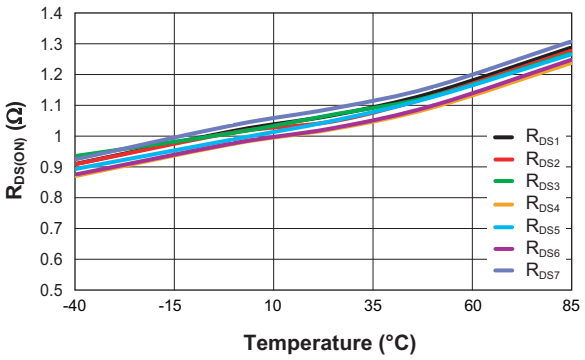
$V_{EN(H)}$ and $V_{EN(L)}$ vs. Input Voltage



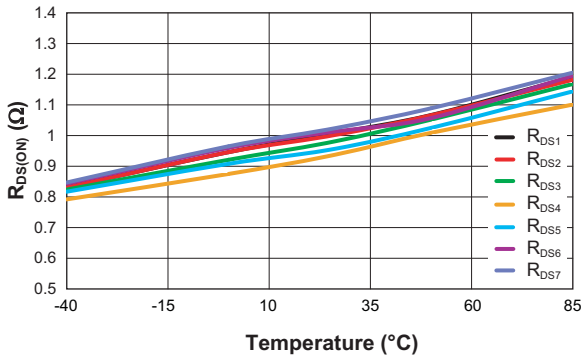
$R_{DS(ON)}$ vs. Input Voltage
(I_{OUT1-7} = 100mA)



$R_{DS(ON)}$ vs. Temperature
(V_{IN} = 5.0V; I_{OUT1-7} = 100mA)



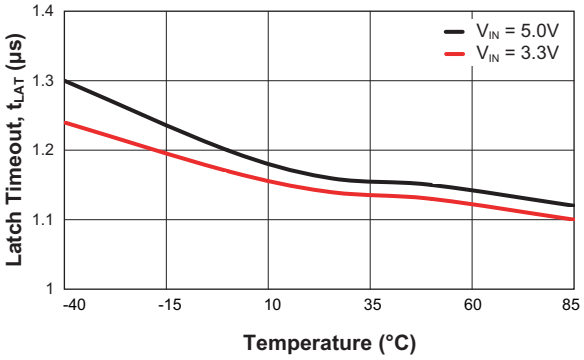
$R_{DS(ON)}$ vs. Temperature
(V_{IN} = 5.0V; I_{OUT1-7} = 10mA)



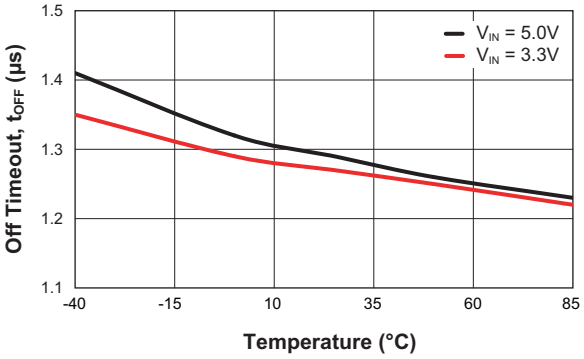
Typical Characteristics

Unless otherwise noted, V_{IN} = 5.0V, C_{IN} = 1µF, C_{OUTn} = 0.1µF, T_A = 25°C.

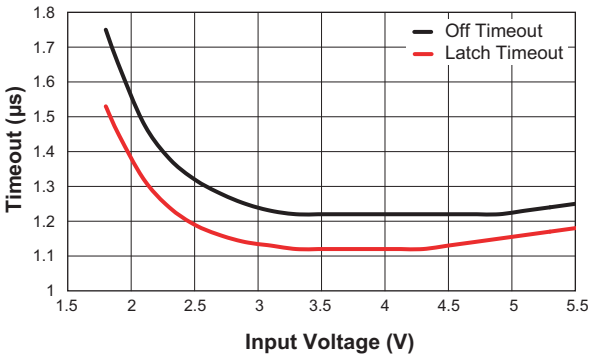
EN/SET Latch Timeout vs. Temperature



EN/SET Off Timeout vs. Temperature

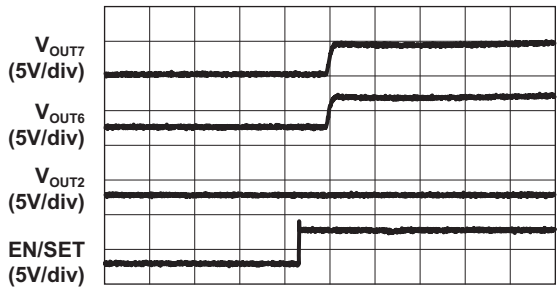


EN/SET Timeout vs. Input Voltage



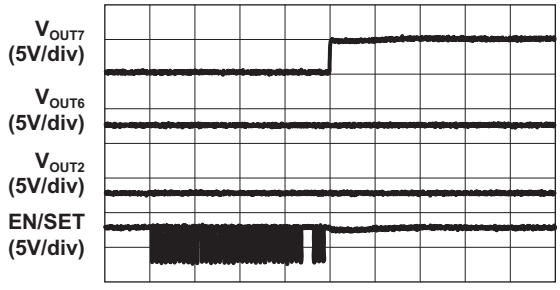
Turn-On Characteristic

(V_{IN} = 5V; R_{L2} = R_{L6} = R_{L7} = 50Ω; C_{O2} = C_{O6} = C_{O7} = 0.1µF)



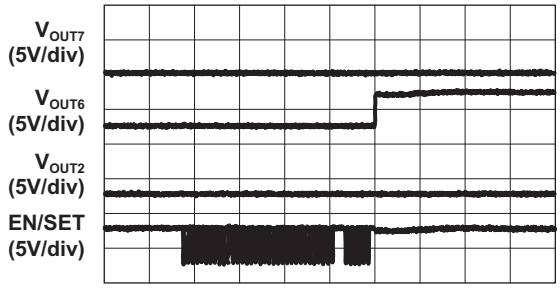
Turn-On Characteristic

(V_{IN} = 5V; R_{L2} = R_{L6} = R_{L7} = 50Ω; C_{O2} = C_{O6} = C_{O7} = 0.1µF)



Turn-On Characteristic

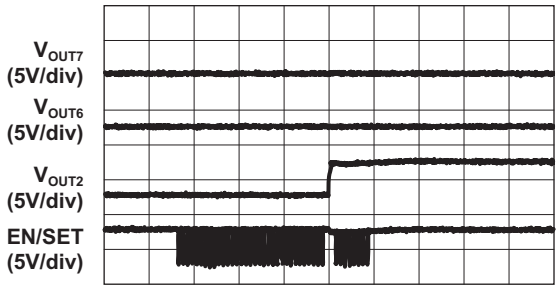
(V_{IN} = 5V; R_{L2} = R_{L6} = R_{L7} = 50Ω; C_{O2} = C_{O6} = C_{O7} = 0.1µF)



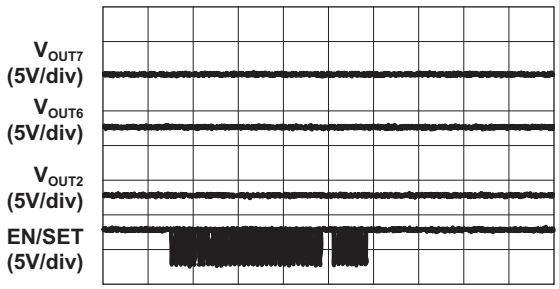
Typical Characteristics

Unless otherwise noted, V_{IN} = 5.0V, C_{IN} = 1µF, C_{OUTn} = 0.1µF, T_A = 25°C.

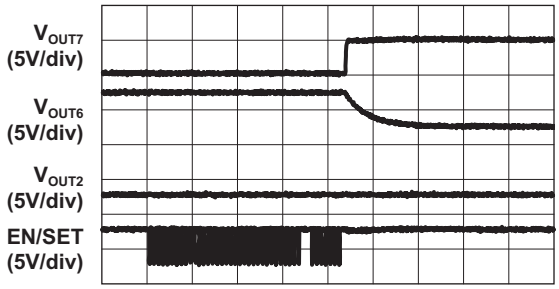
Turn-On Characteristic
(V_{IN} = 5V; R_{L2} = R_{L6} = R_{L7} = 50Ω; C_{O2} = C_{O6} = C_{O7} = 0.1µF)



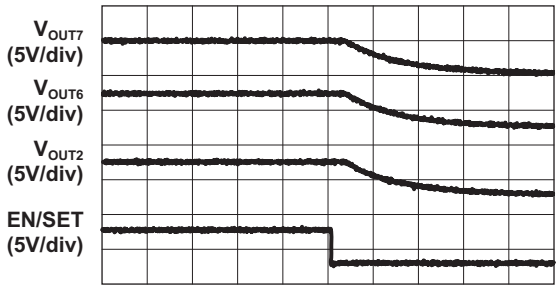
Turn-On Characteristic
(V_{IN} = 5V; R_{L2} = R_{L6} = R_{L7} = 50Ω; C_{O2} = C_{O6} = C_{O7} = 0.1µF)



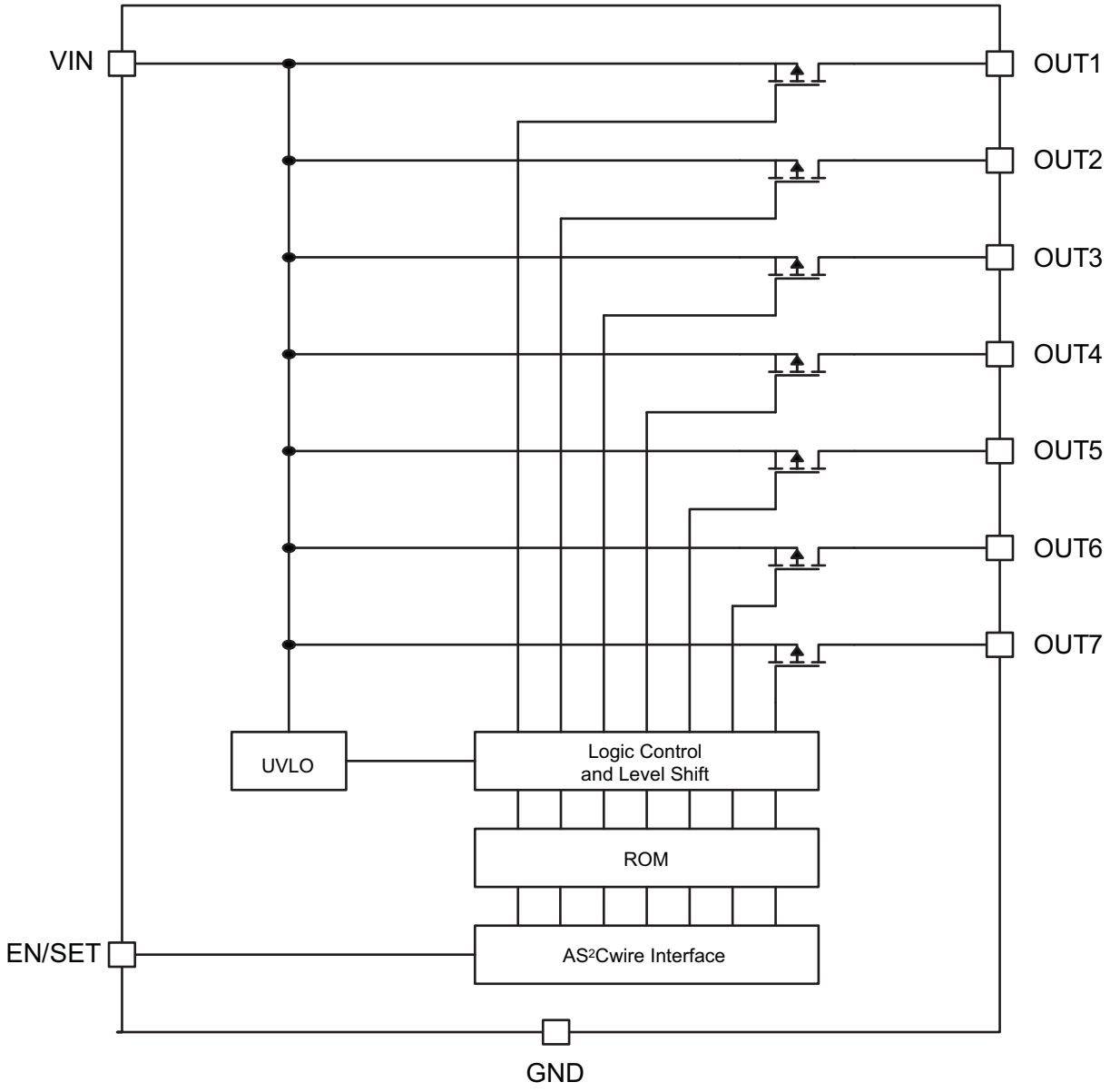
Transition of Outputs
(V_{IN} = 5V; R_{L2} = R_{L6} = R_{L7} = 50Ω; C_{O2} = C_{O6} = C_{O7} = 0.1µF)



Turn-Off Characteristic
(V_{IN} = 5V; R_{L2} = R_{L6} = R_{L7} = 50Ω; C_{O2} = C_{O6} = C_{O7} = 0.1µF)



Functional Block Diagram



Functional Description

The AAT4292 consists of seven P-channel MOSFET power switches designed for I/O expansion applications. The device operates with input voltages ranging from 1.8V to 5.5V which, along with its extremely low operating current, makes it ideal for battery-powered applications. In cases where the input voltage drops below 1.8V, the AAT4292 MOSFETs are protected from entering the linear region of operation by automatically shutting down.

In addition, the TTL-compatible EN/SET pin makes the AAT4292 an ideal level-shifted load switch. An optional slew rate controlling feature eliminates inrush current when a MOSFET is turned on, allowing the AAT4292 to be implemented with a small input capacitor or no capacitor at all, while maintaining isolation between channels. During slewing, the current ramps linearly until it reaches the level required for the output load condition. The proprietary control method works by careful control and monitoring of the MOSFET gate volt-

age. When the device is switched ON, the gate voltage is quickly increased to the threshold level of the MOSFET. Once at this level, the current begins to slew as the gate voltage is slowly increased until the MOSFET becomes fully enhanced. Once it has reached this point, the gate is quickly increased to the full input voltage and $R_{DS(ON)}$ is minimized.

The ON/OFF states of the seven MOSFET switches are controlled by the EN/SET serial clock input. An internal control counter is clocked on the rising edges of the EN/SET pin and is decoded into 128 possible states of the MOSFET (see Table 1 and Table 2). The counter can be clocked at speeds up to 1MHz, but the count value is not latched until clocking has stopped and the EN/SET pin has remained high for the t_{LAT} timeout (approximate 1.15µs typical). The first rising edge of EN/SET enables the AAT4292 and is counted as the first clock.

There are four address switch bank in AAT4292, which is selected by the corresponding rising edges 33 to 36, after remaining the EN/SET high for the t_{LAT} timeout, then the clock number is latched and the relevant address switch bank (0 to 3) is asserted. Next, the corresponding rising edges of Data from 1 to 32 can be serial submitted, and closed by the EN/SET remaining high for t_{LAT} timeout. After the timeout t_{LAT}, the outputs status is updated accordingly.

The AAT4292 is disabled after the EN/SET pin has transitioned and remained in a logic low for t_{OFF} timeout, and the quiescent current drops to 0.1µA typically.

AS²Cwire Serial Interface

The ON/OFF states of the seven output channels are controlled by the EN/SET serial data input. An internal control counter is clocked on the rising edge of the EN/SET pin and is decoded into one of 128 possible states using a short address and data word (see Tables 1 and 2).

AS²Cwire relies on the number of rising edges of the EN/SET pin to address and load the registers, as illustrated in Figure 1. AS²Cwire latches data (1 to 32 edges) or address (33 to 36 edges) after the EN/SET pin has been held high for time t_{LAT}. The interface records rising edges of the EN/SET pin and decodes them into one of four addresses corresponding to the address table (Table 1), or 1 of 32 data settings corresponding to the switch code table (Table 2). The combined address and data is used to decode one of 128 possible switch states. Address and Data are differentiated by the number of rising edges on the EN/SET pin. 1 to 32 rising edges signifies Data, and 33 to 36 rising edges signifies Address. The counter can be clocked at speeds up to 1MHz, such that intermediate states are not visible. The first rising edge of EN/SET enables the IC and turns the switches OUT3-OUT7 on. Once the final clock cycle is received, the EN/SET pin is held high to maintain the device setting. The device is disabled after the EN/SET pin transitions to a logic low state for t_{OFF} timeout (approximate 1.3µs typical).

Address Code

Address Switch Bank Code	EN/SET Rising Edges
0	33
1	34
2	35
3	36

Table 1: AS²Cwire Address Table.

Data Code

Address	Data	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	OUT7	Address	Data	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	OUT7
0	1	on	on	on	on	on	on	on	2	1	off	on	on	on	on	on	on
	2	on	on	on	on	on	on	off		2	off	on	on	on	on	on	off
	3	on	on	on	on	on	off	on		3	off	on	on	on	on	off	on
	4	on	on	on	on	on	off	off		4	off	on	on	on	on	off	off
	5	on	on	on	on	off	on	on		5	off	on	on	on	off	on	on
	6	on	on	on	on	off	on	off		6	off	on	on	on	off	on	off
	7	on	on	on	on	off	off	on		7	off	on	on	on	off	off	on
	8	on	on	on	on	off	off	off		8	off	on	on	on	off	off	off
	9	on	on	on	off	on	on	on		9	off	on	on	off	on	on	on
	10	on	on	on	off	on	on	off		10	off	on	on	off	on	on	off
	11	on	on	on	off	on	off	on		11	off	on	on	off	on	off	on
	12	on	on	on	off	on	off	off		12	off	on	on	off	on	off	off
	13	on	on	on	off	off	on	on		13	off	on	on	off	off	on	on
	14	on	on	on	off	off	on	off		14	off	on	on	off	off	on	off
	15	on	on	on	off	off	off	on		15	off	on	on	off	off	off	on
	16	on	on	on	off	off	off	off		16	off	on	on	off	off	off	off
	17	on	on	off	on	on	on	on		17	off	on	off	on	on	on	on
	18	on	on	off	on	on	on	off		18	off	on	off	on	on	on	off
	19	on	on	off	on	on	off	on		19	off	on	off	on	on	off	on
	20	on	on	off	on	on	off	off		20	off	on	off	on	on	off	off
	21	on	on	off	on	off	on	on		21	off	on	off	on	off	on	on
	22	on	on	off	on	off	on	off		22	off	on	off	on	off	on	off
	23	on	on	off	on	off	off	on		23	off	on	off	on	off	off	on
	24	on	on	off	on	off	off	off		24	off	on	off	on	off	off	off
	25	on	on	off	off	on	on	on		25	off	on	off	off	on	on	on
	26	on	on	off	off	on	on	off		26	off	on	off	off	on	on	off
	27	on	on	off	off	on	off	on		27	off	on	off	off	on	off	on
	28	on	on	off	off	on	off	off		28	off	on	off	off	on	off	off
	29	on	on	off	off	off	on	on		29	off	on	off	off	off	on	on
	30	on	on	off	off	off	on	off		30	off	on	off	off	off	on	off
	31	on	on	off	off	off	off	on		31	off	on	off	off	off	off	on
	32	on	on	off	off	off	off	off		32	off	on	off	off	off	off	off
Address	Data	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	OUT7	Address	Data	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	OUT7
1	1	on	off	on	on	on	on	on	3	1	off	off	on	on	on	on	on
	2	on	off	on	on	on	on	off		2	off	off	on	on	on	on	off
	3	on	off	on	on	on	off	on		3	off	off	on	on	on	off	on
	4	on	off	on	on	on	off	off		4	off	off	on	on	on	off	off
	5	on	off	on	on	off	on	on		5	off	off	on	on	off	on	on
	6	on	off	on	on	off	on	off		6	off	off	on	on	off	on	off
	7	on	off	on	on	off	off	on		7	off	off	on	on	off	off	on
	8	on	off	on	on	off	off	off		8	off	off	on	on	off	off	off
	9	on	off	on	off	on	on	on		9	off	off	on	off	on	on	on
	10	on	off	on	off	on	on	off		10	off	off	on	off	on	on	off
	11	on	off	on	off	on	off	on		11	off	off	on	off	on	off	on
	12	on	off	on	off	on	off	off		12	off	off	on	off	on	off	off
	13	on	off	on	off	off	on	on		13	off	off	on	off	off	on	on
	14	on	off	on	off	off	on	off		14	off	off	on	off	off	on	off
	15	on	off	on	off	off	off	on		15	off	off	on	off	off	off	on
	16	on	off	on	off	off	off	off		16	off	off	on	off	off	off	off
	17	on	off	off	on	on	on	on		17	off	off	off	on	on	on	on
	18	on	off	off	on	on	on	off		18	off	off	off	on	on	on	off
	19	on	off	off	on	on	off	on		19	off	off	off	on	on	off	on
	20	on	off	off	on	on	off	off		20	off	off	off	on	on	off	off
	21	on	off	off	on	off	on	on		21	off	off	off	on	off	on	on
	22	on	off	off	on	off	on	off		22	off	off	off	on	off	on	off
	23	on	off	off	on	off	off	on		23	off	off	off	on	off	off	on
	24	on	off	off	on	off	off	off		24	off	off	off	on	off	off	off
	25	on	off	off	off	on	on	on		25	off	off	off	off	on	on	on
	26	on	off	off	off	on	on	off		26	off	off	off	off	on	on	off
	27	on	off	off	off	on	off	on		27	off	off	off	off	on	off	on
	28	on	off	off	off	on	off	off		28	off	off	off	off	on	off	off
	29	on	off	off	off	off	on	on		29	off	off	off	off	off	on	on
	30	on	off	off	off	off	on	off		30	off	off	off	off	off	on	off
	31	on	off	off	off	off	off	on		31	off	off	off	off	off	off	on
	32	on	off	off	off	off	off	off		32	off	off	off	off	off	off	off

Table 2: AS²Cwire Data Code Table.

Application Information

Thermal Considerations

The AAT4292 is designed to deliver continuous output load currents. Due to its high integration, care must be taken in designing for higher load conditions. If greater loads are required, outputs can be tied together to deliver higher power to a given load.

For the thermal calculation, assuming that the total current capability of the seven channels is I_{TOTAL}, each channel has the same current which is $I_{OUT} = \frac{I_{TOTAL}}{7}$, then

$$P_{TOTAL} = 7I_{OUT}^2R_{DS(ON)} = 7\left(\frac{I_{TOTAL}}{7}\right)^2R_{DS(ON)} = P_D - P_{DERATE}(T_A - 25)$$

Where:

P_D = 440mW when T_A = 25°C
P_{DERATE} = 4.4mW/°C
$R_{DS(ON)}$ = 1.7Ω (maximum) when V_{IN} = 5.0V

For example, at 25°C ambient, the AAT4292 power capability is P_{TOTAL} = 440mW, then $I_{TOTAL} \cong$ 1.35A at V_{IN} = 5.0V. The current capability for each channel is I_{OUT} = 192mA.

At 85°C ambient, the AAT4292 power capability is P_{TOTAL} = 440 - (85 - 25)4.4 = 176mW, then $I_{TOTAL} \cong$ 0.85A at V_{IN} = 5.0V. The current capability for each channel is I_{OUT} = 121mA.

Output Sequencing

If output sequencing is not necessary, then a pulse burst of 33 address clocks followed by 1 data clock will switch on all of the outputs simultaneously. Alternately, the OUT3 to OUT7 will be switched on simultaneously on the first rising edge of the EN/SET pin after the t_{LAT} timeout.

Output sequencing is accomplished via a series of pulses on the EN/SET pin. Each time a new pulse burst is asserted on EN/SET, the AAT4292 internal clock counter starts to count and sends the counted clock number to the register. After the t_{LAT} timeout, the internal clock counter is reset and waits for the next pulse burst. For example, to sequence the outputs in order from OUT1 to OUT7, seven clock bursts are input on the EN/SET pin. From Table 1 and Table 2, the first bust of 34 address clocks followed by 32 data clocks turns on OUT1. The next burst of 33 address clocks followed by 32 data clocks will add OUT2. Then the burst of 33 address clocks followed by 16 data clocks will add OUT3; the burst of 33 address clocks followed by 8 data clocks will add OUT4; the burst of 33 address clocks followed by 4 data clocks will add OUT5; the burst of 33 address clocks followed by 2 data clocks will add OUT6; the burst of 33 address clocks followed by 1 data clock will add OUT7. Likewise, the outputs can be turned on/off in any order by adding the corresponding clock bursts.

Input Capacitor

Normally, the input capacitor value could be ten times that of the total load capacitors. If the device outputs OUT1 to OUT7 have capacitor loads, depending on the load capacitor value, it is recommended that a 1µF to 10µF 0603 or 0805 ceramic capacitor be placed as close as possible between VIN and GND. For example, if the capacitor load at each output is 0.1µF, the Murata GRM21BR61C106K ceramic capacitor (10µF/16V/0805/X5R) or a similar capacitor could be used. This helps to provide a low impendence loop to charge the load capacitors during the MOSFET switches' turn-on transient and keep the V_{IN} voltage stable.

Timing Diagram

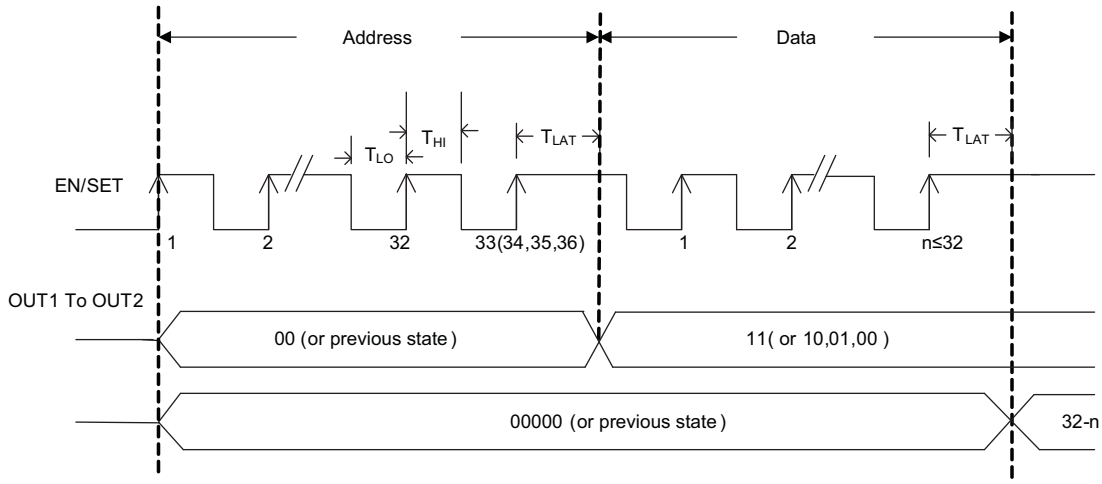


Figure 1: AS²Cwire Timing Diagram.

Application Circuits

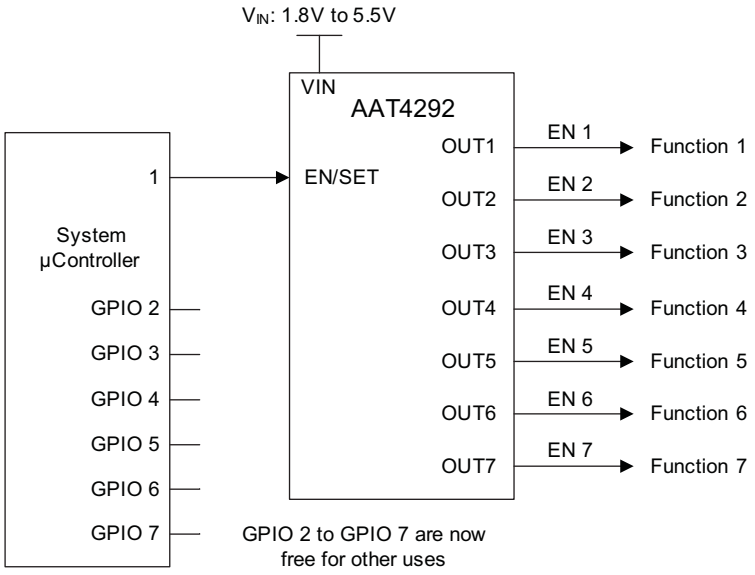


Figure 2: GPIO I/O Expander
(condense seven GPIO control lines to one).

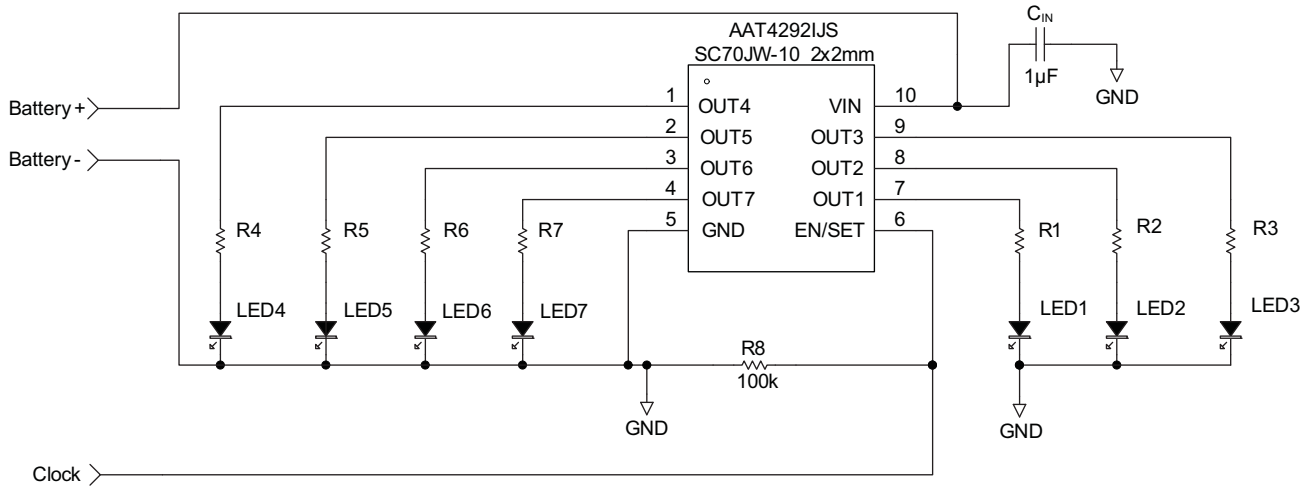


Figure 3: Keypad, Backlighting, or Fashion Lighting Control.

Evaluation Board Schematic

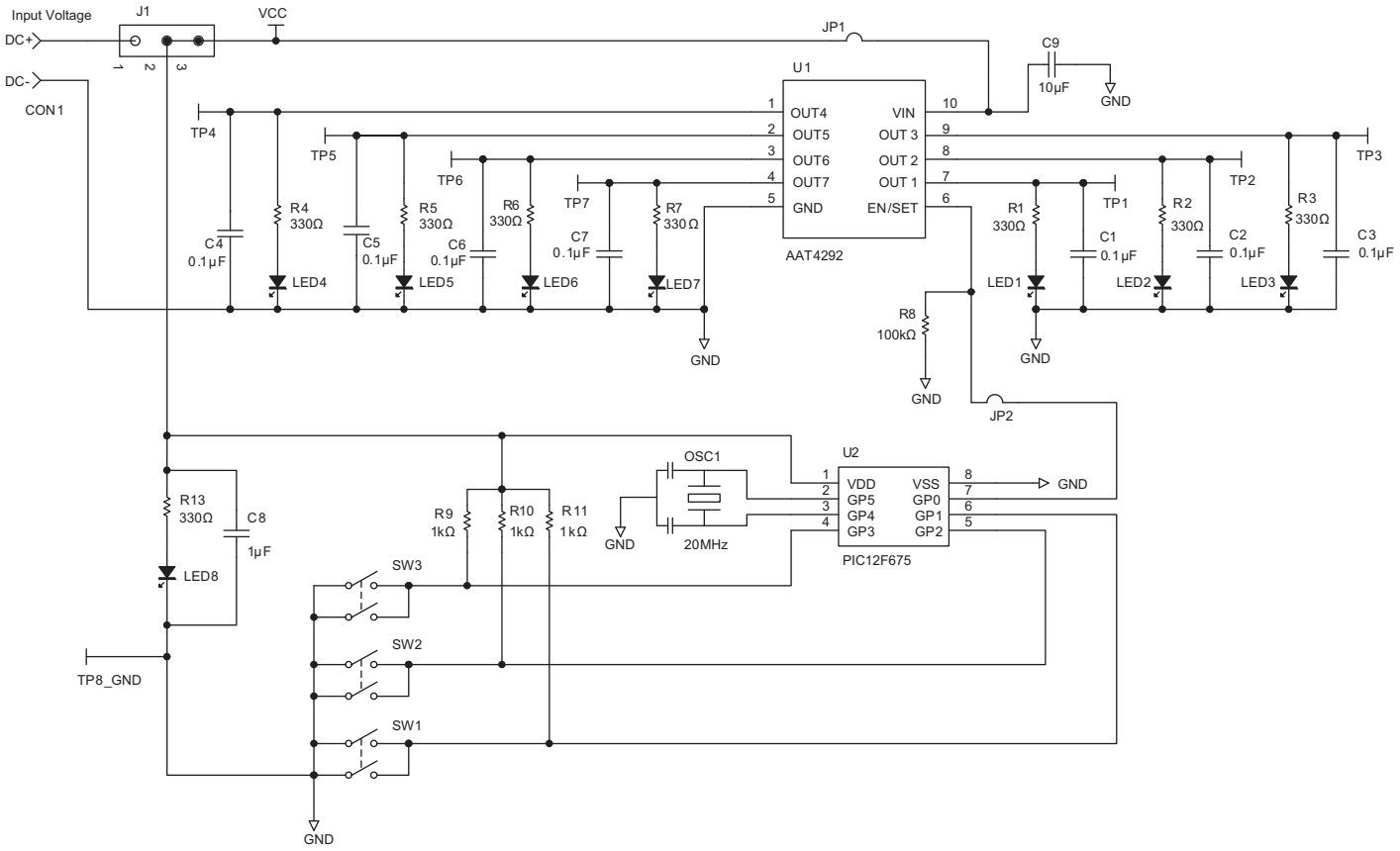


Figure 4: AAT4292 Evaluation Board Schematic.

Evaluation Board Layout

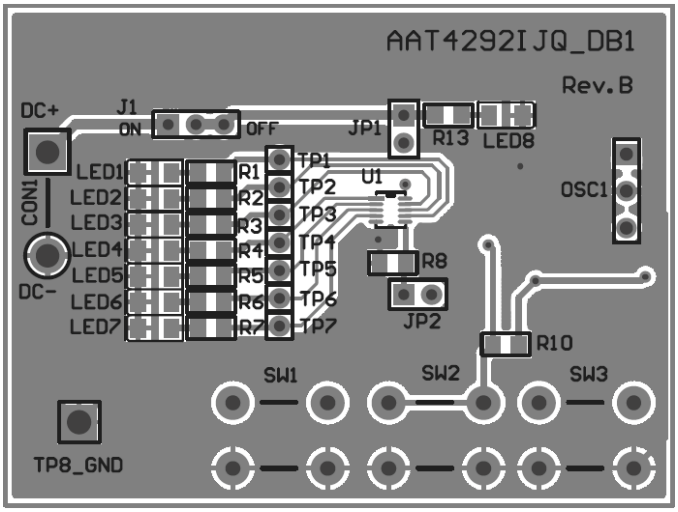


Figure 5: AAT4292 Evaluation Board Layout Top Layer (not to scale).

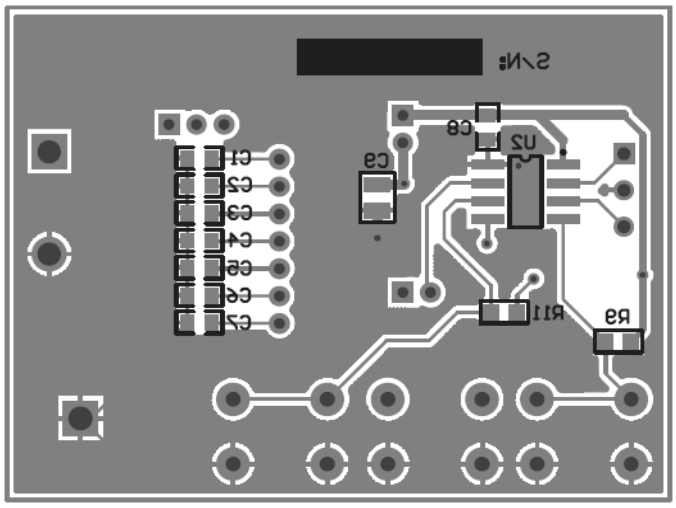


Figure 6: AAT4292 Evaluation Board Layout Bottom Layer (not to scale).

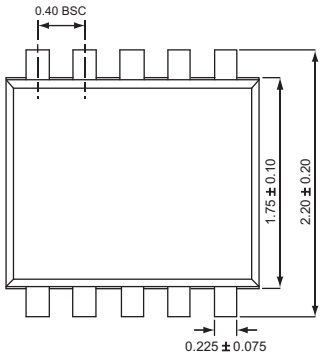
Ordering Information

Package	Marking[1]	Part Number (Tape & Reel)[2]
SC70JW-10	4WXYY	**AAT4292IJQ-T1**

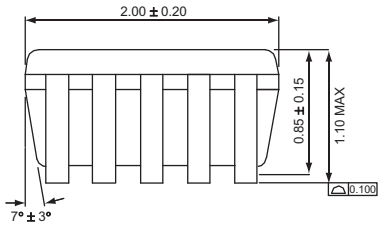
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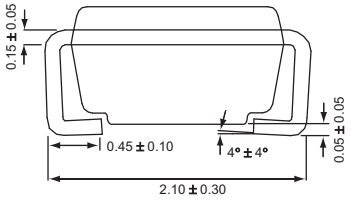
SC70JW-10



Top View



Side View



End View

All dimensions in millimeters.

1. XYY= assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.

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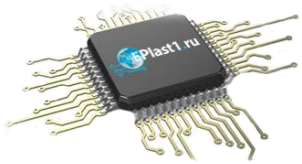
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