

1. General description

Planar passivated Silicon Controlled Rectifier (SCR) with sensitive gate in a SOT89 surface mountable plastic package. This SCR is designed to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

2. Features and benefits

- Sensitive gate
- High voltage capability
- Planar passivated for voltage ruggedness and reliability
- Surface mountable package

3. Applications

- Ground Fault Circuit Interrupters (GFCI)
- General purpose switching and phase control
- Ignition circuits, CDI for 2- and 3-wheelers
- Motor control-e.g. small kitchen appliances

4. Quick reference data

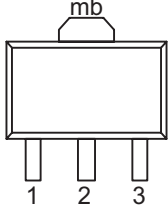

Table 1. Quick reference data

Symbol	Parameter	Conditions	Values	Unit
Absolute maximum rating				
V_{RRM}	repetitive peak reverse voltage		600	V
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{sp} \leq 109\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3	0.8	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(initial)} = 25\text{ °C}$; $t_p = 10\text{ ms}$; Fig. 4 ; Fig. 5	8	A
		half sine wave; $T_{j(initial)} = 25\text{ °C}$; $t_p = 8.3\text{ ms}$	9	A
T_j	junction temperature		125	°C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ °C}$; Fig. 7	15	-	100	μA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ °C}$; $R_{GK(\text{ext})} = 1\text{ k}\Omega$; Fig. 9	-	-	5	mA
V_T	on-state voltage	$I_T = 1.6\text{ A}$; $T_j = 25\text{ °C}$; Fig. 10	-	1.4	1.7	V
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 600\text{ V}$; $T_j = 125\text{ °C}$; $R_{GK} = 1\text{ k}\Omega$; exponential waveform	100	-	-	$\text{V}/\mu\text{s}$

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	A	anode		
3	K	cathode		
mb	mb	mounting base; connected to anode		

6. Ordering information

Table 3. Ordering information

Type number	Package Name	Orderable part number	Packing method	Small packing quantity	Package version	Package issue date
NCR100Q-6M	SOT89	NCR100Q-6MJ	Reel	1000	SOT89L	8-Mar-2019

7. Marking

Table 4. Marking codes

Type number	Marking codes
NCR100Q-6M	NCR1006M

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Values	Unit
V_{DRM}	repetitive peak off-state voltage		600	V
V_{RRM}	repetitive peak reverse voltage		600	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{sp} \leq 109\text{ }^{\circ}\text{C}$	0.51	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{sp} \leq 109\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	0.8	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_p = 10\text{ ms}$; Fig. 4 ; Fig. 5	8	A
		half sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_p = 8.3\text{ ms}$	9	A
I^2t	I^2t for fusing	$t_p = 10\text{ms}$; sine wave	0.32	A^2s
di_T/dt	rate of rise of on-state current	$I_G = 0.2\text{ mA}$	50	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current		1	A
V_{GM}	peak gate voltage		5	V
P_{GM}	peak gate power		2	W
$P_{G(AV)}$	average gate power	over any 20 ms period	0.1	W
T_{stg}	storage temperature		-40 to 150	$^{\circ}\text{C}$
T_j	junction temperature		125	$^{\circ}\text{C}$

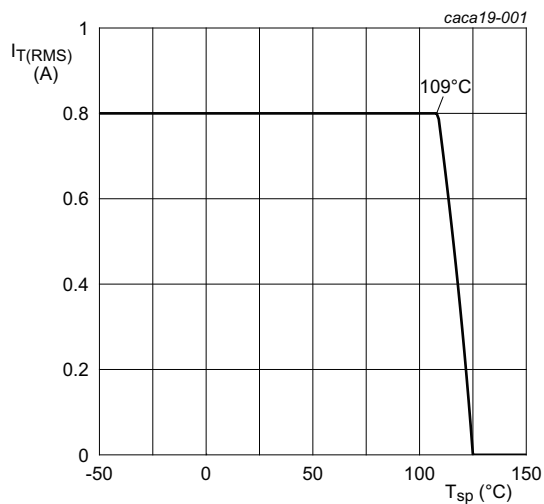
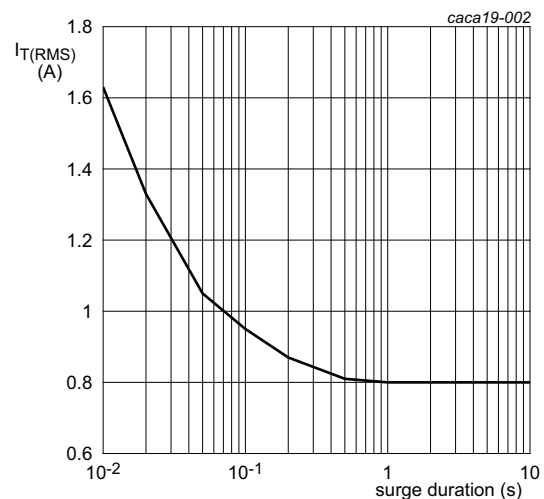
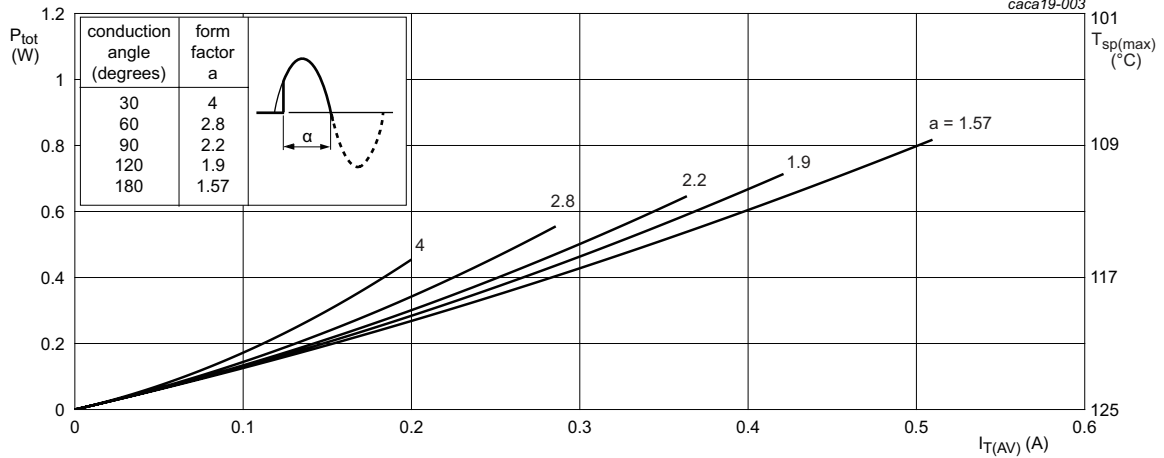


Fig. 1. RMS on-state current as a function of solder point temperature; maximum values



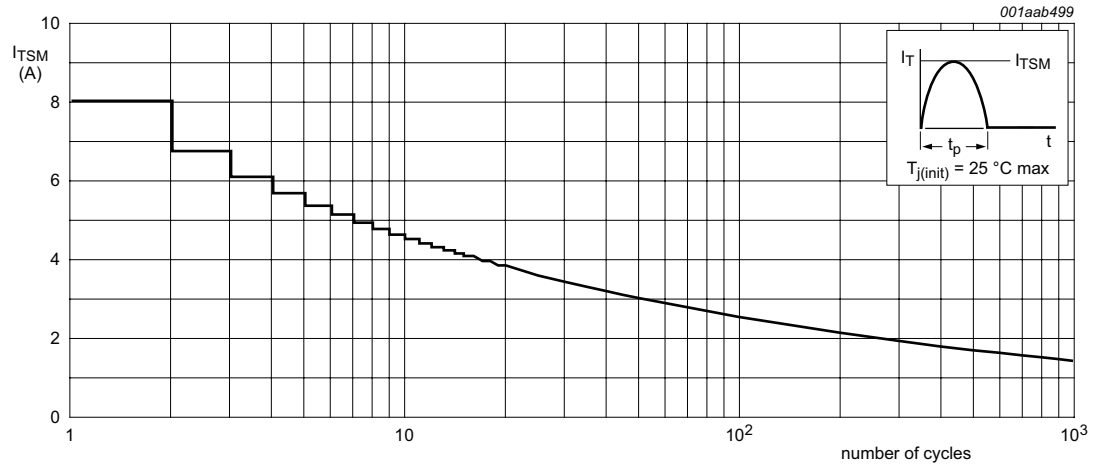
$f = 50\text{Hz}$; $T_{sp} = 109\text{ }^{\circ}\text{C}$

Fig. 2. RMS on-state current as a function of surge duration; maximum values



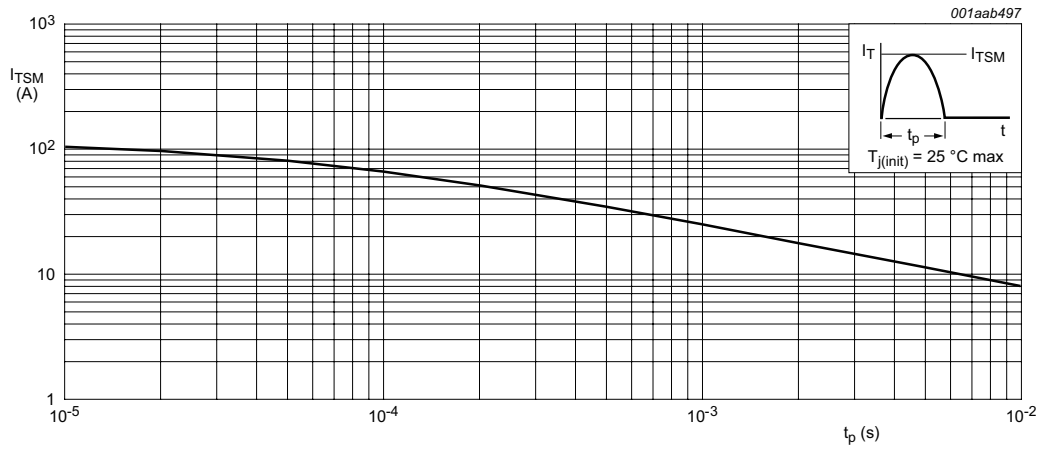
α = conduction angle
 a = form factor = $I_{T(RMS)} / I_{T(AV)}$

Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values



$f = 50$ Hz

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 10$ ms

Fig. 5. Non-repetitive peak on-state current as a function of pulse duration; maximum values

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Fig. 6	-	-	20	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	in free air	-	90	-	K/W

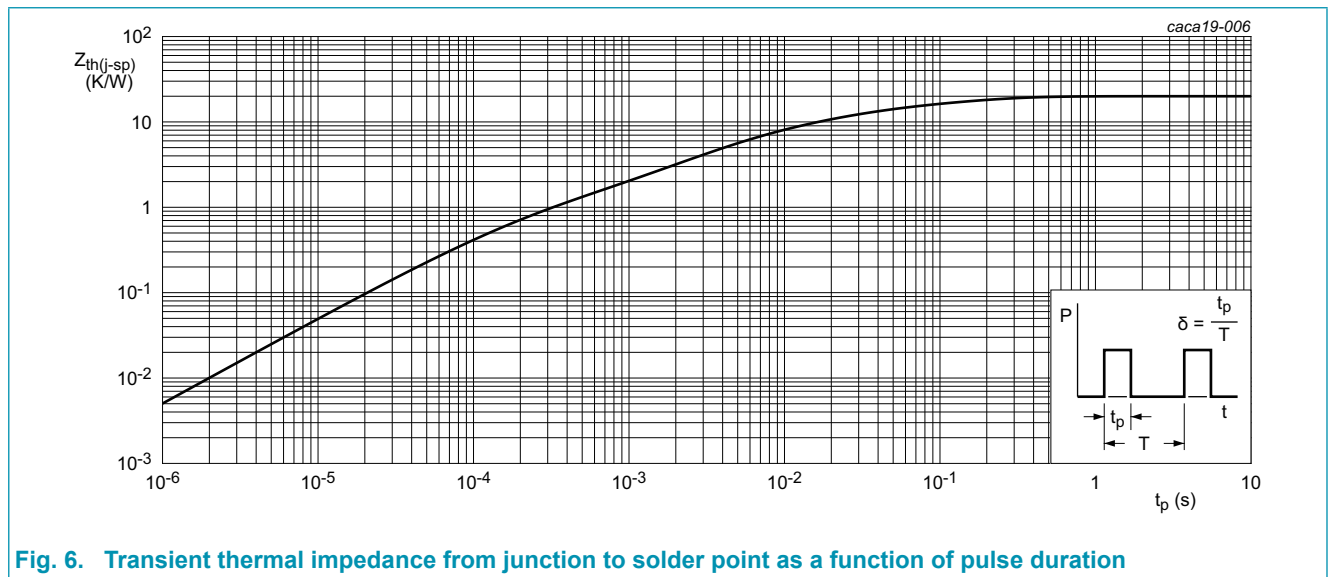


Fig. 6. Transient thermal impedance from junction to solder point as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7	15	-	100	μA
I_L	latching current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; $R_{GK(ext)} = 1\text{ k}\Omega$; Fig. 8	-	-	6	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; $R_{GK(ext)} = 1\text{ k}\Omega$; Fig. 9	-	-	5	mA
V_T	on-state voltage	$I_T = 1.6\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10	-	1.4	1.7	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 11	-	0.7	1	V
		$V_D = 600\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 125\text{ }^\circ\text{C}$	0.2	0.5	-	V
I_D	off-state current	$V_D = 600\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$	-	-	0.1	mA
I_R	reverse current	$V_D = 600\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$	-	-	0.1	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 600\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $R_{GK} = 1\text{ k}\Omega$; exponential waveform	100	-	-	V/ μs
t_{gt}	gate-controlled turn-on time	$I_{TM} = 2\text{ A}$; $V_D = 600\text{ V}$; $I_G = 1\text{ mA}$; $(dI_G/dt)_M = 0.1\text{ A}/\mu\text{s}$; $T_j = 25\text{ }^\circ\text{C}$	-	2	-	μs
t_q	commutated turn-off time	$V_{DM} = 402\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $I_{TM} = 1.6\text{ A}$; $V_R = 35\text{ V}$; $dV_D/dt = 2\text{ V}/\mu\text{s}$; $(dI_T/dt)_M = 30\text{ A}/\mu\text{s}$; $R_{GK(ext)} = 1\text{ k}\Omega$; ($V_{DM} = 67\%$ of V_{DRM})	-	100	-	μs

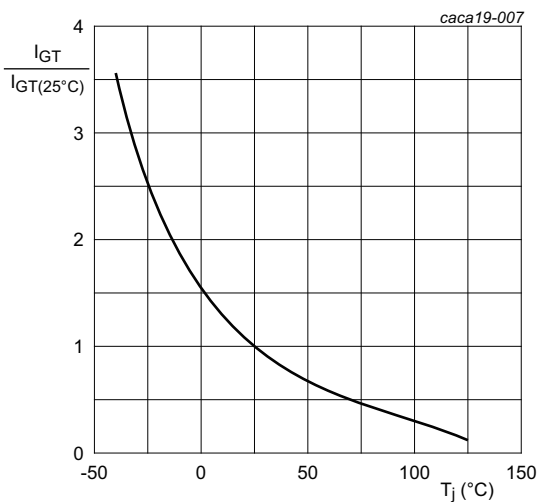


Fig. 7. Normalized gate trigger current as a function of junction temperature

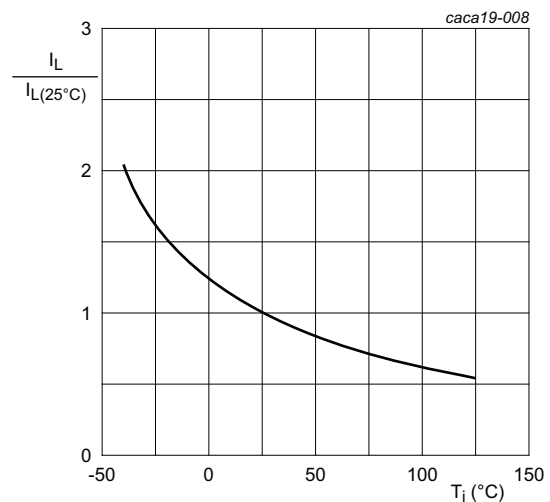


Fig. 8. Normalized latching current as a function of junction temperature

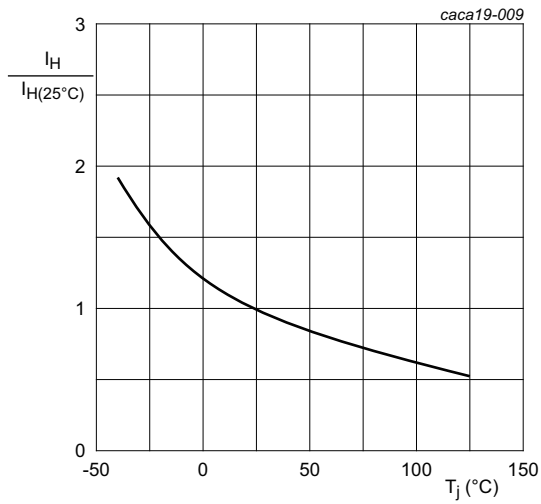
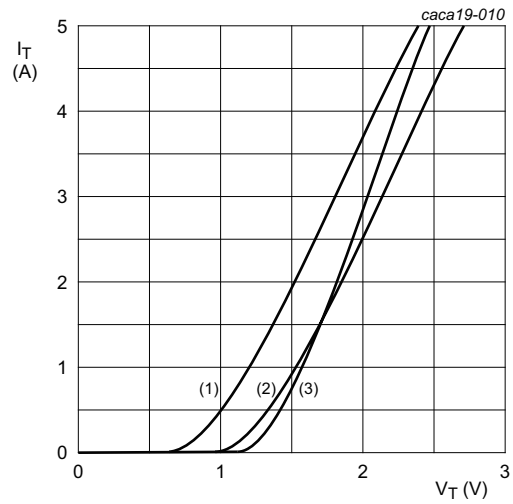


Fig. 9. Normalized holding current as a function of junction temperature



$V_o = 1.173 \text{ V}; R_s = 0.3437 \ \Omega$
 (1) $T_j = 125 \text{ }^\circ\text{C}$; typical values
 (2) $T_j = 125 \text{ }^\circ\text{C}$; maximum values
 (3) $T_j = 25 \text{ }^\circ\text{C}$; maximum values

Fig. 10. On-state current as a function of on-state voltage

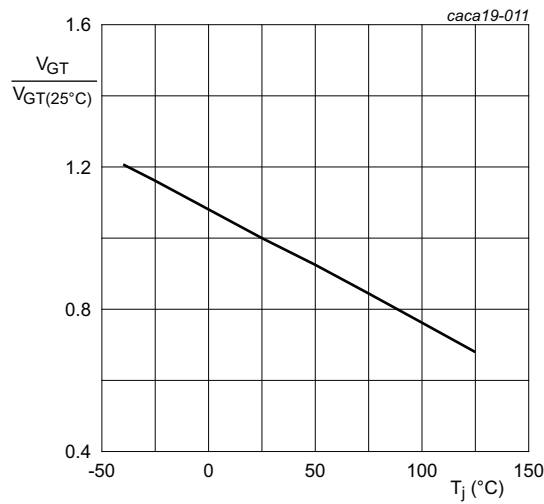
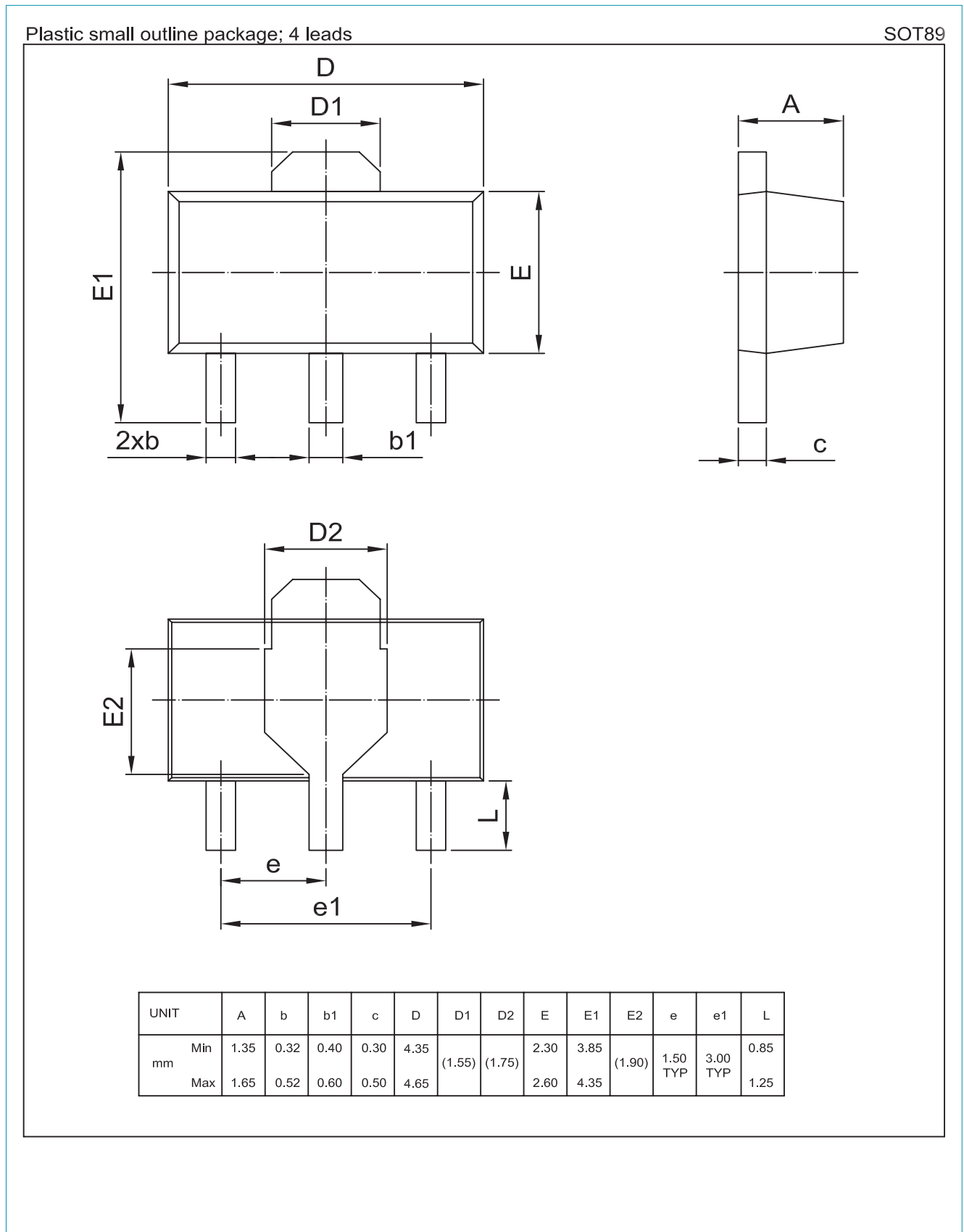


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

11. Package outline



12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.