FAIRCHILD SEMICONDUCTOR®

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FSA9480 — USB 2.0 Accessory Switch

Features

- Automatically Detects USB Accessories:
  - USB OTG Mode
  - CEA-936-A Car Kit and Chargers
  - Headsets
  - Video Cable
  - Factory Mode Cables
  - UART
  - TTY Converter
  - USB Data Cable
  - Chargers
- Auto-configures Connections with Independent Override Capability
- Integrated Audio Amplifier Generates Required Bias for CEA-936-A Car Kit Audio
- Automatic Low-Power Mode When No Accessory is Attached
- Integrated Over-Voltage and Over Current Protection FET on V_{BUS} for Fault Isolation
- Negative-Swing-Capable Audio Channel

Applications

- Cell Phones

Description

The FSA9480 is a USB port accessory detector and switch. The FSA9480 is fully controlled using I^2C™ and enables USB data, stereo and mono audio, video, microphone, and UART data to use a common connector port. It is designed for compatibility with CEA-936-A car kit adapters, USB 2.0 signaling, and USB OTG (on-the-go). The architecture is designed to allow audio signals to swing below ground so a common USB and headphone jack can be used for personal media players and portable peripheral devices.

The FSA9480 meets USB specification Rev. 2.0, micro-USB specification, and CEA-936-A.

Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package
FSA9480UCX	-40 to +85°C	N4	25-Lead, 2.1x2.1x0.625mm WLCSP Package

I^2C™ is a trademark of NXP B.V. Corporation.

Application Diagram

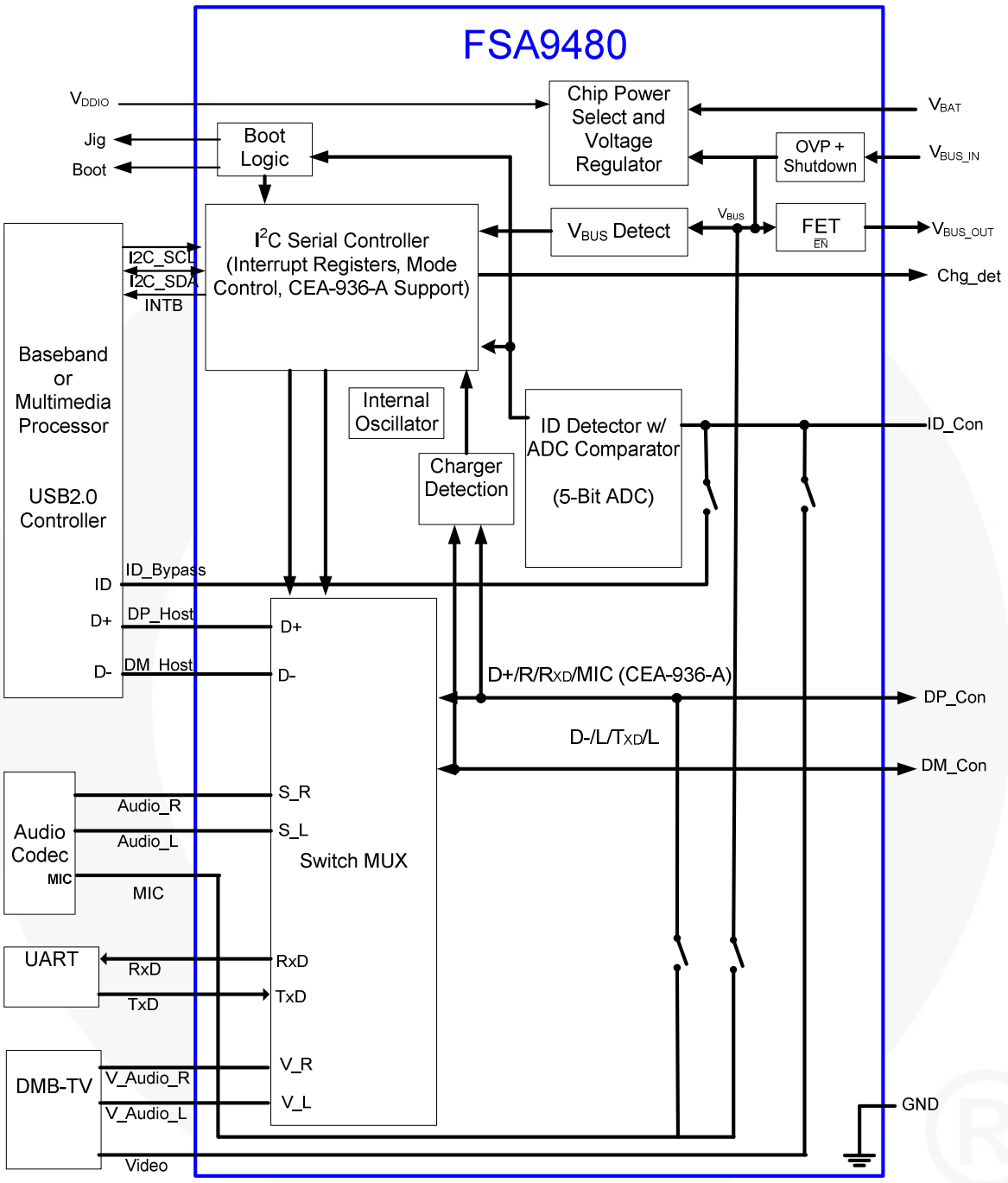


Figure 1. Typical Application

Block Descriptions

This block is used for factory-mode test and debug as described in Table 1.

Table 1. Boot Table

Factory Mode	ID Resistor	JIG	BOOT	Switch Connections
UART, Boot Off	523KΩ	LOW	LOW	*Table 3 - Accessory Auto Configuration Table*
USB, Boot On	301KΩ	LOW	HIGH	*Table 3 - Accessory Auto Configuration Table*
USB, Boot Off	255KΩ	LOW	LOW	*Table 3 - Accessory Auto Configuration Table*
UART, Boot On	619KΩ	LOW	HIGH	*Table 3 - Accessory Auto Configuration Table*
No Factory Mode	N/A	Hi-Z	LOW	*See Notes 1 and 2*

Notes:
1. JIG pin description: Low signals the phone to power up. When disabled this open drain floats and the pin is Hi-Z
2. BOOT pin description: This boot pin level directs the baseband processor which mode to boot in when the JIG box is attached, the JIG pin has been driven LOW, and the phone is powered up.

D+, D- Charger Detection

This block monitors D+ and D- to determine when a USB charger or dedicated charger is attached to the phone. The detection scheme follows the dedicated charger-detect algorithm as defined in the USB Implementers Forum Battery Charging Working Group specification titled *Battery Charging Specification* and as described in the CEA-936-A USB car kit specification. The FSA9480 distinguishes between a dedicated charger and USB charger and reports the appropriate type in the Device Type 1 Register. Whenever either type of charger is detected, the CHG_DET (I_{SET}) pin is pulled LOW.

Chip Power Select and Voltage Regulator

This block independently selects V_{BUS_IN} or V_{BAT} to power the FSA9480 and includes necessary LDO voltage regulators to provide stable power.

Valid ranges (for detecting and accepting supply) for:
V_{BAT}: 3.0V to 4.4V
V_{BUS}: 4.4V to 5.5V.

Voltage reference selection criteria:
- If V_{BUS} is present and in the valid range, the device takes its power from V_{BUS}. Otherwise, the device takes its power from V_{BAT} (if in valid range).
- If the device is operating on V_{BAT} and a valid V_{BUS} becomes available, the device switches to the V_{BUS} reference.

This block also accepts a V_{DDIO} voltage reference for baseband interface I/O signals.

OVP / OCP Shutdown Block

When V_{BUS} is less than 6.8V, this block allows the V_{BUS} supply to enter the chip power select voltage regulator block. For V_{BUS} greater than 7.2V, the input is disconnected, protecting the FSA9480 from excess voltage. This block is capable of withstanding continuous 28V in shutdown mode. Upon entering shutdown, the OVP_EN bit in the Interrupt 1 Register is set HIGH and an interrupt is sent to the baseband. The Over-Current Protection (OCP) feature limits current through the charger FET to ≤1.5A maximum. The FSA9480 automatically senses an over-current event, clamps the current, and reports to the baseband by asserting OCP_EN in the Interrupt 1 Register. OCP mode is only implemented when V_{BUS} is provided by the attached accessory. In PPD Mode *(see below)*, the FSA9480 does not limit current supplied by the phone.

V_{BUS} Detect and FET Blocks

This block monitors the status of the V_{BUS} pin. A valid V_{BUS} level is defined as V_{BUS} greater than 4.4V and less than 5.5V. When V_{BUS} is determined to be valid, the internal NMOS charging FET is enabled, allowing battery charging whenever a valid V_{BUS} is present. The charging FET is designed to limit inrush current to 100mA during enable to allow the voltage levels to stabilize during initial connection. This current limiting is automatic and designed per the requirements outlined in the *USB Battery Charging Specification*.

I^2C™ and Digital Core Block

This block includes a full I^2C slave controller. The I^2C slave fully complies with the I^2C specification version 2.1 requirements. This block also includes the FSA9480 chip master controller. The chip controller monitors commands sent to the FSA9480 via I^2C from the baseband and takes action. The FSA9480 digital core takes inputs from the various functional blocks within the FSA9480 and the I^2C commands received from the phone baseband and relays relevant status updates to the phone.

ID Detector with Analog Digital Converter (ADC) Block

This block monitors the ID pin for accessory attach and detach. After determining which accessory has been attached, the detector block reports this back to the digital core, which sends an interrupt to the baseband. Upon detecting changes in the ID pin voltage, the ADC also writes the ADC value bits in the ADC Register. The baseband processor can then read the I^2C registers and determine the appropriate action. The programmable wait time does not begin until after the baseband acknowledges the interrupt read. Figure 2 outlines the high-level accessory detection flow sequence for Samsung-specific accessories.

Accessory Detection Flow

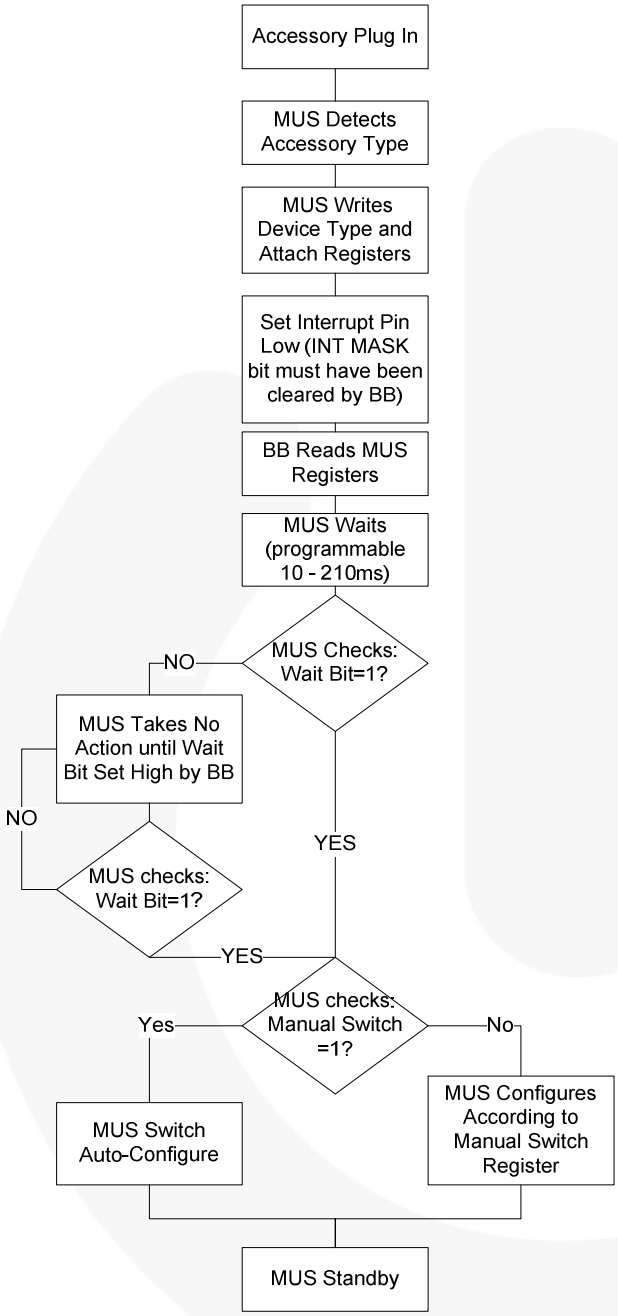


Figure 2. Accessory Detection Flow Chart (Except USB)

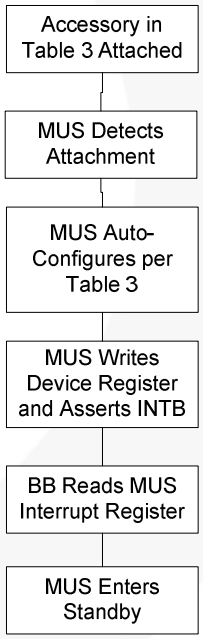


Figure 3. USB Detection Flow Chart

Note:

3. Figure 2 applies to all accessories except USB; see Figure 3 for the USB accessory detection flow.

Table 2. ADC Selection Table

Bit Number					Equivalent R_{ID} (KΩ)	Description
4	3	2	1	0		
0	0	0	0	0	**GND**	**USB OTG Mode**
0	0	0	0	1	2.000	Audio Send_End Button
0	0	0	1	0	2.604	Audio Remote S1 Button
0	0	0	1	1	3.208	Audio Remote S2 Button
0	0	1	0	0	4.014	Audio Remote S3 Button
0	0	1	0	1	4.820	Audio Remote S4 Button
0	0	1	1	0	6.030	Audio Remote S5 Button
0	0	1	1	1	8.030	Audio Remote S6 Button
0	1	0	0	0	10.030	Audio Remote S7 Button
0	1	0	0	1	12.030	Audio Remote S8 Button
0	1	0	1	0	14.460	Audio Remote S9 Button
0	1	0	1	1	17.260	Audio Remote S10 Button
0	1	1	0	0	20.500	Audio Remote S11 Button
0	1	1	0	1	24.070	Audio Remote S12 Button
0	1	1	1	0	28.700	Reserved Accessory #1
0	1	1	1	1	34.000	Reserved Accessory #2
1	0	0	0	0	40.200	Reserved Accessory #3
1	0	0	0	1	49.900	Reserved Accessory #4
1	0	0	1	0	64.900	Reserved Accessory #5
1	0	0	1	1	80.070	Audio Device Type 2
1	0	1	0	0	102.000	Phone Powered Device
1	0	1	0	1	121.000	TTY Converter
1	0	1	1	0	150.000	UART Cable
1	0	1	1	1	200.000	CEA-936-A Type-1 Charger(4)
1	1	0	0	0	255.000	Factory Mode Boot OFF-USB
1	1	0	0	1	301.000	Factory Mode Boot ON-USB
1	1	0	1	0	365.000	Audio/Video Cable
1	1	0	1	1	442.000	CEA-936-A Type-2 Charger(4)
1	1	1	0	0	523.000	Factory Mode Boot OFF-UART
1	1	1	0	1	619.000	Factory Mode Boot ON-UART
1	1	1	1	0	1000.070	Audio Device Type 1 with Remote(4)
					1002.000	Audio Device Type 1 / Only Send-End(5)
1	1	1	1	1	Open	USB Mode, Dedicated Charger or Accessory Detach

Notes:

4. Chargers must provide a valid V_{BUS} for the FSA9480 to report them to the phone baseband.
5. Audio devices with remote and audio device / only send end are reported as audio in the Device Type 1 Register. The FSA9480 auto-configures in Audio Mode, as described in Table 3.

Switch MUX Block

The switch MUX block contains an I^2C controlled DP4T multiplexer with dedicated paths for high-speed USB, audio R/L, TV R/L, and UART signaling. A summary of the switch auto configuration connections for the various states is shown in Table 3.

Table 3. Accessory Auto Configuration Table

Configuration Type		V_{BUS}	DP	DM	ID	BOOT	JIG	CHG_DET (I_{SET})
Audio Type 1		MIC	Audio_R	Audio_L	Key Press Monitor	LOW	Hi-Z	Hi-Z
Audio Type 2		Chg FET Closed	RxD	TxD	(7)	LOW	Hi-Z	Hi-Z
TTY		MIC	Audio_R		(7)	LOW	Hi-Z	Hi-Z
UART		(6)	RxD	TxD	(7)	LOW	Hi-Z	Hi-Z
USB		Chg FET Closed	DP_Host	DM_Host	IDBP	LOW	Hi-Z	Hi-Z
USB Charger		Chg FET Closed	DP_Host	DM_Host	IDBP	LOW	Hi-Z	Low
A/V Cable		(6)	V_Audio_R	V_Audio_L	Video	LOW	Hi-Z	Hi-Z(8)
Dedicated Charger, Car Kit Type I & II Chargers		Chg FET Closed	Open	Open	NA	LOW	Hi-Z	Low
Phone Powered Device (PPD)		Chg FET Closed	Audio_R	Audio_L	(7)	LOW	Hi-Z	Hi-Z
Factory Mode Jig: UART	Boot_On	Chg FET Open	RxD	TxD	(7)	HIGH	LOW	Hi-Z
	Boot_Off	Chg FET Open	RxD	TxD	(7)	LOW	LOW	Hi-Z
Factory Mode Jig: USB	Boot_On	Chg FET closed	DP_Host	DM_Host	(7)	HIGH	LOW	Hi-Z
	Boot_Off	Chg FET closed	DP_Host	DM_Host	(7)	LOW	LOW	Hi-Z

Notes:

6. If V_{BUS} is valid, the charger FET is closed; otherwise, the charger FET is open.
7. ID is monitored by ADC for change of state.
8. Unless V_{BUS} is valid, in which case, a charger adapter has been added and CHG_DET is enabled.

Mode Descriptions

Initialization

On initial power up, all register bits are initialized to their default condition, as defined in the I^2C register map. During initialization, all switch paths are open. Immediately after initializing, all registers transition to Standby/IDLE Mode.

V_{DDIO} Reset Mode

While in active mode, the FSA9480 is reset by the falling edge of the V_{DDIO} signal pin as the V_{DDIO} level transitions from HIGH to LOW. In this case, the FSA9480 automatically resets to its initialization state. All register bits are initialized to their default condition, as defined in the I^2C register map. Immediately following V_{DDIO} reset all switch paths are open and the FSA9480 transitions to Standby/IDLE Mode. The FSA9480 enters Standby/Idle Mode after the initial reset, while the V_{DDIO} pin remains LOW. Immediately after the V_{DDIO} level returns to a High and the Interrupt Mask is cleared the FSA9480 reports any activity detected while in Standby/Idle Mode.

I^2C Reset Mode

The FSA9480 can also be reset by driving both the SDA and SCL signal lines LOW for 30ms. In this case, the FSA9480 automatically resets all registers to default condition, as defined in the I^2C register map. Immediately following I^2C reset, all switch paths are open and FSA9480 transitions to Standby/IDLE mode. *See Figure 5 for detailed timing for I^2C Reset Mode.*

Standby / IDLE

In this state, no accessory is attached. This state is connected to all other states. During this state, the device is in a power-down mode with a minimal set of functions running. The ID detector continuously monitors the ID pin for accessory attach. Upon accessory attach, the FSA9480 transitions to the appropriate mode based on the accessory.

Charger Mode

When any of the possible charger types are attached, the FSA9480 closes the FET switch and CHG_DET (I_{SET}) is asserted LOW. When CHG_DET is asserted LOW this signals the phones charger IC to enable high-current mode. When CHG_DET is Hi-Z, the charger IC defaults to low-current charge mode.

USB 2.0 and USB OTG Modes

When USB2.0 cable is attached, the FSA9480 configures the switch MUX block according to Table 3. The charger FET is closed.

Dead Battery / No Battery Mode

When no battery or a dead battery is present, the FSA9480 disables the following pins to Hi-Z: INTB, I^2C_SDA, I^2C_SCL, Jig, Boot, R_{XD}, T_{XD}, and CHG_DET.

CEA-936-A Car Kit

Upon initial detection of a CEA-936-A car kit accessory, the FSA9480 detects and reports a car kit accessory attachment. The FSA9480 then initiates the car kit signaling protocol, as described in the CEA-936-A specification. Accordingly, the FSA9480 initializes in UART mode, as described section 7.2.2 of the CEA-936-A specification. The FSA9480 implements the four-wire protocol required for state transitions within the CEA-936-A specification. The baseband processor directs the FSA9480, using the mode bits in the Car Kit Register, to signal the FSA9480 to change modes within the car kit protocol. The phone generates the USB, UART, and audio signals and the FSA9480 multiplexes the appropriate signal out to the attached car kit device. The FSA9480 performs all handshaking necessary with the attached car kit accessory and automatically configures the switch MUX based on the mode setting called for by the baseband processor. Car Kit Audio Mode requires a 1.2V bias applied to the audio signal. The FSA9480 contains a special audio path that provides a 1.2V bias to the Audio_R and Audio_L channels when in Car Kit Audio Mode. To achieve the proper bias, the FSA9480 incorporates a separate car kit audio path, containing two unity gain amplifiers. The FSA9480 also uses these audio amplifiers to implement the Car Kit Data During Audio (DDA) Mode. While in DDA mode, the phone must limit the audio signal being driven through the FSA9480 to amplitude no greater than 1V, peak to peak.

Phone Powered Device Mode (PPD)

In Phone Power Device (PPD) Mode, the cell phone provides power to the attached accessory through the charger FET. In this mode, the charger FET is not closed until after the wait time has expired; at which time, the phone should have already biased its output voltage level on the V_{BUS} pin. The phone should never source more than 10mA through the FSA9480 charger FET while in PPD mode. When in PPD mode, the charger FET provides a current path out of the phone to the PPD. There is no inrush current limiting or OCP protection provided by the charger FET when the FSA9480 is in PPD Mode.

Audio Modes

When any of the compatible headsets are attached, the FSA9480 configures as described in Table 3. The FSA9480 is compatible with Samsung headphones that include a remote-control feature. When in Audio Mode, the FSA9480 continuously monitors for remote-control button presses and reports any presses back to the baseband. Figure 15 illustrates the headset with remote basic circuit; Table 4 provides resistor values.

Audio Device Type-1 accessories are passive devices with only one switch configuration per device. They may or may not include a remote controller.

Audio Device Type-2 devices include a built-in UART controller and the FSA9480 auto configures with UART switch paths connected, as described in Table 3. These devices include a remote controller. After initial configuration in UART Mode, the baseband may change the FSA9480 switch mode configuration by writing any of the following bit patterns in the Car Kit Status Register mode bits: 000, 001, 100, 101. While an audio type-2 accessory is attached, it is possible for the baseband to signal changes in switch configuration from any mode to any mode until device detach is detected. While in DDA Mono (100) mode, the FSA9480 DDA circuitry is activated, allowing data to be sent and received during audio transmission between the resident UART transceivers in the phone and the audio type-2 device. The FSA9480 DDA audio scheme follows that of the CEA-936-A specification as implemented in the car kit mode of the FSA9480. Other than implementing the DDA transmission and reception scheme in CEA-936-A, the FSA9480 does not implement any car kit protocols or state machines while in Audio Device Type-2 Mode. In DDA Mode, the phone must limit the audio signal driven through the FSA9480 to amplitude no greater than 1V, peak to peak.

Factory Modes

Factory Modes are initiated with the attachment of a Samsung proprietary JIG Box and are used for phone assembly and testing. The Factory Mode attach procedure is slightly different from the standard accessory attach flow. The primary difference is that the FSA9480 automatically configures the switch paths as soon as a Factory Mode accessory is attached and V_{DDIO} is present. This is unique in that the FSA9480 does not wait for an I^2C read acknowledge from the baseband and does not employ the switch wait timer. A second difference is that, in this mode, the JIG pin is driven LOW even if the VDDIO pin is LOW. Figure 4 provides the attach flow for the JIG Box accessory.

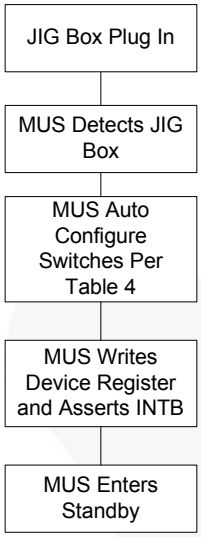


Figure 4. JIG Box Detection Flow

I²C Manual Reset Timing

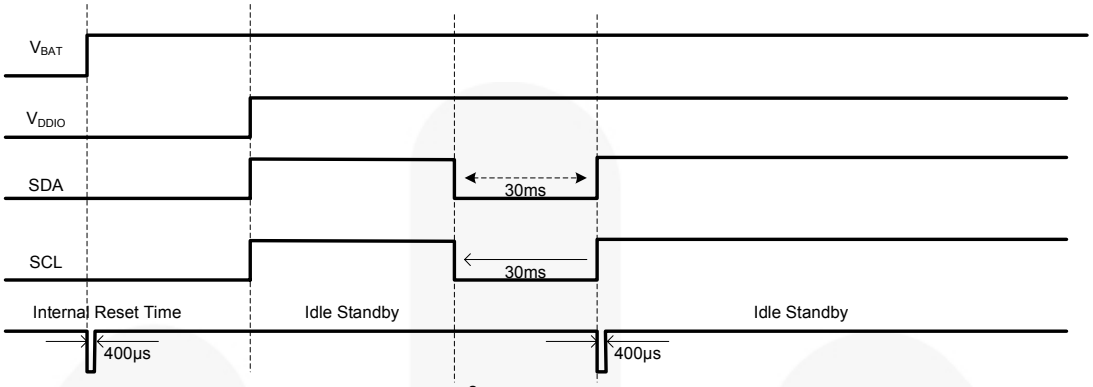


Figure 5. I²C Reset Mode Timing

Interrupt Operation Description

The FSA9480 follows the Interrupt guidelines as described in the Samsung Interrupt Definition and Default Path specification Rev 0.1 released July 15 2008. The baseband processor recognizes interrupt signals by observing the falling edge of the INTB signal in a high-to-low transition. During the phone power-up sequence, V_{DDIO} reset or I^2C reset the INTB pin is masked on initialization and defaults LOW. After the INTB mask is cleared by the baseband processor, the INTB pin is HIGH in preparation of a future interrupt. If the interrupt mask bit in the I^2C Control Register is written HIGH when the system is already powered up, the INTB remains HIGH until the INTB mask is cleared. If an interruptible event occurs while the INTB pin is masked, the FSA9480 changes the appropriate register value and waits until the INTB mask bit is cleared, plus the switch wait time before signaling an interrupt to the baseband. Figure 6 illustrates the interrupt timing for the FSA9480 during initial power up. Figure 7 shows the INTB behavior during a V_{DDIO} reset. Figure 8 illustrates the INTB timing when the INT Mask bit is written by the baseband using I^2C commands.

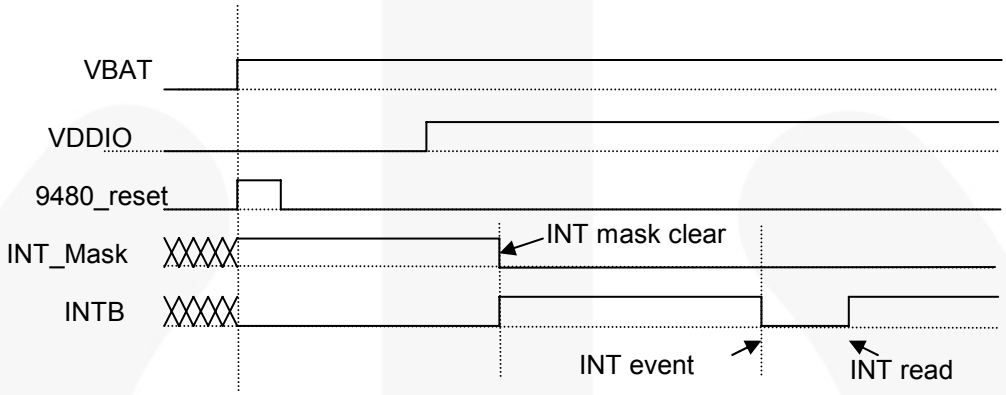


Figure 6. Power-Up Interrupt Timing Diagram

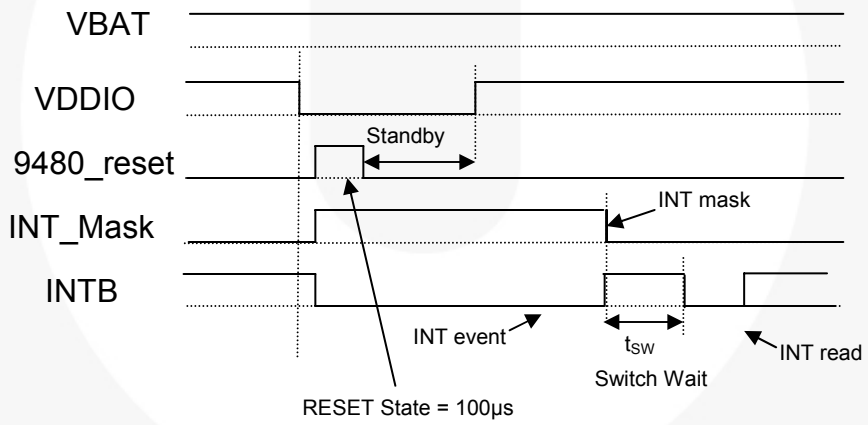


Figure 7. VDDIO Reset Interrupt Timing Diagram

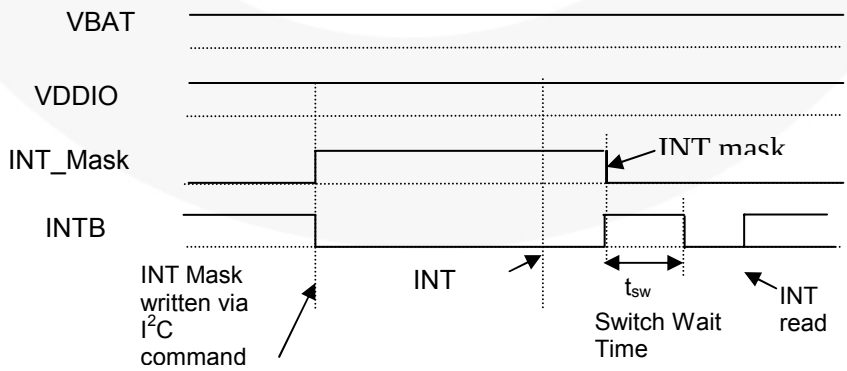


Figure 8. INT Mask via I^2C Command Interrupt Timing Diagram

Device Attach Timing Diagrams

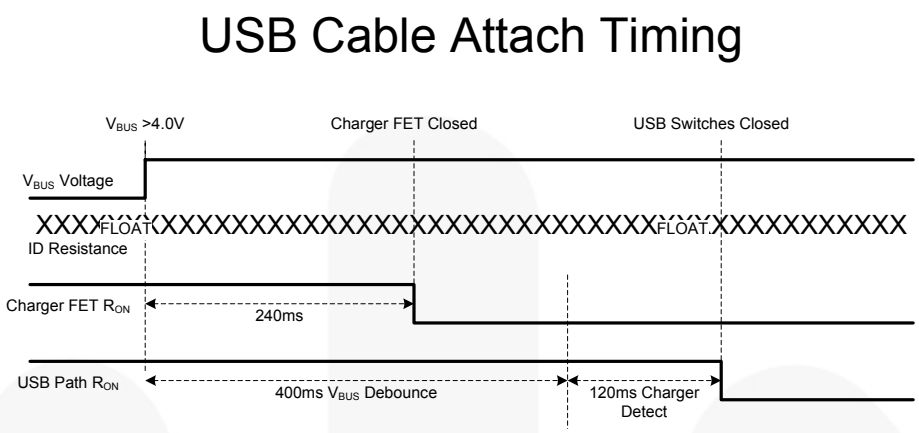


Figure 9. USB Cable Attach Timing Diagram

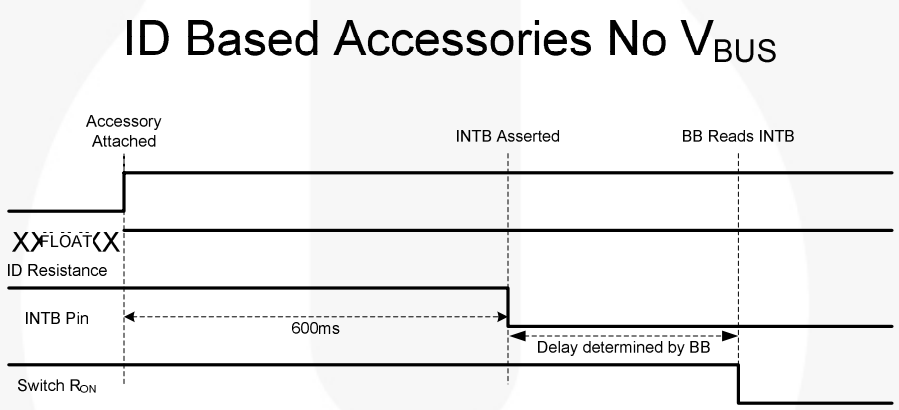


Figure 10. ID Based Accessories Attach Timing

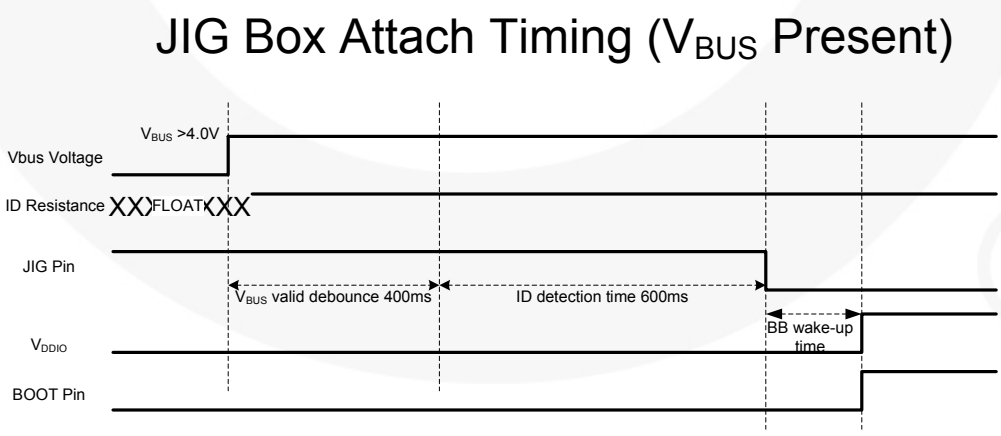


Figure 11. JIG Box Attach Timing (V_{BUS} Present)

Device Attach Timing Diagrams (Continued)

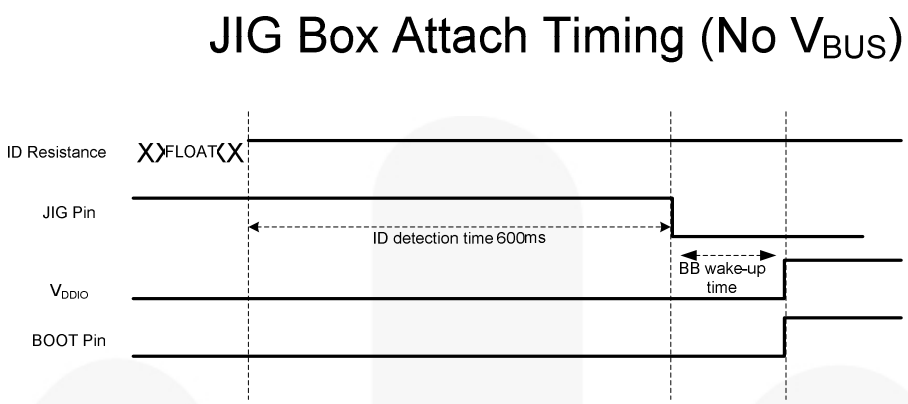


Figure 12. JIG Box Attach Timing (No V_{BUS})

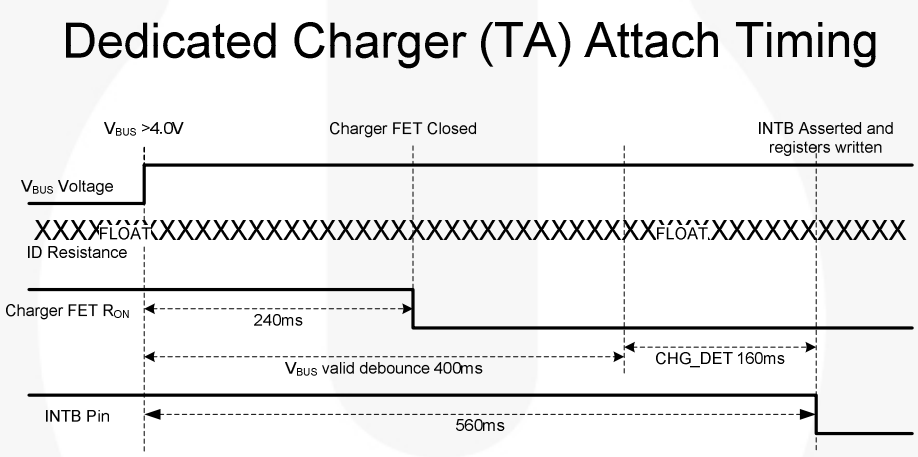


Figure 13. Dedicated Charger (TA) Attach Timing

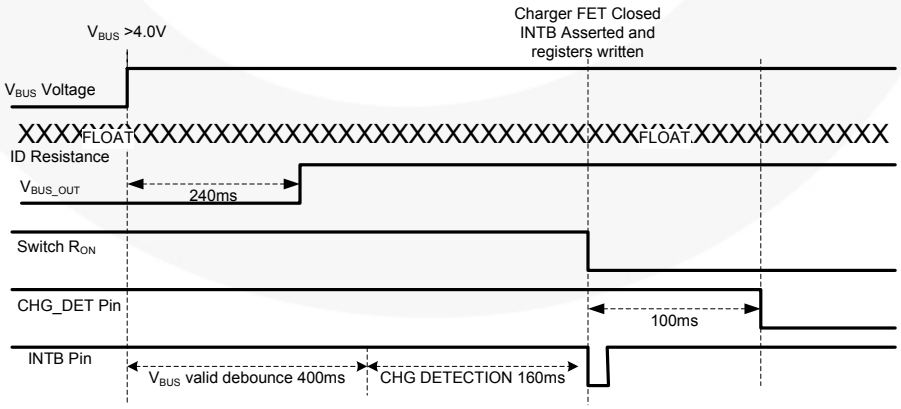


Figure 14. USB Charging Host Port Attach Timing

Audio Type 1 and 2 Remote Control Configuration

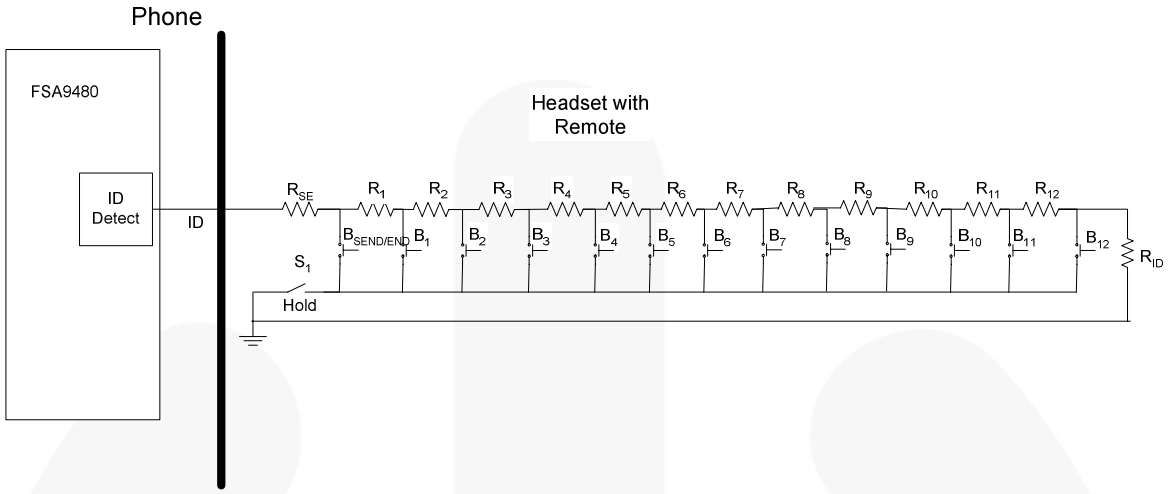


Figure 15. Stereo Headset with Remote Configuration

Table 4. Remote Control Resistor Table (1% Resistor Values)

Switch and Resistor Number	Resistor Value	Resistor Number	Resistor Value
RSE	2KΩ	B7, R7	2KΩ
B1, R1	0.604KΩ	B8, R8	2KΩ
B2, R2	0.604KΩ	B9, R9	2.43KΩ
B3, R3	0.806KΩ	B10, R10	2.8KΩ
B4, R4	0.806KΩ	B11, R11	3.24KΩ
B5, R5	1.21KΩ	B12, R12	3.57KΩ
B6, R6	2KΩ	RID	976KΩ (Audio Type 1)
			56KΩ (Audio Type 2)

Key Press Timing Diagrams

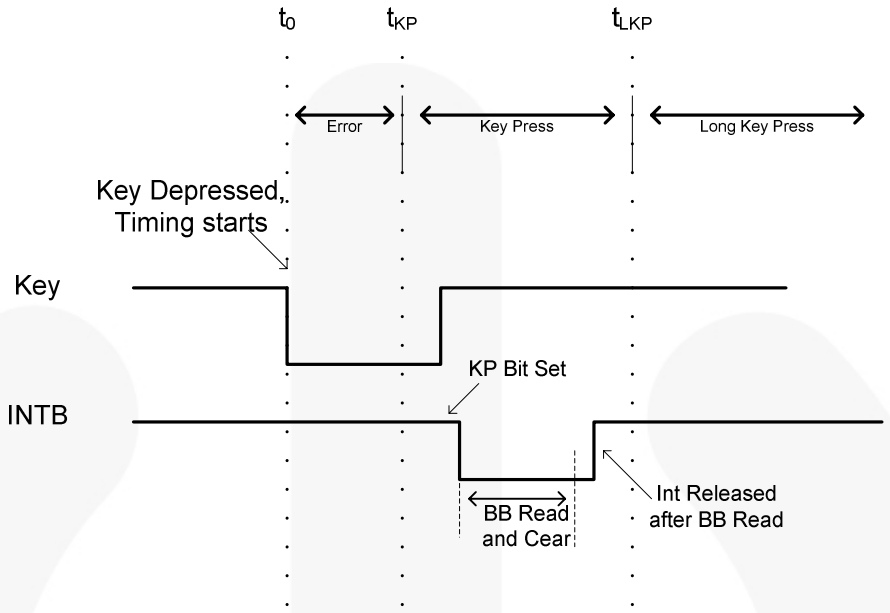


Figure 16. Regular Key Press Timing Diagram

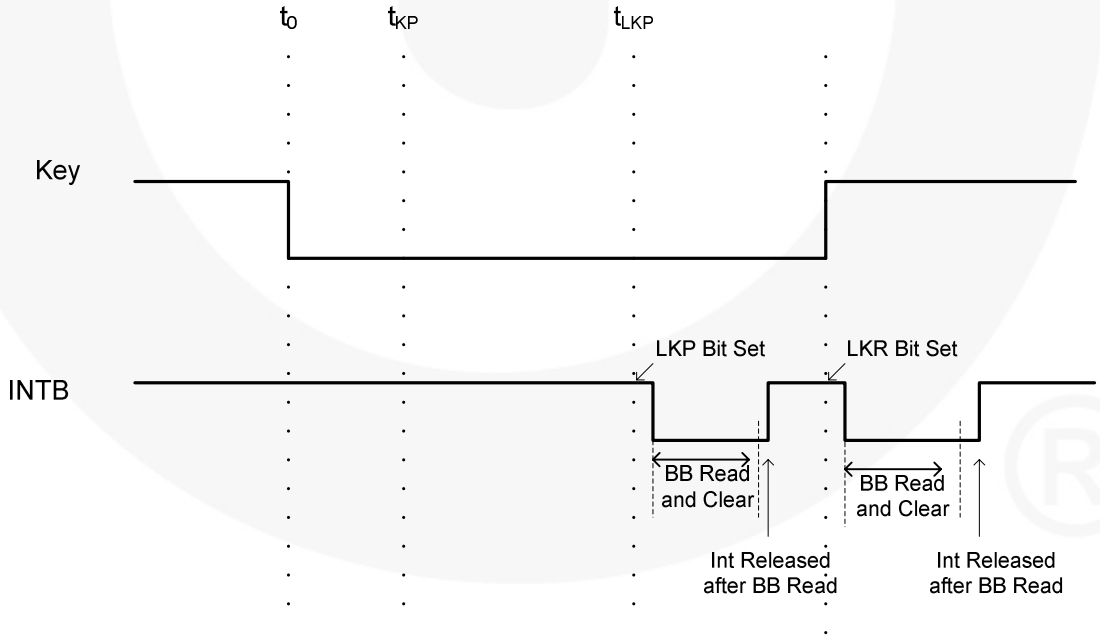


Figure 17. Long Key Press Timing Diagram

Marking Information

Z = Assembly Plant Code

X = Year

Y = Work Week

KK = Lot Trace Code

N4 = Product Identifier

Figure 18. Top Mark with Pin A1 Orientation

Pin Configuration

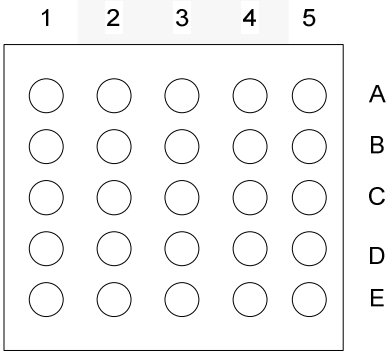


Figure 19. 25-Pin, WLCSP Pin Assignments (Top Through View)

Pin Map

	Column 1	Column 2	Column 3	Column 4	Column 5
Row A	INTB	VDDIO	CHG_DET	VBUS_OUT	VBUS_IN
Row B	DP_Host	I^2C_SDA	Audio_L	MIC	DM_CON
Row C	DM_Host	I^2C_SCL	V_Audio_L	Audio_R	DP_CON
Row D	VBAT	ID_Bypass	V_Audio_R	Video	ID_CON
Row E	RxD	TxD	BOOT	JIG	GND

Pin Descriptions

Name	Pin #	Type	Default State	Description
USB Interface				
DP_Host	B1	Signal Path	Open	D+ signal, dedicated USB port to be connected to the resident USB transceiver on the phone
DM_Host	C1	Signal Path	Open	D- signal, dedicated USB port to be connected to the resident USB transceiver on the phone
ID_Bypass	D2	Signal Path	Open	USB ID pin bypass allows the FSA9480 to pass the ID signal pin through to the resident phone USB controller when a USB accessory is attached
Audio Interface				
Audio_L	B3	Signal Path	Open	Left audio channel from phone audio-out codec
Audio_R	C4	Signal Path	Open	Right audio channel from phone audio-out codec
MIC	B4	Signal Path	Open	Connected to the phone audio codec MIC input pin
Video Interface				
Video	D4	Signal Path	Open	Input signal driven by the phone DMB video-out signal
V_Audio_L	C3	Signal Path	Open	Left audio channel from TV audio out
V_Audio_R	D3	Signal Path	Open	Right audio channel from TV audio out
UART Interface				
TxD	E2	Signal Path	Open	Tx connection from resident UART transceiver on the phone
RxD	E1	Signal Path	Open	Rx connection from resident UART transceiver on the phone
Factory Interface				
Jig	E4	Open-Drain Output	Hi-Z	Output control signal driven by the FSA9480; used by the processor for Samsung factory test modes
Boot	E3	Push-Pull Output	LOW	Output control signal driven by the FSA9480, used by the processor for Samsung factory test modes
Power Interface				
V_{BAT}	D1	Power	N/A	Input voltage supply pin to be connected to the phone battery output
V_{BUS_OUT}	A4	Power	N/A	Output voltage supply pin to be connected to the source voltage pin on the charger IC
V_{DDIO}	A2	Power	N/A	Input baseband interface I/O supply pin
CHG_DET (I_{SET})	A3	Open-Drain Output	Hi-Z	Open-drain I/O pin, active LOW, used to signal charger IC that a charger has been attached

Continued on the following page…

Pin Descriptions (Continued)

Name	Pin #	Type	Default State	Description
Connector Interface				
V_{BUS_IN}	A5	Power	N/A	Input voltage supply pin; connect to the V_{BUS} pin of the USB connector
GND	E5	Power	N/A	Ground
ID_CON	D5	Signal Path	Open	Connected to the USB connector ID pin; depending on the FSA9480 state, this pin can share ID or video signals
DP_CON	C5	Signal Path	Open	Connected to the USB connector D+ pin; depending on the FSA9480 signaling mode, this pin can share D+, S_R, V_R, Rxd, or MIC signals
DM_CON	B5	Signal Path	Open	Connected to the USB connector D- pin; depending on the FSA9480 signaling mode, this pin can share D-, S_L, Txd, or V_L signals
I^2C Interface				
I^2C_SCL	C2	Input	N/A	I^2C serial clock signal to be connected to the phone based I^2C master
I^2C_SDA	B2	Open-Drain I/O	Hi-Z	Open-drain I/O pin; I^2C serial data signal to be connected to the phone based I^2C master
INTB	A1	Push-Pull Output	Low	Interrupt signal to prompt the phone baseband to read the I^2C register bits, indicates a change in ID pin status or accessory attach status

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter			Min.	Max.	Unit
V_{BAT}/V_{DDIO}	Supply Voltage from Battery / Baseband			-0.5	6.0	V
V_{BUS}	Supply Voltage from Mini–USB Connector			-0.5	28.0	V
V_{SW}	Switch I/O Voltage	USB or Car Kit Path Active		-1.0	V_{BUS}+0.5	V
		Stereo/Mono Audio Path Active		-1.5	V_{BAT}+0.5	
		All Other Channels		-0.5	V_{BAT}+0.5	
I_{IK}	Input Clamp Diode Current			-50		mA
Chg_Det	Charger Detect Sets Current Sink Capability of the Charger IC				30	mA
I_{SW}	Switch I/O Current (Continuous)	USB			50	mA
		Audio			60	
		All Other Channels			50	
I_{SWPEAK}	Peak Switch Current (Pulsed at 1ms Duration, <10% Duty Cycle)	USB			150	mA
		Audio			150	mA
		Charger FET			1.2	A
		All Other Channels			150	mA
T_{STG}	Storage Temperature Range			-65	+150	°C
T_J	Maximum Junction Temperature				+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)				+260	°C
ESD	IEC 61000-4-2 System Electrostatic Discharge	USB Connector Pins (D+, D-, V_{BUS}, ID)	Air Gap	15		kV
			Contact	8		
	JEDEC JESD22-A114, Human Body Model		All Pins	4		

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min.	Max.	Units
V_{BAT}	Battery Supply Voltage		3.0	4.4	V
V_{BAT_TH}	Battery Supply Voltage Threshold			3.0	V
V_{BUS}	Supply Voltage		4.00	5.25	V
V_{DDIO}	Baseband-supplied Reference Voltage		1.8	3.6	V
V_{SW}	Switch I/O Voltage	USB Path Active	0	3.6	V
		Audio Path Active	-0.8	0.8	V
		All Other Pins	0	5.0	V
ID_{Cap}	Maximum Capacitive Load on ID pin for Reliable Accessory Detection			1.5	nF
T_A	Operating Temperature		-40	+85	ºC

Switch Path DC Electrical Characteristics

All typical values are at 25ºC unless otherwise specified.

Symbol	Parameter	V_{BAT} (V)	Conditions	T_A = -40 to +85°C			Unit
				Min.	Typ.	Max.	
UART Interface Pins							
V_{OHRXD}	R_{XD} Output High Voltage	3.0 to 4.4	I_{OH}=2mA	0.7 • V_{DDIO}			V
V_{OLRXD}	R_{XD} Output Low Voltage	3.0 to 4.4	I_{OL}=10mA			0.4	V
$V_{IHDPCon}$	UART Input (DP_Con) High Voltage	3.0 to 4.4		0.7 • V_{DDIO}			V
$V_{ILDPCon}$	UART Path (DP_Con) Input Low Voltage	3.0 to 4.4				0.4	V
$V_{OHDMCon}$	UART Output (DM_Con) High Voltage	3.0 to 4.4	I_{OH}=2mA	0.7 • V_{BAT}			V
$V_{OLDMCon}$	UART Output (DM_Con) Low Voltage	3.0 to 4.4	I_{OL}=10mA			0.4	V
V_{IHTXD}	T_{XD} Input High Voltage	3.0 to 4.4		0.7 • V_{DDIO}			V
V_{ILTXD}	T_{XD} Input Low Voltage	3.0 to 4.4				0.4	V
Host Interface Pins (JIG, BOOT, INTB, CHG-DET)							
V_{OH}	Output High Voltage[9]	3.0 to 4.4	I_{OH}=2mA	0.7 • V_{DDIO}			V
V_{OL}	Output Low Voltage	3.0 to 4.4	I_{OL}=10mA			0.4	V
Switch Off Characteristics							
I_{OFF}	Power Off Leakage Current	0	All Data Ports Except Video, ID Bypass and MIC V_{SW}=0V to 4.4V			18	µA
$I_{NO(0FF)}$	Off-Leakage Current	3.0 to 4.4	I/O pins=0.3V, V_{BAT}, or Floating	-100	1	100	nA
USB Switch On Path							
USB Analog Signal Range		3.0 to 4.4		0		3.6	V
R_{ONUSB}	HS Switch On Resistance[10,13]	3.0 to 4.4	$V_{D+/D-}$=0V, 0.4V, I_{ON}=8mA		6	8	Ω
Charging FET On Path							
V_{OVP}	OVP Threshold Voltage[13]	3.8		6.2	6.6	7.0	V
R_{ONFET}	Charging FET On Resistance[10]		V_{BUS}=4.2V to 5.0V, I_{ON}=1A		100		mΩ
I_{OCP}	OCP Threshold Current[13]			1.1	1.5	1.6	A
I_{RUSH}	Charging FET Inrush Current Limiting[13]		C_L=4.7µF Typical, C_L=10µF Maximum, Duration = 100ms after Initial Attach			100	mA
Audio R/L Switch On Paths							
DC Audio Analog Signal Range		3.0 to 4.4		0		3	V
AC Audio Analog Signal Range		3.0 to 4.4		-1.5		3.0	V
R_{ON}	Audio Switch On Resistance[10,13]	3.8	$V_{L/R}$=-0.8V, 0.8V, I_{ON}=30mA, f=0-470kHz		2.0	3.0	Ω
R_{FLAT}	Audio R_{ON} Flatness[11]	3.8			0.1		Ω

Symbol	Parameter	V_{BAT} (V)	Conditions	T_A = -40 to +85°C			Unit
				Min.	Typ.	Max.	
Video Audio R/L Switch On Paths							
DC Audio Analog Signal Range[14]		3.0 to 4.4		0		3	V
AC Audio Analog Signal Range[14]		3.0 to 4.4		-1.5		3.0	V
R_{ON}	Audio Switch On Resistance[10,13]	3.0 to 4.4	$V_{L/R}$=0V, 1.6V, I_{ON}=30mA, f=0-470kHz		2.8	5.0	Ω
R_{FLAT}	Audio R_{ON} Flatness[11,13]	3.0 to 4.4			0.2	0.4	Ω
MIC Switch On Path							
Analog Signal Range[12]		3.0 to 4.4		0		4.4	V
R_{ON}	Switch On Resistance[10]	3.0 to 4.4	V_{SW}=1.4 to 1.8V, I_{ON}=30mA	25	40	52	Ω
IDBP and Video Switch On Paths							
Analog Signal Range		3.0 to 4.4		0		4.4	V
R_{ON}	Switch On Resistance[10,13]	3.0 to 4.4	V_{SW}=0V, 4.4V, I_{ON}=30mA	10	15	20	Ω
Total Switch Current Consumption							
I_{CCSLNA}	Battery Supply Sleep Mode Current No Accessory Attached	3.8	Static Current During Sleep Mode		9	15	µA
I_{CCSLWA}	Battery Supply Sleep Mode Current with Accessory Attached[13]	3.8	Static Current During Sleep Mode		30	40	µA
I_{CCWK}	Battery Supply Active Mode Current[13]	3.8	Average Pulse Current (~100µs Pulse)		2.5	3	mA

Notes:

9. Does not apply to CHG_DET or JIG pins.
10. On resistance is determined by the voltage drop between the A and B pins at the indicated current through the switch.
11. Flatness is defined as the difference between the maximum and minimum values of on resistance over the specified range of conditions.
12. The MIC bias applied by the phone should not exceed 3.5V.
13. Guaranteed by characterization data.
14. Negative swing audio is not recommended when the switch is open.

Capacitance

Symbol	Parameter	V_{BAT} (V)	Conditions	T_A = -40 to +85°C			Unit
				Min.	Typ.	Max.	
C_{INOFF}	Host Interface Pins Off Capacitance	3.8	V_{BIAS}=0V		10		pF
$C_{ON(D+, D-)}$	D+, D- On Capacitance (USB Mode)	3.8	V_{BIAS}=0.2V, f=1MHz		8		pF

I²C™ Controller DC Characteristics

Symbol	Parameter		Fast Mode (400kHz)		
			Min.	Max.	Unit
V_{IL}	Low-Level Input Voltage		-0.5	$0.3V_{DDIO}$	V
V_{IH}	High-Level Input Voltage		$0.7V_{DDIO}$		V
V_{OL1}	Low-Level Output Voltage at 3mA Sink Current (Open-Drain or Open-Collector)	V_{DDIO}>2V	0	0.4	V
		V_{DDIO}<2V		$0.2V_{DDIO}$	
I_I	Input Current of Each I/O Pin, Input Voltage 0.26V to 2.34V		-10	10	µA
C_I	Capacitance for Each I/O Pin			10	pF

Switch Path AC Electrical Characteristics

All typical value are for V_{BAT}=3.8V at 25ºC unless otherwise specified.

Symbol	Parameter		V_{BAT} (V)	Conditions	T_A = -40 to +85°C			Unit
					Min.	Typ.	Max.	
Xtalk	Non-Adjacent Channel Crosstalk	Audio Mode	3.8	f=20kHz, R_T=32Ω, C_L=0pF		-50		dB
		USB Mode	3.8	f=1MHz, R_T=50Ω, C_L=0pF		-60		
O_{IRR}	Off Isolation	Audio Mode	3.8	f=20kHz, R_T=32Ω, C_L=0pF		-100		dB
		USB Mode	3.8	f=1 MHz, R_T=50Ω, C_L=0pF		-60		
PSRR	Power Supply Rejection Ratio		3.8	Power Supply Noise 300mV_{PP}, f=217Hz on MIC, DP_Con, DM_Con		-100		dB
$t_{SK(P)}$	Skew of Opposite Transitions of the Same Output (USB Mode)		3.8	t_r=t_f=750ps (10-90%) at 240MHz, C_L=0pF, R_L=50Ω		35		ps
t_J	Total Jitter (USB Mode)		3.8	R_L=50Ω, C_L=50pF, t_r=t_f=500ps (10-90%) at 480Mbps (PRBS=2^{15}–1)		130		ps

I²C™ AC Electrical Characteristics

Symbol	Parameter	Fast Mode		
		Min.	Max.	Unit
f_{SCL}	SCL Clock Frequency	0	400	kHz
$t_{HD;STA}$	Hold Time (Repeated) START Condition	0.6		µs
t_{LOW}	Low Period of SCL Clock	1.3		µs
t_{HIGH}	High Period of SCL Clock	0.6		µs
$t_{SU;STA}$	Set-up Time for Repeated START Condition	0.6		µs
$t_{HD;DAT}$	Data Hold Time	0	0.9	µs
$t_{SU;DAT}$	Data Set-Up Time	100(15)		ns
t_r	Rise Time of SDA and SCL Signals(16)	20+0.1C_b	300	ns
t_f	Fall Time of SDA and SCL Signals(16)	20+0.1C_b	300	ns
$t_{SU;STO}$	Set-up Time for STOP Condition	0.6		µs
t_{BUF}	Bus Free Time between a STOP and START Conditions	1.3		µs
t_{SP}	Pulse Width of Spikes that Must Be Suppressed by the Input Filter	0	50	ns

Note:

15. A fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SU;DAT} \geq 250ns$ must be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If the device stretches the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r\,max} + t_{SU;DAT}=1000+250=1250ns$ (according to the standard-mode I²C-bus specification) before the SCL line is released.
16. C_b equals the total capacitance of one bus line in pf. If mixed with high-speed mode devices, faster fall times are allowed according to the I²C specification.

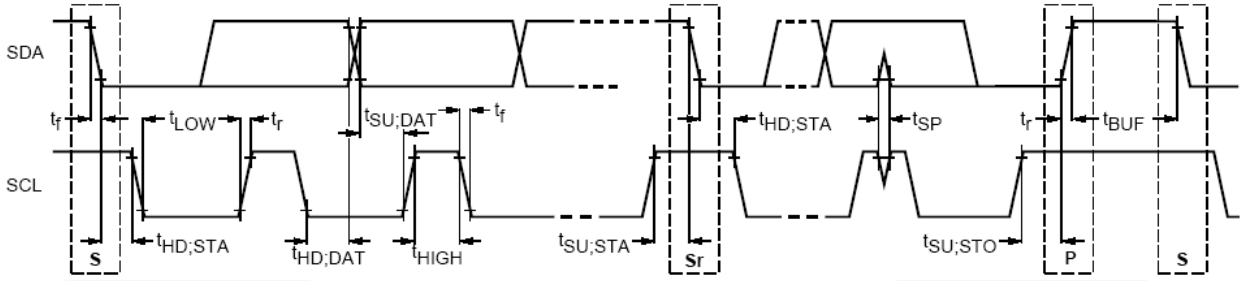


Figure 20. Definition of Timing for Full-Speed Mode Devices on the I²C-bus

Table 5. I²C™ Slave Address

Name	Size (Bits)								
Slave Address	8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		0	1	0	0	1	0	1	R/W

Table 6. I²C™ Register Map

Address	Register	Type	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01H	Device ID	R	N/A	Version ID					Vendor ID		
02H	Control	R/W	XXX11111	Reserved	Reserved	Reserved	Switch Open	RAW Data	Manual S/W	Wait	INT Mask
03H	Interrupt 1[17]	R	00000000	OVP_OCP_DIS	OCP_EN	OVP_EN	LKR	LKP	KP	Detach	Attach
04H	Interrupt 2[17]	R	XXX00000	Reserved	Reserved	Reserved	Stuck Key RCV	Stuck Key	ADC Change	Reserved Attach	A/V Charging
05H	Interrupt Mask 1	R/W	00000000	OVP_OCP_DIS	OCP_EN	OVP_EN	LKR	LKP	KP	Detach	Attach
06H	Interrupt Mask 2	R/W	XXX00000	Reserved	Reserved	Reserved	Stuck Key RCV	Stuck Key	ADC Change	Reserved Attach	A/V Charging
07H	ADC	R	XXX11111	Reserved	Reserved	Reserved	ADC Value				
08H	Timing Set 1	R/W	00000100	Key Press				Device Wake Up			
09H	Timing Set 2	R/W	00000000	Switching Wait				Long Key Press			
0AH	Device Type 1	R	00000000	USB OTG	Dedicated CHG	USB Charger	Car kit	UART	USB	Audio Type 2	Audio Type 1
0BH	Device Type 2	R	X0000000	Reserved	A/V	TTY	PPD	Jig UART Off	Jig UART On	Jig USB Off	Jig USB On
0CH	Button 1	R	00000000	7	6	5	4	3	2	1	Send End
0DH	Button 2	R	X0000000	Reserved	Unknown	Error	12	11	10	9	8
0EH	Car Kit Status	R/W[18]	X0000100	Reserved	DISC_Request	UART Traffic	Mode			Type	
0FH	Car Kit Int 1	R	00000000	CR_UART	PH_Disc	PH_DDA_Stereo	PH_DDA_Mono	PH_Aud_Stereo	PH_Aud_Mono	PH_UART	PH_Init
10H	Car Kit Int 2	R	XXXXX000	Reserved	Reserved	Reserved	Reserved	Reserved	CR_DDA_Stereo	CR_Stereo	CR_Mono
11H	Car Kit Int Mask 1	R/W	00000000	CR_UART	PH_Disc	PH_DDA_Stereo	PH_DDA_Mono	PH_Aud_Stereo	PH_Aud_Mono	PH_UART	PH_Init
12H	Car Kit Int Mask 2	R/W	XXXXX000	Reserved	Reserved	Reserved	Reserved	Reserved	CR_DDA_Stereo	CR_Stereo	CR_Mono
13H	Manual SW 1	R/W	00000000	D- Switching			D+ Switching			V_{BUS} switching	
14H	Manual SW 2	R/W	XXX00000	Reserved	Reserved	Reserved	Reserved	BOOT SW	JIG ON	ID Switching	

Notes:

17. The following four bit pairs are mutually exclusive; OVP_EN/OVP_DIS, Stuck_Key/Stuck_Key_Rcv, LKP/LKR, Detach/Attach. If the FSA9480 writes either bit in these pairs before its counterpart has been read and cleared, the FSA9480 clears the first bit before writing the second bit in the mutually exclusive pair. This ensures only one bit from each pair is ever HIGH.
18. Bits 0 and 1 of the Car Kit Status Register 0EH cannot be written.

Table 7. Device ID

- Address: 01h
- Type: Read

Bit #	Name	Size (Bits)	Description
7:3	Version ID	5	Rev1.0, Rev 1.1 : 000000 Rev2.0: 00001 Rev2.1: 00010 Rev3.0: 00011 Rev3.1: 00100 Rev3.2: 00101
2:0	Vendor ID	3	000: Fairchild Semiconductor

Table 8. Control

- Address: 02h
- Reset Value: xxx11111
- Type: Read/Write

Bit #	Name	Size (Bits)	Description
7:5	Reserved	3	NA
4	Switch Open	1	0: Open all switches 1: Automatic switching by accessory status
3	RAW Data	1	0: Report the status changes on ID to HOST 1: Don't report the status changes on ID to HOST
2	Manual S/W	1	0: Manual switching mode (refer to attach flow diagram Figure 2) 1: Automatic switching mode (refer to attach flow diagram Figure 2)
1	Wait	1	0: Keep all switches open until this bit is reset to 1 by the baseband; when reset to 1, immediately configure the switches 1: Wait for the duration of wait time specified in Timing Set Register before configuring switches
0	INT Mask	1	0: Unmask interrupt – interrupt baseband on change of state in either Interrupt Register 1: Mask interrupt – do not interrupt baseband

Table 9. Interrupt 1

- Address: 03h
- Reset Value: 00000000
- Type: Read/Clear

Bit #	Name	Size (Bits)	Description
7	OVP_OCP_DIS	1	1: OVP and OCP disabled
6	OCP_EN	1	1: OCP enabled
5	OVP_EN	1	1: OVP enabled
4	LKR	1	1: Long key release
3	LKP	1	1: Long key press
2	KP	1	1: Key press
1	Detach	1	1: Accessory detached
0	Attach	1	1: Accessory attached

Table 10. Interrupt 2

- Address: 04h
- Reset Value: xxx00000
- Type: Read/Clear

Bit #	Name	Size (Bits)	Description
7:5	Reserved	3	NA
4	Stuck_Key_RCV	1	1: Stuck key is recovered
3	Stuck_Key	1	1: Stuck key is detected
2	ADC_Change	1	1: ADC value change (when RAW data is enabled)
1	Reserved_Attach	1	1: Reserved device is attached
0	A/V_Charging	1	1: Charger detected when A/V cable is attached

Table 11. Interrupt Mask 1

- Address: 05h
- Reset Value: 00000000
- Type: Read/Write

Bit #	Name	Size (Bits)	Description
7	OVP_OCP_DIS	1	1: Mask OVP and OCP disabled interrupt
6	OCP_EN	1	1: Mask OCP enabled interrupt
5	OVP_EN	1	1: Mask OVP enabled interrupt
4	LKR	1	1: Mask long key release interrupt
3	LKP	1	1: Mask long key press interrupt
2	KP	1	1: Mask key press interrupt
1	Detach	1	1: Mask detach interrupt
0	Attach	1	1: Mask attach interrupt

Table 12. Interrupt Mask 2

- Address: 06h
- Reset Value: xxx00000
- Type: Read/Write

Bit #	Name	Size (Bits)	Description
7:5	Reserved	3	NA
4	Stuck_Key_RCV	1	1: Mask stuck key recovered interrupt
3	Stuck_Key	1	1: Mask stuck key Interrupt
2	ADC_Change	1	1: Mask ADC value change interrupt
1	Reserved_Attach	1	1: Mask reserved device interrupt
0	A/V_Charging	1	1: Mask charger detect when A/V cable attached interrupt

Table 13. ADC

- Address: 07h
- Reset Value: xxx11111
- Type: Read

Bit #	Name	Size (Bits)	Description
7:5	Reserved	3	NA
4:0	ADC Value	5	ADC value read from ID *(see Table 2)*

Table 14. Timing Set 1

- Address: 08h
- Reset Value: 00000100
- Type: Read/Write

Bit #	Name	Size (Bits)	Description
7:4	Key Press	4	Normal key press duration *(see Table 16 — Timing Table for Timing Set 1 & 2 Registers)*
3:0	ADC Detect Time	4	ADC detection time duration *(see Table 16 — Timing Table for Timing Set 1 & 2 Registers)*

Table 15. Timing Set 2

- Address: 09h
- Reset Value: 00000000
- Type: Read/Write

Bit #	Name	Size (Bits)	Description
7:4	Switching Wait	4	Waiting duration before switching *(see Table 16 — Timing Table for Timing Set 1 & 2 Registers)*
3:0	Long Key Press	4	Long key press duration *(see Table 16 — Timing Table for Timing Set 1 & 2 Registers)*

Table 16. Timing Table for Timing Set 1 & 2 Registers

Setting Value[19]	ADC Detection Time by Capacitive Load Register		Key Press Register	Long Key Press Register	Switching Wait Register
	Time	Max Capacitive Load ID Pin[20]			
0000	50ms	128pF	100ms	300ms	10ms
0001	100ms	256pF	200ms	400ms	30ms
0010	150ms	384pF	300ms	500ms	50ms
0011	200ms	512pF	400ms	600ms	70ms
0100	300ms	640pF	500ms	700ms	90ms
0101	400ms	768pF	600ms	800ms	110ms
0110	500ms	896pF	700ms	900ms	130ms
0111	600ms	1.02nF	800ms	1000ms	150ms
1000	700ms	1.15nF	900ms	1100ms	170ms
1001	800ms	1.28nF	1000ms	1200ms	190ms
1010	900ms	1.41nF		1300ms	210ms
1011	1000ms	1.54nF		1400ms	
1100				1500ms	
1101-1111					

Notes:
19. Each of the four registers can have unique register setting values.
20. Maximum capacitive load indicates the maximum load seen by the FSA9480 on the ID pin during accessory detection. Default setting for Rev 3.1 Silicon is 0100 for a 640pF load.

Table 17. Device Type 1

- Address: 0Ah
- Reset Value: 00000000
- Type: Read

Bit #	Name	Size (Bits)	Description
7	USB OTG	1	1: USB OTG device detected
6	Dedicated_Charger	1	1: Dedicated charger detected
5	USB_Charger	1	1: USB charger detected
4	Car Kit	1	1: Car kit detected
3	UART	1	1: UART detected
2	USB	1	1: USB detected
1	Audio Type 2	1	1: Audio device type 2 detected
0	Audio Type 1	1	1: Audio device type 1 detected

Table 18. Device Type 2

- Address: 0Bh
- Reset Value: x0000000
- Type: Read

Bit #	Name	Size (Bits)	Description
7	Reserved	1	NA
6	A/V	1	1: A/V cable detected
5	TTY	1	1: TTY detected
4	PPD	1	1: Phone-powered device detected
3	JIG_UART_OFF	1	1: Factory mode cable detected (JIG_UART_OFF)
2	JIG_UART_ON	1	1: Factory mode cable detected (JIG_UART_ON)
1	JIG_USB_OFF	1	1: Factory mode cable detected (JIG_USB_OFF)
0	JIG_USB_ON	1	1: Factory mode cable detected (JIG_USB_ON)

Table 19. Button 1

- Address: 0Ch
- Reset Value: 00000000
- Type: Read

Bit #	Name	Size (Bits)	Description
7	Button 7	1	1: Button 7 key press
6	Button 6	1	1: Button 6 key press
5	Button 5	1	1: Button 5 key press
4	Button 4	1	1: Button 4 key press
3	Button 3	1	1: Button 3 key press
2	Button 2	1	1: Button 2 key press
1	Button 1	1	1: Button 1 key press
0	Send_End	1	1: Send_End key press

Table 20. Button 2

- Address: 0Dh
- Reset Value: x0000000
- Type: Read

Bit #	Name	Size (Bits)	Description
7	Reserved	1	NA
6	Unknown	1	1: Unknown key press
5	Error	1	1: Error key press
4	Button 12	1	1: Button 12 key press
3	Button 11	1	1: Button 11 key press
2	Button 10	1	1: Button 10 key press
1	Button 9	1	1: Button 9 key press
0	Button 8	1	1: Button 8 key press

Table 21. Car Kit Status

- Address: 0Eh
- Reset Value: x0000100
- Type: Read/Write

Bit #	Name	Size (Bits)	Description
7	Reserved	1	NA
6	Disc_Request	1	0: Car kit disconnect not requested 1: Car kit disconnect requested
5	UART_Traffic	1	0: UART traffic disabled 1: UART traffic enabled
4:2	Mode	3	Car Kit Mode change(21) 000: Open all car kit switch paths 001: UART 010: Mono audio 011: Stereo audio 100: DDA enabled mono audio 101: DDA enabled stereo audio
1:0	Type	2	Detected car kit types 00: No connection 01: Car kit 10: Car kit charger type 1 11: Car kit charger type 2

Note:
21. Audio device type 2 also uses MODE 000, 001, 100, and 101 commands to change device modes.

Table 22. Car Kit Interrupt 1

- Address: 0Fh
- Reset Value: 00000000
- Type: Read/Clear

Bit #	Name	Size (Bits)	Description
7	CR_UART	1	1: Car kit generated interrupt during UART state
6	PH_Disc	1	1: Car kit state machine in disconnect state
5	PH_DDA_Stereo	1	1: Car kit state machine in DDA stereo state
4	PH_DDA_Mono	1	1: Car kit state machine in DDA mono state
3	PH_Aud_Stereo	1	1: Car kit state machine in stereo state
2	PH_Aud_Mono	1	1: Car kit state machine in mono state
1	PH_UART	1	1: Car kit state machine in UART state
0	PH_Int	1	1: Car kit state machine in initial state

Table 23. Car Kit Interrupt 2

- Address: 10h
- Reset Value: xxxxx000
- Type: Read/Clear

Bit #	Name	Size (Bits)	Description
7:3	Reserved	5	NA
2	CR_DDA_Stereo	1	1: Car kit generated interrupt during DDA stereo state
1	CR_Stereo	1	1: Car kit generated interrupt during stereo state
0	CR_Mono	1	1: Car kit generated interrupt during mono state

Table 24. Car Kit Interrupt Mask 1

- Address: 11h
- Reset Value: 00000000
- Type: Read/Write

Bit #	Name	Size (Bits)	Description
7	CR_UART	1	0: Unmask car kit UART interrupt 1: Mask car kit UART interrupt
6	PH_Disc	1	0: Unmask PH_Disc interrupt 1: Mask PH_Disc interrupt
5	PH_DDA_Stereo	1	0: Unmask PH_DDA_Stereo interrupt 1: Mask PH_DDA_Stereo interrupt
4	PH_DDA_Mono	1	0: Unmask PH_DDA_Mono interrupt 1: Mask PH_DDA_Mono interrupt
3	PH_Aud_Stereo	1	0: Unmask PH_Aud_Stereo interrupt 1: Mask PH_Aud_Stereo interrupt
2	PH_Aud_Mono	1	0: Unmask PH_Aud_Mono interrupt 1: Mask PH_Aud_Mono interrupt
1	PH_UART	1	0: Unmask PH_UART interrupt 1: Mask PH_UART interrupt
0	PH_Int	1	0: Unmask PH_Int interrupt 1: Mask PH_Int interrupt

Table 25. Car Kit Interrupt Mask 2

- Address: 12h
- Reset Value: xxxxx000
- Type: Read/Write

Bit #	Name	Size (Bits)	Description
7:3	Reserved	5	NA
2	CR_DDA_Stereo	1	0: Unmask CR_DDA_Stereo interrupt 1: Mask CR_DDA_Stereo interrupt
1	CR_Stereo	1	0: Unmask CR_Stereo interrupt 1: Mask CR_Stereo interrupt
0	CR_Mono	1	0: Unmask CR_Mono interrupt 1: Mask CR_Mono interrupt

Table 26. Manual S/W 1

- Address: 13h
- Reset Value: 00000000
- Type: Read/Write

Bit #	Name	Size (Bits)	Description
7:5	D- Switching	3	000: Open all switches 001: D- connected to D- of USB port 010: D- connected to Audio_L 011: D- connected to TxD of UART 100: D- connected to V_Audio_L
4:2	D+ Switching	3	000: Open all switches 001: D+ connected to D+ of USB port 010: D+ connected to Audio_R 011: D+ connected to RxD of UART 100: D+ connected to V_Audio_R
1:0	V_{BUS} Switching(22)	2	00: Open all switches 01: V_{BUS} connected to charger 10: V_{BUS} connected to MIC

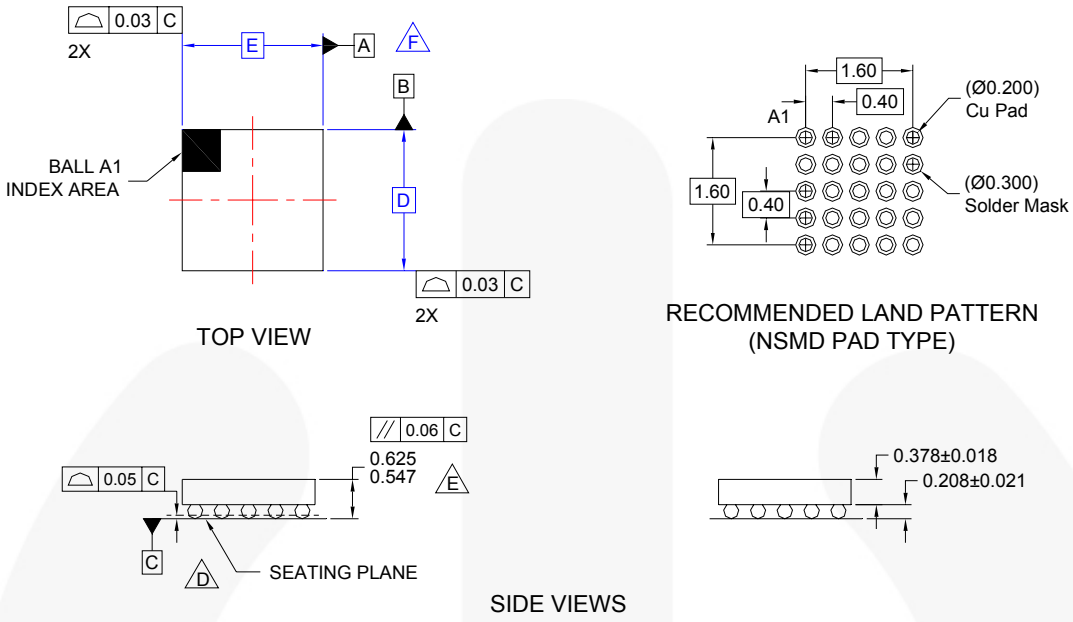
Note:
22. V_{BUS} must be present to allow for signaling in manual USB path configuration.

Table 27. Manual S/W 2

- Address: 14h
- Reset Value: XXX00000
- Type: Read/Write

Bit #	Name	Size (Bits)	Description
7:4	Reserved	4	NA
3	BOOT_SW	1	0: LOW 1: HIGH
2	JIG_ON	1	0: High Impedance 1: GND
1:0	ID Switching	2	00: Open all switches 01: ID connected to video 10: ID connected to bypass port

Physical Dimensions



NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 1994.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILNAME: MKT-UC025AArev2.

Figure 21. 25-Lead, Wafer-Level Chip-Scale Package (WLCSP)

Product-Specific Dimensions

Product	D	E	X	Y
FSA9480UCX	2.10	2.10	0.25	0.25

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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Tape and Reel Specifications

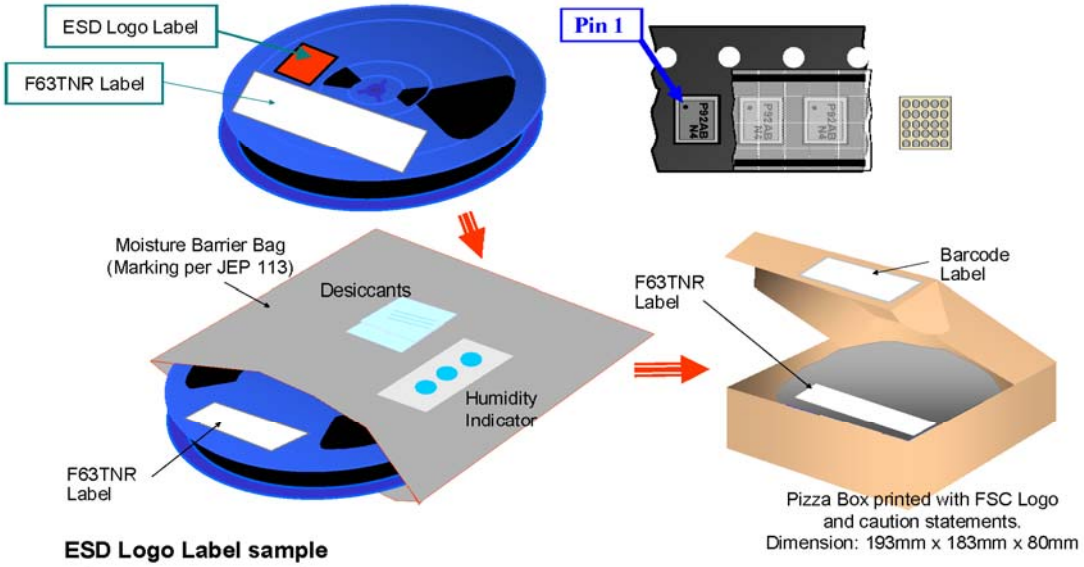
FSA9480UCX Packing - Embossed Tape

Packing Description:

FSA9480UCX, a WLCSP product, is classified under Moisture Sensitive Level 1 and is packed in moisture barrier bag for added protection.

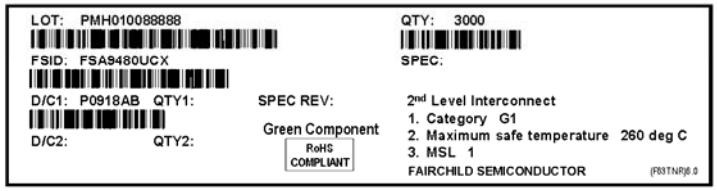
The carrier tape is made from dissipative polystyrene or polycarbonate resin. The cover tape is a multilayer film primarily composed of polyester film, adhesive layer, heat activated sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 3000 units per 178 mm diameter reel. Up to three reels are packed in each intermediate box. The reels is made of polystyrene plastic (anti-static coated or intrinsic).

These full reels are individually barcode labeled and placed inside a pizza box made of recyclable corrugated brown paper with a Fairchild logo printing. The reel is packed single reel in the pizza box. And these pizza boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.

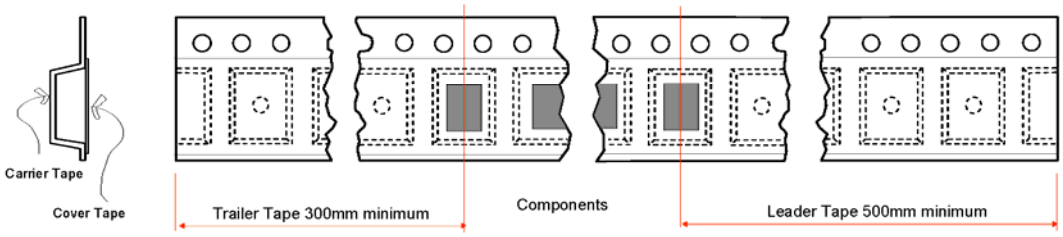


ESD Logo Label sample

F63TNR Label sample



Tape Leader and Trailer Configuration



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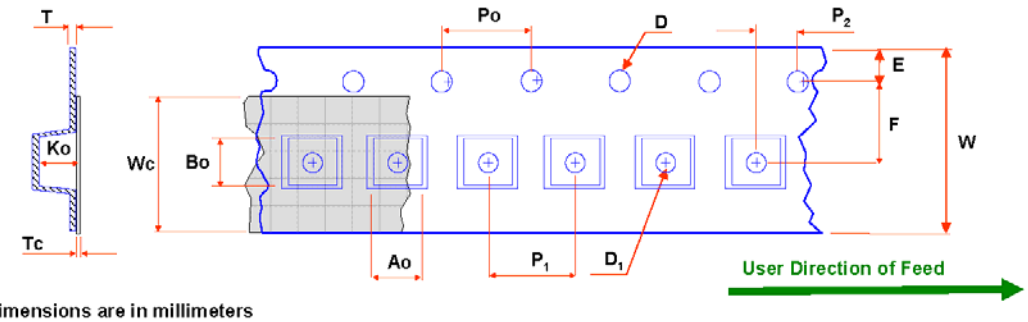
Tape and Reel Specifications (Continued)

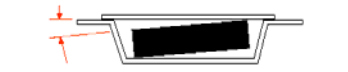
FSA9480UCX Embossed Tape Dimension



Dimensions are in millimeters

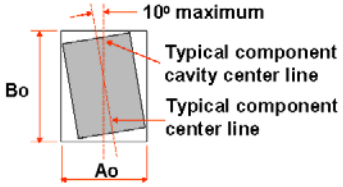
Package	Ao +/-0.10	Bo +/-0.10	D +/-0.05	D_1 min.	E +/-0.1	F +/-0.1	Ko +/-0.1	P_1 TYP	Po TYP	P_2 +/-0/05	T TYP	Tc +/-0.005	W +/-0.3	Wc TYP
FPF1003A	2.35	2.35	1.55	0.5	1.75	3.5	0.81	4	4	2.0	0.254	0.06	8	5.3

Notes: Ao, Bo, and Ko dimensions are determined with respect to the EIA /Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).

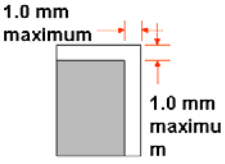


10 deg maximum component rotation

Sketch A (Side or Front Sectional View)
Component Rotation

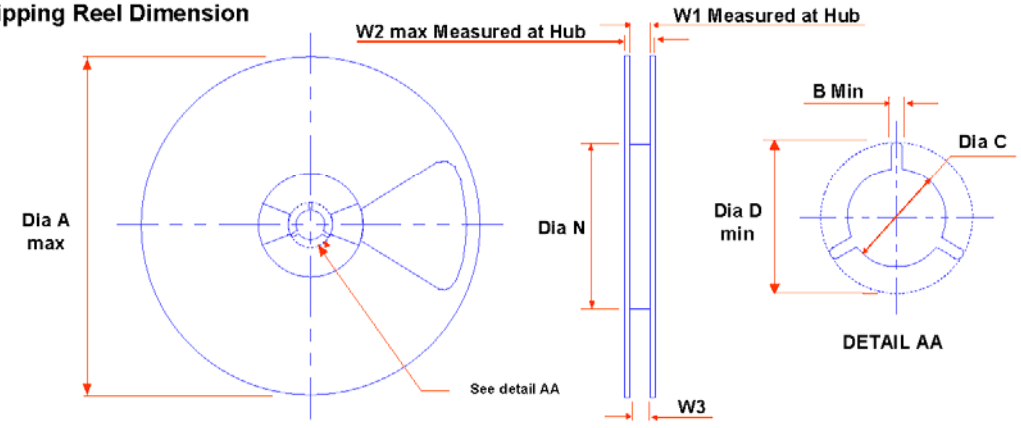


Sketch B (Top View)
Component Rotation



Sketch C (Top View)
Component lateral movement

Shipping Reel Dimension



Dimensions are in millimeters

Tape Width	Dia A max	Dim B min	Dia C +.5/-.2	Dia D min	Dim N min	Dim W1 +2/-0	Dim W2 max	Dim W3 (LSL - USL)
8	178	1.5	13	20.2	55	8.4	14.4	7.9~10.4

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Rev. I49

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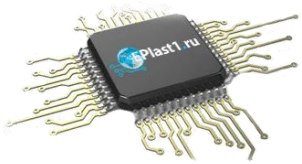

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