

N-Channel Power MOSFET

700V, 4.5A, 0.9Ω

FEATURES

- Super-Junction technology
- High performance due to small figure-of-merit
- High ruggedness performance
- High commutation performance

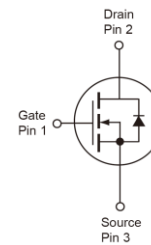
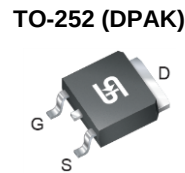
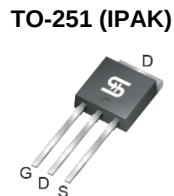
APPLICATION

- Power Supply
- Lighting

KEY PERFORMANCE PARAMETERS

PARAMETER	VALUE	UNIT
V_{DS}	700	V
$R_{DS(on)}$ (max)	0.9	Ω
Q_g	9.7	nC


ROHS
COMPLIANT

HALOGEN
FREE


Notes: MSL 3 (Moisture Sensitivity Level) for TO-252 (DPAK) per J-STD-020.

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	IPAK/DPAK	ITO-220	UNIT
Drain-Source Voltage	V_{DS}	700		V
Gate-Source Voltage	V_{GS}	±30		V
Continuous Drain Current ^(Note 1)	I_D	4.5		A
		2.7		
Pulsed Drain Current ^(Note 2)	I_{DM}	13.5		A
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_{DTOT}	50	20	W
Single Pulsed Avalanche Energy ^(Note 3)	E_{AS}	64		mJ
Single Pulsed Avalanche Current ^(Note 3)	I_{AS}	1.6		A
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150		°C

THERMAL PERFORMANCE

PARAMETER	SYMBOL	IPAK/DPAK	ITO-220	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	2.5	6.25	°C/W
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	62		°C/W

Notes: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 PCB in still air.

ELECTRICAL SPECIFICATIONS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static ^(Note 4)						
Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA	BV _{DSS}	700	--	--	V
Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	V _{GS(TH)}	2.0	3.1	4.0	V
Gate Body Leakage	V _{GS} = ±30V, V _{DS} = 0V	I _{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V _{DS} = 700V, V _{GS} = 0V	I _{DSS}	--	--	1	μA
Drain-Source On-State Resistance	V _{GS} = 10V, I _D = 1.5A	R _{DS(on)}	--	0.83	0.9	Ω
Dynamic ^(Note 5)						
Total Gate Charge	V _{DS} = 380V, I _D = 2.3A, V _{GS} = 10V	Q _g	--	9.7	--	nC
Gate-Source Charge		Q _{gs}	--	2.9	--	
Gate-Drain Charge		Q _{gd}	--	3.5	--	
Input Capacitance	V _{DS} = 100V, V _{GS} = 0V, f = 1.0MHz	C _{iss}	--	482	--	pF
Output Capacitance		C _{oss}	--	34	--	
Gate Resistance	F = 1MHz, open drain	R _g	--	3.6	--	Ω
Switching ^(Note 6)						
Turn-On Delay Time	V _{DD} = 380V, R _{GEN} = 40Ω, I _D = 2.3A, V _{GS} = 10V,	t _{d(on)}	--	20	--	ns
Turn-On Rise Time		t _r	--	54	--	
Turn-Off Delay Time		t _{d(off)}	--	34	--	
Turn-Off Fall Time		t _f	--	48	--	
Source-Drain Diode ^(Note 4)						
Forward On Voltage	I _S = 4.5A, V _{GS} = 0V	V _{SD}	--	--	1.4	V
Reverse Recovery Time	V _R =200V, I _S = 2.3A dI _F /dt = 100A/μs	t _{rr}	--	176	--	ns
Reverse Recovery Charge		Q _{rr}	--	1.1	--	μC

Notes:

- Current limited by package
- Pulse width limited by the maximum junction temperature
- $L = 50mH, I_{AS} = 1.6A, V_{DD} = 50V, R_G = 25\Omega$, Starting $T_J = 25^\circ C$
- Pulse test: $PW \leq 300\mu s$, duty cycle $\leq 2\%$
- For DESIGN AID ONLY, not subject to production testing.
- Switching time is essentially independent of operating temperature.

ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM70N900CI C0G	ITO-220	50pcs / Tube
TSM70N900CH C5G	TO-251 (IPAK)	75pcs / Tube
TSM70N900CP ROG	TO-252 (DPAK)	2,500pcs / 13" Reel

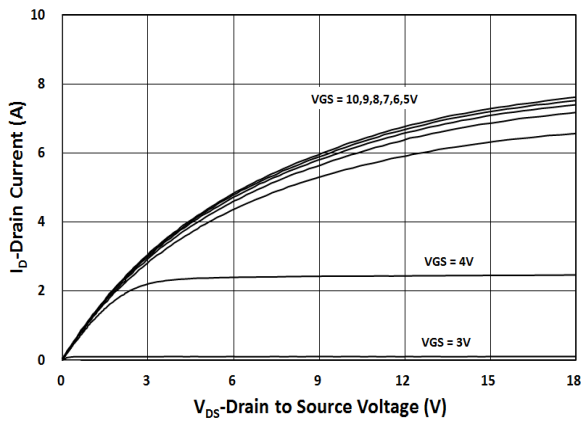
Note:

1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
2. Halogen-free according to IEC 61249-2-21 definition

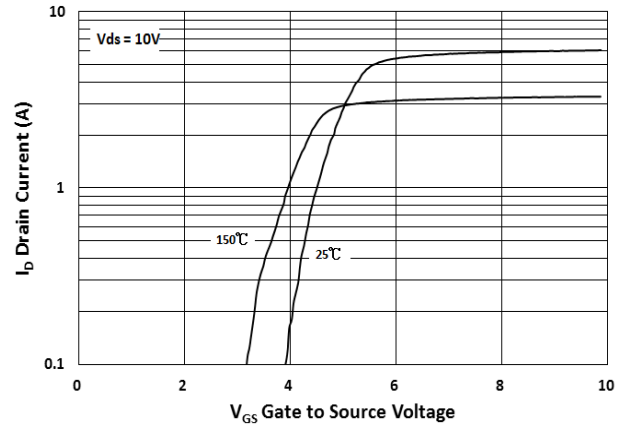
CHARACTERISTICS CURVES

($T_C = 25^\circ\text{C}$ unless otherwise noted)

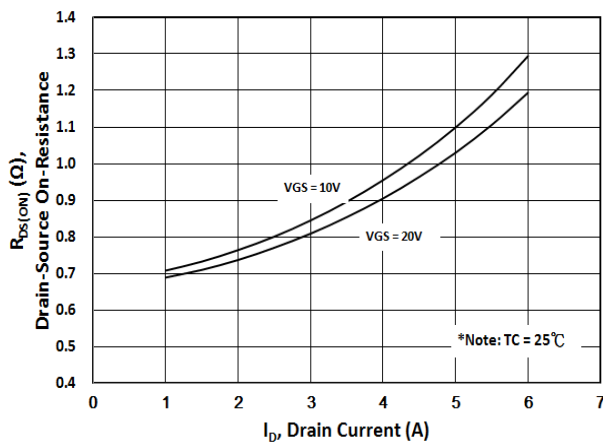
Output Characteristics



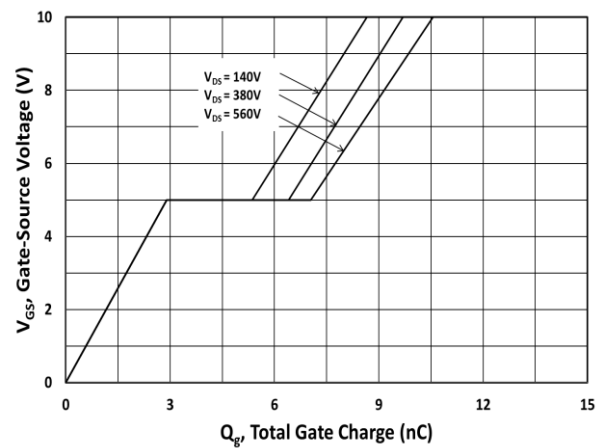
Transfer Characteristics



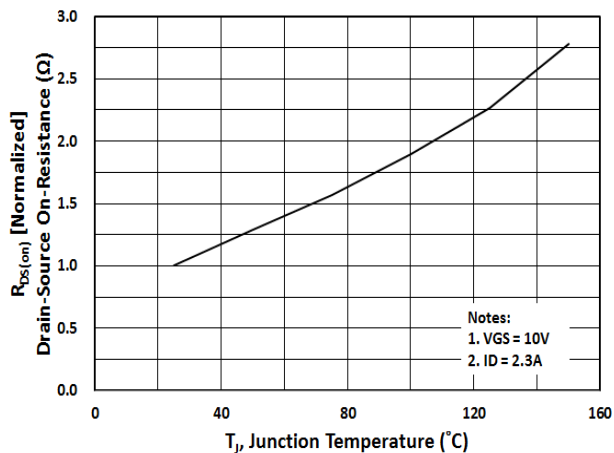
On-Resistance vs. Drain Current



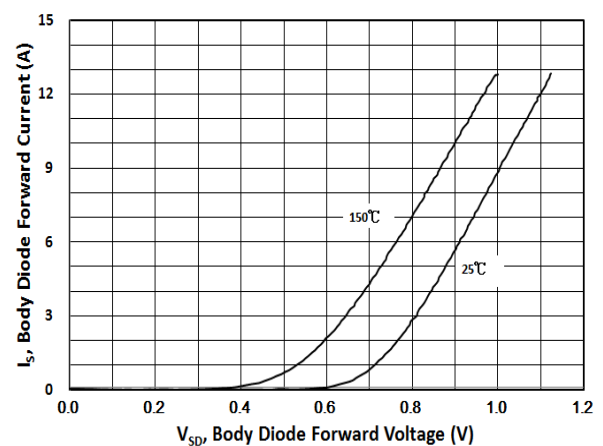
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



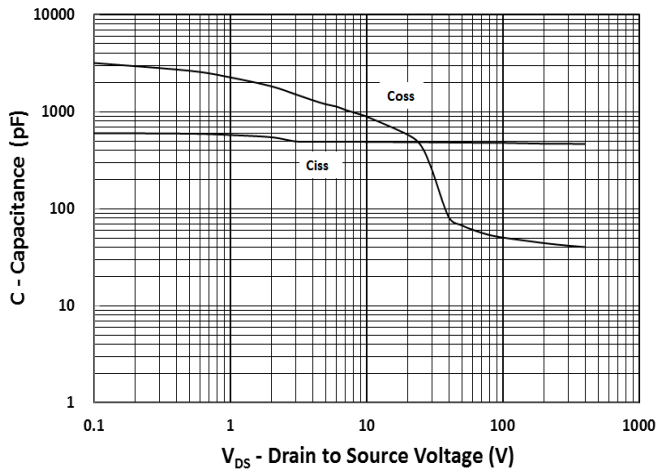
Source-Drain Diode Forward Current vs. Voltage



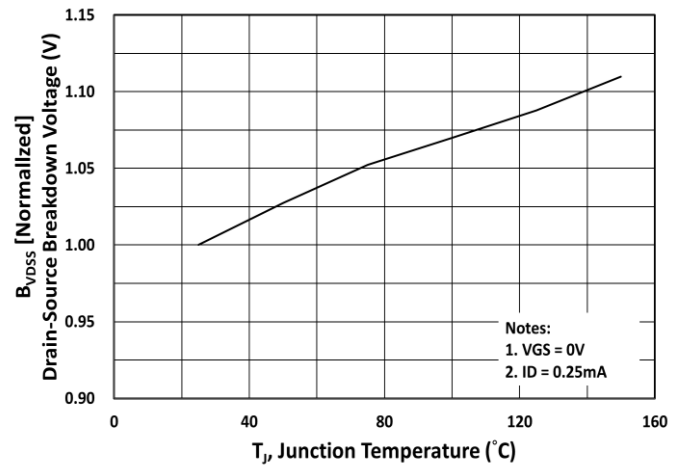
CHARACTERISTICS CURVES

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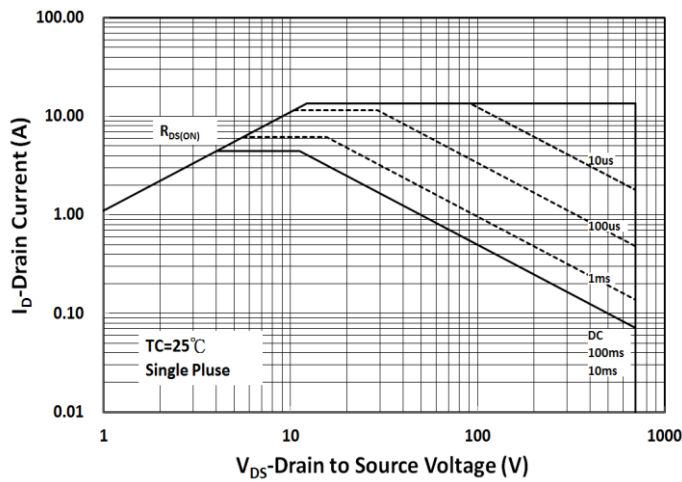
Capacitance vs. Drain-Source Voltage



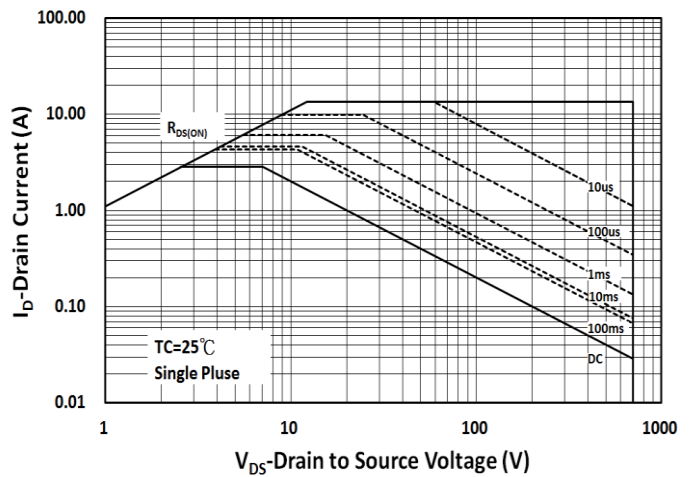
BV_{DSS} vs. Junction Temperature



Maximum Safe Operating Area (DPAK/IPAK)



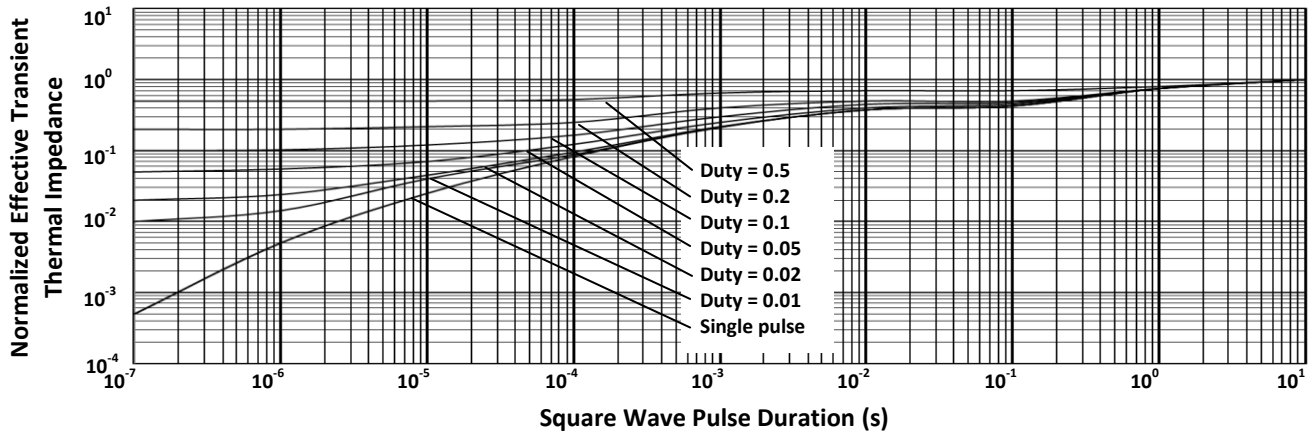
Maximum Safe Operating Area (ITO-220)



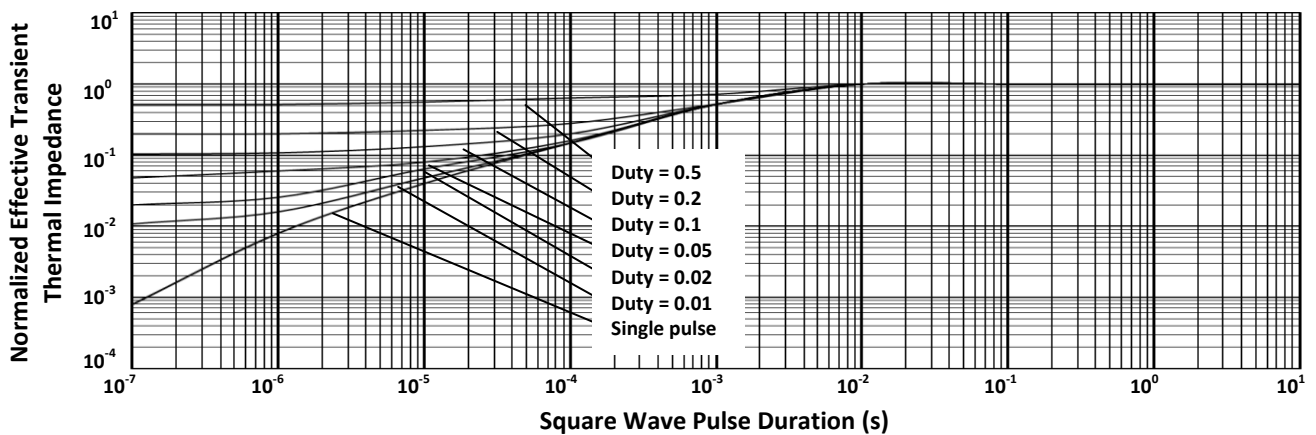
ELECTRICAL CHARACTERISTICS CURVES

($T_C = 25^\circ\text{C}$ unless otherwise noted)

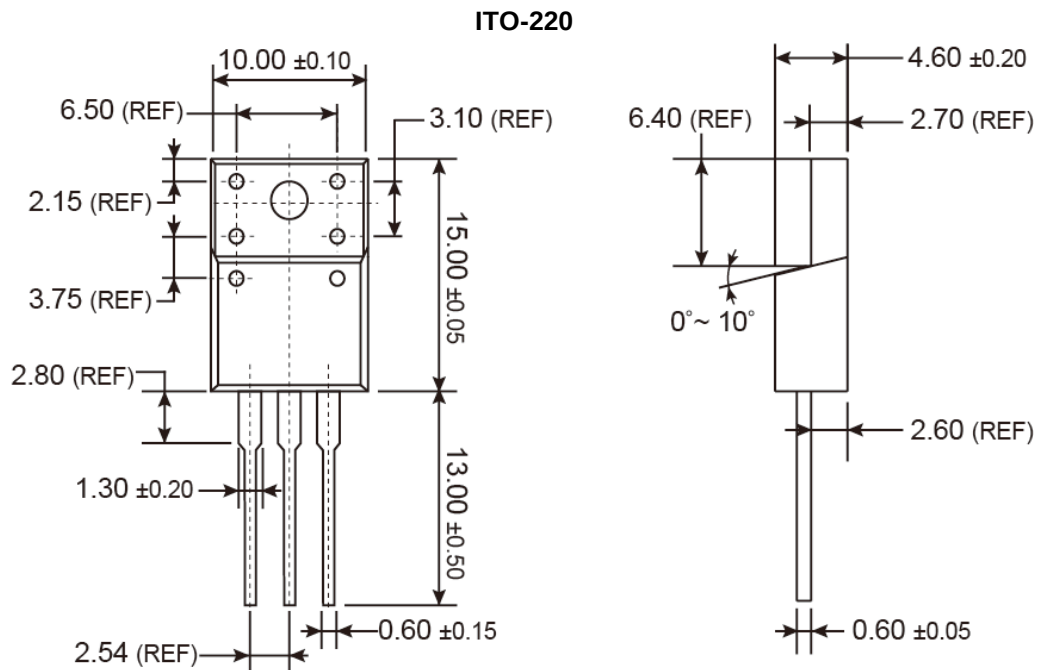
Normalized Thermal Transient Impedance, Junction-to-Case (ITO-220)



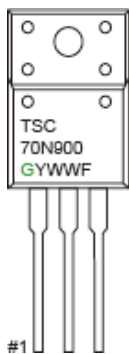
Normalized Thermal Transient Impedance, Junction-to-Case (DPAK/IPAK)



PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)



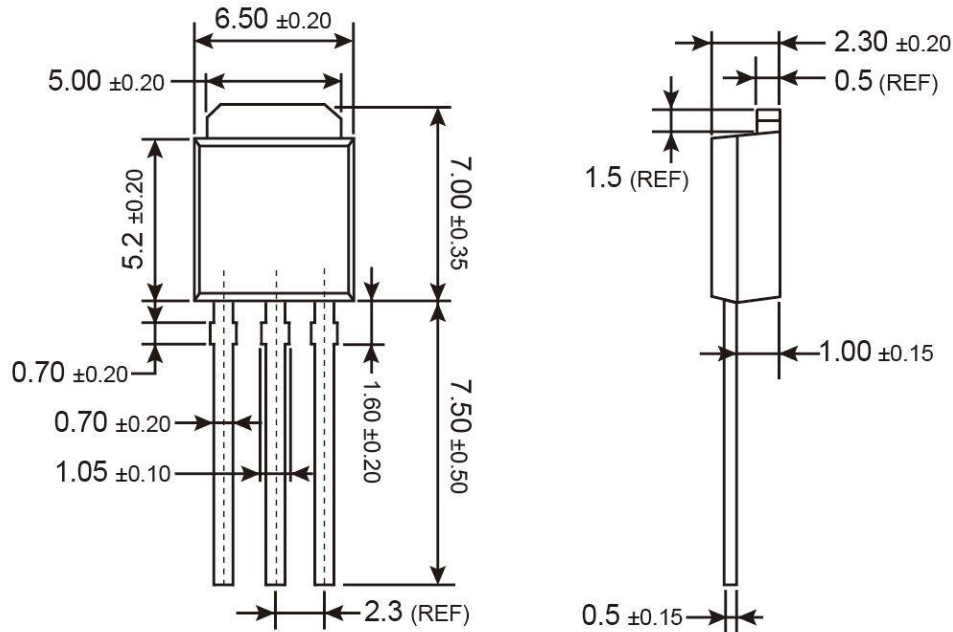
MARKING DIAGRAM



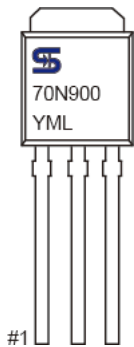
- G** = Halogen Free
- Y** = Year Code
- WW** = Week Code (01~52)
- F** = Factory Code

PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

TO-251

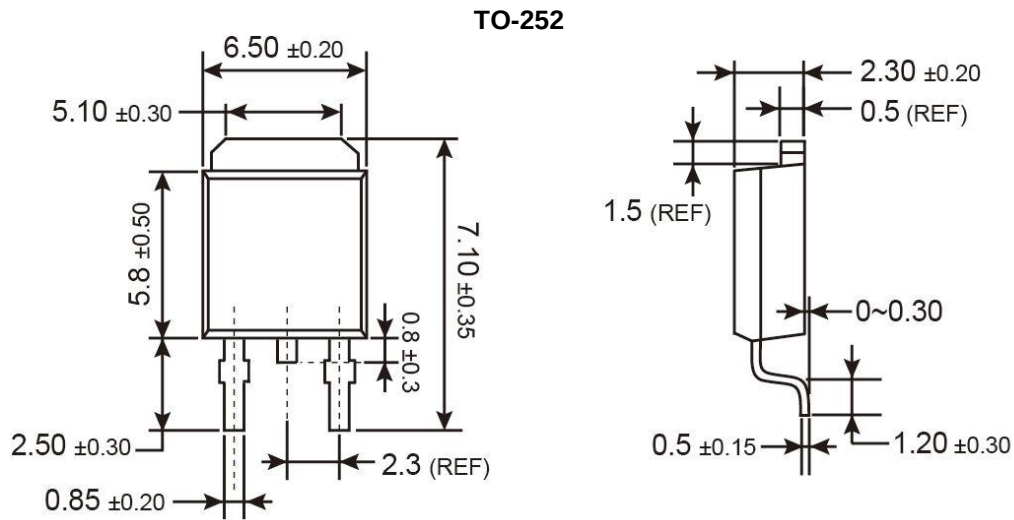


MARKING DIAGRAM

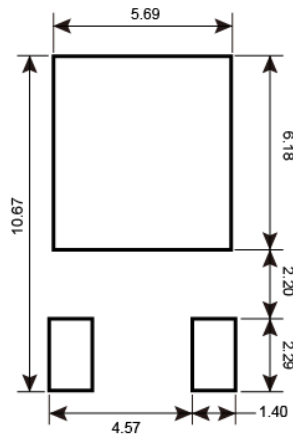


Y = Year Code
M = Month Code for Halogen Free Product
O =Jan **P** =Feb **Q** =Mar **R** =Apr
S =May **T** =Jun **U** =Jul **V** =Aug
W =Sep **X** =Oct **Y** =Nov **Z** =Dec
L = Lot Code (1~9, A~Z)

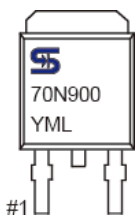
PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



Y = Year Code
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O =Jan **P** =Feb **Q** =Mar **R** =Apr
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- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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