# TMS320DM8127 DaVinci™ Video Processors

**Check for Samples: TMS320DM8127**

## 1 High-Performance System-on-Chip (SoC)

### 1.1 Features

- High-Performance DaVinci Video Processors
  - Up to 1-GHz ARM® Cortex®-A8 RISC Core
  - Up to 750-MHz C674x VLIW DSP
  - Up to 6000 MIPS and 4500 MFLOPS
  - Fully Software-Compatible with C67x+, C64x+
- ARM Cortex-A8 Core
  - ARMv7 Architecture
    - In-Order, Dual-Issue, Superscalar Processor Core
    - Neon™ Multimedia Architecture
    - Supports Integer and Floating Point
    - Jazelle® RCT Execution Environment
- ARM Cortex-A8 Memory Architecture
  - 32KB of Instruction and Data Caches
  - 256KB of L2 Cache
  - 64KB of RAM, 48KB of Boot ROM
- TMS320C674x Floating-Point VLIW DSP
  - 64 General-Purpose Registers (32-Bit)
  - Six ALU (32-/40-Bit) Functional Units
    - Supports 32-Bit Integer, SP (IEEE Single Precision/32-Bit) and DP (IEEE Double Precision/64-Bit) Floating Point
    - Supports up to Four SP Adds Per Clock and Four DP Adds Every Two Clocks
    - Supports up to Two Floating-Point (SP or DP) Approximate Reciprocal or Square Root Operations Per Cycle
  - Two Multiply Functional Units
    - Mixed-Precision IEEE Floating-Point Multiply Supported up to:
      - 2 SP x SP → SP Per Clock
      - 2 SP x SP → DP Every Two Clocks
      - 2 SP x DP → DP Every Three Clocks
      - 2 DP x DP → DP Every Four Clocks
    - Fixed-Point Multiply Supports Two 32 x 32 Multiplies, Four 16 x 16-Bit Multiplies Including Complex Multiplies, or Eight 8 x 8-Bit Multiplies per Clock Cycle
- 128KB of On-Chip Memory Controller (OCMC) RAM
- Imaging Subsystem (ISS)
  - Camera Sensor Connection
    - Parallel Connection for Raw (up to 16-Bit) and BT.656 or BT.1120 (8- and 16-Bit)
    - CSI2 Serial Connection
  - Image Sensor Interface (ISIF) for Handling Image and Video Data From the Camera Sensor
  - Image Pipe Interface (IPIPEIF) for Image and Video Data Connection Between Camera Sensor, ISIF, IPIPE, and DRAM
  - Image Pipe (IPIPE) for Real-Time Image and Video Processing
  - Resizer
    - Resizing Image and Video From 1/16x to 8x
    - Generating Two Different Resizing Outputs Concurrently
  - Hardware 3A Engine (H3A) for Generating Key Statistics for 3A (AE, AWB, and AF) Control
- Face Detect Engine (FD)
  - Hardware Face Detection for up to 35 Faces at OPP100
- Programmable High-Definition Video Image Coprocessing (HDVICP v2) Engine
  - Encode, Decode, Transcode Operations
  - H.264, MPEG-2, VC-1, MPEG-4, SP/ASP, JPEG/MJPEG
- Media Controller
  - Controls the HDVPSS and ISS
- Endianness
  - ARM and DSP Instructions/Data – Little Endian
- HD Video Processing Subsystem (HDVPSS)
  - One 165-MHz HD Video Capture Input
    - One 16- or 24-Bit Input, Splittable into Dual 8-Bit SD Capture Ports
  - Two 165-MHz HD Video Display Outputs
    - One 16-, 24-, or 30-Bit Output and One 16- or 24-Bit Output
  - Composite or S-Video Analog Output
  - Macrovision® Support Available
  - Digital HDMI 1.3 Transmitter With Integrated PHY
  - Advanced Video Processing Features Such as Scan, Format, Rate Conversion
  - Three Graphics Layers and Compositors
- Dual 32-Bit DDR2/DDR3 SDRAM Interfaces
  - Supports up to DDR2-800 and DDR3-1066
  - Up to Eight x 8 Devices Total 2GB of Total Address Space
  - Dynamic Memory Manager (DMM)

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

    - Programmable Multi-Zone Memory Mapping and Interleaving
    - Enables Efficient 2D Block Accesses
    - Supports Tiled Objects in 0°, 90°, 180°, or 270° Orientation and Mirroring
    - Optimizes Interlaced Accesses
- General-Purpose Memory Controller (GPMC)
  - 8- or 16-Bit Multiplexed Address and Data Bus
  - 512MB of Address Space Divided Among up to 8 Chip Selects
  - Glueless Interface to NOR Flash, NAND Flash (BCH/Hamming Error Code Detection), SRAM and Pseudo-SRAM
  - Error Locator Module (ELM) Outside of GPMC to Provide Up to 16-Bit or 512-Byte Hardware ECC for NAND
  - Flexible Asynchronous Protocol Control for Interface to FPGA, CPLD, ASICs, and so Forth
- Enhanced Direct Memory Access (EDMA) Controller
  - Four Transfer Controllers
  - 64 Independent DMA Channels and 8 Independent QDMA Channels
- Dual Port Ethernet (10/100/1000 Mbps) With Optional Switch
  - IEEE 802.3 Compliant (3.3-V I/O Only)
  - MII/RMII/GMII/RGMII Media Independent Interfaces
  - Management Data I/O (MDIO) Module
  - Reset Isolation
  - IEEE 1588 Time-Stamping, AVB, and Industrial Ethernet Protocols
- Dual USB 2.0 Ports With Integrated PHYs
  - USB2.0 High- and Full-Speed Clients
  - USB2.0 High-, Full-, and Low-Speed Hosts, or OTG
  - Supports End Points 0–15
- One PCI Express 2.0 Port With Integrated PHY
  - Single Port With One Lane at 5.0 GT/s
  - Configurable as Root Complex or Endpoint
- Eight 32-Bit General-Purpose Timers (Timer1–8)
- One System Watchdog Timer (WDT0)
- Six Configurable UART/IrDA/CIR Modules
  - UART0 With Modem Control Signals
  - Supports up to 3.6864 Mbps UART0/1/2
  - Supports up to 12 Mbps UART3/4/5
  - SIR, MIR, FIR (4.0 MBAUD), and CIR
- Four Serial Peripheral Interfaces (SPIs) (up to 48 MHz)
  - Each With Four Chip Selects
- Three MMC/SD/SDIO Serial Interfaces (up to 48 MHz)
  - Three Supporting up to 1-, 4-, or 8-Bit Modes
- Four Inter-Integrated Circuit ($I^2C$ Bus) Ports
- Six Multichannel Audio Serial Ports (McASPs)
  - Dual Ten Serializer Transmit and Receive Ports
  - Quad Four Serializer Transmit and Receive Ports
  - DIT-Capable For S/PDIF (All Ports)
- Multichannel Buffered Serial Port (McBSP)
  - Transmit and Receive Clocks up to 48 MHz
  - Two Clock Zones and Two Serial Data Pins
  - Supports TDM, I2S, and Similar Formats
- Real-Time Clock (RTC)
  - One-Time or Periodic Interrupt Generation
- Up to 128 General-Purpose I/O (GPIO) Pins
- One Spin Lock Module with up to 128 Hardware Semaphores
- One Mailbox Module with 12 Mailboxes
- On-Chip ARM ROM Bootloader (RBL)
- Power, Reset, and Clock Management
  - Multiple Independent Core Power Domains
  - Multiple Independent Core Voltage Domains
  - Support for Three Operating Points (OPP100, OPP120, OPP166) per Voltage Domain
  - Clock Enable and Disable Control for Subsystems and Peripherals
- 32KB of Embedded Trace Buffer (ETB) and 5-Pin Trace Interface for Debug
- IEEE 1149.1 (JTAG) Compatible
- 684-Pin Pb-Free BGA Package (CYE Suffix), 0.8-mm Ball Pitch With Via Channel Technology to Reduce PCB Cost
- 45-nm CMOS Technology

## 1.2 Applications

- IP Network Cameras
- Industrial Automation Network Cameras
- Stereo Cameras
- HD Video Conferencing
- Car Black Box
- Home Audio and Video Equipment


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## 1.3 Description

TMS320DM8127 DaVinci Digital Media processors are highly integrated, programmable platforms that leverage the technology to meet the processing needs of the following applications to name a few:

- IP Network Cameras
- Industrial Automation Network Cameras
- Stereo Cameras
- Video Surveillance
- HD Video Conferencing
- Car Black Box
- Home Audio and Video Equipment

The device enables Original-Equipment Manufacturers (OEMs) and Original-Design Manufacturers (ODMs) to quickly bring to market devices featuring robust operating systems support, rich user interfaces, and high processing performance through the maximum flexibility of a fully integrated mixed processor solution. The device also combines programmable video and audio processing with a highly integrated peripheral set.

Programmability is provided by an ARM Cortex-A8 RISC CPU with Neon extension, TI C674x VLIW floating-point DSP core, and high-definition video and imaging coprocessors. The ARM lets developers keep control functions separate from A/V algorithms programmed on the DSP and coprocessors, thus reducing the complexity of the system software. The ARM Cortex-A8 32-Bit RISC Core with Neon floating-point extension includes: 32KB of Instruction cache; 32KB of Data cache; 256KB of L2 Cache; 48KB of Boot ROM; and 64KB of RAM.

The rich peripheral set provides the ability to control external peripheral devices and communicate with external processors. For details on each of the peripherals, see the related sections in this document and the associated peripheral reference guides. The peripheral set includes:

- HD Video Processing Subsystem
- Dual Port Gigabit Ethernet MACs (10/100/1000 Mbps) [Ethernet Switch] with MII/RMII/GMII/RGMII and MDIO interface supporting IEEE 1588 Time-Stamping, AVB, and Industrial Ethernet Protocols
- Two USB ports with integrated 2.0 PHY
- PCIe x1 GEN2 Compliant interface
- Two 10-serializer McASP audio serial ports (with DIT mode)
- Four quad-serilaizer McASP audio serial ports (with DIT mode)
- One McBSP multichannel buffered serial port
- Six UARTs with IrDA and CIR support
- Four SPI serial interfaces
- Three MMC/SD/SDIO serial interfaces
- Four $I^2C$ master and slave interfaces
- Parallel Camera Interface (CAM)
- Up to 128 General-Purpose I/Os (GPIOs)
- Eight 32-bit general-purpose timers
- System watchdog timer
- Dual DDR2, and DDR3 SDRAM interfaces
- Flexible 8- or 16-bit asynchronous memory interface
- Two Controller Area Network (DCAN) modules
- Spin Lock
- Mailbox

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The TMS320DM8127 DaVinci Digital Media processors also include a high-definition video and imaging coprocessor 2 (HDVICP2) to off-load many video and imaging processing tasks from the DSP core, making more DSP MIPS available for common video and imaging algorithms. Additionally, the TMS320DM8127 DaVinci Digital Media processors have a complete set of development tools for both the ARM and DSP which include C compilers, a DSP assembly optimizer to simplify programming and scheduling, and a Microsoft® Windows™ debugger interface for visibility into source code execution.

The C674x DSP core is the high-performance floating-point DSP generation in the TMS320C6000 DSP platform and is code-compatible with previous generation C64x Fixed-Point and C67x Floating-Point DSP generation. The C674x Floating-Point DSP processor uses 32KB of L1 program memory with EDC and 32KB of L1 data memory. Up to 32KB of L1P can be configured as program cache. The remaining memory is noncacheable no-wait-state program memory. Up to 32KB of L1D can be configured as data cache. The remaining memory is noncacheable no-wait-state data memory. The DSP has 256KB of L2 RAM with ECC, which can be defined as SRAM, L2 cache, or a combination of both. All C674x L3 and off-chip memory accesses are routed through an MMU.


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## 1.4 Functional Block Diagram

Figure 1-1 shows the functional block diagram of the device.

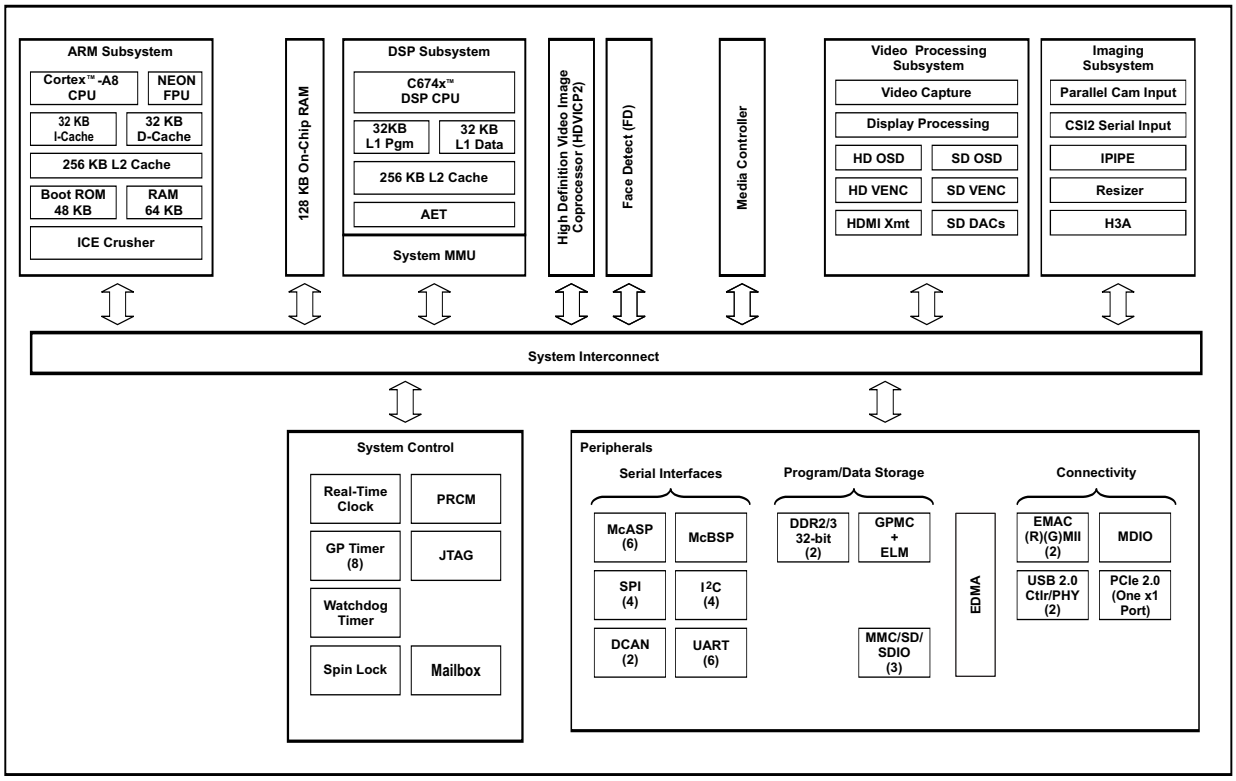


**Figure 1-1. TMS320DM8127 DaVinci Digital Media Processors Functional Block Diagram**

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# 2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

This data manual revision history highlights the technical changes made to the SPRS712A device-specific data manual to make it an SPRS712B revision and also highlights the technical changes made to the SPRS712B device-specific data manual to make it an SPRS712C revision.

**Scope:** Applicable updates to the DM812x DaVinci™ Video DMP device family, specifically relating to the TMS320DM8127 devices(Silicon Revision 3.0, 2.1), which are now in the production data (PD) stage of development have been incorporated.

- Added Supported OPP Combinations table (**Revision C Change**)
- Updated/Changed Power-Up Sequence
- Updated/Changed Power-Down Sequence
- Added RXACTIVE Function (Bit 18) to PINCTRLx Register Description
- Added Power-On Hours (POH) section
- Added Latch-Up Performance Absolute Maximum Ratings
- DDR2/DDR3 supports up to 533 MHz
- OPP50 is **not** supported
- SmartReflex™ (AVS) is **not** supported
- Deep Sleep Mode is **not** supported
- HDMI HDCP encryption is **not** supported
- Added new Device Comparison table

| SEE | ADDITIONS/MODIFICATIONS/DELETIONS |
|---|---|
| **Revision B, December 2013 to Revision C, February 2014** | |
| Global | • Document now released to ti.com<br>• Updated/Changed "DM812x" references to "DM8127" |
| Section 8.2.2.1 Dynamic Voltage Frequency Scaling (DVFS) | • Added Table 8-5, *Supported OPP Combinations* |
| **Revision A, September 2012 to Revision B, December 2013** | |
| Global | • Replaced all instances of "DSP/EDMA MMU" with "**System MMU**"<br>• Deleted all references to OPP50 and Deep Sleep Mode<br>• Updated/Changed the DM812x Davinci...data manual title |
| Section 1 Features | • Updated/Changed description the HD Video Processing Subsystem (HDVPSS)<br>• Updated/Changed the Dual 32-Bit DDR2/DDR3 SDRAM Interfaces sub-bullet from "Supports up to DDR2-800 and DDR3-**800**" to "Supports up to DDR2-800 and DDR3-**1066**" |
| Section 3.1 Device Comparison | Table 3-1, DM8127 Device Comparison:<br>• Added Device Comparison Table **[New]** |
| Section 3.2 Device Characteristics | Table 3-2, Characteristics of the Processor:<br>• Updated/Changed the HD Video Processing Subsystem (HDVPSS) row<br>• Updated/Changed Core Logic (V), OPP100, OPP120 range from "0.95 V – 1.20 V" to "1.10 V – 1.20 V" |
| Section 3.12.3.2 L4 Slow Peripheral Memory Map | Table 3-6, L4 Slow Peripheral Memory Map:<br>• Updated/Changed 0x4818_8000–0x4818_BFFF Device Name from "SmartReflex0/1 Peripheral and Support Registers" to **"Reserved"**<br>• Updated/Changed 0x4819_0000–0x4819_3FFF Device Name from "SmartReflex2/3 Peripheral and Support Registers" to **"Reserved"** |

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| SEE | ADDITIONS/MODIFICATIONS/DELETIONS |
|---|---|
| Section 4.2.8 General-Purpose Input/Outputs (GPIOs) | Table 4-12, GP1 Terminal Functions:<br>• Added "The ENLVCMOS bit in the MLBP_DAT_IO_CTRL register...." to the pin descriptions for pins GP1[10:7] (V2, V1, W2, and W1 respectively). |
| Section 4.2.25 Reserved Pins | Table 4-47, Reserved Terminal Functions:<br>• Updated/Changed TYPE for Signal No. Y14 (RSV4) and AC8 (RSV5) from "S" to **"I"** |
| Section 5 Device Configurations | Section 5.3, Pin Multiplexing Control:<br>• Updated/Changed bit 18 from "RSV" to "RXACTIVE" |
| | Table 5-11, PINCNTL1 – PINCNTL270 (PINCNTLx) Registers Bit Descriptions:<br>• Updated/Changed the MUXMODE[7:0] Description from "Values other than those ..." to **"A value of zero results ..."**<br>• Updated/Changed bit 18 description to now support RXACTIVE |
| | Table 5-13, PINCNTLx Registers MUXMODE Functions:<br>• Updated/Changed PINCNTL173 row under 0x20 from "UART2_TXD(M1)" to **"UART2_TXD(M0)"**<br>• Updated/Changed PINCNTL231 under 0x80 from "GP3[30](M0)" to **"GP3[30](M1)"** |
| | Section 5.4, Handling Unused Pins:<br>• Added "Unless otherwise noted" to the beginning of, "All supply pins must always ..." |
| Section 7 Device Operating Conditions | Section 7.1, Absolute Maximum Ratings:<br>• Deleted the "V I/O...(Transient Overshoot/Undershoot)" rows of Input and Output voltage ranges<br>• Added Latch-Up Performance row and Latch-Up footnotes<br>• Updated/Changed ESD-HBM footnote to "Level listed is passing level per ANSI/ESDA/JEDEC J5-001..."<br>• Updated/Changed ESD-CDM footnote to "Level listed is passing level per EIA-JEDEC JESD22-C101E..." |
| | Section 7.3, Power on Hours (POH):<br>• Added Power-On Hour (POH) section **[New]** |
| Section 8.2.2.1 Dynamic Voltage Frequency Scaling (DVFS) | Table 8-4, Device Operating Points (OPPs):<br>• Updated/Changed the CYEx0, 120% (1.2 V) Cortex A8 (MHz) speed from "–" to "720"<br>• Updated/Changed the CYEx0, 120% (1.2 V) DSP (MHz) speed from "–" to "600"<br>• Updated/Changed the CYEx2, 166% (1.35 V) DSP (MHz) speed from "–" to "700"<br>• Updated/Changed the CYEx2, 166% (1.35 V) HDVICP2 (MHz) speed from "430" to "410" |
| Section 8.2.8.1 Power-Up Sequence | Table 8-6 , Power-Up Sequence Ramping Values:<br>• Added NO. 1 MIN value of "0" ms.<br>• Updated/Changed NO. 1 description to "1.8 V and DVDD_DDR[x] supplies stable..."<br>• Added NO. 13, "CVDD variable supply ramp...."<br>• Updated/Changed Figure 8-1 according to table changes<br>• Deleted 3.3 V Supplies Rising Before 1.8 V Supplies Delta Figure (was Figure 7.2) and associated footnote references<br>• Deleted footnote, "The 3.3 V supplies must be..." |
| Section 8.2.8.2 Power-Down Sequence | Section 8.2.8.2, Power-Down Sequence:<br>• Added, "Ramping down all supplies at the same time...For proper device..." paragraph |
| | Table 8-7, Power-Down Sequence Ramping Values:<br>• Updated/Changed "The 1.5-/1.8-V DVDD_DDR[x]..." footnote<br>• Updated/Changed figure reference to Figure 8-3<br>• Added NO. 14, "CVDD_x variable supplies ramp-down..."<br>• Added associated footnote, "CVDD_x must never exceed CVDD by more than 150mV" |
| | Figure 8-2, Power-Down Sequence:<br>• Updated/Changed figure according to table changes |
| | Figure 8-3,1.8 V Supplies Falling Before 3.3 V Supplies Delta:<br>• Added figure **[New]** |


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| SEE | ADDITIONS/MODIFICATIONS/DELETIONS |
|---|---|
| Section 8.4 Clocking | Section 8.4.1.1, Using the Internal Oscillators:<br>Table 8-11, Requirements for Crystal Circuit on the Device Oscillator (DEVOSC):<br>• Added three conditions and the MAX values to the Crystal Frequency Stability PARAMETER |
| | Table 8-15, Timing Requirements for DEVOSC_MXI/DEV_CLKIN<br>• Added three conditions and the MAX values to the Frequency Stability PARAMETER |
| | Section 8.4.3, AUD_CLKINx Input Clocks:<br>• Added section **[New]** |
| | Section 8.4.4, CLKIN32 Input Clock:<br>• Added "/8" to the TIMER1/2/3/4/5/6/7 bullet |
| | Section 8.4.7, Input/Output Clocks Electrical Data/Timing:<br>• Added Table 8-17, Timing Requirements for AUD_CLKINx **[New]**<br>• Added Figure 8-14, AUD_CLKINx Timing **[New]** |
| | Section 8.4.8, PLLs:<br>• Deleted PLL Electrical Data/Timing subsection |
| Section 8.4.9 SYSCLKs | Table 8-26, Maximum SYSCLK Clock Frequencies:<br>• Added footnote, "The maximum frequencies listed..." |
| Section 8.4.10 Module Clocks | Table 8-27, Maximum Module Clock Frequencies:<br>• Updated/Changed Media Controller **CLOCK SOURCES** from "PLL_MEDIACTL" to "PLL_MEDIACTL/2"<br>• Updated/Changed Media Controller **MAX FREQUENCY OPP100 (MHz)** value from "400" to "200"<br>• Added footnote, "The maximum frequencies listed..." |
| Section 9.4 EDMA | Section 9.4.1, EDMA Channel Synchronization Events:<br>• Updated/Changed paragraphs |
| | Section 9.4.2, EDMA Peripheral Register Descriptions:<br>• Added Table 9-5, EDMA Channel Controller (EDMA TPCC) Control Registers<br>• Added Table 9-6, EDMA Transfer Controller (EDMA TPTC) Control Registers |
| Section 9.5.3 IEEE 1149.1 JTAG | Table 9-8, JTAG ID Register Table:<br>• Added silicon-revision specific information to the VARIANT bit field |
| Section 9.6.2.3 EMAC RGMII Electrical Data/Timing | • Updated/Changed all instances of "at DSP" to "at device" |
| Section 9.10.1 HDVPSS Electrical Data/Timing | Table 9-42, Timing Requirements for HDVPSS Input:<br>• Deleted NO. 7, $t_{t(CLK)}$, Transition time, VIN[x]A_CLK (10%-90%)<br>• Deleted NO. 7, $t_{t(CLK)}$, Transition time, VIN[x]B_CLK (10%-90%) |
| Section 9.13.4, DDR2/DDR3 Memory Controller Electrical Data/Timing | Table 9-53, Switching Characteristics Over Recommended Operating Conditions for DDR2/DDR3 Memory Controller:<br>• Updated/Changed NO. 1, $t_{c(DDR_CLK)}$ , Cycle time, DDR[x]_CLK, **DDR2/DDR3 mode** to **DDR2 mode**<br>• Added additional row to NO.1, $t_{c(DDR_CLK)}$, Cycle time, DDR[x]_CLK: **DDR3 mode** |
| Section 9.13.4.1 DDR2 Routing Specifications | Section 9.13.4.1.1.1, DDR2 Interface Schematic:<br>• Updated/Changed the sentence from, "... pins by pulling the non-inverted DQS pin..." to **"... DDR[x]_DQS[n] pins to the corresponding..."**<br>• Updated/Changed a sentence from, "... inverted DQS pin..." to "... **$\overline{\text{DDR[x]_DQS[n]}}$ pins...**"<br>• Added sentence, "The DVDD_DDR[x] and VREFSSTL_DDR[x] power..." |
| Section 9.13.4.1.2 DDR2 CK and ADDR_CTRL Routing | Table 9-63, CK and ADDR_CTRL Routing Specification:<br>• Updated/Changed the "Series terminator,...the DSP" footnote to "Series terminator,..the processor" |
| Section 9.13.4.2 DDR3 Routing Specifications | Section 9.13.4.2.4, DDR3 Interface Schematic:<br>• Combined 16-Bit and 32-Bit DDR3 Interface subsections<br>• Deleted repeated figure references<br>• Deleted the sentence, "and the unused DQS.....pulled to ground via 1-kΩ resistors."<br>• Added sentence, "The DVDD_DDR[x] and VREFSSTL_DDR[x]..." |

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| SEE | ADDITIONS/MODIFICATIONS/DELETIONS |
|---|---|
| Section 9.13.4.2.4.1 Compatible JEDEC DDR3 Devices | Table 9-66, Compatible JEDEC DDR3 Devices (Per Interface):<br>• Updated/Changed the max clock rate in footnote, "DDR3 devices with speed...." from "400" MHz to "533" MHz |
| Section 9.14.3 McASP (McASP[5:0]) Electrical Data/Timing | Table 9-78, Timing Requirements for McASP:<br>• Updated/Changed **McASP1 Only** ACLKR/X ext out, MIN value for NO. 5, $t_{su(AFSRX-ACLKRX)}$, Setup time, MCA[x]_AFSR/X input valid before MCA[X]_ACLKR/X from "4" to **"2"** ns.<br>• Updated/Changed **McASP1 Only** ACLKR/X ext out, MIN value for NO. 7,$t_{su(AXR-ACLKRX)}$, Setup time, MCA[x]_AXR input valid before MCA[X]_ACLKR/X from "4" to **"2"** ns. |
| Section 9.15 Multichannel Buffered Serial Port (McBSP) | Table 9-80, McBSP Registers:<br>• Updated/Changed McBSP HEX ADDRESS range from "0x4700 0000 - 0x4700 00C0" to **"0x4700 0100 – 0x4700 01C0"** (DDR_REG to STATUS_REG)<br>• Added McBSP registers in HEX ADDRESS range **"0x4700 0000 – 0x4700 004C"** (REVNB to DMATXWAKE_EN) |
| Section 10.1.2 Device and Development-Support Tool Nomenclature | Figure 10-1, Device Nomenclature:<br>• Deleted DM8128 Device |


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# 3 Device Overview

## 3.1 Device Comparison

Table 3-1 shows a comparison between devices, highlighting the differences.

**Table 3-1. DM8127 Device Comparison**

| FEATURES | | DEVICES | |
|---|---|---|---|
| | | TMS320DM8148S | TMS320DM8127 |
| ARM L2 CACHE | | 512KB | 256KB |
| SATA | | YES | NONE |
| HDVPSS | Video Ports (Inputs) | VIN[0]/VIN[1] | VIN[0] |
| | Video Ports (Outputs) | VOUT[0]/VOUT[1] | VOUT[0]/VOUT[1] |
| SGX530 | | YES | NONE |
| ISS: CSI2 | | YES | YES |
| ISS: IPIPE | | YES | YES |
| ISS: H3A | | YES | YES |
| Face Detect | | NONE | YES |

## 3.2 Device Characteristics

Table 3-2 provides an overview of the TMS320DM8127 DaVinci™ Digital Media Processors, which includes significant features of the device, including the capacity of on-chip RAM, peripherals, and the package type with pin count.

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**Table 3-2. Characteristics of the Processor**

| HARDWARE FEATURES | | DM8127 |
|---|---|---|
| Peripherals<br><br>Not all peripherals pins are available at the same time (for more details, see the Device Configurations section). | HD Video Processing Subsystem (HDVPSS) | 1 16-/24-bit HD Capture Port **or**<br>2 8-bit SD Capture Ports<br>**and**<br>1 8-bit SD Capture Port<br>**and**<br>1 16-/24-/30-bit HD Display Port **or**<br>1 8-/16-/24-bit HD Capture Port<br>**and**<br>1 16-24-bit HD Display Port<br>**and**<br>1 HDMI 1.3 Transmitter<br>**and**<br>2 SD Video DACs |
| | Imaging Subsystem (ISS) | 1 Parallel Camera Input for Raw (up to 16-bit)<br>and BT.656/BT.1120 (8/16-bit)<br>***and***<br>1 CSI2 Serial Input |
| | DDR2/3 Memory Controller | 2 (32-bit Bus Widths) |
| | GPMC + ELM | Asynchronous (8-/16-bit bus width)<br>RAM, NOR, NAND |
| | EDMA | 64 Independent Channels<br>8 QDMA Channels |
| | 10/100/1000 Ethernet MAC Switch with Management Data Input/Output (MDIO) | 1 (with 2 MII/RMII/GMII/RGMII Interfaces) |
| | USB 2.0 | 2 (Supports High- and Full-Speed as a Device and<br>High-, Full-, and Low-Speed as a Host, or OTG) |
| | PCI Express 2.0 | 1 Port (1 5.0GT/s lane) |
| | Timers | 8 (32-bit General purpose)<br>***and***<br>1 (System Watchdog) |
| | UART | 6 (with SIR, MIR, FIR, CIR support and RTS/CTS flow control)<br>(UART0 Supports Modem Interface) |
| | SPI | 4 (Supports 4 slave devices) |
| | MMC/SD/SDIO | 1 (1-bit or 4-bit or 8-bit modes)<br>***and***<br>1 (8-bit mode) ***or***<br>2 (1-bit or 4-bit modes) |
| | I2C | 4 (Master/Slave) |
| | Media Controller | Controls HDVPSS, HDVICP2, and ISS |
| | McASP | 6 (10/10/4/4/4/4 Serializers, Each with Transmit/Receive and DIT capability) |
| | McBSP | 1 (2 Data Pins, Transmit/Receive) |
| | Controller Area Network (DCAN) | 2 |
| | RTC | 1 |
| | GPIO | Up to 128 pins |
| | Parallel Camera Interface (CAM) | 1 |
| | Spin Lock Module | 1 (up to 128 H/W Semaphores) |
| | Mailbox Module | 1 (with 12 Mailboxes) |
| | Size (Bytes) | 832KB RAM, 48KB ROM |


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**Table 3-2. Characteristics of the Processor (continued)**

| HARDWARE FEATURES | | | DM8127 |
|---|---|---|---|
| On-Chip Memory | Organization | | **ARM**<br>32KB I-cache<br>32KB D-cache<br>256KB L2 Cache<br>64KB RAM<br>48KB Boot ROM |
| | | | **DSP**<br>32KB L1 Program (L1P)/Cache (up to 32KB) with EDC<br>32KB L1 Data (L1D)/Cache (up to 32KB)<br>256KB Unified Mapped RAM/Cache (L2) with ECC |
| | | | **ADDITIONAL SHARED MEMORY**<br>128KB On-chip RAM |
| ARM® Cortex®-A8 | Main ID Register Variant/Revision | | r3p2 |
| CPU ID + CPU Rev ID | Control Status Register (CSR.[31:16]) | | 0x1401 |
| C674x Megamodule Revision | Revision ID Register (MM_REVID[15:0]) | | 0x0000 |
| JTAG BSDL ID | DEVICE_ID Register (address location: 0x4814_0600) | | see Section 9.5.3.1, JTAG ID (JTAGID) Register Description |
| CPU Frequency | MHz | | ARM Cortex-A8 up to 1000 MHZ |
| | | | DSP up to 750 MHz |
| Cycle Time | ns | | ARM Cortex -A8 1.0 ns |
| | | | DSP 1.33 ns |
| Voltage | Core Logic (V) | OPP100, OPP120 | 1.10 V – 1.20 V |
| | | OPP166 | 1.35 V |
| | I/O (V) | | 1.5 V, 1.8 V, 3.3 V |
| Package | 23 x 23 mm [Flip Chip Ball Grid Array (FCBGA)] | | 684-Pin BGA (CYE) [with Via Channel Technology] |
| Process Technology | µm | | 0.045 µm |
| Product Status(1) | Product Preview (PP),<br>Advance Information (AI),<br>or Production Data (PD) | | PD |

(1) PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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## 3.3 Device Compatibility

## 3.4 ARM Cortex-A8 Microprocessor Unit (MPU) Subsystem Overview

The ARM Cortex-A8 Subsystem is designed to give the ARM Cortex-A8 Master control of the device. In general, the ARM Cortex-A8 is responsible for configuration and control of the various subsystems, peripherals, and external memories.

The ARM Cortex-A8 Subsystem includes the following features:

- ARM Cortex-A8 RISC processor:
  - ARMv7 ISA plus Thumb2™, JazelleX™, and Media Extensions
  - Neon™ Floating-Point Unit
  - Enhanced Memory Management Unit (MMU)
  - Little Endian
  - 32KB L1 Instruction Cache
  - 32KB L1 Data Cache
  - 256KB L2 Cache
- CoreSight Embedded Trace Module (ETM)
- ARM Cortex-A8 Interrupt Controller (AINTC)
- Embedded PLL Controller (PLL_ARM)
- 64KB Internal RAM
- 48KB Internal Public ROM

Figure 3-1 shows the ARM Cortex-A8 Subsystem for the device.

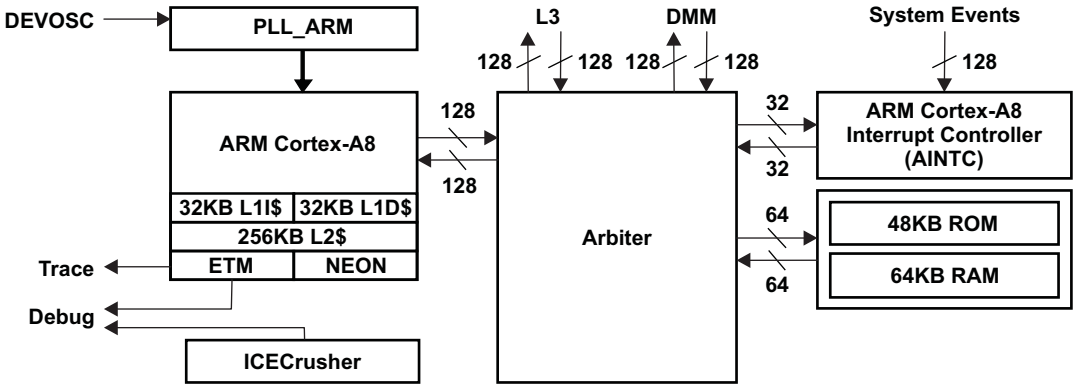


**Figure 3-1. ARM Cortex-A8 Subsystem**

For more details on the ARM Cortex-A8 Subsystem, see the System MMU section of the *Chip Level Resources* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

### *3.4.1 ARM Cortex-A8 RISC Processor*

The ARM Cortex-A8 Subsystem integrates the ARM Cortex-A8 processor. The ARM Cortex-A8 processor is a member of ARM Cortex family of general-purpose microprocessors. This processor is targeted at multi-tasking applications where full memory management, high performance, low die size, and low power are all important. The ARM Cortex-A8 processor supports the ARM debug architecture and includes logic to assist in both hardware and software debug. The ARM Cortex-A8 processor has a Harvard architecture and provides a complete high-performance subsystem, including:

- ARM Cortex-A8 Integer Core
- Superscalar ARMv7 Instruction Set
- Thumb-2 Instruction Set


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- Jazelle RCT Acceleration
- CP14 Debug Coprocessor
- CP15 System Control Coprocessor
- NEON™ 64-/128-bit Hybrid SIMD Engine for Multimedia
- Enhanced VFPv3 Floating-Point Coprocessor
- Enhanced Memory Management Unit (MMU)
- Separate Level-1 Instruction and Data Caches
- Integrated Level-2 Cache
- 128-bit Interconnector-to-System Memories and Peripherals
- Embedded Trace Module (ETM).

### 3.4.2 Embedded Trace Module (ETM)

To support real-time trace, the ARM Cortex-A8 processor provides an interface to enable connection of an embedded trace module (ETM). The ETM consists of two parts:

- The Trace port which provides real-time trace capability for the ARM Cortex-A8.
- Triggering facilities that provide trigger resources, which include address and data comparators, counter, and sequencers.

The ARM Cortex-A8 trace port is not pinned out and is, instead, only connected to the system-level Embedded Trace Buffer (ETB). The ETB has a 32KB buffer memory. ETB enabled debug tools are required to read/interpret the captured trace data.

For more details on the ETM, see Section 9.5.2, *Trace*.

### 3.4.3 ARM Cortex-A8 Interrupt Controller (AINTC)

The ARM Cortex-A8 subsystem contains an interrupt controller (AINTC) that prioritizes all service requests from the system peripherals and generates either IRQ or FIQ to the ARM Cortex-A8 processor. For more details on the AINTC, see Section 8.5.1, *ARM Cortex-A8 Interrupts*.

Note: For General-Purpose devices, the AINTC does not support the generation of FIQs to the ARM processor.

### 3.4.4 ARM Cortex-A8 PLL (PLL_ARM)

The ARM Cortex-A8 subsystem contains an embedded PLL Controller (PLL_ARM) for generating the subsystem's clocks from the DEV Clock input. For more details on the PLL_ARM, see Section 8.4, *Clocking*.

### 3.4.5 ARM MPU Interconnect

The ARM Cortex-A8 processor is connected through the arbiter to both an L3 interconnect port and a DMM port. The DMM port is 128 bits wide and provides the ARM Cortex-A8 direct access to the DDR memories, while the L3 interconnect port is 64 bits wide and provides access to the remaining device modules.

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## 3.5 C674x DSP Overview

The DSP Subsystem includes the following features:

- C674x DSP CPU
- 32KB L1 Program (L1P)/Cache (up to 32KB) with Error Detection Circuitry (EDC)
- 32KB L1 Data (L1D)/Cache (up to 32KB)
- 256KB Unified Mapped RAM/Cache (L2) with Error Correction Circuitry (ECC)
- Little Endian

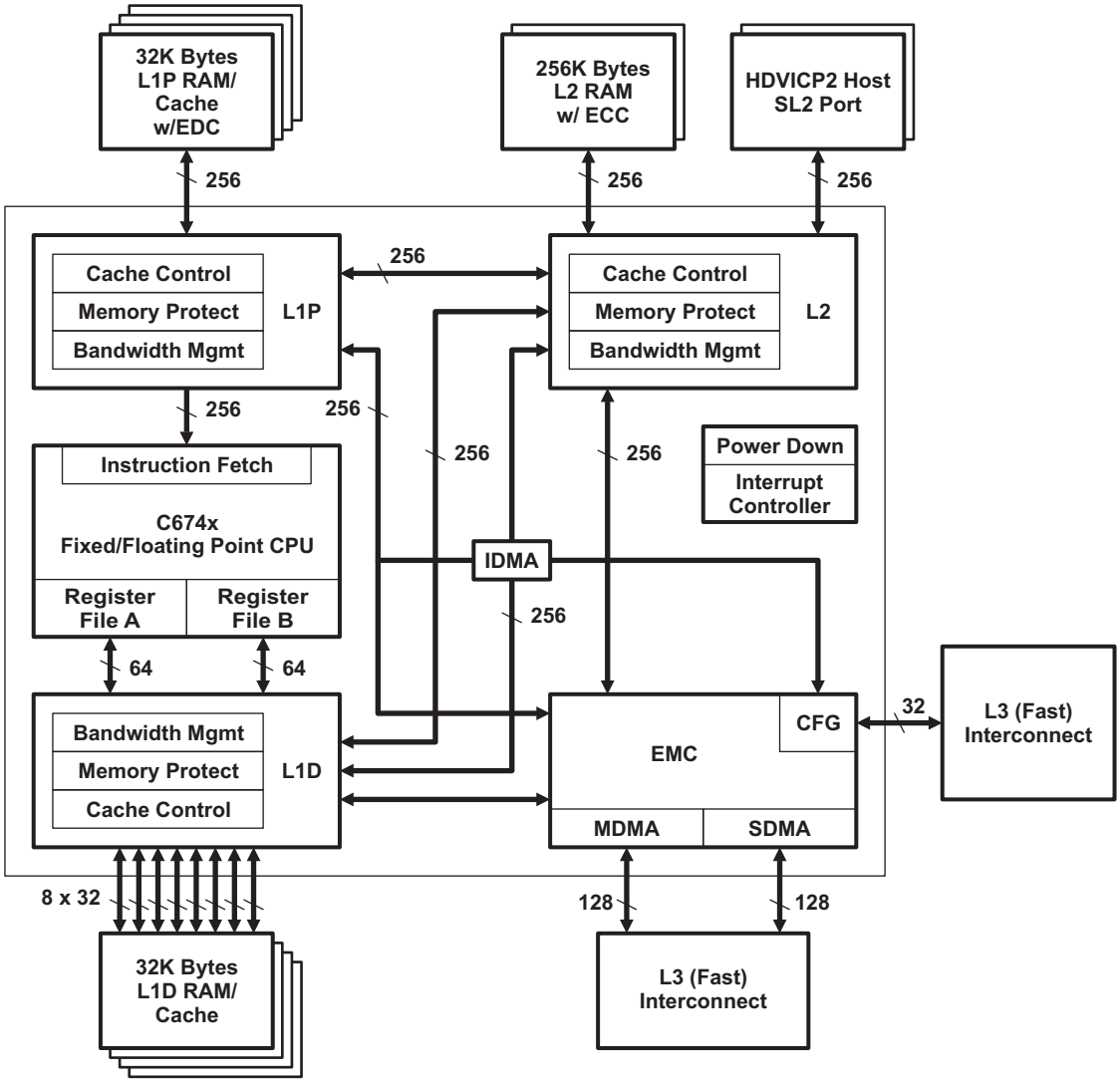


**Figure 3-2. C674x Megamodule Block Diagram**


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### 3.5.1 C674x DSP CPU Description

The C674x central processing unit (CPU) consists of eight functional units, two register files, and two data paths as shown in Figure 3-2. The two general-purpose register files (A and B) each contain 32 32-bit registers for a total of 64 registers. The general-purpose registers can be used for data or can be data address pointers. The data types supported include packed 8-bit data, packed 16-bit data, 32-bit data, 40-bit data, and 64-bit data. Values larger than 32 bits, such as 40-bit-long or 64-bit-long values are stored in register pairs, with the 32 LSBs of data placed in an even register and the remaining 8 or 32 MSBs in the next upper register (which is always an odd-numbered register).

The eight functional units (.M1, .L1, .D1, .S1, .M2, .L2, .D2, and .S2) are each capable of executing one instruction every clock cycle. The .M functional units perform all multiply operations. The .S and .L units perform a general set of arithmetic, logical, and branch functions. The .D units primarily load data from memory to the register file and store results from the register file into memory.

The C674x CPU combines the performance of the C64x+ core with the floating-point capabilities of the C67x+ core.

Each C674x .M unit can perform one of the following each clock cycle: one 32 x 32 bit multiply, one 16 x 32 bit multiply, two 16 x 16 bit multiplies, two 16 x 32 bit multiplies, two 16 x 16 bit multiplies with add/subtract capabilities, four 8 x 8 bit multiplies, four 8 x 8 bit multiplies with add operations, and four 16 x 16 multiplies with add/subtract capabilities (including a complex multiply). There is also support for Galois field multiplication for 8-bit and 32-bit data. Many communications algorithms such as FFTs and modems require complex multiplication. The complex multiply (CMPY) instruction takes four 16-bit inputs and produces a 32-bit real and a 32-bit imaginary output. There are also complex multiplies with rounding capability that produces one 32-bit packed output that contain 16-bit real and 16-bit imaginary values. The 32 x 32 bit multiply instructions provide the extended precision necessary for high-precision algorithms on a variety of signed and unsigned 32-bit data types.

The .L or (Arithmetic Logic Unit) now incorporates the ability to do parallel add/subtract operations on a pair of common inputs. Versions of this instruction exist to work on 32-bit data or on pairs of 16-bit data performing dual 16-bit add and subtracts in parallel. There are also saturated forms of these instructions.

The C674x core enhances the .S unit in several ways. On the previous cores, dual 16-bit MIN2 and MAX2 comparisons were only available on the .L units. On the C674x core they are also available on the .S unit which increases the performance of algorithms that do searching and sorting. Finally, to increase data packing and unpacking throughput, the .S unit allows sustained high performance for the quad 8-bit/16-bit and dual 16-bit instructions. Unpack instructions prepare 8-bit data for parallel 16-bit operations. Pack instructions return parallel results to output precision including saturation support.

Other new features include:

- **SPLOOP** - A small instruction buffer in the CPU that aids in creation of software pipelining loops where multiple iterations of a loop are executed in parallel. The SPLOOP buffer reduces the code size associated with software pipelining. Furthermore, loops in the SPLOOP buffer are fully interruptible.
- **Compact Instructions** - The native instruction size for the C6000 devices is 32 bits. Many common instructions such as MPY, AND, OR, ADD, and SUB can be expressed as 16 bits if the C674x compiler can restrict the code to use certain registers in the register file. This compression is performed by the code generation tools.
- **Instruction Set Enhancement** - As noted above, there are new instructions such as 32-bit multiplications, complex multiplications, packing, sorting, bit manipulation, and 32-bit Galois field multiplication.
- **Exceptions Handling** - Intended to aid the programmer in isolating bugs. The C674x CPU is able to detect and respond to exceptions, both from internally detected sources (such as illegal op-codes) and from system events (such as a watchdog time expiration).
- **Privilege** - Defines user and supervisor modes of operation, allowing the operating system to give a basic level of protection to sensitive resources. Local memory is divided into multiple pages, each with read, write, and execute permissions.

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- **Time-Stamp Counter** - Primarily targeted for Real-Time Operating System (RTOS) robustness, a free-running time-stamp counter is implemented in the CPU which is ***not*** sensitive to system stalls.

For more details on the C674x CPU and its enhancements over the C64x architecture, see the following documents:

- *TMS320C674x DSP CPU and Instruction Set Reference Guide* (Literature Number: SPRUFE8)
- *TMS320C674x DSP Megamodule Reference Guide* (Literature Number: SPRUFK5)


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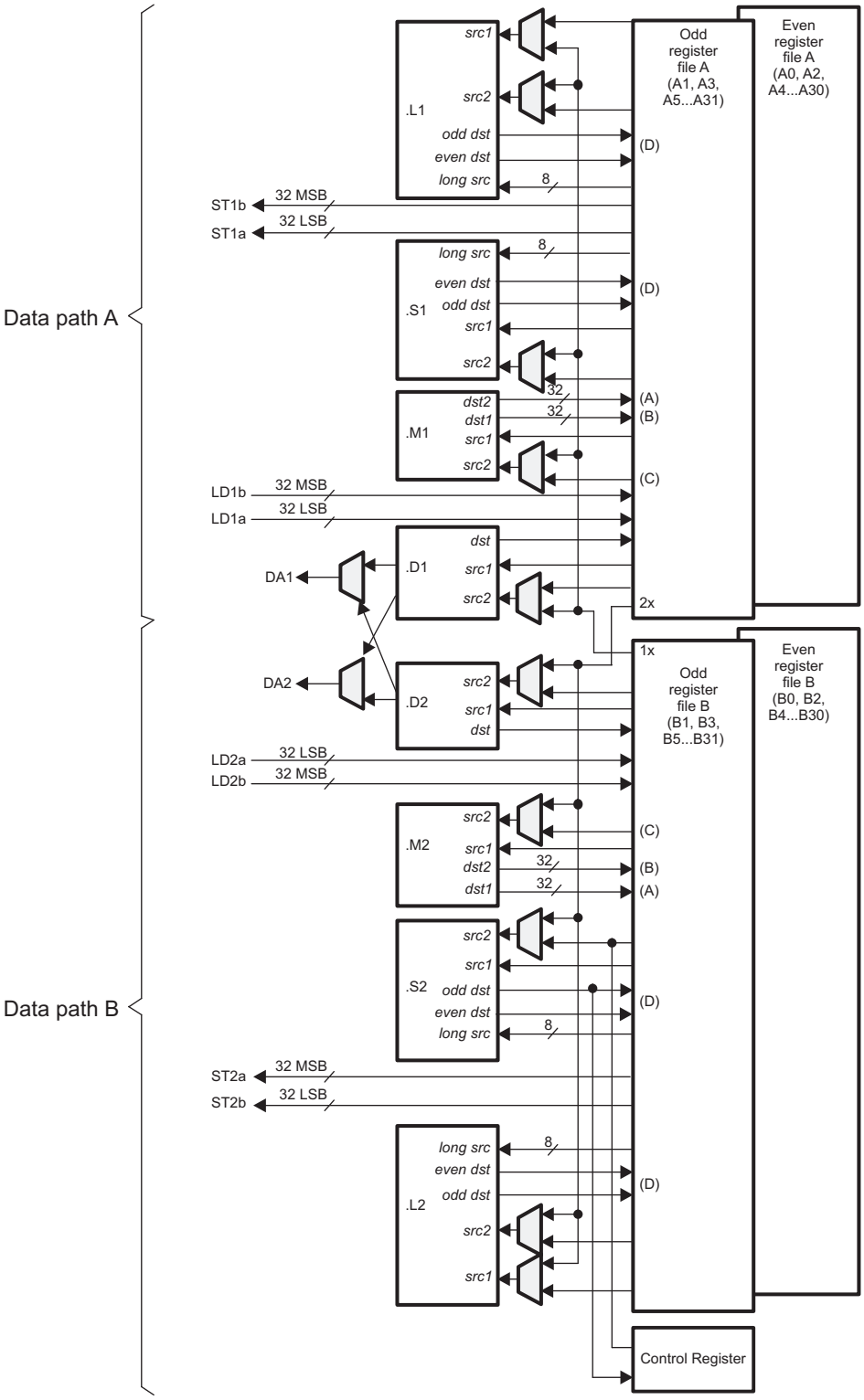


A. .M unit, *dst2* is 32 MSB.
B On .M unit, *dst1* is 32 LSB.
C. On C64x CPU .M unit, *src2* is 32 bits; on C64x+ CPU .M unit, *src2* is 64 bits.
D. On .L and .S units, *odd dst* connects to odd register files and even *dst* connects to even register files

**Figure 3-3. TMS320C674x CPU (DSP Core) Data Paths**

## 3.6 System Memory Management Unit (MMU)

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All C674x accesses through its MDMA port will be directed through the system MMU module where they are remapped to physical system addresses. This protects the ARM Cortex-A8 memory regions from accidental corruption by C674x code and allows for direct allocation of buffers in user space without the need for translation between ARM and DSP applications.

In addition, accesses by the EDMA TC0 and TC1 may optionally be routed through the system MMU. This allows EDMA Channels 0 and 1 to be used by the DSP to perform transfers using only the known virtual addresses of the associated buffers. The MMU_CFG register in the Control Module is used to enable/disable use of the system MMU by the EDMA TCs.

For more details on the system MMU features, see the system MMU section of the *Chip Level Resources* chapter in the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).


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## 3.7 Media Controller Overview

The Media Controller has the responsibility of managing the HDVPSS and ISS modules.

For more details on the Media Controller, see the Media Controller Subsystem section of the *Chip Level Resources* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

## 3.8 HDVICP2 Overview

The HDVICP2 is a Video Encoder/Decoder hardware accelerator supporting a range of encode, decode, and transcode operations for most major video codec standards. The main video Codec standards supported in hardware are MPEG1/2/4 ASP/SP, H.264 BL/MP/HP, VC-1 SP/MP/AP, RV9/10, AVS-1.0, and ON2 VP6.2/VP7.

The HDVICP2 hardware accelerator is composed of the following elements:

- Motion estimation acceleration engine
- Loop filter acceleration engine
- Sequencer, including its memories and an interrupt controller
- Intra-prediction estimation engine
- Calculation engine
- Motion compensation engine
- Entropy coder/decoder
- Video Direct Memory Access (DMA)
- Synchronization boxes
- Shared L2 controller
- Local interconnect

For more details on the HDVICP2, see the HD Video Coprocessor SubSystem section of the *Chip Level Resources* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

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## 3.9 Face Detect (FD) Overview

The device Face Detection (FD) module performs face detection and tracking within a picture stored in memory. This module is typically used for video encoding, face-based priority auto-focusing, or red-eye removal. The FD module supports QVGA resolution inputs stored in DRR memory in 8-bit Luma format. In addition, it uses 51.25KB of DDR for its working memory.

The FD module supports the following features:

- Input image:
  - QVGA Input Image Size (H x V = 320 x 240)
  - 8-bit Gray Scale Data (0x00 = Black and 0xFF = White)
- Detection Capabilities:
  - Face Inclination of ±45°
  - Face Direction:
    - Up/Down: ±30°
    - Left/Right: ±60°
  - Supported Detection Directions:
    - 0° Faces are Vertical
    - +90° Faces are Rotated Right by 90°
    - -90° Faces are Rotated Left by 90°
    - Supported Minimum Face Sizes of 20, 25, 32 or 40 Pixels
  - Supported Detection Start Positions:
    - X = 0 to 160
    - Y = 0 to 120
  - Supported Detection Area Sizes:
    - X = 160 to 320
    - Y = 120 to 240
  - Provides Size, Position, Angle, and Confidence Level for Each Face

## 3.10 Spinlock Module Overview

The Spinlock module provides hardware assistance for synchronizing the processes running on multiple processors in the device:

- ARM Cortex-A8 processor
- C674x DSP
- Media Controller

The Spinlock module implements 128 spinlocks (or hardware semaphores) that provide an efficient way to perform a lock operation of a device resource using a single read-access, avoiding the need for a read-modify-write bus transfer of which the programmable cores are not capable.

For more details on the Spinlock Module, see the Spinlock section of the *Chip Level Resources* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).


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## 3.11 Mailbox Module Overview

The device Mailbox module facilitates communication between the ARM Cortex-A8, C674x DSP, and the Media Controller. The device mailbox consists of twelve mailboxes, each supporting a 1-way communication between two of the above processors. The sender sends information to the receiver by writing a message to the mailbox registers. Interrupt signaling is used to notify the receiver that a message has been queued or to notify the sender about an overflow situation.

The Mailbox module supports the following features (see Figure 3-4):

- 12 mailboxes
- Flexible mailbox-to-processor assignment scheme
- Four-message FIFO depth for each message queue
- 32-bit message width
- Message reception and queue-not-full notification using interrupts
- Four interrupts (one to ARM Cortex-A8, one to C674x, and two to Media Controller)

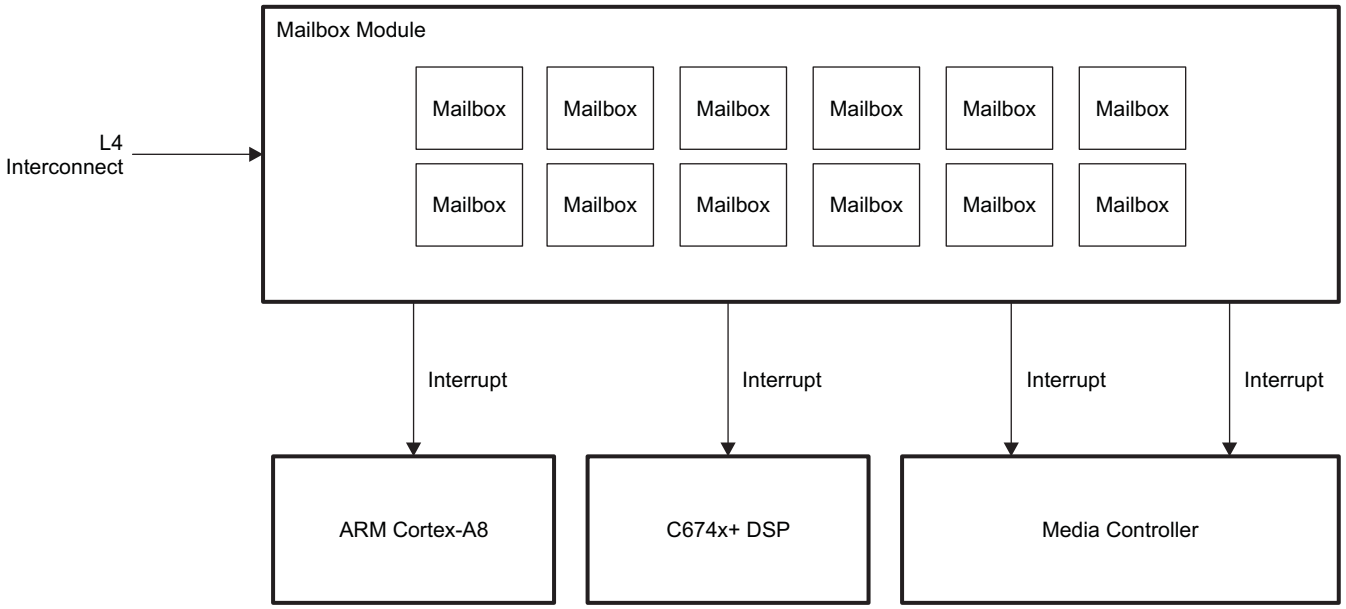


**Figure 3-4. Mailbox Module Block Diagram**

For more details on the Mailbox Module, see the Mailbox section of the *Chip Level Resources* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

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## 3.12 Memory Map Summary

The device has multiple on-chip memories associated with its two processors and various subsystems. To help simplify software development a unified memory map is used where possible to maintain a consistent view of device resources across all bus masters.

### *3.12.1 L3 Memory Map*

Table 3-3 shows the L3 memory map for all system masters (including Cortex-A8). Table 3-3 and Table 3-5 show the memory map of the C674x DSP which has limited access to the following peripherals: McASPx, McBSP, UARTx, I2Cx, SPIx, EDMA, GPIO/INT, GPMC, DDRx, EMAC, PCIe, Timers, and USB. Table 3-4 shows the memory map for the C674x DSP.

For more details on the interconnect topology and connectivity across the L3 and L4 interconnects, see Table 8-17, *System Interconnect*.

**Table 3-3. L3 Memory Map**

| START ADDRESS (HEX) | END ADDRESS (HEX) | SIZE | DESCRIPTION |
|---|---|---|---|
| 0x0000_0000 | 0x00FF_FFFF | 16MB | GPMC (Reserved for BOOTROM) |
| 0x0100_0000 | 0x1FFF_FFFF | 496MB | GPMC |
| 0x2000_0000 | 0x2FFF_FFFF | 256MB | PCIe |
| 0x3000_0000 | 0x3FFF_FFFF | 256MB | Reserved |
| 0x4002_0000 | 0x4002_BFFF | 48KB | ARM Cortex-A8 ROM (Accessible by ARM Cortex-A8 *only*) |
| 0x4002_C000 | 0x402E_FFFF | 2832KB | Reserved |
| 0x402F_0000 | 0x402F_03FF | 1KB | Reserved |
| 0x402F_0400 | 0x402F_FFFF | 64KB - 1KB | ARM Cortex-A8 RAM (Accessible by ARM Cortex-A8 *only*) |
| 0x4030_0000 | 0x4031_FFFF | 128KB | OCMC SRAM |
| 0x4032_0000 | 0x407F_FFFF | 4992KB | Reserved |
| 0x4084_0000 | 0x40DF_FFFF | 5888KB | Reserved |
| 0x40E0_8000 | 0x40EF_FFFF | 992KB | Reserved |
| 0x40F0_8000 | 0x40FF_FFFF | 992KB | Reserved |
| 0x4100_0000 | 0x41FF_FFFF | 16MB | |
| 0x4200_0000 | 0x43FF_FFFF | 32MB | Reserved |
| 0x4400_0000 | 0x443F_FFFF | 4MB | L3 Fast configuration registers |
| 0x4440_0000 | 0x447F_FFFF | 4MB | L3 Mid configuration registers |
| 0x4480_0000 | 0x44BF_FFFF | 4MB | L3 Slow configuration registers |
| 0x44C0_0000 | 0x45FF_FFFF | 20MB | Reserved |
| 0x4600_0000 | 0x463F_FFFF | 4MB | McASP0 Data Peripheral Registers |
| 0x4640_0000 | 0x467F_FFFF | 4MB | McASP1 Data Peripheral Registers |
| 0x4680_0000 | 0x46BF_FFFF | 4MB | McASP2 Data Peripheral Registers |
| 0x46C0_0000 | 0x46FF_FFFF | 4MB | HDMI |
| 0x4700_0000 | 0x473F_FFFF | 4MB | McBSP |
| 0x4740_0000 | 0x477F_FFFF | 4MB | USB |
| 0x4781_2000 | 0x47BF_FFFF | 4MB - 72KB | Reserved |
| 0x47C0_0000 | 0x47C0_BFFF | 48KB | Reserved |
| 0x47C0_C000 | 0x47C0_C3FF | 1KB | Reserved |
| 0x47C0_C400 | 0x47C0_C7FF | 1KB | DDR0 PHY Registers |
| 0x47C0_C800 | 0x47C0_CBFF | 1KB | DDR1 PHY Registers |
| 0x47C0_CC00 | 0x47C0_CFFF | 1KB | Reserved |
| 0x47C0_D000 | 0x47FF FFFF | 4044KB | Reserved |


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**Table 3-3. L3 Memory Map (continued)**

| START ADDRESS (HEX) | END ADDRESS (HEX) | SIZE | DESCRIPTION |
|---|---|---|---|
| 0x4800_0000 | 0x48FF_FFFF | 16MB | L4 Slow Peripheral Domain (see Table 3-6) |
| 0x4900_0000 | 0x490F_FFFF | 1MB | EDMA TPCC Registers |
| 0x4910_0000 | 0x497F_FFFF | 7MB | Reserved |
| 0x4980_0000 | 0x498F_FFFF | 1MB | EDMA TPTC0 Registers |
| 0x4990_0000 | 0x499F_FFFF | 1MB | EDMA TPTC1 Registers |
| 0x49A0_0000 | 0x49AF_FFFF | 1MB | EDMA TPTC2 Registers |
| 0x49B0_0000 | 0x49BF_FFFF | 1MB | EDMA TPTC3 Registers |
| 0x49C0_0000 | 0x49FF_FFFF | 4MB | Reserved |
| 0x4A00_0000 | 0x4AFF_FFFF | 16MB | L4 Fast Peripheral Domain (see Table 3-5) |
| 0x4B00_0000 | 0x4BFF_FFFF | 16MB | Emulation Subsystem |
| 0x4C00_0000 | 0x4CFF_FFFF | 16MB | DDR0 Registers |
| 0x4D00_0000 | 0x4DFF_FFFF | 16MB | DDR1 Registers |
| 0x4E00_0000 | 0x4FFF_FFFF | 32MB | DDR DMM Registers |
| 0x5000_0000 | 0x50FF_FFFF | 16MB | GPMC Registers |
| 0x5100_0000 | 0x51FF_FFFF | 16MB | PCIE Registers |
| 0x5200_0000 | 0x54FF_FFFF | 48MB | Reserved |
| 0x5500_0000 | 0x55FF_FFFF | 16MB | Media Controller |
| 0x5600_0000 | 0x56FF_FFFF | 16MB | Reserved |
| 0x5700_0000 | 0x57FF_FFFF | 16MB | Reserved |
| 0x5800_0000 | 0x58FF_FFFF | 16MB | HDVICP2 Configuration |
| 0x5900_0000 | 0x59FF_FFFF | 16MB | HDVICP2 SL2 |
| 0x5A00_0000 | 0x5BFF_FFFF | | Reserved |
| 0x5C00_0000 | 0x5DFF_FFFF | 32MB | ISS |
| 0x5E00_0000 | 0x5FFF_FFFF | 32MB | Reserved |
| 0x6000_0000 | 0x7FFF_FFFF | 512MB | DDR DMM TILER Window (see Table 3-7) |
| 0x8000_0000 | 0xFFFF_FFFF | 2GB | DDR |
| 0x1 0000 0000 | 0x1 FFFF FFFF | 4GB | DDR DMM TILER Extended Address Map (ISS and HDVPSS only) [see Table 3-7] |

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### 3.12.2 C674x Memory Map

Table 3-4 shows the memory map for the C674x DSP.

**Table 3-4. C674x Memory Map**

| START ADDRESS (HEX) | END ADDRESS (HEX) | SIZE | DESCRIPTION |
|---|---|---|---|
| 0x0000_0000 | 0x003F_FFFF | 4MB | Reserved |
| 0x0044_0000 | 0x007F_FFFF | 3840KB | Reserved |
| 0x0080_0000 | 0x0083_FFFF | 256KB | C674x L2 RAM |
| 0x0084_0000 | 0x00DF_FFFF | 5888KB | Reserved |
| 0x00E0_0000 | 0x00E0_7FFF | 32KB | C674x L1P Cache/RAM |
| 0x00E0_8000 | 0x00EF_FFFF | 992KB | Reserved |
| 0x00F0_0000 | 0x00F0_7FFF | 32KB | C674x L1D Cache/RAM |
| 0x00F0_8000 | 0x017F_FFFF | 9184KB | Reserved |
| 0x0180_0000 | 0x01BF_FFFF | 4MB | C674x Internal CFG registers |
| 0x01C0_0000 | 0x07FF_FFFF | 100MB | Reserved |
| 0x0800_0000 | 0x08FF_FFFF | 16MB | L4 Slow Peripheral Domain (see Table 3-6) |
| 0x0900_0000 | 0x090F_FFFF | 1MB | EDMA TPCC Registers |
| 0x0910_0000 | 0x097F_FFFF | 7MB | Reserved |
| 0x0980_0000 | 0x098F_FFFF | 1MB | EDMA TPTC0 Registers |
| 0x0990_0000 | 0x099F_FFFF | 1MB | EDMA TPTC1 Registers |
| 0x09A0_0000 | 0x09AF_FFFF | 1MB | EDMA TPTC2 Registers |
| 0x09B0_0000 | 0x09BF_FFFF | 1MB | EDMA TPTC3 Registers |
| 0x09C0_0000 | 0x09FF_FFFF | 4MB | Reserved |
| 0x0A00_0000 | 0x0AFF_FFFF | 16MB | L4 Fast Peripheral Domain (see Table 3-5) |
| 0x0B00_0000 | 0x0FFF_FFFF | 80MB | Reserved |
| 0x1000_0000 | 0x10FF_FFFF | 16MB | C674x Internal Global Address(1) |
| 0x1100_0000 | 0xFFFF_FFFF | 3824MB | System MMU Mapped L3 Regions(2) |

(1) Addresses 0x1000_0000 to 0x10FF_FFFF are mapped to C674x internal addresses 0x0000_0000 to 0x00FF_FFFF.
(2) For more details on the system MMU features, see the System MMU section of the *Chip Level Resources* chapter in the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).


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### 3.12.3 L4 Memory Map

The L4 Fast Peripheral Domain, L4 Slow Peripheral Domain regions of the memory maps above are broken out into Table 3-5 and Table 3-6.

For more details on the interconnect topology and connectivity across the L3 and L4 interconnects, see Table 8-17, *System Interconnect*.

#### 3.12.3.1 L4 Fast Peripheral Memory Map

**Table 3-5. L4 Fast Peripheral Memory Map**

| Cortex-A8 and L3 Masters | | C674x DSP | | SIZE | DEVICE NAME |
|---|---|---|---|---|---|
| START ADDRESS (HEX) | END ADDRESS (HEX) | START ADDRESS (HEX) | END ADDRESS (HEX) | | |
| 0x4A00_0000 | 0x4A00_07FF | 0x0A00_0000 | 0x0A00_07FF | 2KB | L4 Fast Configuration - Address/Protection (AP) |
| 0x4A00_0800 | 0x4A00_0FFF | 0x0A00_0800 | 0x0A00_0FFF | 2KB | L4 Fast Configuration - Link Agent (LA) |
| 0x4A00_1000 | 0x4A00_13FF | 0x0A00_1000 | 0x0A00_13FF | 1KB | L4 Fast Configuration - Initiator Port (IP0) |
| 0x4A00_1400 | 0x4A00_17FF | 0x0A00_1400 | 0x0A00_17FF | 1KB | L4 Fast Configuration - Initiator Port (IP1) |
| 0x4A00_1800 | 0x4A00_1FFF | 0x0A00_1800 | 0x0A00_1FFF | 2KB | Reserved |
| 0x4A00_2000 | 0x4A07_FFFF | 0x0A00_2000 | 0x0A07_FFFF | 504KB | Reserved |
| 0x4A10_0000 | 0x4A10_7FFF | 0x0A10_0000 | 0x0A10_7FFF | 32KB | EMAC SW Peripheral Registers |
| 0x4A10_8000 | 0x4A10_8FFF | 0x0A10_8000 | 0x0A10_8FFF | 4KB | EMAC SW Support Registers |
| 0x4A14_0000 | 0x4A14_FFFF | 0x0A14_0000 | 0x0A14_FFFF | 64KB | Reserved |
| 0x4A15_0000 | 0x4A15_0FFF | 0x0A15_0000 | 0x0A15_0FFF | 4KB | Reserved |
| 0x4A15_1000 | 0x4A17_FFFF | 0x0A15_1000 | 0x0A17_FFFF | 188KB | Reserved |
| 0x4A18_0000 | 0x4A1A_1FFF | 0x0A18_0000 | 0x0A1A_1FFF | 136KB | Reserved |
| 0x4A1A_2000 | 0x4A1A_3FFF | 0x0A1A_2000 | 0x0A1A_3FFF | 8KB | McASP3 Configuration Peripheral Registers |
| 0x4A1A_4000 | 0x4A1A_4FFF | 0x0A1A_4000 | 0x0A1A_4FFF | 4KB | McASP3 Configuration Support Registers |
| 0x4A1A_5000 | 0x4A1A_5FFF | 0x0A1A_5000 | 0x0A1A_5FFF | 4KB | McASP3 Data Peripheral Registers |
| 0x4A1A_6000 | 0x4A1A_6FFF | 0x0A1A_6000 | 0x0A1A_6FFF | 4KB | McASP3 Data Support Registers |
| 0x4A1A_7000 | 0x4A1A_7FFF | 0x0A1A_7000 | 0x0A1A_7FFF | 4KB | Reserved |
| 0x4A1A_8000 | 0x4A1A_9FFF | 0x0A1A_8000 | 0x0A1A_9FFF | 8KB | McASP4 Configuration Peripheral Registers |
| 0x4A1A_A000 | 0x4A1A_AFFF | 0x0A1A_A000 | 0x0A1A_AFFF | 4KB | McASP4 Configuration Support Registers |
| 0x4A1A_B000 | 0x4A1A_BFFF | 0x0A1A_B000 | 0x0A1A_BFFF | 4KB | McASP4 Data Peripheral Registers |
| 0x4A1A_C000 | 0x4A1A_CFFF | 0x0A1A_C000 | 0x0A1A_CFFF | 4KB | McASP4 Data Support Registers |
| 0x4A1A_D000 | 0x4A1A_DFFF | 0x0A1A_D000 | 0x0A1A_DFFF | 4KB | Reserved |
| 0x4A1A_E000 | 0x4A1A_FFFF | 0x0A1A_E000 | 0x0A1A_FFFF | 8KB | McASP5 Configuration Peripheral Registers |
| 0x4A1B_0000 | 0x4A1B_0FFF | 0x0A1B_0000 | 0x0A1B_0FFF | 4KB | McASP5 Configuration Support Registers |
| 0x4A1B_1000 | 0x4A1B_1FFF | 0x0A1B_1000 | 0x0A1B_1FFF | 4KB | McASP5 Data Peripheral Registers |
| 0x4A1B_2000 | 0x4A1B_2FFF | 0x0A1B_2000 | 0x0A1B_2FFF | 4KB | McASP5 Data Support Registers |
| 0x4A1B_6000 | 0x4A1B_6FFF | 0x0A1B_6000 | 0x0A1B_6FFF | 4KB | Reserved |
| 0x4A1B_4000 | 0x4AFF_FFFF | 0x0A1B_4000 | 0x0AFF_FFFF | 14632KB | Reserved |

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### 3.12.3.2 L4 Slow Peripheral Memory Map

**Table 3-6. L4 Slow Peripheral Memory Map**

| Cortex-A8 and L3 Masters | | C674x DSP | | SIZE | DEVICE NAME |
|---|---|---|---|---|---|
| START ADDRESS (HEX) | END ADDRESS (HEX) | START ADDRESS (HEX) | END ADDRESS (HEX) | | |
| 0x4800_0000 | 0x4800_07FF | 0x0800_0000 | 0x0800_07FF | 2KB | L4 Slow Configuration – Address/Protection (AP) |
| 0x4800_0800 | 0x4800_0FFF | 0x0800_0800 | 0x0800_0FFF | 2KB | L4 Slow Configuration – Link Agent (LA) |
| 0x4800_1000 | 0x4800_13FF | 0x0800_1000 | 0x0800_13FF | 1KB | L4 Slow Configuration – Initiator Port (IP0) |
| 0x4800_1400 | 0x4800_17FF | 0x0800_1400 | 0x0800_17FF | 1KB | L4 Slow Configuration – Initiator Port (IP1) |
| 0x4800_1800 | 0x4800_1FFF | 0x0800_1800 | 0x0800_1FFF | 2KB | Reserved |
| 0x4800_2000 | 0x4800_7FFF | 0x0800_2000 | 0x0800_7FFF | 24KB | Reserved |
| 0x4800_8000 | 0x4800_8FFF | 0x0800_8000 | 0x0800_8FFF | 32KB | Reserved |
| 0x4801_0000 | 0x4801_0FFF | 0x0801_0000 | 0x0801_0FFF | 4KB | System MMU Peripheral Registers |
| 0x4801_1000 | 0x4801_1FFF | 0x0801_1000 | 0x0801_1FFF | 4KB | System MMU Support Registers |
| 0x4801_2000 | 0x4801_FFFF | 0x0801_2000 | 0x0801_FFFF | 56KB | Reserved |
| 0x4802_0000 | 0x4802_0FFF | 0x0802_0000 | 0x0802_0FFF | 4KB | UART0 Peripheral Registers |
| 0x4802_1000 | 0x4802_1FFF | 0x0802_1000 | 0x0802_1FFF | 4KB | UART0 Support Registers |
| 0x4802_2000 | 0x4802_2FFF | 0x0802_2000 | 0x0802_2FFF | 4KB | UART1 Peripheral Registers |
| 0x4802_3000 | 0x4802_3FFF | 0x0802_3000 | 0x0802_3FFF | 4KB | UART1 Support Registers |
| 0x4802_4000 | 0x4802_4FFF | 0x0802_4000 | 0x0802_4FFF | 4KB | UART2 Peripheral Registers |
| 0x4802_5000 | 0x4802_5FFF | 0x0802_5000 | 0x0802_5FFF | 4KB | UART2 Support Registers |
| 0x4802_6000 | 0x4802_7FFF | 0x0802_6000 | 0x0802_7FFF | 8KB | Reserved |
| 0x4802_8000 | 0x4802_8FFF | 0x0802_8000 | 0x0802_8FFF | 4KB | I2C0 Peripheral Registers |
| 0x4802_9000 | 0x4802_9FFF | 0x0802_9000 | 0x0802_9FFF | 4KB | I2C0 Support Registers |
| 0x4802_A000 | 0x4802_AFFF | 0x0802_A000 | 0x0802_AFFF | 4KB | I2C1 Peripheral Registers |
| 0x4802_B000 | 0x4802_BFFF | 0x0802_B000 | 0x0802_BFFF | 4KB | I2C1 Support Registers |
| 0x4802_C000 | 0x4802_DFFF | 0x0802_C000 | 0x0802_DFFF | 8KB | Reserved |
| 0x4802_E000 | 0x4802_EFFF | 0x0802_E000 | 0x0802_EFFF | 4KB | TIMER1 Peripheral Registers |
| 0x4802_F000 | 0x4802_FFFF | 0x0802_F000 | 0x0802_FFFF | 4KB | TIMER1 Support Registers |
| 0x4803_0000 | 0x4803_0FFF | 0x0803_0000 | 0x0803_0FFF | 4KB | SPI0 Peripheral Registers |
| 0x4803_1000 | 0x4803_1FFF | 0x0803_1000 | 0x0803_1FFF | 4KB | SPI0 Support Registers |
| 0x4803_2000 | 0x4803_2FFF | 0x0803_2000 | 0x0803_2FFF | 4KB | GPIO0 Peripheral Registers |
| 0x4803_3000 | 0x4803_3FFF | 0x0803_3000 | 0x0803_3FFF | 4KB | GPIO0 Support Registers |
| 0x4803_4000 | 0x4803_7FFF | 0x0803_4000 | 0x0803_7FFF | 16KB | Reserved |
| 0x4803_8000 | 0x4803_9FFF | 0x0803_8000 | 0x0803_9FFF | 8KB | McASP0 CFG Peripheral Registers |
| 0x4803_A000 | 0x4803_AFFF | 0x0803_A000 | 0x0803_AFFF | 4KB | McASP0 CFG Support Registers |
| 0x4803_B000 | 0x4803_BFFF | 0x0803_B000 | 0x0803_BFFF | 4KB | Reserved |
| 0x4803_C000 | 0x4803_DFFF | 0x0803_C000 | 0x0803_DFFF | 8KB | McASP1 CFG Peripheral Registers |
| 0x4803_E000 | 0x4803_EFFF | 0x0803_E000 | 0x0803_EFFF | 4KB | McASP1 CFG Support Registers |
| 0x4803_F000 | 0x4803_FFFF | 0x0803_F000 | 0x0803_FFFF | 4KB | Reserved |
| 0x4804_0000 | 0x4804_0FFF | 0x0804_0000 | 0x0804_0FFF | 4KB | TIMER2 Peripheral Registers |
| 0x4804_1000 | 0x4804_1FFF | 0x0804_1000 | 0x0804_1FFF | 4KB | TIMER2 Support Registers |
| 0x4804_2000 | 0x4804_2FFF | 0x0804_2000 | 0x0804_2FFF | 4KB | TIMER3 Peripheral Registers |
| 0x4804_3000 | 0x4804_3FFF | 0x0804_3000 | 0x0804_3FFF | 4KB | TIMER3 Support Registers |
| 0x4804_4000 | 0x4804_4FFF | 0x0804_4000 | 0x0804_4FFF | 4KB | TIMER4 Peripheral Registers |


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**Table 3-6. L4 Slow Peripheral Memory Map (continued)**

| Cortex-A8 and L3 Masters | | C674x DSP | | SIZE | DEVICE NAME |
|---|---|---|---|---|---|
| START ADDRESS (HEX) | END ADDRESS (HEX) | START ADDRESS (HEX) | END ADDRESS (HEX) | | |
| 0x4804_5000 | 0x4804_5FFF | 0x0804_5000 | 0x0804_5FFF | 4KB | TIMER4 Support Registers |
| 0x4804_6000 | 0x4804_6FFF | 0x0804_6000 | 0x0804_6FFF | 4KB | TIMER5 Peripheral Registers |
| 0x4804_7000 | 0x4804_7FFF | 0x0804_7000 | 0x0804_7FFF | 4KB | TIMER5 Support Registers |
| 0x4804_8000 | 0x4804_8FFF | 0x0804_8000 | 0x0804_8FFF | 4KB | TIMER6 Peripheral Registers |
| 0x4804_9000 | 0x4804_9FFF | 0x0804_9000 | 0x0804_9FFF | 4KB | TIMER6 Support Registers |
| 0x4804_A000 | 0x4804_AFFF | 0x0804_A000 | 0x0804_AFFF | 4KB | TIMER7 Peripheral Registers |
| 0x4804_B000 | 0x4804_BFFF | 0x0804_B000 | 0x0804_BFFF | 4KB | TIMER7 Support Registers |
| 0x4804_C000 | 0x4804_CFFF | 0x0804_C000 | 0x0804_CFFF | 4KB | GPIO1 Peripheral Registers |
| 0x4804_D000 | 0x4804_DFFF | 0x0804_D000 | 0x0804_DFFF | 4KB | GPIO1 Support Registers |
| 0x4804_E000 | 0x4804_FFFF | 0x0804_E000 | 0x0804_FFFF | 8KB | Reserved |
| 0x4805_0000 | 0x4805_1FFF | 0x0805_0000 | 0x0805_1FFF | 8KB | McASP2 CFG Peripheral Registers |
| 0x4805_2000 | 0x4805_2FFF | 0x0805_2000 | 0x0805_2FFF | 4KB | McASP2 CFG Support Registers |
| 0x4805_3000 | 0x4805_FFFF | 0x0805_3000 | 0x0805_FFFF | 52KB | Reserved |
| 0x4806_0000 | 0x4806_FFFF | | | 64KB | MMC/SD/SDIO0 Peripheral Registers |
| 0x4807_0000 | 0x4807_0FFF | | | 4KB | MMC/SD/SDIO0 Support Registers |
| 0x4807_1000 | 0x4807_FFFF | 0x0807_1000 | 0x0807_FFFF | 60KB | Reserved |
| 0x4808_0000 | 0x4808_FFFF | | | 64KB | ELM Peripheral Registers |
| 0x4809_0000 | 0x4809_0FFF | | | 4KB | ELM Support Registers |
| 0x4809_1000 | 0x4809_FFFF | 0x0809_1000 | 0x0809_FFFF | 60KB | Reserved |
| 0x480A_0000 | 0x480A_FFFF | 0x080A_0000 | 0x080A_FFFF | 64KB | Reserved |
| 0x480B_0000 | 0x480B_0FFF | 0x080B_0000 | 0x080B_0FFF | 4KB | Reserved |
| 0x480B_1000 | 0x480B_FFFF | 0x080B_1000 | 0x080B_FFFF | 60KB | Reserved |
| 0x480C_0000 | 0x480C_0FFF | | | 4KB | RTC Peripheral Registers |
| 0x480C_1000 | 0x480C_1FFF | | | 4KB | RTC Support Registers |
| 0x480C_2000 | 0x480C_3FFF | 0x080C_2000 | 0x080C_3FFF | 8KB | Reserved |
| 0x480C_4000 | 0x480C_7FFF | 0x080C_4000 | 0x080C_7FFF | 16KB | Reserved |
| 0x480C_8000 | 0x480C_8FFF | 0x080C_8000 | 0x080C_8FFF | 4KB | Mailbox Peripheral Registers |
| 0x480C_9000 | 0x480C_9FFF | 0x080C_9000 | 0x080C_9FFF | 4KB | Mailbox Support Registers |
| 0x480C_A000 | 0x480C_AFFF | 0x080C_A000 | 0x080C_AFFF | 4KB | Spinlock Peripheral Registers |
| 0x480C_B000 | 0x480C_BFFF | 0x080C_B000 | 0x080C_BFFF | 4KB | Spinlock Support Registers |
| 0x480C_C000 | 0x480F_FFFF | 0x080C_C000 | 0x080F_FFFF | 208KB | Reserved |
| 0x4810_0000 | 0x4811_FFFF | | | 128KB | HDVPSS Peripheral Registers |
| 0x4812_0000 | 0x4812_0FFF | | | 4KB | HDVPSS Support Registers |
| 0x4812_1000 | 0x4812_1FFF | 0x0812_1000 | 0x0812_1FFF | 4KB | Reserved |
| 0x4812_2000 | 0x4812_2FFF | | | 4KB | HDMI Peripheral Registers |
| 0x4812_3000 | 0x4812_3FFF | | | 4KB | HDMI Support Registers |
| 0x4812_4000 | 0x4813_FFFF | 0x0812_4000 | 0x0813_FFFF | 112KB | Reserved |
| 0x4814_0000 | 0x4815_FFFF | 0x0814_0000 | 0x0815_FFFF | 128KB | Control Module Peripheral Registers (C674x DSP Restricted to only exposed peripherals) |
| 0x4816_0000 | 0x4816_0FFF | 0x0816_0000 | 0x0816_0FFF | 4KB | Control Module Support Registers (C674x DSP Restricted to only exposed peripherals) |
| 0x4816_1000 | 0x4817_FFFF | 0x0816_1000 | 0x0817_FFFF | 124KB | Reserved |
| 0x4818_0000 | 0x4818_2FFF | 0x0818_0000 | 0x0818_2FFF | 12KB | PRCM Peripheral Registers (C674x DSP Restricted to only exposed peripherals) |

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**Table 3-6. L4 Slow Peripheral Memory Map (continued)**

| Cortex-A8 and L3 Masters | | C674x DSP | | SIZE | DEVICE NAME |
|---|---|---|---|---|---|
| START ADDRESS (HEX) | END ADDRESS (HEX) | START ADDRESS (HEX) | END ADDRESS (HEX) | | |
| 0x4818_3000 | 0x4818_3FFF | 0x0818_3000 | 0x0818_3FFF | 4KB | PRCM Support Registers (C674x DSP Restricted to only exposed peripherals) |
| 0x4818_4000 | 0x4818_7FFF | 0x0818_4000 | 0x0818_7FFF | 16KB | Reserved |
| 0X4818_8000 | 0X4818_BFFF | 0x0818_8000 | 0x0818_BFFF | 16KB | Reserved |
| 0x4818_C000 | 0x4818_CFFF | | | 4KB | OCP Watchpoint Peripheral Registers |
| 0x4818_D000 | 0x4818_DFFF | | | 4KB | OCP Watchpoint Support Registers |
| 0x4818_E000 | 0x4818_EFFF | 0x0818_E000 | 0x0818_EFFF | 4KB | Reserved |
| 0x4818_F000 | 0x4818_FFFF | 0x0818_F000 | 0x0818_FFFF | 4KB | Reserved |
| 0x4819_0000 | 0x4819_3FFF | 0x0819_0000 | 0x0819_3FFF | 16KB | Reserved |
| 0x4819_4000 | 0x4819_BFFF | 0x0819_4000 | 0x0819_BFFF | 32KB | Reserved |
| 0x4819_C000 | 0x481F_FFFF | 0x0819_C000 | 0x081F_FFFF | 400KB | Reserved |
| 0x4819_C000 | 0x4819_CFFF | 0x0819_C000 | 0x0819_CFFF | 4KB | I2C2 Peripheral Registers |
| 0x4819_D000 | 0x4819_DFFF | 0x0819_D000 | 0x0819_DFFF | 4KB | I2C2 Support Registers |
| 0x4819_E000 | 0x4819_EFFF | 0x0819_E000 | 0x0819_EFFF | 4KB | I2C3 Peripheral Registers |
| 0x4819_F000 | 0x4819_FFFF | 0x0819_F000 | 0x0819_FFFF | 4KB | I2C3 Support Registers |
| 0x481A_0000 | 0x481A_0FFF | 0x081A_0000 | 0x081A_0FFF | 4KB | SPI1 Peripheral Registers |
| 0x481A_1000 | 0x481A_1FFF | 0x081A_1000 | 0x081A_1FFF | 4KB | SPI1 Support Registers |
| 0x481A_2000 | 0x481A_2FFF | 0x081A_2000 | 0x081A_2FFF | 4KB | SPI2 Peripheral Registers |
| 0x481A_3000 | 0x481A_3FFF | 0x081A_3000 | 0x081A_3FFF | 4KB | SPI2 Support Registers |
| 0x481A_4000 | 0x481A_4FFF | 0x081A_4000 | 0x081A_4FFF | 4KB | SPI3 Peripheral Registers |
| 0x481A_5000 | 0x481A_5FFF | 0x081A_5000 | 0x081A_5FFF | 4KB | SPI3 Support Registers |
| 0x481A_6000 | 0x481A_6FFF | 0x081A_6000 | 0x081A_6FFF | 4KB | UART3 Peripheral Registers |
| 0x481A_7000 | 0x481A_7FFF | 0x081A_7000 | 0x081A_7FFF | 4KB | UART3 Support Registers |
| 0x481A_8000 | 0x481A_8FFF | 0x081A_8000 | 0x081A_8FFF | 4KB | UART4 Peripheral Registers |
| 0x481A_9000 | 0x481A_9FFF | 0x081A_9000 | 0x081A_9FFF | 4KB | UART4 Support Registers |
| 0x481A_A000 | 0x481A_AFFF | 0x081A_A000 | 0x081A_AFFF | 4KB | UART5 Peripheral Registers |
| 0x481A_B000 | 0x481A_BFFF | 0x081A_B000 | 0x081A_BFFF | 4KB | UART5 Support Registers |
| 0x481A_C000 | 0x481A_CFFF | 0x081A_C000 | 0x081A_CFFF | 4KB | GPIO2 Peripheral Registers |
| 0x481A_D000 | 0x481A_DFFF | 0x081A_D000 | 0x081A_DFFF | 4KB | GPIO2 Support Registers |
| 0x481A_E000 | 0x481A_EFFF | 0x081A_E000 | 0x081A_EFFF | 4KB | GPIO3 Peripheral Registers |
| 0x481A_F000 | 0x481A_FFFF | 0x081A_F000 | 0x081A_FFFF | 4KB | GPIO3 Support Registers |
| 0x481B_0000 | 0x481B_FFFF | 0x081B_0000 | 0x081B_FFFF | 64KB | Reserved |
| 0x481C_0000 | 0x481C_0FFF | 0x081C_0000 | 0x081C_0FFF | 4KB | Reserved |
| 0x481C_1000 | 0x481C_1FFF | 0x081C_1000 | 0x081C_1FFF | 4KB | TIMER8 Peripheral Registers |
| 0x481C_2000 | 0x481C_2FFF | 0x081C_2000 | 0x081C_2FFF | 4KB | TIMER8 Support Registers |
| 0x481C_3000 | 0x481C_3FFF | | | 4KB | SYNCTIMER32K Peripheral Registers |
| 0x481C_4000 | 0x481C_4FFF | | | 4KB | SYNCTIMER32K Support Registers |
| 0x481C_5000 | 0x481C_5FFF | | | 4KB | PLLSS Peripheral Registers |
| 0x481C_6000 | 0x481C_6FFF | | | 4KB | PLLSS |
| 0x481C_7000 | 0x481C_7FFF | | | 4KB | WDT0 Peripheral Registers |
| 0x481C_8000 | 0x481C_8FFF | | | 4KB | WDT0 Support Registers |
| 0x481C_9000 | 0x481C_9FFF | 0x081C_9000 | 0x081C_9FFF | 8KB | Reserved |
| 0x481C_A000 | 0x481C_BFFF | 0x081C_A000 | 0x081C_BFFF | 8KB | Reserved |
| 0x481C_C000 | 0x481C_DFFF | | | 8KB | DCAN0 Peripheral Registers |


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**Table 3-6. L4 Slow Peripheral Memory Map (continued)**

| Cortex-A8 and L3 Masters | | C674x DSP | | SIZE | DEVICE NAME |
|---|---|---|---|---|---|
| START ADDRESS (HEX) | END ADDRESS (HEX) | START ADDRESS (HEX) | END ADDRESS (HEX) | | |
| 0x481C_E000 | 0x481C_FFFF | | | 8KB | DCAN0 Support Registers |
| 0x481D_0000 | 0x481D_1FFF | | | 8KB | DCAN1 Peripheral Registers |
| 0x481D_2000 | 0x481D_3FFF | | | 8KB | DCAN1 Support Registers |
| 0x481D_4000 | 0x481D_5FFF | 0x081D_4000 | 0x081D_5FFF | 8KB | Reserved |
| 0x481D_6000 | 0x481D_6FFF | 0x081D_6000 | 0x081D_6FFF | 4KB | FDIF Peripheral Registers |
| 0x481D_7000 | 0x481D_7FFF | 0x081D_7000 | 0x081D_7FFF | 4KB | FDIF Support Registers |
| 0x481D_8000 | 0x481E_7FFF | | | 64KB | MMC/SD/SDIO1 Peripheral Registers |
| 0x481E_8000 | 0x481E_8FFF | | | 4KB | MMC/SD/SDIO1 Support Registers |
| 0x481E_9000 | 0x481F_FFFF | 0x081E_9000 | 0x081F_FFFF | 52KB | Reserved |
| 0x4820_0000 | 0x4820_0FFF | | | 4KB | Interrupt controller(1) |
| 0x4820_1000 | 0x4823_FFFF | 0x0820_1000 | 0x0823_FFFF | 252KB | Reserved(1) |
| 0x4824_0000 | 0x4824_0FFF | | | 4KB | MPUSS config register(1) |
| 0x4824_1000 | 0x4827_FFFF | 0x0824_1000 | 0x0827_FFFF | 252KB | Reserved(1) |
| 0x4828_0000 | 0x4828_0FFF | | | 4KB | Reserved(1) |
| 0x4828_1000 | 0x482F_FFFF | 0x0828_1000 | 0x082F_FFFF | 508KB | Reserved(1) |
| 0x4830_0000 | 0x48FF_FFFF | 0x0830_0000 | 0x08FF_FFFF | 13MB | Reserved |

(1) These regions decoded internally by the Cortex-A8 Subsystem and are not physically part of the L4 Slow. They are included here only for reference when considering the Cortex-A8 Memory Map. For Masters other than the Cortex-A8 these regions are reserved.

### 3.12.4 DDR DMM TILER Extended Addressing Map

The TILER includes an additional 4-GBytes of addressing range, enabled by a 33rd address bit, to access the frame buffer in rotated and mirrored views. shows the details of the TILER Extended Address Mapping. This entirety of this additional range is only accessible to the HDVPSS and ISS subsystems. However, other masters can access any one single view through the 512-MB TILER region in the base 4GByte address memory map.

**Table 3-7. DDR DMM TILER Extended Address Mapping**

| BLOCK NAME | START ADDRESS (HEX) | END ADDRESS (HEX) | SIZE | DESCRIPTION |
|---|---|---|---|---|
| TILER View 0 | 0x1 0000_0000 | 0x1 1FFF_FFFF | 512MB | Natural 0° View |
| TILER View 1 | 0x1 2000_0000 | 0x1 3FFF_FFFF | 512MB | 0° with Vertical Mirror View |
| TILER View 2 | 0x1 4000_0000 | 0x1 5FFF_FFFF | 512MB | 0° with Horizontal Mirror View |
| TILER View 3 | 0x1 6000_0000 | 0x1 7FFF_FFFF | 512MB | 180° View |
| TILER View 4 | 0x1 8000_0000 | 0x1 9FFF_FFFF | 512MB | 90° with Vertical Mirror View |
| TILER View 5 | 0x1 A000_0000 | 0x1 BFFF_FFFF | 512MB | 270° View |
| TILER View 6 | 0x1 C000_0000 | 0x1 DFFF_FFFF | 512MB | 90° View |
| TILER View 7 | 0x1 E000_0000 | 0x1 FFFF_FFFF | 512MB | 90° with Horizontal Mirror View |

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# 4 Device Pins

## 4.1 Pin Maps

Figure 4-1 through Figure 4-8 show the bottom view of the package pin assignments in eight pin maps (A, B, C, D, E, F, G, and H).


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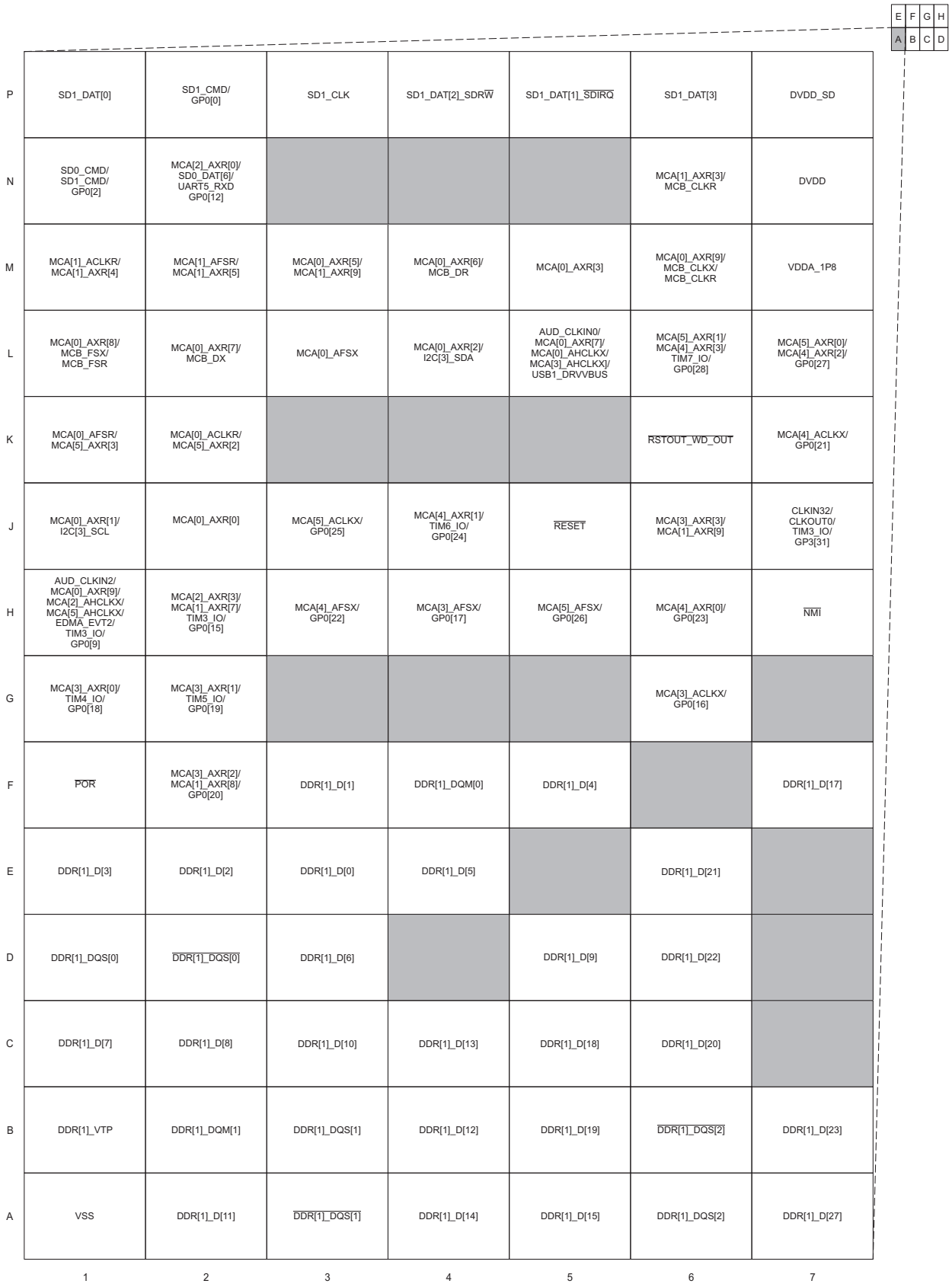

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| P | SD1_DAT[0] | SD1_CMD/ GP0[0] | SD1_CLK | SD1_DAT[2]_SDRW | SD1_DAT[1]_SDIRQ | SD1_DAT[3] | DVDD_SD |
| N | SD0_CMD/ SD1_CMD/ GP0[2] | MCA[2]_AXR[0]/ SD0_DAT[6]/ UART5_RXD GP0[12] | | | | MCA[1]_AXR[3]/ MCB_CLKR | DVDD |
| M | MCA[1]_ACLKR/ MCA[1]_AXR[4] | MCA[1]_AFSR/ MCA[1]_AXR[5] | MCA[0]_AXR[5]/ MCA[1]_AXR[9] | MCA[0]_AXR[6]/ MCB_DR | MCA[0]_AXR[3] | MCA[0]_AXR[9]/ MCB_CLKX/ MCB_CLKR | VDDA_1P8 |
| L | MCA[0]_AXR[8]/ MCB_FSX/ MCB_FSR | MCA[0]_AXR[7]/ MCB_DX | MCA[0]_AFSX | MCA[0]_AXR[2]/ I2C[3]_SDA | AUD_CLKIN0/ MCA[0]_AXR[7]/ MCA[0]_AHCLKX/ MCA[3]_AHCLKX)/ USB1_DRVVBUS | MCA[5]_AXR[1]/ MCA[4]_AXR[3]/ TIM7_IO/ GP0[28] | MCA[5]_AXR[0]/ MCA[4]_AXR[2]/ GP0[27] |
| K | MCA[0]_AFSR/ MCA[5]_AXR[3] | MCA[0]_ACLKR/ MCA[5]_AXR[2] | | | | RSTOUT_WD_OUT | MCA[4]_ACLKX/ GP0[21] |
| J | MCA[0]_AXR[1]/ I2C[3]_SCL | MCA[0]_AXR[0] | MCA[5]_ACLKX/ GP0[25] | MCA[4]_AXR[1]/ TIM6_IO/ GP0[24] | RESET | MCA[3]_AXR[3]/ MCA[1]_AXR[9] | CLKIN32/ CLKOUT0/ TIM3_IO/ GP3[31] |
| H | AUD_CLKIN2/ MCA[0]_AXR[9]/ MCA[2]_AHCLKX/ MCA[5]_AHCLKX/ EDMA_EVT2/ TIM3_IO/ GP0[9] | MCA[2]_AXR[3]/ MCA[1]_AXR[7]/ TIM3_IO/ GP0[15] | MCA[4]_AFSX/ GP0[22] | MCA[3]_AFSX/ GP0[17] | MCA[5]_AFSX/ GP0[26] | MCA[4]_AXR[0]/ GP0[23] | NMI |
| G | MCA[3]_AXR[0]/ TIM4_IO/ GP0[18] | MCA[3]_AXR[1]/ TIM5_IO/ GP0[19] | | | | MCA[3]_ACLKX/ GP0[16] | |
| F | POR | MCA[3]_AXR[2]/ MCA[1]_AXR[8]/ GP0[20] | DDR[1]_D[1] | DDR[1]_DQM[0] | DDR[1]_D[4] | | DDR[1]_D[17] |
| E | DDR[1]_D[3] | DDR[1]_D[2] | DDR[1]_D[0] | DDR[1]_D[5] | | DDR[1]_D[21] | |
| D | DDR[1]_DQS[0] | DDR[1]_DQS[0] | DDR[1]_D[6] | | DDR[1]_D[9] | DDR[1]_D[22] | |
| C | DDR[1]_D[7] | DDR[1]_D[8] | DDR[1]_D[10] | DDR[1]_D[13] | DDR[1]_D[18] | DDR[1]_D[20] | |
| B | DDR[1]_VTP | DDR[1]_DQM[1] | DDR[1]_DQS[1] | DDR[1]_D[12] | DDR[1]_D[19] | DDR[1]_DQS[2] | DDR[1]_D[23] |
| A | VSS | DDR[1]_D[11] | DDR[1]_DQS[1] | DDR[1]_D[14] | DDR[1]_D[15] | DDR[1]_DQS[2] | DDR[1]_D[27] |

**Figure 4-1. Pin Map A**

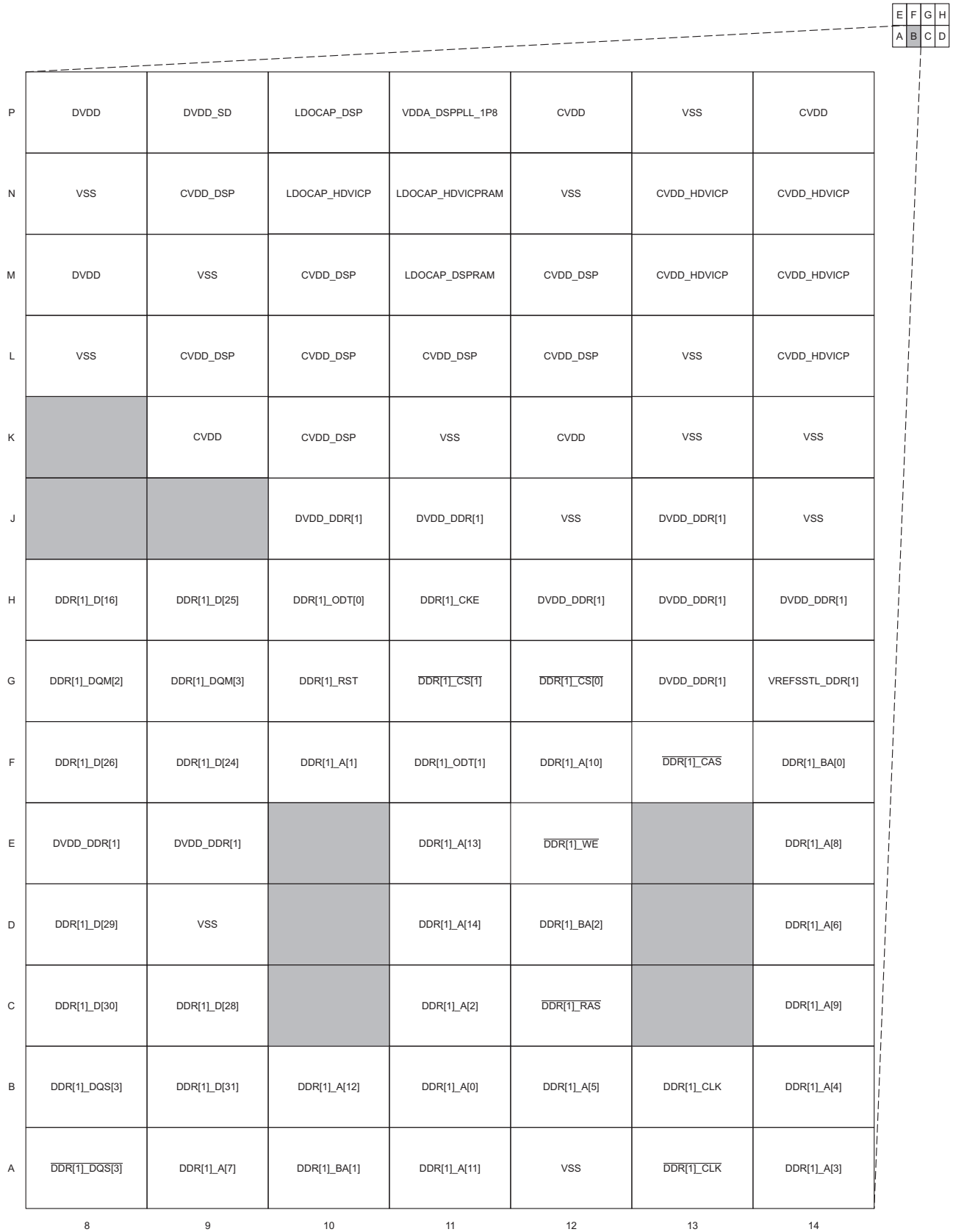


**Figure 4-2. Pin Map B**


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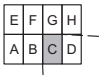


| | | | | | | | |
|---|---|---|---|---|---|---|---|
| VSS | CVDD | VSS | LDOCAP_RAM0 | VSS | DVDD_GPMCB | VSS | P |
| VSS | VSS | CVDD | VDDA_L3PLL_1P8 | CVDD | VSS | VSS | N |
| VSS | CVDD | VSS | CVDD | VSS | DVDD_GPMC | VSS | M |
| CVDD | VSS | CVDD | LDOCAP_RAM2 | CVDD | VDDA_1P8 | DVDD_GPMC | L |
| VSS | VSS | VSS | CVDD | VSS | DVDD_GPMC | | K |
| DVDD_DDR[0] | DVDD_DDR[0] | DVDD_DDR[0] | DVDD_DDR[0] | VSS | | | J |
| VDDA_DDRPLL_1P8 | DVDD_DDR[0] | DVDD_DDR[0] | DDR[0]_CKE | DDR[0]_ODT[1] | DDR[0]_D[24] | DDR[0]_D[18] | H |
| VREFSSTL_DDR[0] | DVDD_DDR[0] | DDR[0]_CS[1] | DDR[0]_ODT[0] | DDR[0]_RST | DDR[0]_D[26] | DDR[0]_D[19] | G |
| DDR[0]_BA[0] | DDR[0]_A[14] | DDR[0]_A[13] | DDR[0]_CS[0] | DDR[0]_A[1] | DDR[0]_DQM[3] | DDR[0]_D[25] | F |
| DDR[0]_A[3] | | DDR[0]_A[12] | DDR[0]_A[7] | | DVDD_DDR[0] | DVDD_DDR[0] | E |
| DDR[0]_A[4] | | DDR[0]_A[11] | DDR[0]_A[2] | | VSS | DDR[0]_D[30] | D |
| DDR[0]_A[9] | | DDR[0]_WE | DDR[0]_CAS | | DDR[0]_D[28] | DDR[0]_D[29] | C |
| DDR[0]_A[8] | DDR[0]_CLK | DDR[0]_A[5] | DDR[0]_RAS | DDR[0]_A[0] | DDR[0]_D[31] | DDR[0]_DQS[3] | B |
| DDR[0]_A[6] | DDR[0]_CLK | VSS | DDR[0]_BA[2] | DDR[0]_A[10] | DDR[0]_BA[1] | DDR[0]_DQS[3] | A |
| 15 | 16 | 17 | 18 | 19 | 20 | 21 | |

**Figure 4-3. Pin Map C**

| | 22 | 23 | 24 | 25 | 26 | 27 | 28 | |
|---|---|---|---|---|---|---|---|---|
| P | SD2_DAT[5]/ GPMC_A[26]/ GPMC_A[22]/ TIM6_IO/ GP1[21] | EMAC[0]_MRXD[1]/ EMAC[0]_RGRXD[0]/ EMAC[0]_RMTXD[1]/ GP3[29] | MDIO/ GP1[12] | GPMC_CS[4]/ SD2_CMD/ GP1[8] | GPMC_CS[3]/ SPI[2]_SCS[0]/ GP1[26] | CSI2_DY[3] | CSI2_DX[3] | P |
| N | VSSA_CSI2 | SD2_DAT[6]/ GPMC_A[25]/ GPMC_A[21]/ UART2_TXD/ GP1[20] | | | | CSI2_DY[2] | CSI2_DX[2] | N |
| M | VDDA_CSI2_1P8 | SD2_CLK/ GP1[15] | SD2_DAT[1]_SDIRQ/ GPMC_A[3]/ GP1[13] | GPMC_CS[2]/ GPMC_A[24]/ GP1[25] | GPMC_ADV_ALE/ GPMC_CS[6]/ TIM5_IO/ GP1[28] | CSI2_DX[1] | CSI2_DY[1] | M |
| L | VSS | EMAC[0]_MCOL/ EMAC[0]_RGRXCTL/ EMAC[0]_RMRXD[0]/ GP3[24] | EMAC[0]_MTCLK/ EMAC[0]_RGRXC/ SPI[3]_SCS[3]/ I2C[2]_SDA/ GP3[23] | SD2_DAT[7]/ GPMC_A[24]/ GPMC_A[20]/ UART2_RXD/ GP1[19] | SD2_DAT[0]/ GPMC_A[4]/ GP1[14] | CSI2_DX[0] | CSI2_DY[0] | L |
| K | EMAC[0]_MRXDV/ EMAC[1]_RGRXD[1]/ GPMC_A[5]/ SPI[2]_SCLK | EMAC[0]_GMTCLK/ EMAC[1]_RGRXC/ GPMC_A[6]/ SPI[2]_D[1] | | | | SD2_DAT[2]_SDRW/ GPMC_A[2]/ GP2[6] | GPMC_CS[1]/ GPMC_A[25]/ GP1[24] | K |
| J | EMAC[0]_MTXD[6]/ EMAC[1]_RGRXD[0]/ EMAC[1]_RMTXD[0]/ GPMC_A[13]/ UART1_TXD | EMAC[0]_MTXEN/ EMAC[1]_RGRXD[2]/ EMAC[1]_RMTXEN/ GPMC_A[15]/ UART1_RTS | EMAC[0]_MTXD[0]/ EMAC[1]_RGRXD[3]/ GPMC_A[7]/ SPI[2]_D[0] | EMAC[0]_MRXD[3]/ EMAC[1]_RGRXCTL/ GPMC_A[27]/ GPMC_A[26]/ GPMC_A[0]/ UART5_RXD | EMAC[0]_MRXER/ EMAC[0]_RGTXCTL/ EMAC[0]_RMRXER/ GP3[26] | EMAC_RMREFCLK/ TIM2_IO/ GP1[10] | SD2_DAT[3]/ GPMC_A[1]/ GP2[5] | J |
| H | EMAC[0]_MTXD[2]/ EMAC[1]_RGTXCTL/ EMAC[1]_RMRXD[0]/ GPMC_A[9]/ UART4_TXD | EMAC[0]_MTXD[3]/ EMAC[1]_RGTXD[0]/ EMAC[1]_RMRXD[1]/ GPMC_A[10]/ UART4_CTS | EMAC[0]_MTXD[7]/ EMAC[1]_RGTXD[3]/ EMAC[1]_RMTXD[1]/ GPMC_A[14]/ UART1_CTS | EMAC[0]_MTXD[1]/ EMAC[1]_RGTXD[1]/ GPMC_A[8]/ UART4_RXD | EMAC[0]_MRXD[5]/ EMAC[0]_RGTXD[3]/ GPMC_A[2]/ UART5_CTS | EMAC[0]_MRCLK/ EMAC[0]_RGTXC/ EMAC[0]_RMCRSDV/ SPI[3]_SCS[2]/ GP3[27] | MDCLK/ GP1[11] | H |
| G | | EMAC[0]_MTXD[4]/ EMAC[1]_RGTXD[2]/ EMAC[1]_RMRXER/ GPMC_A[11]/ UART4_RTS | | | | EMAC[0]_MRXD[7]/ EMAC[0]_RGTXD[1]/ GPMC_A[4]/ SPI[2]_SCS[3] | EMAC[0]_MRXD[0]/ EMAC[0]_RGTXD[0]/ EMAC[0]_RMTXD[0]/ GP3[28] | G |
| F | DDR[0]_D[17] | | DDR[0]_D[4] | DDR[0]_D[3] | DDR[0]_D[1] | EMAC[0]_MTXD[5]/ EMAC[1]_RGTXC/ EMAC[1]_RMCRSDV/ GPMC_A[12]/ UART1_RXD | EMAC[0]_MRXD[6]/ EMAC[0]_RGTXD[2]/ GPMC_A[3]/ UART5_RTS | F |
| E | | DDR[0]_D[21] | | DDR[0]_D[5] | DDR[0]_D[2] | DDR[0]_D[0] | DDR[0]_DQM[0] | E |
| D | | DDR[0]_D[20] | DDR[0]_D[13] | | DDR[0]_D[6] | DDR[0]_DQS[0] | DDR[0]_DQS[0] | D |
| C | | DDR[0]_D[22] | DDR[0]_DQM[2] | DDR[0]_D[9] | DDR[0]_D[10] | DDR[0]_D[8] | DDR[0]_D[7] | C |
| B | DDR[0]_D[23] | DDR[0]_DQS[2] | DDR[0]_D[16] | DDR[0]_D[12] | DDR[0]_DQS[1] | DDR[0]_VTP | DDR[0]_DQM[1] | B |
| A | DDR[0]_D[27] | DDR[0]_DQS[2] | DDR[0]_D[15] | DDR[0]_D[14] | DDR[0]_DQS[1] | DDR[0]_D[11] | VSS | A |

**Figure 4-4. Pin Map D**


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| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| AH | VSS | DEVOSC_MXI/ DEV_CLKIN | DEVOSC_MXO | UART0_DCD/ UART3_RXD/ SPI[0]_SCS[3]/ I2C[2]_SCL/ SD1_POW/ GP1[2] | UART0_RXD | DCAN0_TX/ UART2_TXD/ I2C[3]_SDA/ GP1[0] | VOUT[0]_G_Y_YC[2]/ EMU3/ GP2[24] |
| AG | VSS | UART0_DTR/ UART3_CTS/ UART1_TXD/ GP1[4] | VSSA_DEVOSC | UART0_DSR/ UART3_TXD/ SPI[0]_SCS[2]/ I2C[2]_SDA/ SD1_SDWP/ GP1[3] | UART0_TXD | DCAN0_RX/ UART2_RXD/ I2C[3]_SCL/ GP1[1] | VOUT[0]_B_CB_C[2] EMU2/ GP2[22] |
| AF | SERDES_CLKP | SERDES_CLKN | SPI[0]_D[1] | UART0_RIN/ UART3_RTS/ UART1_RXD/ GP1[5] | UART0_RTS/ UART4_TXD/ DCAN1_RX/ SPI[1]_SCS[2]/ SD2_SDCD | VOUT[0]_R_CR[6]/ | |
| AE | VSS | VSS | SPI[0]_D[0] | | SPI[0]_SCS[1]/ SD1_SDCD/ EDMA_EVT1/ TIM4_IO/ GP1[6] | UART0_CTS/ UART4_RXD/ DCAN1_TX/ SPI[1]_SCS[3]/ SD0_SDCD | |
| AD | PCIE_TXN0 | PCIE_TXP0 | SPI[1]_SCS[0]/ GP1[16] | RTCK | | SPI[0]_SCS[0] | |
| AC | PCIE_RXN0 | PCIE_RXP0 | SPI[1]_SCLK/ GP1[17] | I2C[0]_SCL | TDO | | SPI[0]_SCLK |
| AB | RSV23 | RSV24 | | | | I2C[0]_SDA | |
| AA | RSV26 | RSV25 | SPI[1]_D[1]/ GP1[18] | TRST | MCA[2]_AFSX/ GP0[11] | SPI[1]_D[0]/ GP1[26] | TMS |
| Y | VSS | VSS | SD0_DAT[2]_SDRW/ SD1_DAT[6]/ GP0[5] | SD0_DAT[3]/ SD1_DAT[7]/ GP0[6] | SD0_DAT[1]_SDIRQ/ SD1_DAT[5]/ GP0[4] | SD0_CLK/ GP0[1] | TDI |
| W | GP1[7] | GP1[8] | | | | DEVOSC_WAKE/ SPI[1]_SCS[1]/ TIM5_IO/ GP1[7] | TCLK |
| V | GP1[9] | GP1[10] | MCA[1]_AFSX | MCA[1]_AXR[0]/ SD0_DAT[4] | MCA[2]_AXR[2]/ MCA[1]_AXR[6]/ TIM2_IO/ GP0[14] | MCA[2]_AXR[1]/ SD0_DAT[7]/ UART5_TXD/ GP0[13] | VSS |
| U | RSV16 | RSV17 | UART2_TXD/ GP0[31] | UART2_RXD/ GP0[29] | MCA[1]_ACLKX | MCA[2]_ACLKX// GP0[10] | VDDA_1P8 |
| T | AUXOSC_MXO | TCLKIN/ GP0[30] | | | | MCA[1]_AXR[1]/ SD0_DAT[5] | DVDD |
| R | AUXOSC_MXI/ AUX_CLKIN | VSSA_AUXOSC | MCA[1]_AXR[2]/ MCB_FSR | MCA[0]_ACLKX | AUD_CLKIN1/ MCA[0]_AXR[8]/ MCA[1]_AHCLKX/ MCA[4]_AHCLKX/ EDMA_EVT3/ TIM2_IO/ GP0[8] | MCA[0]_AXR[4]/ MCA[1]_AXR[8] | SD0_DAT[0]/ SD1_DAT[4]/ GP0[3] |

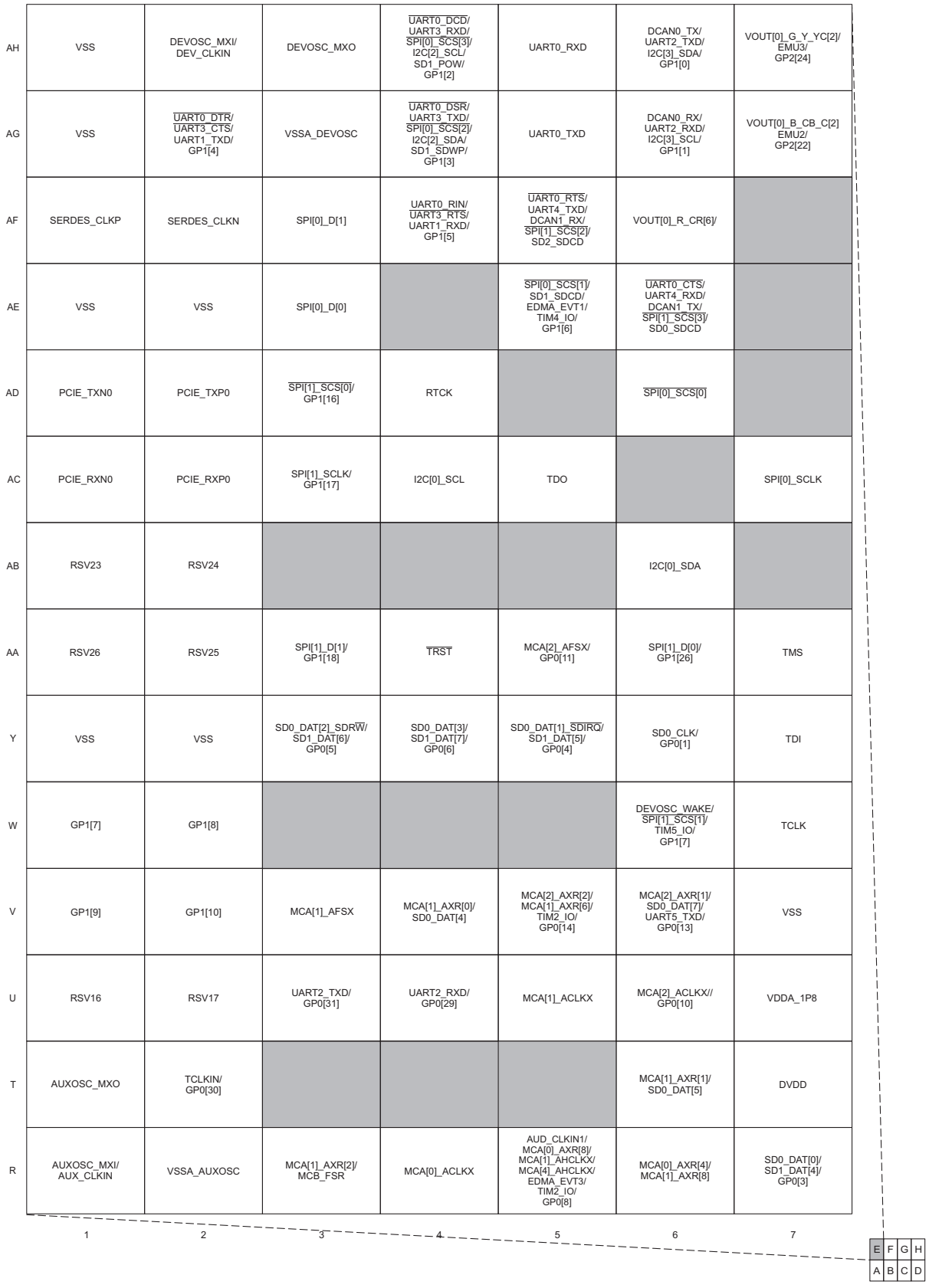


**Figure 4-5. Pin Map E**

| | 8 | 9 | 10 | 11 | 12 | 13 | 14 |
|---|---|---|---|---|---|---|---|
| AH | VIN[0]A_D[4]/ GP2[9] | VIN[0]A_D[10]_BD[2]/ GP2[15] | USB0_CE | USB0_DM | USB1_ID | USB1_DM | USB1_CE |
| AG | EMU0 | VIN[0]A_D[9]_BD[1]/ GP2[14] | USB0_ID | USB0_DP | USB0_VBUSIN | USB1_DP | USB1_VBUSIN |
| AF | VOUT[0]_R_CR[5] | VIN[0]A_D[0]/ GP1[11] | | USB0_DRVVBUS/ GP0[7] | VOUT[0]_R_CR[7] | | VOUT[0]_G_Y_YC[9] |
| AE | VOUT[0]_R_CR[8] | VSS | | EMU1 | VIN[0]A_D[3]/ GP2[8] | | VOUT[0]_G_Y_YC[8] |
| AD | RSV1 | VOUT[0]_R_CR[2]/ EMU4/ GP2[26] | | VOUT[0]_B_CB_C[4] | VOUT[0]_CLK | | VOUT[0]_G_Y_YC[7] |
| AC | RSV5 | VIN[0]A_D[2]/ GP2[7] | VOUT[0]_B_CB_C[6] | VOUT[0]_HSYNC | VIN[0]A_D[14]_BD[6]/ CAM_STROBE/ GP2[19] | VOUT[0]_R_CR[9] | VIN[0]A_D[15]_BD[7]/ CAM_SHUTTER/ GP2[20] |
| AB | VOUT[0]_G_Y_YC[4] | VOUT[0]_R_CR[3]/ GP2[27] | VOUT[0]_B_CB_C[7] | VIN[0]A_D[1]/ GP1[12] | VOUT[0]_G_Y_YC[5] | VOUT[0]_VSYNC | DVDD |
| AA | VOUT[0]_G_Y_YC[6] | VOUT[0]_R_CR[4] | VOUT[0]_AVID/ VOUT[0]_FLD/ SPI[3]_SCLK/ TIM7_IO/ GP2[21] | VIN[0]A_D[7]/ GP2[12] | VDDA_USB0_1P8 | VDDA_USB_3P3 | VSS |
| Y | | | VSS | DVDD | VSS | VDDA_1P8 | RSV4 |
| W | | VDDA_PCIE_1P8 | VDDA_PCIE_1P8 | CVDD | VSS | VDDA_USB1_1P8 | LDOCAP_ARM |
| V | RSV3 | VSS | VDDA_1P8 | VSS | VSSA_USB | VSSA_USB | LDOCAP_ARMRAM |
| U | RSV2 | VDDA_1P8 | VDDA_1P8 | CVDD | VSS | CVDD | VSS |
| T | VSS | VSS | RSV27 | LDOCAP_SERDESCLK | CVDD | VSS | CVDD_ARM |
| R | VSS | VSS | DVDD_M | LDOCAP_RAM1 | VSS | VDDA_ARMPLL_1P8 | VSS |

E F G H
A B C D

**Figure 4-6. Pin Map F**


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| 15 | 16 | 17 | 18 | 19 | 20 | 21 | |
|---|---|---|---|---|---|---|---|
| VOUT[0]_G_Y_YC[3]/ GP2[25] | VIN[0]A_D[6]/ GP2[11] | VIN[0]A_D[11]_BD[3]/ CAM_WE/ GP2[16] | HDMI_CLKN | HDMI_DN0 | HDMI_DN1 | HDMI_DN2 | AH |
| VOUT[0]_B_CB_C[9] | VIN[0]A_D[5]/ GP2[10] | VIN[0]A_D[12]_BD[4]/ CLKOUT1/ GP2[17] | HDMI_CLKP | HDMI_DP0 | HDMI_DP1 | HDMI_DP2 | AG |
| VOUT[0]_B_CB_C[8] | | VIN[0]A_D[13]_BD[5]/ CAM_RESET/ GP2[18] | VOUT[0]_FLD/ CAM_PCLK/ GPMC_A[12]/ UART2_RTS/ GP2[2] | | VIN[0]A_D[18]/ CAM_D[10]/ EMAC[1]_RMRXD[1]/ I2C[3]_SCL/ GP0[12] | VIN[0]A_D[19]/ CAM_D[11]/ EMAC[1]_RMRXD[0]/ I2C[3]_SDA/ GP0[13] | AF |
| VOUT[0]_B_CB_C[3]/ GP2[23] | | VIN[0]B_CLK/ CLKOUT0/ GP1[9] | VIN[0]A_D[21]/ CAM_D[13]/ EMAC[1]_RMTXD[0]/ SPI[3]_SCLK/ GP0[15] | | VSS | VIN[0]A_DE/ VIN[0]B_HSYNC/ UART5_TXD/ I2C[2]_SDA/ GP2[0] | AE |
| VOUT[0]_B_CB_C[5] | | VIN[0]B_FLD/ CAM_D[4]/ GP0[21] | VOUT[1]_G_Y_YC[1]/ CAM_D[3]/ GPMC_A[5]/ UART4_RXD/ GP0[22] | | VIN[0]A_VSYNC/ UART5_CTS/ GP2[4] | VSS | AD |
| VIN[0]B_DE/ CAM_D[6]/ GP0[19] | VIN[0]A_D[23]/ CAM_D[15]/ EMAC[1]_RMTXEN/ SPI[3]_D[0]/ GP0[17] | VIN[0]A_D[20]/ CAM_D[12]/ EMAC[1]_RMCRSDV/ SPI[3]_SCS[0]/ GP0[14] | VOUT[1]_G_Y_YC[0]/ CAM_D[2]/ GPMC_A[6]/ UART4_TXD/ GP0[23] | VOUT[1]_R_CR[1]/ CAM_D[1]/ GPMC_A[7]/ UART4_CTS/ GP0[24] | VIN[0]A_HSYNC/ UART5_RTS/ GP2[3] | VIN[0]A_D[22]/ CAM_D[14]/ EMAC[1]_RMTXD[1]/ SPI[3]_D[1]/ GP0[16] | AC |
| VIN[0]A_D[8]_BD[0]/ GP2[13] | DVDD | VIN[0]A_DE/ CAM_D[7]/ GP0[18] | VDDA_VID0PLL_1P8 | VDDA_VDAC_1P8 | VIN[0]A_CLK/ GP2[2] | VIN[0]A_D[17]/ CAM_D[9]/ EMAC[1]_RMRXER/ GP0[11] | AB |
| DVDD | VSS | DVDD | VDDA_VID1PLL_1P8 | VSSA_VDAC | VIN[0]A_FLD/ VIN[0]B_VSYNC/ UART5_RXD/ I2C[2]_SCL/ GP2[1] | VIN[0]A_D[16]/ CAM_D[8]/ I2C[2]_SCL/ GP0[10] | AA |
| VSS | DVDD | VSS | VSS | VSS | | | Y |
| VDDA_1P8 | VSS | VSS | VDDA_HDMI_1P8 | DVDD_C | DVDD_C | | W |
| CVDD_ARM | CVDD_ARM | VSS | VSSA_HDMI | VSS | DVDD | VSS | V |
| CVDD_ARM | CVDD_ARM | CVDD | VSS | CVDD | VSS | DVDD | U |
| CVDD_ARM | CVDD_ARM | VSS | VSS | VSS | DVDD_GPMCB | VSS | T |
| CVDD | VSS | CVDD | VDDA_AUDIOPLL_1P8 | CVDD | VDDA_1P8 | VSS | R |

E F G H
A B C D

**Figure 4-7. Pin Map G**

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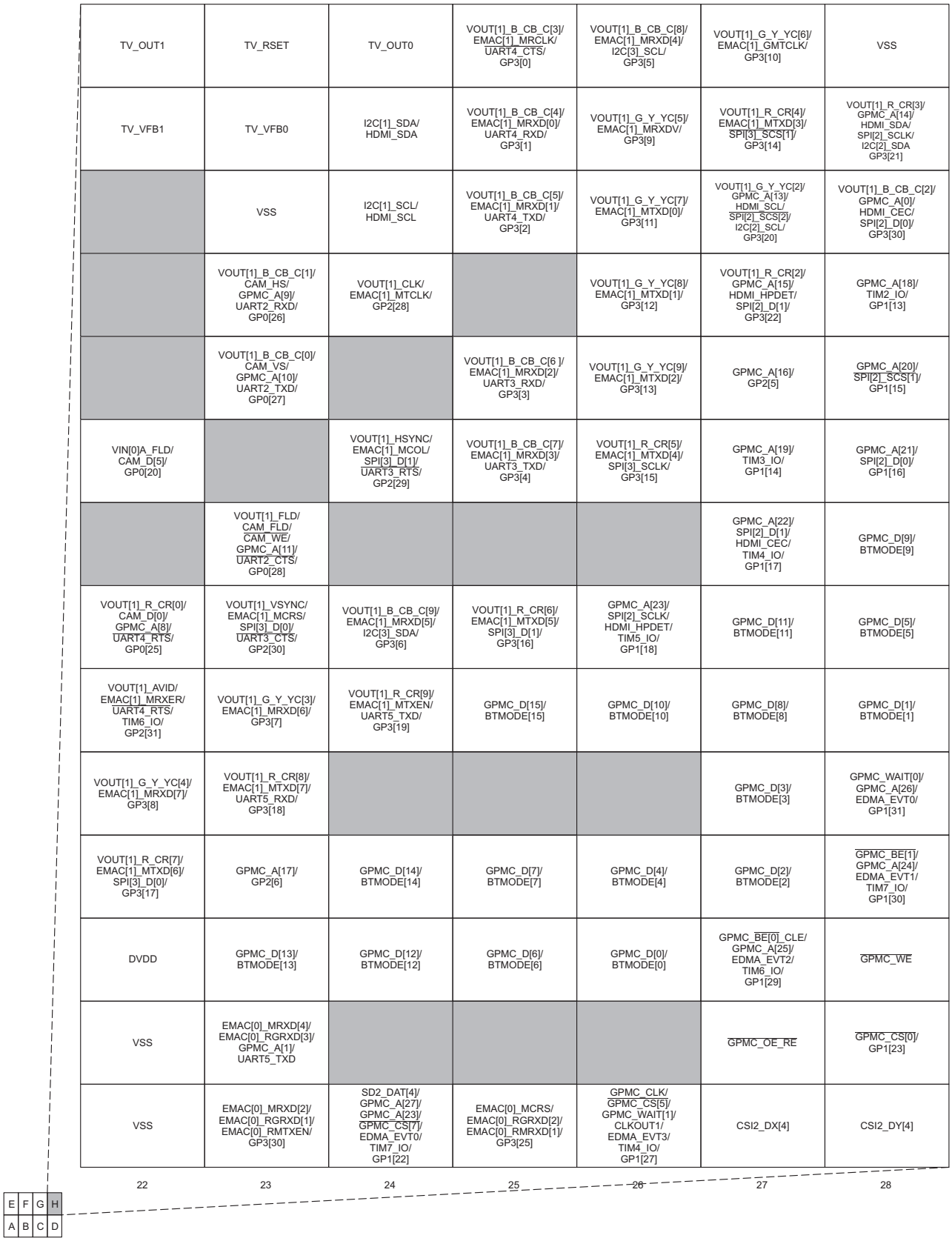


**Figure 4-8. Pin Map H**


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## 4.2 Terminal Functions

The terminal functions tables identify the external signal names and their pin multiplexing, the associated pin (ball) numbers along with the mechanical package designator, the pin type (for example, I, O, Z, S, A, or GND), whether the pin has any internal pullup or pulldown resistors (for example, IPU, IPD, or DIS), the supply voltage source, and describe the function or functions on the pin. The MUXED column in the tables also identifies all peripheral pin functions multiplexed on a pin, the pin control register (PINCNTLx) that controls which peripheral pin function is selected for that particular pin, and indicates the state driven on the peripheral input (logic 0, logic 1, or PIN level) when the peripheral pin function is ***not*** selected (that is, the de-selected input state [DSIS]), and the Multi-Muxed [MM] option for that peripheral pin function). For more detailed information on device configuration, boot mode order, peripheral selection, and multiplexed/shared pin control, and so on, see Section 5, *Device Configurations* of this data manual.

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### 4.2.1 Boot Configuration

**Table 4-1. Boot Configuration Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **BOOT** | | | | | |
| GPMC_D[15]/ **BTMODE[15]** | Y25 | I | DIS DVDD_GPMC | GPMC PINCNTL104 DSIS: PIN | GPMC CS0 default GPMC_Wait enable input. This pin is multiplexed between ARM Cortex-A8 boot mode and General-Purpose Memory Controller (GPMC) peripheral functions. At reset, BTMODE[15] is sampled to determine the GPMC CS0 Wait enable:<br>• 0 = Wait disabled<br>• 1 = Wait enabled<br>After reset, this pin functions as GPMC multiplexed data/address pin 15 (GPMC_D[15]). |
| GPMC_D[14]/ **BTMODE[14]** | V24 | I | DIS DVDD_GPMC | GPMC PINCNTL103 DSIS: PIN | GPMC CS0 default Address/Data multiplexing mode input. These pins are multiplexed between ARM Cortex-A8 boot mode and General-Purpose Memory Controller (GPMC) peripheral functions. At reset, BTMODE[14:13] are sampled to determine the GPMC CS0 Address/Data multiplexing:<br>• 00 = Not muxed<br>• 01 = A/A/D muxed<br>• 10 = A/D muxed<br>• 11 = Reserved<br>After reset, this pin functions as GPMC multiplexed data/address pins 14 through 13 (GPMC_D[14:13]). |
| GPMC_D[13]/ **BTMODE[13]** | U23 | I | DIS DVDD_GPMC | GPMC PINCNTL102 DSIS: PIN | |
| GPMC_D[12]/ **BTMODE[12]** | U24 | I | DIS DVDD_GPMC | GPMC PINCNTL101 DSIS: PIN | GPMC CS0 default Data Bus Width input. This pin is multiplexed between ARM Cortex-A8 boot mode and General-Purpose Memory Controller (GPMC) peripheral functions. At reset, BTMODE[12] is sampled to determine the GPMC CS0 bus width:<br>• 0 = 8-bit data bus<br>• 1 = 16-bit data bus<br>After reset, this pin functions as GPMC multiplexed data/address pin 12 (GPMC_D[12]). |
| GPMC_D[11]/ **BTMODE[11]** | AA27 | I | DIS DVDD_GPMC | GPMC PINCNTL100 DSIS: PIN | $\overline{\text{RSTOUT_WD_OUT}}$ Configuration. This pin is multiplexed between ARM Cortex-A8 boot mode and General-Purpose Memory Controller (GPMC) peripheral functions. At reset, BTMODE[11] is sampled to determine the function of the $\overline{\text{RSTOUT_WD_OUT}}$ pin:<br>• 0 = $\overline{\text{RSTOUT}}$ is asserted when a Watchdog Timer reset, $\overline{\text{POR}}$, $\overline{\text{RESET}}$, or Emulation/Software-Global Cold/Warm reset occurs<br>• 1 = $\overline{\text{RSTOUT_WD_OUT}}$ is asserted only when a Watchdog Timer reset occurs<br>After reset, this pin functions as GPMC multiplexed data/address pin 11 (GPMC_D[11]). |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull during and after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal


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**Table 4-1. Boot Configuration Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE[1] | OTHER[2] [3] | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| GPMC_D[10]/ **BTMODE[10]** | Y26 | I | DIS DVDD_GPMC | GPMC PINCNTL99 DSIS: PIN | XIP (NOR) on GPMC Configuration. This pin is multiplexed between ARM Cortex-A8 boot mode and General-Purpose Memory Controller (GPMC) peripheral functions. At reset, when the XIP (MUX0), XIP (MUX1), XIP w/ WAiT (MUX0) or XIP w/ WAiT (MUX1) bootmode is selected (see Table 5-1), BTMODE[10] is sampled to select between GPMC pin muxing options A or B shown in Table 5-2, *XIP (on GPMC) Boot Options [Muxed or Non-Muxed]*.<br>• 0 = GPMC Option A<br>• 1 = GPMC Option B<br>After reset, this pin functions as GPMC multiplexed data/address pin 10 (GPMC_D[10]). |
| GPMC_D[9]/ **BTMODE[9]** | AB28 | I | DIS DVDD_GPMC | GPMC PINCNTL98 DSIS: PIN | Ethernet PHY Configuration. These pins are multiplexed between ARM Cortex-A8 boot mode and General-Purpose Memory Controller (GPMC) peripheral functions. At reset, when EMAC bootmode is selected (see Table 5-1), BTMODE[9:8] pins are sampled to determine the function of the Ethernet PHY Mode selection.<br>• 00 = MII (GMII)<br>• 01 = RMII<br>• 10 = RGMII<br>• 11 = Reserved<br>For more detailed information on the EMAC PHY boot modes and the EMAC pin functions selected, see Section 5.2.6, *Ethernet PHY Mode Selection*.<br>After reset, these pins function as GPMC multiplexed data/address pins 9 and 8 (GPMC_D[9] and GPMC_D[8]). |
| GPMC_D[8]/ **BTMODE[8]** | Y27 | I | DIS DVDD_GPMC | GPMC PINCNTL97 DSIS: PIN | |
| GPMC_D[7]/ **BTMODE[7]** | V25 | I | DIS DVDD_GPMC | GPMC PINCNTL96 DSIS: PIN | Reserved Boot Pins. These pins are multiplexed between ARM Cortex-A8 boot mode and General-Purpose Memory Controller (GPMC) peripheral functions.<br>For proper device operation at reset, these pins should be externally pulled low.<br>After reset, these pins function as GPMC multiplexed data/address pins 10 through 5 (GPMC_D[7:5]). |
| GPMC_D[6]/ **BTMODE[6]** | U25 | I | DIS DVDD_GPMC | GPMC PINCNTL95 DSIS: PIN | |
| GPMC_D[5]/ **BTMODE[5]** | AA28 | I | DIS DVDD_GPMC | GPMC PINCNTL94 DSIS: PIN | |
| GPMC_D[4]/ **BTMODE[4]** | V26 | I | DIS DVDD_GPMC | GPMC PINCNTL93 DSIS: PIN | ARM Cortex-A8 Boot Mode Configuration Bits. These pins are multiplexed between ARM Cortex-A8 boot mode and the General-Purpose Memory Controller (GPMC) peripheral functions.<br>At reset, the boot mode inputs BTMODE[4:0] are sampled to determine the ARM boot configuration. For more details on the types of boot modes supported, see Section 5.2, *Boot Modes*, of this document, along with the *TMS320DM814x ROM Code Memory and Peripheral Booting* chapter of the *TMS320DM814x DaVinci™ Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).<br>After reset, these pins function as GPMC multiplexed data/address pins 4 through 0 (GPMC_D[4:0]). |
| GPMC_D[3]/ **BTMODE[3]** | W27 | I | DIS DVDD_GPMC | GPMC PINCNTL92 DSIS: PIN | |
| GPMC_D[2]/ **BTMODE[2]** | V27 | I | DIS DVDD_GPMC | GPMC PINCNTL91 DSIS: PIN | |
| GPMC_D[1]/ **BTMODE[1]** | Y28 | I | DIS DVDD_GPMC | GPMC PINCNTL90 DSIS: PIN | |
| GPMC_D[0]/ **BTMODE[0]** | U26 | I | DIS DVDD_GPMC | GPMC PINCNTL89 DSIS: PIN | |

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### 4.2.2 Camera Interface (I/F)

**Table 4-2. Camera I/F Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **CAMERA I/F** | | | | | |
| VOUT[0]_FLD/ **CAM_PCLK**/ GPMC_A[12]/ UART2_RTS/ GP2[2] | AF18 | I | IPD DVDD_C | VOUT[0], GPMC, UART2, GP2 PINCNTL175 DSIS: 0 | Camera Pixel Clock. |
| VIN[0]A_D[23]/ **CAM_D[15]**/ EMAC[1]_RMTXEN/ SPI[3]_D[0]/ GP0[17] | AC16 | I | IPD DVDD_C | VIN[0]A, EMAC[1], SPI[3], GP0 PINCNTL163 DSIS: PIN | Camera data inputs |
| VIN[0]A_D[22]/ **CAM_D[14]**/ EMAC[1]_RMTXD[1]/ SPI[3]_D[1]/ GP0[16] | AC21 | I | IPD DVDD_C | VIN[0]A, EMAC[1]_RM, SPI[3], GP0 PINCNTL162 DSIS: PIN | |
| VIN[0]A_D[21]/ **CAM_D[13]**/ EMAC[1]_RMTXD[0]/ SPI[3]_SCLK/ GP0[15] | AE18 | I | IPD DVDD_C | VIN[0]A, EMAC[1]_RM, SPI[3], GP0 PINCNTL161 DSIS: PIN | |
| VIN[0]A_D[20]/ **CAM_D[12]**/ EMAC[1]_RMCRSDV/ SPI[3]_SCS[0]/ GP0[14] | AC17 | I | IPD DVDD_C | VIN[0]A, EMAC[1]_RM, SPI[3], GP0 PINCNTL160 DSIS: PIN | |
| VIN[0]A_D[19]/ **CAM_D[11]**/ EMAC[1]_RMRXD[0]/ I2C[3]_SDA/ GP0[13] | AF21 | I | IPU DVDD_C | VIN[0]A, EMAC[1]_RM, I2C[3], GP0 PINCNTL159 DSIS: PIN | |
| VIN[0]A_D[18]/ **CAM_D[10]**/ EMAC[1]_RMRXD[1]/ I2C[3]_SCL/ GP0[12] | AF20 | I | IPU DVDD_C | VIN[0]A, EMAC[1]_RM, I2C[3], GP0 PINCNTL158 DSIS: PIN | |
| VIN[0]A_D[17]/ **CAM_D[9]**/ EMAC[1]_RMRXER/ GP0[11] | AB21 | I | IPD DVDD_C | VIN[0]A, EMAC[1]_RM, GP0 PINCNTL157 DSIS: PIN | |
| VIN[0]A_D[16]/ **CAM_D[8]**/ I2C[2]_SCL/ GP0[10] | AA21 | I | IPU DVDD_C | VIN[0]A, I2C[2], GP0 PINCNTL156 DSIS: PIN | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal


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**Table 4-2. Camera I/F Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| VIN[0]A_DE/ **CAM_D[7]**/ GP0[18] | AB17 | I | IPU DVDD_C | VIN[0]A, GP0 PINCNTL164 DSIS: PIN | Camera data inputs |
| VIN[0]B_DE/ **CAM_D[6]**/ GP0[19] | AC15 | I | IPU DVDD_C | VIN[0]A, GP0 PINCNTL165 DSIS: PIN | |
| VIN[0]A_FLD/ **CAM_D[5]**/ GP0[20] | AC22 | I | IPU DVDD_C | VIN[0]A, GP0 PINCNTL166 DSIS: PIN | |
| VIN[0]B_FLD/ **CAM_D[4]**/ GP0[21] | AD17 | I | IPU DVDD_C | VIN[0]B, GP0 PINCNTL167 DSIS: PIN | |
| VOUT[1]_G_Y_YC[1]/ **CAM_D[3]**/ GPMC_A[5]/ UART4_RXD/ GP0[22] | AD18 | I | IPU DVDD_C | VOUT[1], GPMC, UART4, GP0 PINCNTL168 DSIS: PIN | |
| VOUT[1]_G_Y_YC[0]/ **CAM_D[2]**/ GPMC_A[6]/ UART4_TXD/ GP0[23] | AC18 | I | IPD DVDD_C | VOUT[1], GPMC, UART4, GP0 PINCNTL169 DSIS: PIN | |
| VOUT[1]_R_CR[1]/ **CAM_D[1]**/ GPMC_A[7]/ UART4_CTS/ GP0[24] | AC19 | I | IPD DVDD_C | VOUT[1], GPMC, UART4, GP0 PINCNTL170 DSIS: PIN | |
| VOUT[1]_R_CR[0]/ **CAM_D[0]**/ GPMC_A[8]/ UART4_RTS/ GP0[25] | AA22 | I | IPD DVDD_C | VOUT[1], GPMC, UART4, GP0 PINCNTL171 DSIS: PIN | |
| VOUT[1]_B_CB_C[1]/ **CAM_HS**/ GPMC_A[9]/ UART2_RXD/ GP0[26] | AE23 | I/O | IPD DVDD_C | VOUT[1], GPMC, UART2, GP0 PINCNTL172 DSIS: 0 | Camera Horizontal Synchronization |
| VOUT[1]_B_CB_C[0]/ **CAM_VS**/ GPMC_A[10]/ UART2_TXD/ GP0[27] | AD23 | I/O | IPU DVDD_C | VOUT[1], GPMC, UART2, GP0 PINCNTL173 DSIS: 0 | Camera Vertical Synchronization |
| VIN[0]A_D[13]_BD[5]/ **CAM_RESET**/ GP2[18] | AF17 | I/O | IPD DVDD | VIN[0]AB, GP2 PINCNTL153 DSIS: 0 | Camera Reset. Used for Strobe Synchronization |
| VIN[0]A_D[11]_BD[3]/ **CAM_WE**/ GP2[16] | AH17 | I | IPD DVDD | VIN[0]AB. GP2 PINCNTL151 DSIS: 0 MM: MUX1 | Camera Write Enable |
| VOUT[1]_FLD/ CAM_FLD/ **CAM_WE**/ GPMC_A[11]/ UART2_CTS/ GP0[28] | AB23 | I | IPD DVDD_C | VOUT[1], CAMERA_I/F, GPMC, UART2, GP0 PINCNTL174 DSIS: 0 MM: MUX0 | |
| VOUT[1]_FLD/ **CAM_FLD**/ CAM_WE/ GPMC_A[11]/ UART2_CTS/ GP0[28] | AB23 | I/O | IPD DVDD_C | VOUT[1], CAMERA_I/F, GPMC, UART2, GP0 PINCNTL174 DSIS: 0 | Camera Field Identification input |

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**Table 4-2. Camera I/F Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| VIN[0]A_D[14]_BD[6]/ **CAM_STROBE**/ GP2[19] | AC12 | O | IPD DVDD | VIN[0]AB, GP2 PINCNTL154 DSIS: N/A | Camera Flash Strobe Control Signal |
| VIN[0]A_D[15]_BD[7]/ **CAM_SHUTTER**/ GP2[20] | AC14 | O | IPD DVDD | VIN[0]AB, GP2 PINCNTL155 DSIS: N/A | Camera Mechanical Shutter Control Signal |


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### 4.2.3 CSI2 Interface (I/F) Signals

**Table 4-3. CSI2 I/F Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| CSI2_DX[0] | L27 | I | – VDDA_CSI2_1P8 | – | CSI2 Camera lane 0 differential pair |
| CSI2_DY[0] | L28 | I | – VDDA_CSI2_1P8 | – | |
| CSI2_DX[1] | M27 | I | – VDDA_CSI2_1P8 | – | CSI2 Camera lane 1 differential pair |
| CSI2_DY[1] | M28 | I | – VDDA_CSI2_1P8 | – | |
| CSI2_DX[2] | N28 | I | – VDDA_CSI2_1P8 | – | CSI2 Camera lane 2 differential pair |
| CSI2_DY[2] | N27 | I | – VDDA_CSI2_1P8 | – | |
| CSI2_DX[3] | P28 | I | – VDDA_CSI2_1P8 | – | CSI2 Camera lane 3 differential pair |
| CSI2_DY[3] | P27 | I | – VDDA_CSI2_1P8 | – | |
| CSI2_DX[4] | R27 | I | – VDDA_CSI2_1P8 | – | CSI2 Camera lane 4 differential pair |
| CSI2_DY[4] | R28 | I | – VDDA_CSI2_1P8 | – | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal

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### 4.2.4 Controller Area Network (DCAN) Modules (DCAN0, DCAN1)

**Table 4-4. DCAN Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **DCAN0** | | | | | |
| **DCAN0_RX**/ UART2_RXD/ I2C[3]_SCL/ GP1[1] | AG6 | I/O | IPU DVDD | UART2, I2C[3], GP1 PINCNTL69 DSIS: 1 | DCAN0 receive data pin. |
| **DCAN0_TX**/ UART2_TXD/ I2C[3]_SDA/ GP1[0] | AH6 | I/O | IPU DVDD | UART2, I2C[3], GP1 PINCNTL68 DSIS: 1 | DCAN0 transmit data pin. |
| **DCAN1** | | | | | |
| $\overline{\text{UART0_RTS}}$/ UART4_TXD/ **DCAN1_RX**/ SPI[1]_SCS[2]/ SD2_SDCD | AF5 | I/O | IPU DVDD | UART0, UART4, SPI[1], SD2 PINCNTL73 DSIS: 1 | DCAN1 receive data pin. |
| $\overline{\text{UART0_CTS}}$/ UART4_RXD/ **DCAN1_TX**/ SPI[1]_SCS[3]/ SD0_SDCD | AE6 | I/O | IPU DVDD | UART0, UART4, SPI[1], SD0 PINCNTL72 DSIS: 1 | DCAN1 transmit data pin. |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal


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### 4.2.5 DDR2/DDR3 Memory Controller

**Table 4-5. DDR2/DDR3 Memory Controller 0 Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| **DDR2/DDR3 Memory Controller 0 (DDR[0])** | | | | |
| DDR[0]_CLK | B16 | O | IPD/DIS DVDD_DDR[0] | DDR[0] Clock<br>The internal pulldown (IPD) is enabled for this pin when the device is in reset and the IPD is disabled (DIS) when reset is released. |
| $\overline{\text{DDR[0]_CLK}}$ | A16 | O | IPU/DIS DVDD_DDR[0] | DDR[0] Negative Clock<br>The internal pullup (IPU) is enabled for this pin when the device is in reset and the IPU is disabled (DIS) when reset is released. |
| DDR[0]_CKE | H18 | O | IPD DVDD_DDR[0] | DDR[0] Clock Enable |
| $\overline{\text{DDR[0]_WE}}$ | C17 | O | IPU/DIS DVDD_DDR[0] | DDR[0] Write Enable<br>The internal pullup (IPU) is enabled for this pin when the device is in reset and the IPU is disabled (DIS) when reset is released. |
| $\overline{\text{DDR[0]_CS[0]}}$ | F18 | O | IPU/DIS DVDD_DDR[0] | DDR[0] Chip Select 0<br>The internal pullup (IPU) is enabled for this pin when the device is in reset and the IPU is disabled (DIS) when reset is released. |
| $\overline{\text{DDR[0]_CS[1]}}$ | G17 | O | IPU/DIS DVDD_DDR[0] | DDR[0] Chip Select 1<br>The internal pullup (IPU) is enabled for this pin when the device is in reset and the IPU is disabled (DIS) when reset is released. |
| $\overline{\text{DDR[0]_RAS}}$ | B18 | O | IPU/DIS DVDD_DDR[0] | DDR[0] Row Address Strobe output<br>The internal pullup (IPU) is enabled for this pin when the device is in reset and the IPU is disabled (DIS) when reset is released. |
| $\overline{\text{DDR[0]_CAS}}$ | C18 | O | IPU/DIS DVDD_DDR[0] | DDR[0] Column Address Strobe output<br>The internal pullup (IPU) is enabled for this pin when the device is in reset and the IPU is disabled (DIS) when reset is released. |
| DDR[0]_DQM[3] | F20 | O | IPU/IPD DVDD_DDR[0] | DDR[0] Data Mask outputs<br>DDR[0]_DQM[3]: For upper byte data bus DDR[0]_D[31:24]<br>DDR[0]_DQM[2]: For DDR[0]_D[23:16]<br>DDR[0]_DQM[1]: For DDR[0]_D[15:8]<br>DDR[0]_DQM[0]: For lower byte data bus DDR[0]_D[7:0]<br>The internal pullup (IPU) is enabled for these pins when the device is in reset and switches to an IPD enabled when reset is released. |
| DDR[0]_DQM[2] | C24 | O | IPU/IPD DVDD_DDR[0] | |
| DDR[0]_DQM[1] | B28 | O | IPU/IPD DVDD_DDR[0] | |
| DDR[0]_DQM[0] | E28 | O | IPU/IPD DVDD_DDR[0] | |
| DDR[0]_DQS[3] | B21 | I/O | IPD DVDD_DDR[0] | Data strobe input/outputs for each byte of the 32-bit data bus. They are outputs to the DDR[0] memory when writing and inputs when reading. They are used to synchronize the data transfers.<br>DDR[0]_DQS[3]: For upper byte data bus DDR[0]_D[31:24]<br>DDR[0]_DQS[2]: For DDR[0]_D[23:16]<br>DDR[0]_DQS[1]: For DDR[0]_D[15:8]<br>DDR[0]_DQS[0]: For lower byte data bus DDR[0]_D[7:0] |
| DDR[0]_DQS[2] | B23 | I/O | IPD DVDD_DDR[0] | |
| DDR[0]_DQS[1] | B26 | I/O | IPD DVDD_DDR[0] | |
| DDR[0]_DQS[0] | D28 | I/O | IPD DVDD_DDR[0] | |
| $\overline{\text{DDR[0]_DQS[3]}}$ | A21 | I/O | IPU DVDD_DDR[0] | Complementary data strobe input/outputs for each byte of the 32-bit data bus. They are outputs to the DDR[0] memory when writing and inputs when reading. They are used to synchronize the data transfers.<br>$\overline{\text{DDR[0]_DQS[3]}}$: For upper byte data bus DDR[0]_D[31:24]<br>$\overline{\text{DDR[0]_DQS[2]}}$: For DDR[0]_D[23:16]<br>$\overline{\text{DDR[0]_DQS[1]}}$: For DDR[0]_D[15:8]<br>DDR[0]_DQS[0]: For lower byte data bus DDR[0]_D[7:0] |
| $\overline{\text{DDR[0]_DQS[2]}}$ | A23 | I/O | IPU DVDD_DDR[0] | |
| $\overline{\text{DDR[0]_DQS[1]}}$ | A26 | I/O | IPU DVDD_DDR[0] | |
| $\overline{\text{DDR[0]_DQS[0]}}$ | D27 | I/O | IPU DVDD_DDR[0] | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull during and after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal

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**Table 4-5. DDR2/DDR3 Memory Controller 0 Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| DDR[0]_ODT[0] | G18 | O | IPD/DIS DVDD_DDR[0] | DDR[0] On-Die Termination for Chip Select 0. The internal pulldown (IPD) is enabled for this pin when the device is in reset and the IPD is disabled (DIS) when reset is released. |
| DDR[0]_ODT[1] | H19 | O | IPD/DIS DVDD_DDR[0] | DDR[0] On-Die Termination for Chip Select 1. The internal pulldown (IPD) is enabled for this pin when the device is in reset and the IPD is disabled (DIS) when reset is released. |
| DDR[0]_RST | G19 | O | IPD/DIS DVDD_DDR[0] | DDR[0] Reset output<br>The internal pulldown (IPD) is enabled for this pin when the device is in reset and the IPD is disabled (DIS) when reset is released. |
| DDR[0]_BA[2] | A18 | O | IPU/DIS DVDD_DDR[0] | DDR[0] Bank Address outputs<br>The internal pullup (IPU) is enabled for these pins when the device is in reset and the IPU is disabled (DIS) when reset is released. |
| DDR[0]_BA[1] | A20 | O | IPU/DIS DVDD_DDR[0] | |
| DDR[0]_BA[0] | F15 | O | IPU/DIS DVDD_DDR[0] | |
| DDR[0]_A[14] | F16 | O | IPU/DIS DVDD_DDR[0] | DDR[0] Address Bus<br>The internal pullup (IPU) is enabled for these pins when the device is in reset and the IPU is disabled (DIS) when reset is released. |
| DDR[0]_A[13] | F17 | O | IPU/DIS DVDD_DDR[0] | |
| DDR[0]_A[12] | E17 | O | IPU/DIS DVDD_DDR[0] | |
| DDR[0]_A[11] | D17 | O | IPU/DIS DVDD_DDR[0] | |
| DDR[0]_A[10] | A19 | O | IPU/DIS DVDD_DDR[0] | |
| DDR[0]_A[9] | C15 | O | IPU/DIS DVDD_DDR[0] | |
| DDR[0]_A[8] | B15 | O | IPU/DIS DVDD_DDR[0] | |
| DDR[0]_A[7] | E18 | O | IPU/DIS DVDD_DDR[0] | |
| DDR[0]_A[6] | A15 | O | IPU/DIS DVDD_DDR[0] | |
| DDR[0]_A[5] | B17 | O | IPU/DIS DVDD_DDR[0] | |
| DDR[0]_A[4] | D15 | O | IPU/DIS DVDD_DDR[0] | |
| DDR[0]_A[3] | E15 | O | IPU/DIS DVDD_DDR[0] | |
| DDR[0]_A[2] | D18 | O | IPU/DIS DVDD_DDR[0] | |
| DDR[0]_A[1] | F19 | O | IPU/DIS DVDD_DDR[0] | |
| DDR[0]_A[0] | B19 | O | IPU/DIS DVDD_DDR[0] | |


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**Table 4-5. DDR2/DDR3 Memory Controller 0 Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| DDR[0]_D[31] | B20 | I/O | IPD DVDD_DDR[0] | DDR[0] Data Bus |
| DDR[0]_D[30] | D21 | I/O | IPD DVDD_DDR[0] | |
| DDR[0]_D[29] | C21 | I/O | IPD DVDD_DDR[0] | |
| DDR[0]_D[28] | C20 | I/O | IPD DVDD_DDR[0] | |
| DDR[0]_D[27] | A22 | I/O | IPD DVDD_DDR[0] | |
| DDR[0]_D[26] | G20 | I/O | IPD DVDD_DDR[0] | |
| DDR[0]_D[25] | F21 | I/O | IPD DVDD_DDR[0] | |
| DDR[0]_D[24] | H20 | I/O | IPD DVDD_DDR[0] | |
| DDR[0]_D[23] | B22 | I/O | IPD DVDD_DDR[0] | |
| DDR[0]_D[22] | C23 | I/O | IPD DVDD_DDR[0] | |
| DDR[0]_D[21] | E23 | I/O | IPD DVDD_DDR[0] | |
| DDR[0]_D[20] | D23 | I/O | IPD DVDD_DDR[0] | |
| DDR[0]_D[19] | G21 | I/O | IPD DVDD_DDR[0] | |
| DDR[0]_D[18] | H21 | I/O | IPD DVDD_DDR[0] | |
| DDR[0]_D[17] | F22 | I/O | IPD DVDD_DDR[0] | |
| DDR[0]_D[16] | B24 | I/O | IPD DVDD_DDR[0] | |

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**Table 4-5. DDR2/DDR3 Memory Controller 0 Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| DDR[0]_D[15] | A24 | I/O | IPD DVDD_DDR[0] | DDR[0] Data Bus |
| DDR[0]_D[14] | A25 | I/O | IPD DVDD_DDR[0] | |
| DDR[0]_D[13] | D24 | I/O | IPD DVDD_DDR[0] | |
| DDR[0]_D[12] | B25 | I/O | IPD DVDD_DDR[0] | |
| DDR[0]_D[11] | A27 | I/O | IPD DVDD_DDR[0] | |
| DDR[0]_D[10] | C26 | I/O | IPD DVDD_DDR[0] | |
| DDR[0]_D[9] | C25 | I/O | IPD DVDD_DDR[0] | |
| DDR[0]_D[8] | C27 | I/O | IPD DVDD_DDR[0] | |
| DDR[0]_D[7] | C28 | I/O | IPD DVDD_DDR[0] | |
| DDR[0]_D[6] | D26 | I/O | IPD DVDD_DDR[0] | |
| DDR[0]_D[5] | E25 | I/O | IPD DVDD_DDR[0] | |
| DDR[0]_D[4] | F24 | I/O | IPD DVDD_DDR[0] | |
| DDR[0]_D[3] | F25 | I/O | IPD DVDD_DDR[0] | |
| DDR[0]_D[2] | E26 | I/O | IPD DVDD_DDR[0] | |
| DDR[0]_D[1] | F26 | I/O | IPD DVDD_DDR[0] | |
| DDR[0]_D[0] | E27 | I/O | IPD DVDD_DDR[0] | |
| DDR[0]_VTP | B27 | I | – DVDD_DDR[0] | DDR VTP Compensation Resistor Connection |


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## Table 4-6. DDR2/DDR3 Memory Controller 1 Terminal Functions

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| **DDR2/DDR3 Memory Controller 1 (DDR[1])** | | | | |
| DDR[1]_CLK | B13 | O | IPD/DIS DVDD_DDR[1] | DDR[1] Clock<br>The internal pulldown (IPD) is enabled for this pin when the device is in reset and the IPD is disabled (DIS) when reset is released. |
| $\overline{\text{DDR[1]_CLK}}$ | A13 | O | IPU/DIS DVDD_DDR[1] | DDR[1] Negative Clock<br>The internal pullup (IPU) is enabled for this pin when the device is in reset and the IPU is disabled (DIS) when reset is released. |
| DDR[1]_CKE | H11 | O | IPD DVDD_DDR[1] | DDR[1] Clock Enable |
| $\overline{\text{DDR[1]_WE}}$ | E12 | O | IPU/DIS DVDD_DDR[1] | DDR[1] Write Enable<br>The internal pullup (IPU) is enabled for this pin when the device is in reset and the IPU is disabled (DIS) when reset is released. |
| $\overline{\text{DDR[1]_CS[0]}}$ | G12 | O | IPU/DIS DVDD_DDR[1] | DDR[1] Chip Select 0<br>The internal pullup (IPU) is enabled for this pin when the device is in reset and the IPU is disabled (DIS) when reset is released. |
| $\overline{\text{DDR[1]_CS[1]}}$ | G11 | O | IPU/DIS DVDD_DDR[1] | DDR[1] Chip Select 1<br>The internal pullup (IPU) is enabled for this pin when the device is in reset and the IPU is disabled (DIS) when reset is released. |
| $\overline{\text{DDR[1]_RAS}}$ | C12 | O | IPU/DIS DVDD_DDR[1] | DDR[1] Row Address Strobe output<br>The internal pullup (IPU) is enabled for this pin when the device is in reset and the IPU is disabled (DIS) when reset is released. |
| $\overline{\text{DDR[1]_CAS}}$ | F13 | O | IPU/DIS DVDD_DDR[1] | DDR[1] Column Address Strobe output<br>The internal pullup (IPU) is enabled for this pin when the device is in reset and the IPU is disabled (DIS) when reset is released. |
| DDR[1]_DQM[3] | G9 | O | IPU/IPD DVDD_DDR[1] | DDR[1] Data Mask outputs<br>DDR[1]_DQM[3]: For upper byte data bus DDR[1]_D[31:24]<br>DDR[1]_DQM[2]: For DDR[1]_D[23:16]<br>DDR[1]_DQM[1]: For DDR[1]_D[15:8]<br>DDR[1]_DQM[0]: For lower byte data bus DDR[1]_D[7:0]<br><br>The internal pullup (IPU) is enabled for these pins when the device is in reset and switches to an IPD enabled when reset is released. |
| DDR[1]_DQM[2] | G8 | O | IPU/IPD DVDD_DDR[1] | |
| DDR[1]_DQM[1] | B2 | O | IPU/IPD DVDD_DDR[1] | |
| DDR[1]_DQM[0] | F4 | O | IPU/IPD DVDD_DDR[1] | |
| DDR[1]_DQS[3] | B8 | I/O | IPD DVDD_DDR[1] | Data strobe input/outputs for each byte of the 32-bit data bus. They are outputs to the DDR[1] memory when writing and inputs when reading. They are used to synchronize the data transfers.<br>DDR[1]_DQS[3]: For upper byte data bus DDR[1]_D[31:24]<br>DDR[1]_DQS[2]: For DDR[1]_D[23:16]<br>DDR[1]_DQS[1]: For DDR[1]_D[15:8]<br>DDR[1]_DQS[0]: For lower byte data bus DDR[1]_D[7:0] |
| DDR[1]_DQS[2] | A6 | I/O | IPD DVDD_DDR[1] | |
| DDR[1]_DQS[1] | B3 | I/O | IPD DVDD_DDR[1] | |
| DDR[1]_DQS[0] | D1 | I/O | IPD DVDD_DDR[1] | |
| $\overline{\text{DDR[1]_DQS[3]}}$ | A8 | I/O | IPU DVDD_DDR[1] | Complementary data strobe input/outputs for each byte of the 32-bit data bus. They are outputs to the DDR[1] memory when writing and inputs when reading. They are used to synchronize the data transfers.<br>$\overline{\text{DDR[1]_DQS[3]}}$: For upper byte data bus DDR[1]_D[31:24]<br>$\overline{\text{DDR[1]_DQS[2]}}$: For DDR[1]_D[23:16]<br>$\overline{\text{DDR[1]_DQS[1]}}$: For DDR[1]_D[15:8]<br>DDR[1]_DQS[0]: For lower byte data bus DDR[1]_D[7:0] |
| $\overline{\text{DDR[1]_DQS[2]}}$ | B6 | I/O | IPU DVDD_DDR[1] | |
| $\overline{\text{DDR[1]_DQS[1]}}$ | A3 | I/O | IPU DVDD_DDR[1] | |
| $\overline{\text{DDR[1]_DQS[0]}}$ | D2 | I/O | IPU DVDD_DDR[1] | |
| DDR[1]_ODT[0] | H10 | O | IPD/DIS DVDD_DDR[1] | DDR[1] On-Die Termination for Chip Select 0.<br>The internal pulldown (IPD) is enabled for this pin when the device is in reset and the IPD is disabled (DIS) when reset is released. |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull during and after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal

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**Table 4-6. DDR2/DDR3 Memory Controller 1 Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE[1] | OTHER[2] [3] | DESCRIPTION |
|---|---|---|---|---|
| DDR[1]_ODT[1] | F11 | O | IPD/DIS DVDD_DDR[1] | DDR[1] On-Die Termination for Chip Select 1. The internal pulldown (IPD) is enabled for this pin when the device is in reset and the IPD is disabled (DIS) when reset is released. |
| DDR[1]_RST | G10 | O | IPD/DIS DVDD_DDR[1] | DDR[1] Reset output. The internal pulldown (IPD) is enabled for this pin when the device is in reset and the IPD is disabled (DIS) when reset is released. |
| DDR[1]_BA[2] | D12 | O | IPU/DIS DVDD_DDR[1] | DDR[1] Bank Address outputs<br>The internal pullup (IPU) is enabled for these pins when the device is in reset and the IPU is disabled (DIS) when reset is released. |
| DDR[1]_BA[1] | A10 | O | IPU/DIS DVDD_DDR[1] | |
| DDR[1]_BA[0] | F14 | O | IPU/DIS DVDD_DDR[1] | |
| DDR[1]_A[14] | D11 | O | IPU/DIS DVDD_DDR[1] | DDR[1] Address Bus<br>The internal pullup (IPU) is enabled for these pins when the device is in reset and the IPU is disabled (DIS) when reset is released. |
| DDR[1]_A[13] | E11 | O | IPU/DIS DVDD_DDR[1] | |
| DDR[1]_A[12] | B10 | O | IPU/DIS DVDD_DDR[1] | |
| DDR[1]_A[11] | A11 | O | IPU/DIS DVDD_DDR[1] | |
| DDR[1]_A[10] | F12 | O | IPU/DIS DVDD_DDR[1] | |
| DDR[1]_A[9] | C14 | O | IPU/DIS DVDD_DDR[1] | |
| DDR[1]_A[8] | E14 | O | IPU/DIS DVDD_DDR[1] | |
| DDR[1]_A[7] | A9 | O | IPU/DIS DVDD_DDR[1] | |
| DDR[1]_A[6] | D14 | O | IPU/DIS DVDD_DDR[1] | |
| DDR[1]_A[5] | B12 | O | IPU/DIS DVDD_DDR[1] | |
| DDR[1]_A[4] | B14 | O | IPU/DIS DVDD_DDR[1] | |
| DDR[1]_A[3] | A14 | O | IPU/DIS DVDD_DDR[1] | |
| DDR[1]_A[2] | C11 | O | IPU/DIS DVDD_DDR[1] | |
| DDR[1]_A[1] | F10 | O | IPU/DIS DVDD_DDR[1] | |
| DDR[1]_A[0] | B11 | O | IPU/DIS DVDD_DDR[1] | |


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**Table 4-6. DDR2/DDR3 Memory Controller 1 Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| DDR[1]_D[31] | B9 | I/O | IPD DVDD_DDR[1] | DDR[1] Data Bus |
| DDR[1]_D[30] | C8 | I/O | IPD DVDD_DDR[1] | |
| DDR[1]_D[29] | D8 | I/O | IPD DVDD_DDR[1] | |
| DDR[1]_D[28] | C9 | I/O | IPD DVDD_DDR[1] | |
| DDR[1]_D[27] | A7 | I/O | IPD DVDD_DDR[1] | |
| DDR[1]_D[26] | F8 | I/O | IPD DVDD_DDR[1] | |
| DDR[1]_D[25] | H9 | I/O | IPD DVDD_DDR[1] | |
| DDR[1]_D[24] | F9 | I/O | IPD DVDD_DDR[1] | |
| DDR[1]_D[23] | B7 | I/O | IPD DVDD_DDR[1] | |
| DDR[1]_D[22] | D6 | I/O | IPD DVDD_DDR[1] | |
| DDR[1]_D[21] | E6 | I/O | IPD DVDD_DDR[1] | |
| DDR[1]_D[20] | C6 | I/O | IPD DVDD_DDR[1] | |
| DDR[1]_D[19] | B5 | I/O | IPD DVDD_DDR[1] | |
| DDR[1]_D[18] | C5 | I/O | IPD DVDD_DDR[1] | |
| DDR[1]_D[17] | F7 | I/O | IPD DVDD_DDR[1] | |
| DDR[1]_D[16] | H8 | I/O | IPD DVDD_DDR[1] | |

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**Table 4-6. DDR2/DDR3 Memory Controller 1 Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE[1] | OTHER[2] [3] | DESCRIPTION |
|---|---|---|---|---|
| DDR[1]_D[15] | A5 | I/O | IPD DVDD_DDR[1] | DDR[1] Data Bus |
| DDR[1]_D[14] | A4 | I/O | IPD DVDD_DDR[1] | |
| DDR[1]_D[13] | C4 | I/O | IPD DVDD_DDR[1] | |
| DDR[1]_D[12] | B4 | I/O | IPD DVDD_DDR[1] | |
| DDR[1]_D[11] | A2 | I/O | IPD DVDD_DDR[1] | |
| DDR[1]_D[10] | C3 | I/O | IPD DVDD_DDR[1] | |
| DDR[1]_D[9] | D5 | I/O | IPD DVDD_DDR[1] | |
| DDR[1]_D[8] | C2 | I/O | IPD DVDD_DDR[1] | |
| DDR[1]_D[7] | C1 | I/O | IPD DVDD_DDR[1] | |
| DDR[1]_D[6] | D3 | I/O | IPD DVDD_DDR[1] | |
| DDR[1]_D[5] | E4 | I/O | IPD DVDD_DDR[1] | |
| DDR[1]_D[4] | F5 | I/O | IPD DVDD_DDR[1] | |
| DDR[1]_D[3] | E1 | I/O | IPD DVDD_DDR[1] | |
| DDR[1]_D[2] | E2 | I/O | IPD DVDD_DDR[1] | |
| DDR[1]_D[1] | F3 | I/O | IPD DVDD_DDR[1] | |
| DDR[1]_D[0] | E3 | I/O | IPD DVDD_DDR[1] | |
| DDR[1]_VTP | B1 | I | – DVDD_DDR[1] | DDR[1] VTP Compensation Resistor Connection |


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### 4.2.6 EDMA

**Table 4-7. EDMA Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **EDMA** | | | | | |
| AUD_CLKIN1/ MCA[0]_AXR[8]/ MCA[1]_AHCLKX/ MCA[4]_AHCLKX/ **EDMA_EVT3**/ TIM2_IO/ GP0[8] | R5 | I | IPD DVDD | AUD_CLKIN1, MCA[0], MCA[1], MCA[4], TIMER2, GP0 PINCNTL15 DSIS: PIN MM: MUX1 | External EDMA Event 3 |
| GPMC_CLK/ GPMC_CS[5]/ GPMC_WAIT[1]/ CLKOUT1/ **EDMA_EVT3**/ TIM4_IO/ GP1[27] | R26 | I | IPU DVDD_GPMC | GPMC, CLKOUT1, TIMER4, GP1 PINCNTL127 DSIS: PIN MM: MUX0 | |
| AUD_CLKIN2/ MCA[0]_AXR[9]/ MCA[2]_AHCLKX/ MCA[5]_AHCLKX/ **EDMA_EVT2**/ TIM3_IO/ GP0[9] | H1 | I | IPD DVDD | AUD_CLKIN2, MCA[0], MCA[2]. MCA[5], TIMER3, GP0 PINCNTL16 DSIS: PIN MM: MUX1 | External EDMA Event 2 |
| GPMC_BE[0]_CLE/ GPMC_A[25]/ **EDMA_EVT2**/ TIM6_IO/ GP1[29] | U27 | I | IPD DVDD_GPMC | GPMC, TIMER6, GP1 PINCNTL131 DSIS: PIN MM: MUX0 | |
| SPI[0]_SCS[1]/ SD1_SDCD/ **EDMA_EVT1**/ TIM4_IO/ GP1[6] | AE5 | I | IPU DVDD | SPI[0], SD1 TIMER4, GP1 PINCNTL80 DSIS: PIN MM: MUX1 | External EDMA Event 1 |
| GPMC_BE[1]/ GPMC_A[24]/ **EDMA_EVT1**/ TIM7_IO/ GP1[30] | V28 | I | IPD DVDD_GPMC | GPMC, TIMER7, GP1 PINCNTL132 DSIS: PIN MM: MUX0 | |
| SD2_DAT[4]/ GPMC_A[27]/ GPMC_A[23]/ GPMC_CS[7]/ **EDMA_EVT0**/ TIM7_IO/ GP1[22] | R24 | I | IPU DVDD_GPMC | SD2, GPMC, TIMER7, GP1 PINCNTL116 DSIS: PIN MM: MUX1 | External EDMA Event 0 |
| GPMC_WAIT[0]/ GPMC_A[26]/ **EDMA_EVT0**/ GP1[31] | W28 | I | IPU DVDD_GPMC | GPMC, GP1 PINCNTL133 DSIS: PIN MM: MUX0 | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and the Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal

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### 4.2.7 EMAC [(R)(G)MII Modes] and MDIO

**Table 4-8. EMAC[0] Terminal Functions [(R)(G)MII]**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **EMAC[0] (G)MII Mode** | | | | | |
| An EMAC bootmode must be selected via the BTMODE[4:0] pins. Once the EMAC bootmode is selected, the BTMODE[9:8] pins determine the Ethernet PHY Mode Selection (for example, 00b is MII mode). For more detailed information on EMAC bootmodes and Ethernet PHY Mode selection, see Section 5.2.6, *Ethernet PHY Mode Selection*.<br>These pin functions are available *only* when GMII or MII modes are selected. | | | | | |
| **EMAC[0]_MCOL**/<br>EMAC[0]_RGRXCTL/<br>EMAC[0]_RMRXD[0]/<br>GP3[24] | L23 | I | IPD<br>DVDD_GPMC | EMAC[0], GP3<br>PINCNTL236<br>DSIS: 0 | [G]MII Collision Detect (Sense) input |
| **EMAC[0]_MCRS**/<br>EMAC[0]_RGRXD[2]/<br>EMAC[0]_RMRXD[1]/<br>GP3[25] | R25 | I | IPD<br>DVDD_GPMC | EMAC[0], GP3<br>PINCNTL237<br>DSIS: 0 | [G]MII Carrier Sense input |
| **EMAC[0]_GMTCLK**/<br>EMAC[1]_RGRXC/<br>GPMC_A[6]/<br>SPI[2]_D[1] | K23 | O | IPD<br>DVDD_GPMC | EMAC[1],<br>GPMC, SPI[2]<br>PINCNTL249<br>DSIS: N/A | GMII Source Synchronous Transmit Clock |
| **EMAC[0]_MRCLK**/<br>EMAC[0]_RGTXC/<br>EMAC[0]_RMCRSDV/<br>SPI[3]_SCS[2]/<br>GP3[27] | H27 | I | IPD<br>DVDD_GPMC | EMAC[0],<br>SPI[3], GP3<br>PINCNTL239<br>DSIS: 0 | [G]MII Receive Clock |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal


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**Table 4-8. EMAC[0] Terminal Functions [(R)(G)MII] (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **EMAC[0]_MRXD[7]**/ EMAC[0]_RGTXD[1]/ GPMC_A[4]/ SPI[2]_SCS[3] | G27 | I | IPD DVDD_GPMC | EMAC[0], GPMC, SPI[2] PINCNTL247 DSIS: PIN | [G]MII Receive Data [7:0]. For 1000 EMAC GMII operation, EMAC[0]_RXD[7:0] are used. For 10/100 EMAC MII operation, *only* EMAC[0]_RXD[3:0] are used. |
| **EMAC[0]_MRXD[6]**/ EMAC[0]_RGTXD[2]/ GPMC_A[3]/ UART5_RTS | F28 | | | EMAC[0], GPMC, UART5 PINCNTL246 DSIS: PIN | |
| **EMAC[0]_MRXD[5]**/ EMAC[0]_RGTXD[3]/ GPMC_A[2]/ UART5_CTS | H26 | | | EMAC[0], GPMC, UART5 PINCNTL245 DSIS: PIN | |
| **EMAC[0]_MRXD[4]**/ EMAC[0]_RGRXD[3]/ GPMC_A[1]/ UART5_TXD | T23 | | | EMAC[0], GPMC, UART5 PINCNTL244 DSIS: PIN | |
| **EMAC[0]_MRXD[3]**/ EMAC[1]_RGRXCTL/ GPMC_A[27]/ GPMC_A[26]/ GPMC_A[0]/ UART5_RXD | J25 | | | EMAC[1], GPMC, UART5 PINCNTL243 DSIS: PIN | |
| **EMAC[0]_MRXD[2]**/ EMAC[0]_RGRXD[1]/ EMAC[0]_RMTXEN/ GP3[30] | R23 | | | EMAC[0], GP3 PINCNTL242 DSIS: PIN | |
| **EMAC[0]_MRXD[1]**/ EMAC[0]_RGRXD[0]/ EMAC[0]_RMTXD[1]/ GP3[29] | P23 | | | EMAC[0], GP3 PINCNTL241 DSIS: PIN | |
| **EMAC[0]_MRXD[0]**/ EMAC[0]_RGTXD[0]/ EMAC[0]_RMTXD[0]/ GP3[28] | G28 | | | EMAC[0], GP3 PINCNTL240 DSIS: PIN | |
| **EMAC[0]_MRXDV**/ EMAC[1]_RGRXD[1]/ GPMC_A[5]/ SPI[2]_SCLK | K22 | I | IPD DVDD_GPMC | EMAC[1], GPMC, SPI[2] PINCNTL248 DSIS: 0 | [G]MII Receive Data Valid input |
| **EMAC[0]_MRXER**/ EMAC[0]_RGTXCTL/ EMAC[0]_RMRXER/ GP3[26] | J26 | I | IPD DVDD_GPMC | EMAC[0], GP3 PINCNTL238 DSIS: 0 | [G]MII Receive Data Error input |
| **EMAC[0]_MTCLK**/ EMAC[0]_RGRXC/ SPI[3]_SCS[3]/ I2C[2]_SDA/ GP3[23] | L24 | I | IPD DVDD_GPMC | EMAC[0], SPI[3], I2C[2], GP3 PINCNTL235 DSIS: 0 | [G]MII Transmit Clock input |

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**Table 4-8. EMAC[0] Terminal Functions [(R)(G)MII] (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **EMAC[0]_MTXD[7]**/ EMAC[1]_RGTXD[3]/ EMAC[1]_RMTXD[1]/ GPMC_A[14]/ UART1_CTS | H24 | O | IPD DVDD_GPMC | EMAC[1], GPMC, UART1 PINCNTL257 DSIS: N/A | [G]MII Transmit Data [7:0]. For 1000 EMAC GMII operation, EMAC[0]_TXD[7:0] are used. For 10/100 EMAC MII operation, *only* EMAC[0]_TXD[3:0] are used. |
| **EMAC[0]_MTXD[6]**/ EMAC[1]_RGRXD[0]/ EMAC[1]_RMTXD[0]/ GPMC_A[13]/ UART1_TXD | J22 | | | EMAC[1], GPMC, UART1 PINCNTL256 DSIS: N/A | |
| **EMAC[0]_MTXD[5]**/ EMAC[1]_RGTXC/ EMAC[1]_RMCRSDV/ GPMC_A[12]/ UART1_RXD | F27 | | | EMAC[1], GPMC, UART1 PINCNTL255 DSIS: N/A | |
| **EMAC[0]_MTXD[4]**/ EMAC[1]_RGTXD[2]/ EMAC[1]_RMRXER/ GPMC_A[11]/ UART4_RTS | G23 | | | EMAC[1], GPMC, UART4 PINCNTL254 DSIS: N/A | |
| **EMAC[0]_MTXD[3]**/ EMAC[1]_RGTXD[0]/ EMAC[1]_RMRXD[1]/ GPMC_A[10]/ UART4_CTS | H23 | | | EMAC[1], GPMC, UART4 PINCNTL253 DSIS: N/A | |
| **EMAC[0]_MTXD[2]**/ EMAC[1]_RGTXCTL/ EMAC[1]_RMRXD[0]/ GPMC_A[9]/ UART4_TXD | H22 | | | EMAC[1], GPMC, UART4 PINCNTL252 DSIS: N/A | |
| **EMAC[0]_MTXD[1]**/ EMAC[1]_RGTXD[1]/ GPMC_A[8]/ UART4_RXD | H25 | | | EMAC[1], GPMC, UART4 PINCNTL251 DSIS: N/A | |
| **EMAC[0]_MTXD[0]**/ EMAC[1]_RGRXD[3]/ GPMC_A[7]/ SPI[2]_D[0] | J24 | | | EMAC[1], GPMC, UART4 PINCNTL250 DSIS: N/A | |
| **EMAC[0]_MTXEN**/ EMAC[1]_RGRXD[2]/ EMAC[1]_RMTXEN/ GPMC_A[15]/ UART1_RTS | J23 | O | IPD DVDD_GPMC | EMAC[1], GPMC, UART4 PINCNTL258 DSIS: N/A | [G]MII Transmit Data Enable output |
| **EMAC[0] RMII Mode** | | | | | |
| An EMAC bootmode must be selected via the BTMODE[4:0] pins. Once the EMAC bootmode is selected, the BTMODE[9:8] pins determine the Ethernet PHY Mode Selection (for example, 01b is RMII mode). For more detailed information on EMAC bootmodes and Ethernet PHY Mode selection, see Section 5.2.6, *Ethernet PHY Mode Selection*. These pin functions are available *only* when RMII mode is selected. | | | | | |
| **EMAC_RMREFCLK**/ TIM2_IO/ GP1[10] | J27 | I/O | IPD DVDD_GPMC | TIMER2, GP1 PINCNTL232 DSIS: PIN | RMII Reference Clock (EMAC[0] and EMAC[1] RMII mode) Regardless of EMAC[0] RMII Mode, the GMII_EN bit in the MACCONTROL register, of the Control Module, configures the RMREFCLK pin function as an INPUT or OUTPUT clock reference. During RMII ROM Boot, the RMREFCLK pin function is configured as an OUTPUT clock reference (driving 50 MHz). |
| EMAC[0]_MRCLK/ EMAC[0]_RGTXC/ **EMAC[0]_RMCRSDV**/ SPI[3]_SCS[2]/ GP3[27] | H27 | I | IPD DVDD_GPMC | EMAC[0], SPI[3], GP3 PINCNTL239 DSIS: 0 | RMII Carrier Sense input |


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**Table 4-8. EMAC[0] Terminal Functions [(R)(G)MII] (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| EMAC[0]_MCRS/ EMAC[0]_RGRXD[2]/ **EMAC[0]_RMRXD[1]**/ GP3[25] | R25 | I | IPD DVDD_GPMC | EMAC[0], SPI[3], GPI3 PINCNTL237 DSIS: PIN | RMII Receive Data [1:0]. For 10/100 EMAC RMII operation, EMAC[0]_RMRXD[1:0] are used. |
| EMAC[0]_MCOL/ EMAC[0]_RGRXCTL/ **EMAC[0]_RMRXD[0]**/ GP3[24] | L23 | I | IPD DVDD_GPMC | EMAC[0], GP3 PINCNTL236 DSIS: PIN | |
| EMAC[0]_MRXER/ EMAC[0]_RGTXCTL/ **EMAC[0]_RMRXER**/ GP3[26] | J26 | I | IPD DVDD_GPMC | EMAC[0], GP3 PINCNTL238 DSIS: 0 | RMII Receive Data Error input |
| EMAC[0]_MRXD[1]/ EMAC[0]_RGRXD[0]/ **EMAC[0]_RMTXD[1]**/ GP3[29] | P23 | O | IPD DVDD_GPMC | EMAC[0], GP3 PINCNTL241 DSIS: N/A | RMII Transmit Data [7:0]. For 10/100 EMAC RMII operation, EMAC[0]_RMTXD[1:0] are used. |
| EMAC[0]_MRXD[0]/ EMAC[0]_RGTXD[0]/ **EMAC[0]_RMTXD[0]**/ GP3[28] | G28 | O | IPD DVDD_GPMC | EMAC[0], GP3 PINCNTL240 DSIS: N/A | |
| EMAC[0]_MRXD[2]/ EMAC[0]_RGRXD[1]/ **EMAC[0]_RMTXEN**/ GP3[30] | R23 | O | IPD DVDD_GPMC | EMAC[0], GP3 PINCNTL242 DSIS: N/A | RMII Transmit Data Enable output |
| **EMAC[0] RGMII Mode** | | | | | |
| An EMAC bootmode must be selected via the BTMODE[4:0] pins. Once the EMAC bootmode is selected, the BTMODE[9:8] pins determine the Ethernet PHY Mode Selection (for example, 10b is RGMII mode). For more detailed information on EMAC bootmodes and Ethernet PHY Mode selection, see Section 5.2.6, *Ethernet PHY Mode Selection*<br>These pin functions are available *only* when RGMII mode is selected. | | | | | |
| EMAC[0]_MTCLK/ **EMAC[0]_RGRXC**/ SPI[3]_SCS[3]/ I2C[2]_SDA/ GP3[23] | L24 | I | IPD DVDD_GPMC | EMAC[0], SPI[3], I2C[2], GP3 PINCNTL235 DSIS: PIN | RGMII Receive Clock |
| EMAC[0]_MCOL/ **EMAC[0]_RGRXCTL**/ EMAC[0]_RMRXD[0]/ GP3[24] | L23 | I | IPD DVDD_GPMC | EMAC[0], GP3 PINCNTL236 DSIS: PIN | RGMII Receive Control |
| EMAC[0]_MRXD[4]/ **EMAC[0]_RGRXD[3]**/ GPMC_A[1]/ UART5_TXD | T23 | I | IPD DVDD_GPMC | EMAC[0], GPMC, UART5 PINCNTL244 DSIS: PIN | RGMII Receive Data [3:0] |
| EMAC[0]_MCRS/ **EMAC[0]_RGRXD[2]**/ EMAC[0]_RMRXD[1]/ GP3[25] | R25 | I | IPD DVDD_GPMC | EMAC[0], GP3 PINCNTL237 DSIS: PIN | |
| EMAC[0]_MRXD[2]/ **EMAC[0]_RGRXD[1]**/ EMAC[0]_RMTXEN/ GP3[30] | R23 | I | IPD DVDD_GPMC | EMAC[0], GP3 PINCNTL242 DSIS: PIN | |
| EMAC[0]_MRXD[1]/ **EMAC[0]_RGRXD[0]**/ EMAC[0]_RMTXD[1]/ GP3[29] | P23 | I | IPD DVDD_GPMC | EMAC[0], GP3 PINCNTL241 DSIS: PIN | |
| EMAC[0]_MRCLK/ **EMAC[0]_RGTXC**/ EMAC[0]_RMCRSDV/ SPI[3]_SCS[2]/ GP3[27] | H27 | O | IPD DVDD_GPMC | EMAC[0], SPI[3], GP3 PINCNTL239 DSIS: N/A | RGMII Transmit Clock |

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**Table 4-8. EMAC[0] Terminal Functions [(R)(G)MII] (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| EMAC[0]_MRXER/ **EMAC[0]_RGTXCTL**/ EMAC[0]_RMRXER/ GP3[26] | J26 | O | IPD DVDD_GPMC | EMAC[0], GP3 PINCNTL238 DSIS: N/A | RGMII Transmit Enable |
| EMAC[0]_MRXD[5]/ **EMAC[0]_RGTXD[3]**/ GPMC_A[2]/ UART5_CTS | H26 | O | IPD DVDD_GPMC | EMAC[0], GPMC, UART5 PINCNTL245 DSIS: N/A | RGMII Transmit Data [3:0] |
| EMAC[0]_MRXD[6]/ **EMAC[0]_RGTXD[2]**/ GPMC_A[3]/ UART5_RTS | F28 | O | IPD DVDD_GPMC | EMAC[0], GPMC, UART5 PINCNTL246 DSIS: N/A | |
| EMAC[0]_MRXD[7]/ **EMAC[0]_RGTXD[1]**/ GPMC_A[4]/ SPI[2]_SCS[3] | G27 | O | IPD DVDD_GPMC | EMAC[0], GPMC, SPI[2] PINCNTL247 DSIS: N/A | |
| EMAC[0]_MRXD[0]/ **EMAC[0]_RGTXD[0]**/ EMAC[0]_RMTXD[0]/ GP3[28] | G28 | O | IPD DVDD_GPMC | EMAC[0], GP3 PINCNTL240 DSIS: N/A | |


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## Table 4-9. EMAC[1] Terminal Functions [(R)(G)MII]

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **EMAC[1] (G)MII Mode** | | | | | |
| An EMAC bootmode must be selected via the BTMODE[4:0] pins. Once the EMAC bootmode is selected, the BTMODE[9:8] pins determine the Ethernet PHY Mode Selection (for example, 00b is MII mode). For more detailed information on EMAC bootmodes and Ethernet PHY Mode selection, see Section 5.2.6, *Ethernet PHY Mode Selection*.<br>These pin functions are available *only* when GMII and MII modes are selected. | | | | | |
| VOUT[1]_HSYNC/ **EMAC[1]_MCOL**/ SPI[3]_D[1]/ UART3_RTS/ GP2[29] | AC24 | I | IPD DVDD | VOUT[1], SPI[3], UART3, GP2 PINCNTL205 DSIS: 0 | [G]MII Collision Detect (Sense) input |
| VOUT[1]_VSYNC/ **EMAC[1]_MCRS**/ SPI[3]_D[0]/ UART3_CTS/ GP2[30] | AA23 | I | IPD DVDD | VOUT[1], SPI[3], UART3, GP2 PINCNTL206 DSIS: 0 | [G]MII Carrier Sense input |
| VOUT[1]_G_Y_YC[6]/ **EMAC[1]_GMTCLK**/ GP3[10] | AH27 | O | IPD DVDD | VOUT[1], GP3 PINCNTL218 DSIS: N/A | GMII Source Synchronous Transmit Clock |
| VOUT[1]_B_CB_C[3]/ **EMAC[1]_MRCLK**/ UART4_CTS/ GP3[0] | AH25 | I | IPD DVDD | VOUT[1], UART4, GP3 PINCNTL208 DSIS: 0 | [G]MII Receive Clock |
| VOUT[1]_G_Y_YC[4]/ **EMAC[1]_MRXD[7]**/ GP3[8] | W22 | I | IPD DVDD | VOUT[1], GP3 PINCNTL216 DSIS: PIN | [G]MII Receive Data [7:0]. For 1000 EMAC GMII operation, EMAC[0]_RXD[7:0] are used. For 10/100 EMAC MII operation, *only* EMAC[0]_RXD[3:0] are used. |
| VOUT[1]_G_Y_YC[3]/ **EMAC[1]_MRXD[6]**/ GP3[7] | Y23 | | | VOUT[1], GP3 PINCNTL215 DSIS: PIN | |
| VOUT[1]_B_CB_C[9]/ **EMAC[1]_MRXD[5]**/ I2C[3]_SDA/ GP3[6] | AA24 | | | VOUT[1], I2C[3], GP3 PINCNTL214 DSIS: PIN | |
| VOUT[1]_B_CB_C[8]/ **EMAC[1]_MRXD[4]**/ I2C[3]_SCL/ GP3[5] | AH26 | | | VOUT[1], I2C[3], GP3 PINCNTL213 DSIS: PIN | |
| VOUT[1]_B_CB_C[7]/ **EMAC[1]_MRXD[3]**/ UART3_TXD/ GP3[4] | AC25 | | | VOUT[1], UART3, GP3 PINCNTL212 DSIS: PIN | |
| VOUT[1]_B_CB_C[6]/ **EMAC[1]_MRXD[2]**/ UART3_RXD/ GP3[3] | AD25 | | | VOUT[1], UART3, GP3 PINCNTL211 DSIS: PIN | |
| VOUT[1]_B_CB_C[5]/ **EMAC[1]_MRXD[1]**/ UART4_TXD/ GP3[2] | AF25 | | | VOUT[1], UART4, GP3 PINCNTL210 DSIS: PIN | |
| VOUT[1]_B_CB_C[4]/ **EMAC[1]_MRXD[0]**/ UART4_RXD/ GP3[1] | AG25 | | | VOUT[1], UART4, GP3 PINCNTL209 DSIS: PIN | |
| VOUT[1]_G_Y_YC[5]/ **EMAC[1]_MRXDV**/ GP3[9] | AG26 | I | IPD DVDD | VOUT[1], GP3 PINCNTL217 DSIS: 0 | [G]MII Receive Data Valid input |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and the Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal

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**Table 4-9. EMAC[1] Terminal Functions [(R)(G)MII] (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| VOUT[1]_AVID/ **EMAC[1]_MRXER**/ UART4_RTS/ TIM6_IO/ GP2[31] | Y22 | I | IPD DVDD | VOUT[1], UART4, TIMER 6, GP2 PINCNTL207 DSIS: 0 | [G]MII Receive Data Error input |
| VOUT[1]_CLK/ **EMAC[1]_MTCLK**/ GP2[28] | AE24 | I | IPD DVDD | VOUT[1], GP2 PINCNTL204 DSIS: 0 | [G]MII Transmit Clock input |
| VOUT[1]_R_CR[8]/ **EMAC[1]_MTXD[7]**/ UART5_RXD/ GP3[18] | W23 | O | IPD DVDD | VOUT[1], UART5, GP3 PINCNTL226 DSIS: N/A | [G]MII Transmit Data [7:0]. For 1000 EMAC GMII operation, EMAC[0]_TXD[7:0] are used. For 10/100 EMAC MII operation, *only* EMAC[0]_TXD[3:0] are used. |
| VOUT[1]_R_CR[7]/ **EMAC[1]_MTXD[6]**/ SPI[3]_D[0]/ GP3[17] | V22 | | | VOUT[1], SPI[3], GP3 PINCNTL225 DSIS: N/A | |
| VOUT[1]_R_CR[6]/ **EMAC[1]_MTXD[5]**/ SPI[3]_D[1]/ GP3[16] | AA25 | | | VOUT[1], SPI[3], GP3 PINCNTL224 DSIS: N/A | |
| VOUT[1]_R_CR[5]/ **EMAC[1]_MTXD[4]**/ SPI[3]_SCLK/ GP3[15] | AC26 | | | VOUT[1], SPI[3], GP3 PINCNTL223 DSIS: N/A | |
| VOUT[1]_R_CR[4]/ **EMAC[1]_MTXD[3]**/ SPI[3]_SCS[1]/ GP3[14] | AG27 | | | VOUT[1], SPI[3], GP3 PINCNTL222 DSIS: N/A | |
| VOUT[1]_G_Y_YC[9]/ **EMAC[1]_MTXD[2]**/ GP3[13] | AD26 | | | VOUT[1], GP3 PINCNTL221 DSIS: N/A | |
| VOUT[1]_G_Y_YC[8]/ **EMAC[1]_MTXD[1]**/ GP3[12] | AE26 | | | VOUT[1], GP3 PINCNTL220 DSIS: N/A | |
| VOUT[1]_G_Y_YC[7]/ **EMAC[1]_MTXD[0]**/ GP3[11] | AF26 | | | VOUT[1], GP3 PINCNTL219 DSIS: N/A | |
| VOUT[1]_R_CR[9]/ **EMAC[1]_MTXEN**/ UART5_TXD/ GP3[19] | Y24 | O | IPD DVDD | VOUT[1], UART5, GP3 PINCNTL227 DSIS: N/A | [G]MII Transmit Data Enable output |
| **EMAC[1] RMII Mode** | | | | | |
| An EMAC bootmode must be selected via the BTMODE[4:0] pins. Once the EMAC bootmode is selected, the BTMODE[9:8] pins determine the Ethernet PHY Mode Selection (for example, 01b is RMII mode). For more detailed information on EMAC bootmodes and Ethernet PHY Mode selection, see Section 5.2.6, *Ethernet PHY Mode Selection*. These pin functions are available *only* when RMII mode is selected. | | | | | |
| **EMAC_RMREFCLK**/ TIM2_IO/ GP1[10] | J27 | I/O | IPD DVDD_GPMC | TIMER2, GP1 PINCNTL232 DSIS: PIN | RMII Reference Clock (EMAC[0] and EMAC[1] RMII mode) |
| VIN[0]A_D[20]/ CAM_D[12]/ **EMAC[1]_RMCRSDV**/ SPI[3]_SCS[0]/ GP0[14] | AC17 | I | IPD DVDD_C | VIN[0]A, CAMERA_I/F, SPI[3], GP0 PINCNTL160 DSIS: 0 MM: MUX1 | RMII Carrier Sense input |
| EMAC[0]_MTXD[5]/ EMAC[1]_RGTXC/ **EMAC[1]_RMCRSDV**/ GPMC_A[12]/ UART1_RXD | F27 | I | IPD DVDD_GPMC | EMAC[0], EMAC[1], GPMC, UART1 PINCNTL255 DSIS: 0 MM: MUX0 | |


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**Table 4-9. EMAC[1] Terminal Functions [(R)(G)MII] (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| VIN[0]A_D[18]/ CAM_D[10]/ **EMAC[1]_RMRXD[1]**/ I2C[3]_SCL/ GP0[12] | AF20 | I | IPU DVDD_C | VIN[0]A, CAMERA_I/F, I2C[3], GP0 PINCNTL158 DSIS: PIN MM: MUX1 | RMII Receive Data [1:0]. |
| EMAC[0]_MTXD[3]/ EMAC[1]_RGTXD[0]/ **EMAC[1]_RMRXD[1]**/ GPMC_A[10]/ UART4_CTS | H23 | I | IPD DVDD_GPMC | EMAC[0], EMAC[1], GPMC, UART4 PINCNTL253 DSIS: PIN MM: MUX0 | |
| VIN[0]A_D[19]/ CAM_D[11]/ **EMAC[1]_RMRXD[0]**/ I2C[3]_SDA/ GP0[13] | AF21 | I | IPU DVDD_C | VIN[0]A, CAMERA_I/F, I2C[3], GP0 PINCNTL159 DSIS: PIN MM: MUX1 | |
| EMAC[0]_MTXD[2]/ EMAC[1]_RGTXCTL/ **EMAC[1]_RMRXD[0]**/ GPMC_A[9]/ UART4_TXD | H22 | I | IPD DVDD_GPMC | EMAC[0], EMAC[1], GPMC, UART4 PINCNTL252 DSIS: PIN MM: MUX0 | |
| VIN[0]A_D[17]/ CAM_D[9]/ **EMAC[1]_RMRXER**/ GP0[11] | AB21 | I | IPD DVDD_C | VIN[0]A, CAMERA_I/F, SPI[3], GP0 PINCNTL157 DSIS: 0 MM: MUX1 | RMII Receive Data Error input |
| EMAC[0]_MTXD[4]/ EMAC[1]_RGTXD[2]/ **EMAC[1]_RMRXER**/ GPMC_A[11]/ UART4_RTS | G23 | I | IPD DVDD_GPMC | EMAC[0], EMAC[1], GPMC, UART1 PINCNTL254 DSIS: 0 MM: MUX0 | |
| VIN[0]A_D[22]/ CAM_D[14]/ **EMAC[1]_RMTXD[1]**/ SPI[3]_D[1]/ GP0[16] | AC21 | O | IPD DVDD_C | VIN[0]A, CAMERA_I/F, SPI[3], GP0 PINCNTL162 DSIS: N/A MM: MUX1 | RMII Transmit Data [1:0]. |
| EMAC[0]_MTXD[7]/ EMAC[1]_RGTXD[3]/ **EMAC[1]_RMTXD[1]**/ GPMC_A[14]/ UART1_CTS | H24 | O | IPD DVDD_GPMC | EMAC[0], GPMC, UART1 PINCNTL257 DSIS: N/A MM: MUX0 | |
| VIN[0]A_D[21]/ CAM_D[13]/ **EMAC[1]_RMTXD[0]**/ SPI[3]_SCLK/ GP0[15] | AE18 | O | IPD DVDD_C | VIN[0]A CAMERA_I/F, SPI[3], GP0 PINCNTL161 DSIS: N/A MM: MUX1 | |
| EMAC[0]_MTXD[6]/ EMAC[1]_RGRXD[0]/ **EMAC[1]_RMTXD[0]**/ GPMC_A[13]/ UART1_TXD | J22 | O | IPD DVDD_GPMC | EMAC[0], EMAC[1], GPMC, UART1 PINCNTL256 DSIS: N/A MM: MUX0 | |

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**Table 4-9. EMAC[1] Terminal Functions [(R)(G)MII] (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| VIN[0]A_D[23]/ CAM_D[15]/ **EMAC[1]_RMTXEN**/ SPI[3]_D[0]/ GP0[17] | AC16 | O | IPD DVDD_C | VIN[0]A, CAMERA_I/F, SPI[3], GP0 PINCNTL163 DSIS: N/A MM: MUX1 | RMII Transmit Data Enable output |
| EMAC[0]_MTXEN/ EMAC[1]_RGRXD[2]/ **EMAC[1]_RMTXEN**/ GPMC_A[15]/ UART1_RTS | J23 | O | IPD DVDD_GPMC | EMAC[0], EMAC[1], GPMC, UART1 PINCNTL258 DSIS: N/A MM: MUX0 | |
| **EMAC[1] RGMII MODE** | | | | | |
| An EMAC bootmode must be selected via the BTMODE[4:0] pins. Once the EMAC bootmode is selected, the BTMODE[9:8] pins determine the Ethernet PHY Mode Selection (for example, 10b is RGMII mode). For more detailed information on EMAC bootmodes and Ethernet PHY Mode selection, see Section 5.2.6, *Ethernet PHY Mode Selection*<br>These pin functions are available *only* when RGMII mode is selected. | | | | | |
| EMAC[0]_GMTCLK/ **EMAC[1]_RGRXC**/ GPMC_A[6]/ SPI[2]_D[1] | K23 | I | IPD DVDD_GPMC | EMAC[0], GPMC, SPI[2] PINCNTL249 DSIS: PIN | RGMII Receive Clock |
| EMAC[0]_MRXD[3]/ **EMAC[1]_RGRXCTL**/ GPMC_A[27]/ GPMC_A[26]/ GPMC_A[0]/ UART5_RXD | J25 | I | IPD DVDD_GPMC | EMAC[0], GPMC, UART5 PINCNTL243 DSIS: PIN | RGMII Receive Control |
| EMAC[0]_MTXD[0]/ **EMAC[1]_RGRXD[3]**/ GPMC_A[7]/ SPI[2]_D[0] | J24 | I | IPD DVDD_GPMC | EMAC[0], GPMC, UART4 PINCNTL250 DSIS: PIN | RGMII Receive Data [3:0] |
| EMAC[0]_MTXEN/ **EMAC[1]_RGRXD[2]**/ EMAC[1]_RMTXEN/ GPMC_A[15]/ UART1_RTS | J23 | I | IPD DVDD_GPMC | EMAC[0], GPMC, UART4 PINCNTL258 DSIS: PIN | |
| EMAC[0]_MRXDV/ **EMAC[1]_RGRXD[1]**/ GPMC_A[5]/ SPI[2]_SCLK | K22 | I | IPD DVDD_GPMC | EMAC[0], GPMC, SPI[2] PINCNTL248 DSIS: PIN | |
| EMAC[0]_MTXD[6]/ **EMAC[1]_RGRXD[0]**/ EMAC[1]_RMTXD[0]/ GPMC_A[13]/ UART1_TXD | J22 | I | IPD DVDD_GPMC | EMAC[0], GPMC, UART1 PINCNTL256 DSIS: PIN | |
| EMAC[0]_MTXD[5]/ **EMAC[1]_RGTXC**/ EMAC[1]_RMCRSDV/ GPMC_A[12]/ UART1_RXD | F27 | O | IPD DVDD_GPMC | EMAC[0], GPMC, UART1 PINCNTL255 DSIS: N/A | RGMII Transmit Clock |
| EMAC[0]_MTXD[2]/ **EMAC[1]_RGTXCTL**/ EMAC[1]_RMRXD[0]/ GPMC_A[9]/ UART4_TXD | H22 | O | IPD DVDD_GPMC | EMAC[0], GPMC, UART4 PINCNTL252 DSIS: N/A | RGMII Transmit Enable |


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**Table 4-9. EMAC[1] Terminal Functions [(R)(G)MII] (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| EMAC[0]_MTXD[7]/ **EMAC[1]_RGTXD[3]**/ EMAC[1]_RMTXD[1]/ GPMC_A[14]/ UART1_CTS | H24 | O | IPD DVDD_GPMC | EMAC[0], GPMC, UART1 PINCNTL257 DSIS: N/A | RGMII Transmit Data [3:0] |
| EMAC[0]_MTXD[4]/ **EMAC[1]_RGTXD[2]**/ EMAC[1]_RMRXER/ GPMC_A[11]/ UART4_RTS | G23 | O | IPD DVDD_GPMC | EMAC[0], GPMC, UART4 PINCNTL254 DSIS: N/A | |
| EMAC[0]_MTXD[1]/ **EMAC[1]_RGTXD[1]**/ GPMC_A[8]/ UART4_RXD | H25 | O | IPD DVDD_GPMC | EMAC[0], GPMC, UART4 PINCNTL251 DSIS: N/A | |
| EMAC[0]_MTXD[3]/ **EMAC[1]_RGTXD[0]**/ EMAC[1]_RMRXD[1]/ GPMC_A[10]/ UART4_CTS | H23 | O | IPD DVDD_GPMC | EMAC[0], EMAC[1], GPMC, UART4 PINCNTL253 DSIS: N/A | |

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**Table 4-10. MDIO Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **MDIO** | | | | | |
| **MDCLK**/ GP1[11] | H28 | O | IPU DVDD_GPMC | GP1 PINCNTL233 DSIS: N/A | Management Data Serial Clock output |
| **MDIO**/ GP1[12] | P24 | I/O | IPU DVDD_GPMC | GP1 PINCNTL234 DSIS: 1 | Management Data I/O |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal


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### 4.2.8 General-Purpose Input/Outputs (GPIOs)

**Table 4-11. GP0 Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **GPIO0** | | | | | |
| **Note:** General-Purpose Input/Output (I/O) pins can also serve as external interrupt inputs. | | | | | |
| UART2_TXD/ **GP0[31]** | U3 | I/O | IPD DVDD | UART2 PINCNTL61 DSIS: PIN | General-Purpose Input/Output (I/O) 0 [GP0] pin 31 |
| TCLKIN/ **GP0[30]** | T2 | I/O | IPD DVDD | TCLKIN PINCNTL60 DSIS: PIN | General-Purpose Input/Output (I/O) 0 [GP0] pin 30 |
| UART2_RXD/ **GP0[29]** | U4 | I/O | IPD DVDD | UART2 PINCNTL59 DSIS: PIN | General-Purpose Input/Output (I/O) 0 [GP0] pin 29 |
| MCA[5]_AXR[1]/ MCA[4]_AXR[3]/ TIM7_IO/ **GP0[28]** | L6 | I/O | IPD DVDD | MCA[5], MCA[4], TIMER7 PINCNTL58 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 0 [GP0] pin 28 |
| VOUT[1]_FLD/ CAM_FLD/ CAM_WE/ GPMC_A[11]/ UART2_CTS/ **GP0[28]** | AB23 | I/O | IPD DVDD_C | VOUT[1], CAMERA_I/F, GPMC, UART2 PINCNTL174 DSIS: PIN MM: MUX0 | |
| MCA[5]_AXR[0]/ MCA[4]_AXR[2]/ **GP0[27]** | L7 | I/O | IPD DVDD | MCA[5], MCA[4] PINCNTL57 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 0 [GP0] pin 27 |
| VOUT[1]_B_CB_C[0]/ CAM_VS/ GPMC_A[10]/ UART2_TXD/ **GP0[27]** | AD23 | I/O | IPU DVDD_C | VOUT[1], CAMERA_I/F, GPMC, UART2 PINCNTL173 DSIS: PIN MM: MUX0 | |
| MCA[5]_AFSX/ **GP0[26]** | H5 | I/O | IPD DVDD | MCA[5] PINCNTL56 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 0 [GP0] pin 26 |
| VOUT[1]_B_CB_C[1]/ CAM_HS/ GPMC_A[9]/ UART2_RXD/ **GP0[26]** | AE23 | I/O | IPD DVDD_C | VOUT[1], CAMERA_I/F, GPMC, UART2 PINCNTL172 DSIS: PIN MM: MUX0 | |
| MCA[5]_ACLKX/ **GP0[25]** | J3 | I/O | IPD DVDD | MCA[5] PINCNTL55 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 0 [GP0] pin 25 |
| VOUT[1]_R_CR[0]/ CAM_D[0]/ GPMC_A[8]/ UART4_RTS/ **GP0[25]** | AA22 | I/O | IPD DVDD_C | VOUT[1], CAMERA_I/F, GPMC, UART4 PINCNTL171 DSIS: PIN MM: MUX0 | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal

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**Table 4-11. GP0 Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| MCA[4]_AXR[1]/ TIM6_IO/ **GP0[24]** | J4 | I/O | IPD DVDD | MCA[4], TIMER6 PINCNTL54 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 0 [GP0] pin 24 |
| VOUT[1]_R_CR[1]/ CAM_D[1]/ GPMC_A[7]/ UART4_CTS/ **GP0[24]** | AC19 | I/O | IPD DVDD_C | VOUT[1], CAMERA_I/F, GPMC, UART4 PINCNTL170 DSIS: PIN MM: MUX0 | |
| MCA[4]_AXR[0]/ **GP0[23]** | H6 | I/O | IPD DVDD | MCA[4] PINCNTL53 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 0 [GP0] pin 23 |
| VOUT[1]_G_Y_YC[0]/ CAM_D[2]/ GPMC_A[6]/ UART4_TXD/ **GP0[23]** | AC18 | I/O | IPD DVDD_C | VOUT[1], CAMERA_I/F, GPMC, UART4 PINCNTL169 DSIS: PIN MM: MUX0 | |
| MCA[4]_AFSX/ **GP0[22]** | H3 | I/O | IPD DVDD | MCA[4] PINCNTL52 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 0 [GP0] pin 22 |
| VOUT[1]_G_Y_YC[1]/ CAM_D[3]/ GPMC_A[5]/ UART4_RXD/ **GP0[22]** | AD18 | I/O | IPU DVDD_C | VOUT[1], CAMERA_I/F, GPMC, UART4 PINCNTL168 DSIS: PIN MM: MUX0 | |
| MCA[4]_ACLKX/ **GP0[21]** | K7 | I/O | IPD DVDD | MCA[4] PINCNTL51 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 0 [GP0] pin 21 |
| VIN[0]B_FLD/ CAM_D[4]/ **GP0[21]** | AD17 | I/O | IPU DVDD_C | VIN[0]B, CAMERA_I/F PINCNTL167 DSIS: PIN MM: MUX0 | |
| MCA[3]_AXR[2]/ MCA[1]_AXR[8]/ **GP0[20]** | F2 | I/O | IPD DVDD | MCA[3], MCA[1] PINCNTL49 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 0 [GP0] pin 20 |
| VIN[0]A_FLD/ CAM_D[5]/ **GP0[20]** | AC22 | I/O | IPU DVDD_C | VIN[0]A, CAMERA_I/F PINCNTL166 DSIS: PIN MM: MUX0 | |
| MCA[3]_AXR[1]/ TIM5_IO/ **GP0[19]** | G2 | I/O | IPD DVDD | MCA[3], TIMER5 PINCNTL48 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 0 [GP0] pin 19 |
| VIN[0]B_DE/ CAM_D[6]/ **GP0[19]** | AC15 | I/O | IPU DVDD_C | VIN[0]B, CAMERA_I/F PINCNTL165 DSIS: PIN MM: MUX0 | |


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**Table 4-11. GP0 Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| MCA[3]_AXR[0]/ TIM4_IO/ **GP0[18]** | G1 | I/O | IPD DVDD | MCA[3], TIMER4 PINCNTL47 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 0 [GP0] pin 18 |
| VIN[0]A_DE/ CAM_D[7]/ **GP0[18]** | AB17 | I/O | IPU DVDD_C | VIN[0]A, CAMERA_I/F PINCNTL164 DSIS: PIN MM: MUX0 | |
| MCA[3]_AFSX/ **GP0[17]** | H4 | I/O | IPD DVDD | MCA[3] PINCNTL46 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 0 [GP0] pin 17 |
| VIN[0]A_D[23]/ CAM_D[15]/ EMAC[1]_RMTXEN/ SPI[3]_D[0]/ **GP0[17]** | AC16 | I/O | IPD DVDD_C | VIN[0]A, CAMERA_I/F, EMAC[1]_RM, SPI[3] PINCNTL163 DSIS: PIN MM: MUX0 | |
| MCA[3]_ACLKX/ **GP0[16]** | G6 | I/O | IPD DVDD | MCA[3] PINCNTL45 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 0 [GP0] pin 16 |
| VIN[0]A_D[22]/ CAM_D[14]/ EMAC[1]_RMTXD[1]/ SPI[3]_D[1]/ **GP0[16]** | AC21 | I/O | IPD DVDD_C | VIN[0]A, CAMERA_I/F, EMAC[1]_RM, SPI[3] PINCNTL162 DSIS: PIN MM: MUX0 | |
| MCA[2]_AXR[3]/ MCA[1]_AXR[7]/ TIM3_IO/ **GP0[15]** | H2 | I/O | IPD DVDD | MCA[2], MCA[1], TIMER3 PINCNTL44 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 0 [GP0] pin 15 |
| VIN[0]A_D[21]/ CAM_D[13]/ EMAC[1]_RMTXD[0]/ SPI[3]_SCLK/ **GP0[15]** | AE18 | I/O | IPD DVDD_C | VIN[0]A, CAMERA_I/F, EMAC[1]_RM, SPI[3] PINCNTL161 DSIS: PIN MM: MUX0 | |
| MCA[2]_AXR[2]/ MCA[1]_AXR[6]/ TIM2_IO/ **GP0[14]** | V5 | I/O | IPD DVDD | MCA[2], MCA[1], TIMER2 PINCNTL43 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 0 [GP0] pin 14 |
| VIN[0]A_D[20]/ CAM_D[12]/ EMAC[1]_RMCRSDV/ SPI[3]_SCS[0]/ **GP0[14]** | AC17 | I/O | IPD DVDD_C | VIN[0]A, CAMERA_I/F, EMAC[1]_RM, SPI[3] PINCNTL160 DSIS: PIN MM: MUX0 | |

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**Table 4-11. GP0 Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE[1] | OTHER[2] [3] | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| MCA[2]_AXR[1]/ SD0_DAT[7]/ UART5_TXD/ **GP0[13]** | V6 | I/O | IPU DVDD | MCA[2], SD0, UART5 PINCNTL42 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 0 [GP0] pin 13 |
| VIN[0]A_D[19]/ CAM_D[11]/ EMAC[1]_RMRXD[0]/ I2C[3]_SDA/ **GP0[13]** | AF21 | I/O | IPU DVDD_C | VIN[0]A, CAMERA_I/F, EMAC[1]_RM, I2C[3] PINCNTL159 DSIS: PIN MM: MUX0 | |
| MCA[2]_AXR[0]/ SD0_DAT[6]/ UART5_RXD/ **GP0[12]** | N2 | I/O | IPU DVDD | MCA[2], SD0, UART5 PINCNTL41 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 0 [GP0] pin 12 |
| VIN[0]A_D[18]/ CAM_D[10]/ EMAC[1]_RMRXD[1]/ I2C[3]_SCL/ **GP0[12]** | AF20 | I/O | IPU DVDD_C | VIN[0]A, CAMERA_I/F, EMAC[1]_RM, I2C[3] PINCNTL158 DSIS: PIN MM: MUX0 | |
| MCA[2]_AFSX/ **GP0[11]** | AA5 | I/O | IPU DVDD | MCA[2] PINCNTL40 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 0 [GP0] pin 11 |
| VIN[0]A_D[17]/ CAM_D[9]/ EMAC[1]_RMRXER/ **GP0[11]** | AB21 | I/O | IPD DVDD_C | VIN[0]A, CAMERA_I/F, EMAC[1]_RM PINCNTL157 DSIS: PIN MM: MUX0 | |
| MCA[2]_ACLKX/ **GP0[10]** | U6 | I/O | IPU DVDD | MCA[2] PINCNTL39 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 0 [GP0] pin 10 |
| VIN[0]A_D[16]/ CAM_D[8]/ I2C[2]_SCL/ **GP0[10]** | AA21 | I/O | IPU DVDD_C | VIN[0]A, CAMERA_I/F, I2C[2] PINCNTL156 DSIS: PIN MM: MUX0 | |
| AUD_CLKIN2/ MCA[0]_AXR[9]/ MCA[2]_AHCLKX/ MCA[5]_AHCLKX/ EDMA_EVT2/ TIM3_IO/ **GP0[9]** | H1 | I/O | IPD DVDD | AUD_CLKIN2, MCA[0], MCA[2], MCA[5], EDMA, TIMER3 PINCNTL16 DSIS: PIN | General-Purpose Input/Output (I/O) 0 [GP0] pin 9 |
| AUD_CLKIN1/ MCA[0]_AXR[8]/ MCA[1]_AHCLKX/ MCA[4]_AHCLKX/ EDMA_EVT3/ TIM2_IO/ **GP0[8]** | R5 | I/O | IPD DVDD | AUD_CLKIN1, MCA[0], MCA[1], MCA[4], EDMA, TIMER2 PINCNTL15 DSIS: PIN | General-Purpose Input/Output (I/O) 0 [GP0] pin 8 |
| USB0_DRVVBUS/ **GP0[7]** | AF11 | I/O | IPD DVDD | USB0 PINCNTL270 DSIS: PIN | General-Purpose Input/Output (I/O) 0 [GP0] pin 7 |


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**Table 4-11. GP0 Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| SD0_DAT[3]/<br>SD1_DAT[7]/<br>**GP0[6]** | Y4 | I/O | IPU<br>DVDD_SD | SD0, SD1<br>PINCNTL13<br>DSIS: PIN | General-Purpose Input/Output (I/O) 0 [GP0] pin 6 |
| SD0_DAT[2]_SDR$\overline{W}$/<br>SD1_DAT[6]/<br>**GP0[5]** | Y3 | I/O | IPU<br>DVDD_SD | SD0, SD1<br>PINCNTL12<br>DSIS: PIN | General-Purpose Input/Output (I/O) 0 [GP0] pin 5 |
| SD0_DAT[1]_$\overline{SDIRQ}$/<br>SD1_DAT[5]/<br>**GP0[4]** | Y5 | I/O | IPU<br>DVDD_SD | SD0, SD1<br>PINCNTL11<br>DSIS: PIN | General-Purpose Input/Output (I/O) 0 [GP0] pin 4 |
| SD0_DAT[0]/<br>SD1_DAT[4]/<br>**GP0[3]** | R7 | I/O | IPU<br>DVDD_SD | SD0, SD1<br>PINCNTL10<br>DSIS: PIN | General-Purpose Input/Output (I/O) 0 [GP0] pin 3 |
| SD0_CMD/<br>SD1_CMD/<br>**GP0[2]** | N1 | I/O | IPU<br>DVDD_SD | SD0, SD1<br>PINCNTL9<br>DSIS: PIN | General-Purpose Input/Output (I/O) 0 [GP0] pin 2 |
| SD0_CLK/<br>**GP0[1]** | Y6 | I/O | IPU<br>DVDD_SD | SD0<br>PINCNTL8<br>DSIS: PIN | General-Purpose Input/Output (I/O) 0 [GP0] pin 1 |
| SD1_CMD/<br>**GP0[0]** | P2 | I/O | IPU<br>DVDD_SD | SD1<br>PINCNTL2<br>DSIS: PIN | General-Purpose Input/Output (I/O) 0 [GP0] pin 0 |

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## Table 4-12. GP1 Terminal Functions

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **GPIO1** | | | | | |
| **Note:** General-Purpose Input/Output (I/O) pins can also serve as external interrupt inputs. | | | | | |
| GPMC_WAIT[0]/ GPMC_A[26]/ EDMA_EVT0/ **GP1[31]** | W28 | I/O | IPU DVDD_GP MC | GPMC, EDMA PINCNTL133 DSIS: PIN | General-Purpose Input/Output (I/O) 1 [GP1] pin 31 |
| GPMC_$\overline{BE[1]}$/ GPMC_A[24]/ EDMA_EVT1/ TIM7_IO/ **GP1[30]** | V28 | I/O | IPD DVDD_GP MC | GPMC, EDMA, TIMER7 PINCNTL132 DSIS: PIN | General-Purpose Input/Output (I/O) 1 [GP1] pin 30 |
| GPMC_$\overline{BE[0]}$_CLE/ GPMC_A[25]/ EDMA_EVT2/ TIM6_IO/ **GP1[29]** | U27 | I/O | IPD DVDD_GP MC | GPMC, EDMA, TIMER6 PINCNTL131 DSIS: PIN | General-Purpose Input/Output (I/O) 1 [GP1] pin 29 |
| GPMC_$\overline{ADV}$_ALE/ GPMC_CS[6]/ TIM5_IO/ **GP1[28]** | M26 | I/O | IPU DVDD_GP MC | GPMC, TIMER5 PINCNTL128 DSIS: PIN | General-Purpose Input/Output (I/O) 1 [GP1] pin 28 |
| GPMC_CLK/ GPMC_CS[5]/ GPMC_WAIT[1]/ CLKOUT1/ EDMA_EVT3/ TIM4_IO/ **GP1[27]** | R26 | I/O | IPU DVDD_GP MC | GPMC, CLKOUT1, EDMA, TIMER4 PINCNTL127 DSIS: PIN | General-Purpose Input/Output (I/O) 1 [GP1] pin 27 |
| SPI[1]_D[0]/ **GP1[26]** | AA6 | I/O | IPU DVDD | SPI[1] PINCNTL88 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 1 [GP1] pin 26 |
| $\overline{GPMC_CS[3]}$/ SPI[2]_SCS[0]/ **GP1[26]** | P26 | I/O | IPU DVDD_GP MC | GPMC, SPI[2] PINCNTL125 DSIS: PIN MM: MUX0 | |
| $\overline{GPMC_CS[2]}$/ GPMC_A[24]/ **GP1[25]** | M25 | I/O | IPU DVDD_GP MC | GPMC PINCNTL124 DSIS: PIN | General-Purpose Input/Output (I/O) 1 [GP1] pin 25 |
| $\overline{GPMC_CS[1]}$/ GPMC_A[25]/ **GP1[24]** | K28 | I/O | IPU DVDD_GP MC | GPMC PINCNTL123 DSIS: PIN | General-Purpose Input/Output (I/O) 1 [GP1] pin 24 |
| $\overline{GPMC_CS[0]}$/ **GP1[23]** | T28 | I/O | IPU DVDD_GP MC | GPMC PINCNTL122 DSIS: PIN | General-Purpose Input/Output (I/O) 1 [GP1] pin 23 |
| SD2_DAT[4]/ GPMC_A[27]/ GPMC_A[23]/ $\overline{GPMC_CS[7]}$/ EDMA_EVT0/ TIM7_IO/ **GP1[22]** | R24 | I/O | IPU DVDD_GP MC | SD2, GPMC, EDMA, TIMER7 PINCNTL116 DSIS: PIN | General-Purpose Input/Output (I/O) 1 [GP1] pin 22 |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal


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**Table 4-12. GP1 Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| SD2_DAT[5]/ GPMC_A[26]/ GPMC_A[22]/ TIM6_IO/ **GP1[21]** | P22 | I/O | IPU DVDD_GP MC | SD2, GPMC, TIMER6 PINCNTL115 DSIS: PIN | General-Purpose Input/Output (I/O) 1 [GP1] pin 21 |
| SD2_DAT[6]/ GPMC_A[25]/ GPMC_A[21]/ UART2_TXD/ **GP1[20]** | N23 | I/O | IPU DVDD_GP MC | SD2, GPMC, UART2 PINCNTL114 DSIS: PIN | General-Purpose Input/Output (I/O) 1 [GP1] pin 20 |
| SD2_DAT[7]/ GPMC_A[24]/ GPMC_A[20]/ UART2_RXD/ **GP1[19]** | L25 | I/O | IPU DVDD_GP MC | SD2, GPMC, UART2 PINCNTL113 DSIS: PIN | General-Purpose Input/Output (I/O) 1 [GP1] pin 19 |
| SPI[1]_D[1]/ **GP1[18]** | AA3 | I/O | IPU DVDD | SPI[1] PINCNTL87 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 1 [GP1] pin 18 |
| GPMC_A[23]/ SPI[2]_SCLK/ HDMI_HPDET/ TIM5_IO/ **GP1[18]** | AA26 | I/O | IPD DVDD_GP MC | GPMC, SPI[2], HDMI, TIMER5 PINCNTL112 DSIS: PIN MM: MUX0 | |
| SPI[1]_SCLK/ **GP1[17]** | AC3 | I/O | IPU DVDD | SPI[1] PINCNTL86 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 1 [GP1] pin 17 |
| GPMC_A[22]/ SPI[2]_D[1]/ HDMI_CEC/ TIM4_IO/ **GP1[17]** | AB27 | I/O | IPU DVDD_GP MC | GPMC, SPI[2], HDMI, TIMER4 PINCNTL111 DSIS: PIN MM: MUX0 | |
| $\overline{\text{SPI[1]_SCS[0]}}$/ **GP1[16]** | AD3 | I/O | IPU DVDD | SPI[1] PINCNTL85 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 1 [GP1] pin 16 |
| GPMC_A[21]/ SPI[2]_D[0]/ **GP1[16]** | AC28 | I/O | IPD DVDD_GP MC | GPMC, SPI[2] PINCNTL110 DSIS: PIN MM: MUX0 | |
| SD2_CLK/ **GP1[15]** | M23 | I/O | IPU DVDD_GP MC | SD2 PINCNTL121 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 1 [GP1] pin 15 |
| $\overline{\text{GPMC_A[20]}}$/ $\overline{\text{SPI[2]_SCS[1]}}$/ **GP1[15]** | AD28 | I/O | IPU DVDD_GP MC | GPMC, SPI[2] PINCNTL109 DSIS: PIN MM: MUX0 | |
| SD2_DAT[0]/ GPMC_A[4]/ **GP1[14]** | L26 | I/O | IPU DVDD_GP MC | SD2, GPMC PINCNTL120 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 1 [GP1] pin 14 |
| GPMC_A[19]/ TIM3_IO/ **GP1[14]** | AC27 | I/O | IPD DVDD_GP MC | GPMC, TIMER3 PINCNTL108 DSIS: PIN MM: MUX0 | |

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**Table 4-12. GP1 Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| SD2_DAT[1]_$\overline{\text{SDIRQ}}$ / GPMC_A[3]/ **GP1[13]** | M24 | I/O | IPU DVDD_GPMC | SD2, GPMC PINCNTL119 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 1 [GP1] pin 13 |
| GPMC_A[18]/ TIM2_IO/ **GP1[13]** | AE28 | I/O | IPD DVDD_GPMC | GPMC, TIMER2 PINCNTL107 DSIS: PIN MM: MUX0 | |
| VIN[0]A_D[1]/ **GP1[12]** | AB11 | I/O | IPD DVDD | VIN[0]A PINCNTL141 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 1 [GP1] pin 12 |
| MDIO/ **GP1[12]** | P24 | I/O | IPU DVDD_GPMC | MDIO PINCNTL234 DSIS: PIN MM: MUX0 | |
| VIN[0]A_D[0]/ **GP1[11]** | AF9 | I/O | IPD DVDD | VIN[0]A PINCNTL140 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 1 [GP1] pin 11 |
| MDCLK/ **GP1[11]** | H28 | I/O | IPU DVDD_GPMC | MDIO PINCNTL233 DSIS: PIN MM: MUX0 | |
| **GP1[10]** | V2 | I/O | IPU DVDD_M | PINCNTL65 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 1 [GP1] pin 10<br>The ENLVCMOS bit in the MLBP_DAT_IO_CTRL register should be set to 1 to enable GPIO LVCMOS mode. The ENN bit in the MLBP_DAT_IO_CTRL register should also be set to 1 to enable the GPIO LVCMOS receiver. The internal Pullup/Pulldown is always disabled, regardless of the state of the PULLUDEN bit in the PINCNTL65 register. An external Pullup/Pulldown can be used to control the floating state of this pin. |
| EMAC_RMREFCLK/ TIM2_IO/ **GP1[10]** | J27 | I/O | IPD DVDD_GPMC | EMAC, TIMER2 PINCNTL232 DSIS: PIN MM: MUX0 | General-Purpose Input/Output (I/O) 1 [GP1] pin 10 |
| **GP1[9]** | V1 | I/O | IPD DVDD_M | PINCNTL64 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 1 [GP1] pin 9<br>The ENLVCMOS bit in the MLBP_DAT_IO_CTRL register should be set to 1 to enable GPIO LVCMOS mode. The ENP bit in the MLBP_DAT_IO_CTRL register should also be set to 1 to enable the GPIO LVCMOS receiver. The internal Pullup/Pulldown is always disabled, regardless of the state of the PULLUDEN bit in the PINCNTL64 register. An external Pullup/Pulldown can be used to control the floating state of this pin. |
| VIN[0]B_CLK/ CLKOUT0/ **GP1[9]** | AE17 | I/O | IPD DVDD | VIN[0]B, CLKOUT0 PINCNTL134 DSIS: PIN MM: MUX0 | General-Purpose Input/Output (I/O) 1 [GP1] pin 9 |
| **GP1[8]** | W2 | I/O | IPU DVDD_M | PINCNTL63 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 1 [GP1] pin 8<br>The ENLVCMOS bit in the MLBP_DAT_IO_CTRL register should be set to 1 to enable GPIO LVCMOS mode. The ENN bit in the MLBP_DAT_IO_CTRL register should also be set to 1 to enable the GPIO LVCMOS receiver. The internal Pullup/Pulldown is always disabled, regardless of the state of the PULLUDEN bit in the PINCNTL63 register. An external Pullup/Pulldown can be used to control the floating state of this pin. |


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**Table 4-12. GP1 Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| GPMC_CS[4]/ SD2_CMD/ **GP1[8]** | P25 | I/O | IPU DVDD_GPMC | GPMC, SD2 PINCNTL126 DSIS: PIN MM: MUX0 | General-Purpose Input/Output (I/O) 1 [GP1] pin 8 |
| **GP1[7]** | W1 | I/O | IPD DVDD_M | PINCNTL62 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 1 [GP1] pin 7<br>The ENLVCMOS bit in the MLBP_DAT_IO_CTRL register should be set to 1 to enable GPIO LVCMOS mode. The ENP bit in the MLBP_DAT_IO_CTRL register should also be set to 1 to enable the GPIO LVCMOS receiver. The internal Pullup/Pulldown is always disabled, regardless of the state of the PULLUDEN bit in the PINCNTL62 register. An external Pullup/Pulldown can be used to control the floating state of this pin. |
| DEVOSC_WAKE/ SPI[1]_SCS[1]/ TIM5_IO/ **GP1[7]** | W6 | I/O | IPU DVDD_SD | DEVOSC, SPI[1], TIMER5 PINCNTL7 DSIS: PIN MM: MUX0 | General-Purpose Input/Output (I/O) 1 [GP1] pin 7 |
| SPI[0]_SCS[1]/ SD1_SDCD/ EDMA_EVT1/ TIM4_IO/ **GP1[6]** | AE5 | I/O | IPU DVDD | SPI[0], SD1, EDMA, TIMER4 PINCNTL80 DSIS: PIN | General-Purpose Input/Output (I/O) 1 [GP1] pin 6 |
| UART0_RIN/ UART3_RTS/ UART1_RXD/ **GP1[5]** | AF4 | I/O | IPU DVDD | UART0, UART3, UART1 PINCNTL77 DSIS: PIN | General-Purpose Input/Output (I/O) 1 [GP1] pin 5 |
| UART0_DTR/ UART3_CTS/ UART1_TXD/ **GP1[4]** | AG2 | I/O | IPU DVDD | UART0, UART3, UART1 PINCNTL76 DSIS: PIN | General-Purpose Input/Output (I/O) 1 [GP1] pin 4 |
| UART0_DSR/ UART3_TXD/ SPI[0]_SCS[2]/ I2C[2]_SDA/ SD1_SDWP/ **GP1[3]** | AG4 | I/O | IPU DVDD | UART0, UART3, SPI[0], I2C[2], SD1 PINCNTL75 DSIS: PIN | General-Purpose Input/Output (I/O) 1 [GP1] pin 3 |
| UART0_DCD/ UART3_RXD/ SPI[0]_SCS[3]/ I2C[2]_SCL/ SD1_POW/ **GP1[2]** | AH4 | I/O | IPU DVDD | UART0, UART3, SPI[0], I2C[2], SD1 PINCNTL74 DSIS: PIN | General-Purpose Input/Output (I/O) 1 [GP1] pin 2 |
| DCAN0_RX/ UART2_RXD/ I2C[3]_SCL/ **GP1[1]** | AG6 | I/O | IPU DVDD | DCAN0, UART2, I2C[3] PINCNTL69 DSIS: PIN | General-Purpose Input/Output (I/O) 1 [GP1] pin 1 |
| DCAN0_TX/ UART2_TXD/ I2C[3]_SDA/ **GP1[0]** | AH6 | I/O | IPU DVDD | DCAN0, UART2, I2C[3] PINCNTL68 DSIS: PIN | General-Purpose Input/Output (I/O) 1 [GP1] pin 0 |

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## Table 4-13. GP2 Terminal Functions

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **GPIO2** | | | | | |
| **Note:** General-Purpose Input/Output (I/O) pins can also serve as external interrupt inputs. | | | | | |
| VOUT[1]_AVID/ EMAC[1]_MRXER/ UART4_RTS/ TIM6_IO/ **GP2[31]** | Y22 | I/O | IPD DVDD | VOUT[1], EMAC[1], UART4, TIMER6 PINCNTL207 DSIS: PIN | General-Purpose Input/Output (I/O) 2 [GP2] pin 31 |
| VOUT[1]_VSYNC/ EMAC[1]_MCRS/ SPI[3]_D[0]/ UART3_CTS/ **GP2[30]** | AA23 | I/O | IPD DVDD | VOUT[1], EMAC[1], SPI[3], UART3 PINCNTL206 DSIS: PIN | General-Purpose Input/Output (I/O) 2 [GP2] pin 30 |
| VOUT[1]_HSYNC/ EMAC[1]_MCOL/ SPI[3]_D[1]/ UART3_RTS/ **GP2[29]** | AC24 | I/O | IPD DVDD | VOUT[1], EMAC[1], SPI[3], UART3 PINCNTL205 DSIS: PIN | General-Purpose Input/Output (I/O) 2 [GP2] pin 29 |
| VOUT[1]_CLK/ EMAC[1]_MTCLK/ **GP2[28]** | AE24 | I/O | IPD DVDD | VOUT[1], EMAC[1] PINCNTL204 DSIS: PIN | General-Purpose Input/Output (I/O) 2 [GP2] pin 28 |
| VOUT[0]_R_CR[3]/ **GP2[27]** | AB9 | I/O | IPD DVDD | VOUT[0] PINCNTL197 DSIS: PIN | General-Purpose Input/Output (I/O) 2 [GP2] pin 27 |
| VOUT[0]_R_CR[2]/ EMU4/ **GP2[26]** | AD9 | I/O | IPD DVDD | VOUT[0], EMU PINCNTL196 DSIS: PIN | General-Purpose Input/Output (I/O) 2 [GP2] pin 26 |
| VOUT[0]_G_Y_YC[3]/ **GP2[25]** | AH15 | I/O | IPD DVDD | VOUT[0] PINCNTL189 DSIS: PIN | General-Purpose Input/Output (I/O) 2 [GP2] pin 25 |
| VOUT[0]_G_Y_YC[2]/ EMU3/ **GP2[24]** | AH7 | I/O | IPD DVDD | VOUT[0], EMU PINCNTL188 DSIS: PIN | General-Purpose Input/Output (I/O) 2 [GP2] pin 24 |
| VOUT[0]_B_CB_C[3]/ **GP2[23]** | AE15 | I/O | IPD DVDD | VOUT[0] PINCNTL181 DSIS: PIN | General-Purpose Input/Output (I/O) 2 [GP2] pin 23 |
| VOUT[0]_B_CB_C[2]/ EMU2/ **GP2[22]** | AG7 | I/O | IPD DVDD | VOUT[0], EMU PINCNTL180 DSIS: PIN | General-Purpose Input/Output (I/O) 2 [GP2] pin 22 |
| VOUT[0]_AVID/ VOUT[0]_FLD/ SPI[3]_SCLK/ TIM7_IO/ **GP2[21]** | AA10 | I/O | IPD DVDD | VOUT[0], SPI[3], TIMER7 PINCNTL179 DSIS: PIN | General-Purpose Input/Output (I/O) 2 [GP2] pin 21 |
| VIN[0]A_D[15]_BD[7]/ CAM_SHUTTER/ **GP2[20]** | AC14 | I/O | DIS DVDD | VIN[0]AB, CAMERA_I/F PINCNTL155 DSIS: PIN | General-Purpose Input/Output (I/O) 2 [GP2] pin 20 |
| VIN[0]A_D[14]_BD[6]/ CAM_STROBE/ **GP2[19]** | AC12 | I/O | IPD DVDD | VIN[0]AB, CAMERA_I/F PINCNTL154 DSIS: PIN | General-Purpose Input/Output (I/O) 2 [GP2] pin 19 |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal


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**Table 4-13. GP2 Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| VIN[0]A_D[13]_BD[5]/ CAM_RESET/ **GP2[18]** | AF17 | I/O | IPD DVDD | VIN[0]AB, CAMERA_I/F PINCNTL153 DSIS: PIN | General-Purpose Input/Output (I/O) 2 [GP2] pin 18 |
| VIN[0]A_D[12]_BD[4]/ CLKOUT1/ **GP2[17]** | AG17 | I/O | IPD DVDD | VIN[0]AB, CLKOUT1 PINCNTL152 DSIS: PIN | General-Purpose Input/Output (I/O) 2 [GP2] pin 17 |
| VIN[0]A_D[11]_BD[3]/ CAM_WE/ **GP2[16]** | AH17 | I/O | IPD DVDD | VIN[0]AB, CAMERA_I/F PINCNTL151 DSIS: PIN | General-Purpose Input/Output (I/O) 2 [GP2] pin 16 |
| VIN[0]A_D[10]_BD[2]/ **GP2[15]** | AH9 | I/O | IPD DVDD | VIN[0]AB PINCNTL150 DSIS: PIN | General-Purpose Input/Output (I/O) 2 [GP2] pin 15 |
| VIN[0]A_D[9]_BD[1]/ **GP2[14]** | AG9 | I/O | IPD DVDD | VIN[0]AB PINCNTL149 DSIS: PIN | General-Purpose Input/Output (I/O) 2 [GP2] pin 14 |
| VIN[0]A_D[8]_BD[0]/ **GP2[13]** | AB15 | I/O | IPD DVDD | VIN[0]AB PINCNTL148 DSIS: PIN | General-Purpose Input/Output (I/O) 2 [GP2] pin 13 |
| VIN[0]A_D[7]/ **GP2[12]** | AA11 | I/O | IPD DVDD | VIN[0]A PINCNTL147 DSIS: PIN | General-Purpose Input/Output (I/O) 2 [GP2] pin 12 |
| VIN[0]A_D[6]/ **GP2[11]** | AH16 | I/O | IPD DVDD | VIN[0]A PINCNTL146 DSIS: PIN | General-Purpose Input/Output (I/O) 2 [GP2] pin 11 |
| VIN[0]A_D[5]/ **GP2[10]** | AG16 | I/O | IPD DVDD | VIN[0]A PINCNTL145 DSIS: PIN | General-Purpose Input/Output (I/O) 2 [GP2] pin 10 |
| VIN[0]A_D[4]/ **GP2[9]** | AH8 | I/O | IPD DVDD | VIN[0]A PINCNTL144 DSIS: PIN | General-Purpose Input/Output (I/O) 2 [GP2] pin 9 |
| VIN[0]A_D[3]/ **GP2[8]** | AE12 | I/O | IPD DVDD | VIN[0]A PINCNTL143 DSIS: PIN | General-Purpose Input/Output (I/O) 2 [GP2] pin 8 |
| VIN[0]A_D[2]/ **GP2[7]** | AC9 | I/O | IPD DVDD | VIN[0]A PINCNTL142 DSIS: PIN | General-Purpose Input/Output (I/O) 2 [GP2] pin 7 |
| SD2_DAT[2]_SDRW/ GPMC_A[2]/ **GP2[6]** | K27 | I/O | IPU DVDD_GP MC | SD2, GPMC PINCNTL118 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 2 [GP2] pin 6 |
| GPMC_A[17]/ **GP2[6]** | V23 | I/O | IPD DVDD_GP MC | GPMC PINCNTL106 DSIS: PIN MM: MUX0 | |
| SD2_DAT[3]/ GPMC_A[1]/ **GP2[5]** | J28 | I/O | IPU DVDD_GP MC | SD2, GPMC PINCNTL117 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 2 [GP2] pin 5 |
| GPMC_A[16]/ **GP2[5]** | AD27 | I/O | IPD DVDD_GP MC | GPMC PINCNTL105 DSIS: PIN MM: MUX0 | |
| VIN[0]A_VSYNC/ UART5_CTS/ **GP2[4]** | AD20 | I/O | IPU DVDD | VIN[0]A, UART5 PINCNTL139 DSIS: PIN | General-Purpose Input/Output (I/O) 2 [GP2] pin 4 |

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**Table 4-13. GP2 Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| VIN[0]A_HSYNC/ UART5_RTS/ **GP2[3]** | AC20 | I/O | IPU DVDD | VIN[0]A, UART5 PINCNTL138 DSIS: PIN | General-Purpose Input/Output (I/O) 2 [GP2] pin 3 |
| VIN[0]A_CLK/ **GP2[2]** | AB20 | I/O | IPD DVDD | VIN[0]A PINCNTL137 DSIS: PIN MM: MUX1 | General-Purpose Input/Output (I/O) 2 [GP2] pin 2 |
| VOUT[0]_FLD/ CAM_PCLK/ GPMC_A[12]/ UART2_RTS/ **GP2[2]** | AF18 | I/O | IPD DVDD_C | VOUT[0], CAMERA_I/F, GPMC, UART2 PINCNTL175 DSIS: PIN MM: MUX0 | |
| VIN[0]A_FLD/ VIN[0]B_VSYNC/ UART5_RXD/ I2C[2]_SCL/ **GP2[1]** | AA20 | I/O | IPU DVDD | VIN[0]A, VIN[0]B, UART5, I2C[2] PINCNTL136 DSIS: PIN | General-Purpose Input/Output (I/O) 2 [GP2] pin 1 |
| VIN[0]A_DE/ VIN[0]B_HSYNC/ UART5_TXD/ I2C[2]_SDA/ **GP2[0]** | AE21 | I/O | IPU DVDD | VIN[0]A, VIN[0]B, UART5, I2C[2] PINCNTL135 DSIS: PIN | General-Purpose Input/Output (I/O) 2 [GP2] pin 0 |


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**Table 4-14. GP3 Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **GPIO3** | | | | | |
| **Note:** General-Purpose Input/Output (I/O) pins can also serve as external interrupt inputs. | | | | | |
| CLKIN32/<br>CLKOUT0/<br>TIM3_IO/<br>**GP3[31]** | J7 | I/O | IPD<br>DVDD | CLKIN32,<br>CLKOUT0,<br>TIMER3<br>PINCNTL259<br>DSIS: PIN | General-Purpose Input/Output (I/O) 3 [GP3] pin 31. |
| VOUT[1]_B_CB_C[2]/<br>GPMC_A[0]/<br>HDMI_CEC/<br>SPI[2]_D[0]/<br>**GP3[30]** | AF28 | I/O | IPU<br>DVDD | VOUT[1], GPMC,<br>HDMI, SPI[2]<br>PINCNTL231<br>DSIS: PIN<br>MM: MUX1 | General-Purpose Input/Output (I/O) 3 [GP3] pin 30. |
| EMAC[0]_MRXD[2]/<br>EMAC[0]_RGRXD[1]/<br>EMAC[0]_RMTXEN/<br>**GP3[30]** | R23 | I/O | IPD<br>DVDD_GPMC | EMAC[0]<br>PINCNTL242<br>DSIS: PIN<br>MM: MUX0 | |
| EMAC[0]_MRXD[1]/<br>EMAC[0]_RGRXD[0]/<br>EMAC[0]_RMTXD[1]/<br>**GP3[29]** | P23 | I/O | IPD<br>DVDD_GPMC | EMAC[0]<br>PINCNTL241<br>DSIS: PIN | General-Purpose Input/Output (I/O) 3 [GP3] pin 29. |
| EMAC[0]_MRXD[0]/<br>EMAC[0]_RGTXD[0]/<br>EMAC[0]_RMTXD[0]/<br>**GP3[28]** | G28 | I/O | IPD<br>DVDD_GPMC | EMAC[0]<br>PINCNTL240<br>DSIS: PIN | General-Purpose Input/Output (I/O) 3 [GP3] pin 28. |
| EMAC[0]_MRCLK/<br>EMAC[0]_RGTXC/<br>EMAC[0]_RMCRSDV/<br>SPI[3]_SCS[2]/<br>**GP3[27]** | H27 | I/O | IPD<br>DVDD_GPMC | EMAC[0], SPI[3]<br>PINCNTL239<br>DSIS: PIN | General-Purpose Input/Output (I/O) 3 [GP3] pin 27. |
| EMAC[0]_MRXER/<br>EMAC[0]_RGTXCTL/<br>EMAC[0]_RMRXER/<br>**GP3[26]** | J26 | I/O | IPD<br>DVDD_GPMC | EMAC[0]<br>PINCNTL238<br>DSIS: PIN | General-Purpose Input/Output (I/O) 3 [GP3] pin 26. |
| EMAC[0]_MCRS/<br>EMAC[0]_RGRXD[2]/<br>EMAC[0]_RMRXD[1]/<br>**GP3[25]** | R25 | I/O | IPD<br>DVDD_GPMC | EMAC[0]<br>PINCNTL237<br>DSIS: PIN | General-Purpose Input/Output (I/O) 3 [GP3] pin 25. |
| EMAC[0]_MCOL/<br>EMAC[0]_RGRXCTL/<br>EMAC[0]_RMRXD[0]/<br>**GP3[24]** | L23 | I/O | IPD<br>DVDD_GPMC | EMAC[0]<br>PINCNTL236<br>DSIS: PIN | General-Purpose Input/Output (I/O) 3 [GP3] pin 24. |
| EMAC[0]_MTCLK/<br>EMAC[0]_RGRXC/<br>SPI[3]_SCS[3]/<br>I2C[2]_SDA/<br>**GP3[23]** | L24 | I/O | IPD<br>DVDD_GPMC | EMAC[0], SPI[3],<br>I2C[2]<br>PINCNTL235<br>DSIS: PIN | General-Purpose Input/Output (I/O) 3 [GP3] pin 23. |
| VOUT[1]_R_CR[2]/<br>GPMC_A[15]/<br>HDMI_HPDET/<br>SPI[2]_D[1]/<br>**GP3[22]** | AE27 | I/O | IPD<br>DVDD | VOUT[1], GPMC,<br>HDMI, SPI[2]<br>PINCNTL230<br>DSIS: PIN | General-Purpose Input/Output (I/O) 3 [GP3] pin 22. |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal

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**Table 4-14. GP3 Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| VOUT[1]_R_CR[3]/ GPMC_A[14]/ HDMI_SDA/ SPI[2]_SCLK/ I2C[2]_SDA **GP3[21]** | AG28 | I/O | IPU DVDD | VOUT[1], GPMC, HDMI, SPI[2], I2C[2] PINCNTL229 DSIS: PIN | General-Purpose Input/Output (I/O) 3 [GP3] pin 21. |
| VOUT[1]_G_Y_YC[2]/ GPMC_A[13]/ HDMI_SCL/ SPI[2]_SCS[2]/ I2C[2]_SCL/ **GP3[20]** | AF27 | I/O | IPU DVDD | VOUT[1], GPMC, HDMI, SPI[2], I2C[2] PINCNTL228 DSIS: PIN | General-Purpose Input/Output (I/O) 3 [GP3] pin 20. |
| VOUT[1]_R_CR[9]/ EMAC[1]_MTXEN/ UART5_TXD/ **GP3[19]** | Y24 | I/O | IPD DVDD | VOUT[1], EMAC[1], UART5 PINCNTL227 DSIS: PIN | General-Purpose Input/Output (I/O) 3 [GP3] pin 19. |
| VOUT[1]_R_CR[8]/ EMAC[1]_MTXD[7]/ UART5_RXD/ **GP3[18]** | W23 | I/O | IPD DVDD | VOUT[1], EMAC[1], UART5 PINCNTL226 DSIS: PIN | General-Purpose Input/Output (I/O) 3 [GP3] pin 18. |
| VOUT[1]_R_CR[7]/ EMAC[1]_MTXD[6]/ SPI[3]_D[0]/ **GP3[17]** | V22 | I/O | IPD DVDD | VOUT[1], EMAC[1], SPI[3] PINCNTL225 DSIS: PIN | General-Purpose Input/Output (I/O) 3 [GP3] pin 17. |
| VOUT[1]_R_CR[6]/ EMAC[1]_MTXD[5]/ SPI[3]_D[1]/ **GP3[16]** | AA25 | I/O | IPD DVDD | VOUT[1], EMAC[1], SPI[3] PINCNTL224 DSIS: PIN | General-Purpose Input/Output (I/O) 3 [GP3] pin 16. |
| VOUT[1]_R_CR[5]/ EMAC[1]_MTXD[4]/ SPI[3]_SCLK/ **GP3[15]** | AC26 | I/O | IPD DVDD | VOUT[1], EMAC[1], , SPI[3] PINCNTL223 DSIS: PIN | General-Purpose Input/Output (I/O) 3 [GP3] pin 15. |
| VOUT[1]_R_CR[4]/ EMAC[1]_MTXD[3]/ SPI[3]_SCS[1]/ **GP3[14]** | AG27 | I/O | IPD DVDD | VOUT[1], EMAC[1], SPI[3] PINCNTL222 DSIS: PIN | General-Purpose Input/Output (I/O) 3 [GP3] pin 14. |
| VOUT[1]_G_Y_YC[9]/ EMAC[1]_MTXD[2]/ **GP3[13]** | AD26 | I/O | IPD DVDD | VOUT[1], EMAC[1] PINCNTL221 DSIS: PIN | General-Purpose Input/Output (I/O) 3 [GP3] pin 13. |
| VOUT[1]_G_Y_YC[8]/ EMAC[1]_MTXD[1]/ **GP3[12]** | AE26 | I/O | IPD DVDD | VOUT[1], EMAC[1] PINCNTL220 DSIS: PIN | General-Purpose Input/Output (I/O) 3 [GP3] pin 12. |
| VOUT[1]_G_Y_YC[7]/ EMAC[1]_MTXD[0]/ **GP3[11]** | AF26 | I/O | IPD DVDD | VOUT[1], EMAC[1] PINCNTL219 DSIS: PIN | General-Purpose Input/Output (I/O) 3 [GP3] pin 11. |
| VOUT[1]_G_Y_YC[6]/ EMAC[1]_GMTCLK/ **GP3[10]** | AH27 | I/O | IPD DVDD | VOUT[1], EMAC[1] PINCNTL218 DSIS: PIN | General-Purpose Input/Output (I/O) 3 [GP3] pin 10. |
| VOUT[1]_G_Y_YC[5]/ EMAC[1]_MRXDV/ **GP3[9]** | AG26 | I/O | IPD DVDD | VOUT[1], EMAC[1] PINCNTL217 DSIS: PIN | General-Purpose Input/Output (I/O) 3 [GP3] pin 9. |
| VOUT[1]_G_Y_YC[4]/ EMAC[1]_MRXD[7]/ **GP3[8]** | W22 | I/O | IPD DVDD | VOUT[1], EMAC[1] PINCNTL216 DSIS: PIN | General-Purpose Input/Output (I/O) 3 [GP3] pin 8. |
| VOUT[1]_G_Y_YC[3]/ EMAC[1]_MRXD[6]/ **GP3[7]** | Y23 | I/O | IPD DVDD | VOUT[1], EMAC[1] PINCNTL215 DSIS: PIN | General-Purpose Input/Output (I/O) 3 [GP3] pin 7. |
| VOUT[1]_B_CB_C[9]/ EMAC[1]_MRXD[5]/ I2C[3]_SDA/ **GP3[6]** | AA24 | I/O | IPD DVDD | VOUT[1], EMAC[1], I2C[3] PINCNTL214 DSIS: PIN | General-Purpose Input/Output (I/O) 3 [GP3] pin 6. |


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**Table 4-14. GP3 Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| VOUT[1]_B_CB_C[8]/ EMAC[1]_MRXD[4]/ I2C[3]_SCL/ **GP3[5]** | AH26 | I/O | IPD DVDD | VOUT[1], EMAC[1], I2C[3] PINCNTL213 DSIS: PIN | General-Purpose Input/Output (I/O) 3 [GP3] pin 5. |
| VOUT[1]_B_CB_C[7]/ EMAC[1]_MRXD[3]/ UART3_TXD/ **GP3[4]** | AC25 | I/O | IPD DVDD | VOUT[1], EMAC[1], UART3 PINCNTL212 DSIS: PIN | General-Purpose Input/Output (I/O) 3 [GP3] pin 4. |
| VOUT[1]_B_CB_C[6]/ EMAC[1]_MRXD[2]/ UART3_RXD/ **GP3[3]** | AD25 | I/O | IPD DVDD | VOUT[1], EMAC[1], UART3 PINCNTL211 DSIS: PIN | General-Purpose Input/Output (I/O) 3 [GP3] pin 3. |
| VOUT[1]_B_CB_C[5]/ EMAC[1]_MRXD[1]/ UART4_TXD/ **GP3[2]** | AF25 | I/O | IPD DVDD | VOUT[1], EMAC[1], UART4 PINCNTL210 DSIS: PIN | General-Purpose Input/Output (I/O) 3 [GP3] pin 2. |
| VOUT[1]_B_CB_C[4]/ EMAC[1]_MRXD[0]/ UART4_RXD/ **GP3[1]** | AG25 | I/O | IPD DVDD | VOUT[1], EMAC[1], UART4 PINCNTL209 DSIS: PIN | General-Purpose Input/Output (I/O) 3 [GP3] pin 1. |
| VOUT[1]_B_CB_C[3]/ EMAC[1]_MRCLK/ UART4_CTS/ **GP3[0]** | AH25 | I/O | IPD DVDD | VOUT[1], EMAC[1], UART4 PINCNTL208 DSIS: PIN | General-Purpose Input/Output (I/O) 2 [GP2] pin 0. |

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### 4.2.9 GPMC

**Table 4-15. GPMC Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **GPMC_CLK**/ GPMC_CS[5]/ GPMC_WAIT[1]/ CLKOUT1/ EDMA_EVT3/ TIM4_IO/ GP1[27] | R26 | O | IPU DVDD_GPMCB | GPMC, CLKOUT1, EDMA, TIMER4, GP1 PINCNTL127 DSIS: 0 | GPMC Clock output |
| SD2_DAT[4]/ GPMC_A[27]/ GPMC_A[23]/ **GPMC_CS[7]**/ EDMA_EVT0/ TIM7_IO/ GP1[22] | R24 | O | IPU DVDD_GPMC | SD2, GPMC, EDMA, TIMER7, GP1 PINCNTL116 DSIS: N/A | GPMC Chip Select 7 |
| GPMC_ADV_ALE/ **GPMC_CS[6]**/ TIM5_IO/ GP1[28] | M26 | O | IPU DVDD_GPMCB | GPMC, TIMER5, GP1 PINCNTL128 DSIS: N/A | GPMC Chip Select 6 |
| GPMC_CLK/ **GPMC_CS[5]**/ GPMC_WAIT[1]/ CLKOUT1/ EDMA_EVT3/ TIM4_IO/ GP1[27] | R26 | O | IPU DVDD_GPMCB | GPMC, CLKOUT1, EDMA, TIMER4, GP1 PINCNTL127 DSIS: N/A | GPMC Chip Select 5 |
| **GPMC_CS[4]**/ SD2_CMD/ GP1[8] | P25 | O | IPU DVDD_GPMC | SD2, GP1 PINCNTL126 DSIS: N/A | GPMC Chip Select 4 |
| **GPMC_CS[3]**/ SPI[2]_SCS[0]/ GP1[26] | P26 | O | IPU DVDD_GPMC | SPI[2], GP1 PINCNTL125 DSIS: N/A | GPMC Chip Select 3 |
| **GPMC_CS[2]**/ GPMC_A[24]/ GP1[25] | M25 | O | IPU DVDD_GPMC | GPMC, GP1 PINCNTL124 DSIS: N/A | GPMC Chip Select 2 |
| **GPMC_CS[1]**/ GPMC_A[25]/ GP1[24] | K28 | O | IPU DVDD_GPMCB | GPMC, GP1 PINCNTL123 DSIS: N/A | GPMC Chip Select 1 |
| **GPMC_CS[0]**/ GP1[23] | T28 | O | IPU DVDD_GPMCB | GP1 PINCNTL122 DSIS: N/A | GPMC Chip Select 0 |
| GPMC_WE | U28 | O | IPU DVDD_GPMCB | – PINCNTL130 DSIS: N/A | GPMC Write Enable output |
| GPMC_OE_RE | T27 | O | IPU DVDD_GPMCB | – PINCNTL129 DSIS: N/A | GPMC Output Enable output |
| **GPMC_BE[1]**/ GPMC_A[24]/ EDMA_EVT1/ TIM7_IO/ GP1[30] | V28 | O | IPD DVDD_GPMCB | GPMC, EDMA, TIMER7, GP1 PINCNTL132 DSIS: N/A | GPMC Upper Byte Enable output |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and the Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal


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**Table 4-15. GPMC Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **GPMC_$\overline{\text{BE[0]}}$_CLE/** GPMC_A[25]/ EDMA_EVT2/ TIM6_IO/ GP1[29] | U27 | O | IPD DVDD_GPMCB | GPMC, EDMA, TIMER6, GP1 PINCNTL131 DSIS: PIN | GPMC Lower Byte Enable output or Command Latch Enable output |
| **GPMC_$\overline{\text{ADV}}$_ALE/** GPMC_CS[6]/ TIM5_IO/ GP1[28] | M26 | O | IPU DVDD_GPMCB | GPMC, TIMER5, GP1 PINCNTL128 DSIS: N/A | GPMC Address Valid output or Address Latch Enable output |
| GPMC_CLK/ $\overline{\text{GPMC_CS[5]}}$/ **GPMC_WAIT[1]/** CLKOUT1/ EDMA_EVT3/ TIM4_IO/ GP1[27] | R26 | I | IPU DVDD_GPMCB | GPMC, CLKOUT1, EDMA, TIMER4, GP1 PINCNTL127 DSIS: 1 | GPMC Wait input 1 |
| **GPMC_WAIT[0]/** GPMC_A[26]/ EDMA_EVT0/ GP1[31] | W28 | I | IPU DVDD_GPMCB | GPMC, EDMA, GP1 PINCNTL133 DSIS: 1 | GPMC Wait input 0 |
| EMAC[0]_MRXD[3]/ EMAC[1]_RGRXCTL/ **GPMC_A[27]/** GPMC_A[26]/ GPMC_A[0]/ UART5_RXD | J25 | O | IPD DVDD_GPMC | EMAC[0], EMAC[1], GPMC, UART5 PINCNTL243 DSIS: N/A MM: MUX1 | GPMC Address 27 |
| SD2_DAT[4]/ **GPMC_A[27]/** $\overline{\text{GPMC_A[23]}}$/ $\overline{\text{GPMC_CS[7]}}$/ EDMA_EVT0/ TIM7_IO/ GP1[22] | R24 | O | IPU DVDD_GPMC | SD2, GPMC, EDMA, TIMER7, GP1 PINCNTL116 DSIS: N/A MM: MUX0 | |
| GPMC_WAIT[0]/ **GPMC_A[26]/** EDMA_EVT0/ GP1[31] | W28 | O | IPU DVDD_GPMCB | GPMC, EDMA, GP1 PINCNTL133 DSIS: N/A MM: MUX2 | GPMC Address 26 |
| EMAC[0]_MRXD[3]/ EMAC[1]_RGRXCTL/ GPMC_A[27]/ **GPMC_A[26]/** GPMC_A[0]/ UART5_RXD | J25 | O | IPD DVDD_GPMC | EMAC[0], EMAC[1], GPMC, UART5 PINCNTL243 DSIS: N/A MM: MUX1 | |
| SD2_DAT[5]/ **GPMC_A[26]/** GPMC_A[22]/ TIM6_IO/ GP1[21] | P22 | O | IPU DVDD_GPMC | SD2, GPMC, TIMER6, GP1 PINCNTL115 DSIS: N/A MM: MUX0 | |

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**Table 4-15. GPMC Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| GPMC_BE[0]_CLE/ **GPMC_A[25]**/ EDMA_EVT2/ TIM6_IO/ GP1[29] | U27 | O | IPD DVDD_GPMCB | GPMC, EDMA, TIMER6, GP1 PINCNTL131 DSIS: N/A MM: MUX2 | GPMC Address 25 |
| GPMC_CS[1]/ **GPMC_A[25]**/ GP1[24] | K28 | O | IPU DVDD_GPMCB | GPMC, GP1 PINCNTL123 DSIS: N/A MM: MUX1 | |
| SD2_DAT[6]/ **GPMC_A[25]**/ GPMC_A[21]/ UART2_TXD/ GP1[20] | N23 | O | IPU DVDD_GPMC | SD2, GPMC, UART2, GP1 PINCNTL114 DSIS: N/A MM: MUX0 | |
| GPMC_BE[1]/ **GPMC_A[24]**/ EDMA_EVT1/ TIM7_IO/ GP1[30] | V28 | O | IPD DVDD_GPMCB | GPMC, EDMA, TIMER7, GP1 PINCNTL132 DSIS: N/A MM: MUX2 | GPMC Address 24 |
| GPMC_CS[2]/ **GPMC_A[24]**/ GP1[25] | M25 | O | IPU DVDD_GPMC | GPMC, GP1 PINCNTL124 DSIS: N/A MM: MUX1 | |
| SD2_DAT[7]/ **GPMC_A[24]**/ GPMC_A[20]/ UART2_RXD/ GP1[19] | L25 | O | IPU DVDD_GPMC | SD2, GPMC, UART2, GP1 PINCNTL113 DSIS: N/A MM: MUX0 | |
| SD2_DAT[4]/ GPMC_A[27]/ **GPMC_A[23]**/ GPMC_CS[7]/ EDMA_EVT0/ TIM7_IO/ GP1[22] | R24 | O | IPU DVDD_GPMC | SD2, GPMC, EDMA, TIMER5, GP1 PINCNTL116 DSIS: N/A MM: MUX1 | GPMC Address 23 |
| **GPMC_A[23]**/ SPI[2]_SCLK/ HDMI_HPDET/ TIM5_IO/ GP1[18] | AA26 | O | IPD DVDD_GPMCB | SPI[2], HDMI, TIMER5, GP1 PINCNTL112 DSIS: N/A MM: MUX0 | |
| SD2_DAT[5]/ GPMC_A[26]/ **GPMC_A[22]**/ TIM6_IO/ GP1[21] | P22 | O | IPU DVDD_GPMC | SD2, GPMC, TIMER6, GP1 PINCNTL115 DSIS: N/A MM: MUX1 | GPMC Address 22 |
| **GPMC_A[22]**/ SPI[2]_D[1]/ HDMI_CEC/ TIM4_IO/ GP1[17] | AB27 | O | IPU DVDD_GPMCB | SPI[2], HDMI, TIMER4, GP1 PINCNTL111 DSIS: N/A MM: MUX0 | |
| SD2_DAT[6]/ GPMC_A[25]/ **GPMC_A[21]**/ UART2_TXD/ GP1[20] | N23 | O | IPU DVDD_GPMC | SD2, GPMC, UART2, GP1 PINCNTL114 DSIS: N/A MM: MUX1 | GPMC Address 21 |
| **GPMC_A[21]**/ SPI[2]_D[0]/ GP1[16] | AC28 | O | IPD DVDD_GPMCB | SPI[2], GP1 PINCNTL110 DSIS: N/A MM: MUX0 | |


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**Table 4-15. GPMC Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| SD2_DAT[7]/ GPMC_A[24]/ **GPMC_A[20]**/ UART2_RXD/ GP1[19] | L25 | O | IPU DVDD_GPMC | SD2, GPMC, UART2, GP1 PINCNTL113 DSIS: N/A MM: MUX1 | GPMC Address 20 |
| **GPMC_A[20]**/ SPI[2]_SCS[1]/ GP1[15] | AD28 | O | IPU DVDD_GPMCB | SPI[2], GP1 PINCNTL109 DSIS: N/A MM: MUX0 | |
| **GPMC_A[19]**/ TIM3_IO/ GP1[14] | AC27 | O | IPD DVDD_GPMCB | TIMER2, GP1 PINCNTL108 DSIS: N/A | GPMC Address 19 |
| **GPMC_A[18]**/ TIM2_IO/ GP1[13] | AE28 | O | IPD DVDD_GPMCB | TIMER2, GP1 PINCNTL107 DSIS: N/A | GPMC Address 18 |
| **GPMC_A[17]**/ GP2[6] | V23 | O | IPD DVDD_GPMCB | GP2 PINCNTL106 DSIS: N/A | GPMC Address 17 |
| **GPMC_A[16]**/ GP2[5] | AD27 | O | IPD DVDD_GPMCB | GP2 PINCNTL105 DSIS: N/A | GPMC Address 16 |
| VOUT[1]_R_CR[2]/ **GPMC_A[15]**/ HDMI_HPDET/ SPI[2]_D[1]/ GP3[22] | AE27 | O | IPD DVDD | VOUT[1], HDMI, SPI[2],GP3 PINCNTL230 DSIS: N/A MM: MUX1 | GPMC Address 15 |
| EMAC[0]_MTXEN/ EMAC[1]_RGRXD[2]/ EMAC[1]_RMTXEN/ **GPMC_A[15]**/ UART1_RTS | J23 | O | IPD DVDD_GPMC | EMAC[0], EMAC[1], UART1 PINCNTL258 DSIS: N/A MM: MUX0 | |
| VOUT[1]_R_CR[3]/ **GPMC_A[14]**/ HDMI_SDA/ SPI[2]_SCLK/ I2C[2]_SDA/ GP3[21] | AG28 | O | IPU DVDD | VOUT[1], HDMI, SPI[2], I2C[2], GP3 PINCNTL229 DSIS: N/A MM: MUX1 | GPMC Address 14 |
| EMAC[0]_MTXD[7]/ EMAC[1]_RGTXD[3]/ EMAC[1]_RMTXD[1]/ **GPMC_A[14]**/ UART1_CTS | H24 | O | IPD DVDD_GPMC | EMAC[0], EMAC[1], UART1 PINCNTL257 DSIS: N/A MM: MUX0 | |
| VOUT[1]_G_Y_YC[2]/ **GPMC_A[13]**/ HDMI_SCL/ SPI[2]_SCS[2]/ I2C[2]_SCL/ GP3[20] | AF27 | O | IPU DVDD | VOUT[1], HDMI, SPI[2], I2C[2], GP3 PINCNTL228 DSIS: N/A MM: MUX1 | GPMC Address 13 |
| EMAC[0]_MTXD[6]/ EMAC[1]_RGRXD[0]/ EMAC[1]_RMTXD[0]/ **GPMC_A[13]**/ UART1_TXD | J22 | O | IPD DVDD_GPMC | EMAC[0], EMAC[1], UART1 PINCNTL256 DSIS: N/A MM: MUX0 | |

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**Table 4-15. GPMC Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| VOUT[0]_FLD/ CAM_PCLK/ **GPMC_A[12]**/ UART2_RTS/ GP2[2] | AF18 | O | IPD DVDD_C | VOUT[0], CAMERA_I/F, UART2, GP2 PINCNTL175 DSIS: N/A MM: MUX1 | GPMC Address 12 |
| EMAC[0]_MTXD[5]/ EMAC[1]_RGTXC/ EMAC[1]_RMCRSDV/ **GPMC_A[12]**/ UART1_RXD | F27 | O | IPD DVDD_GPMC | EMAC[0], EMAC[1], UART1 PINCNTL255 DSIS: N/A MM: MUX0 | |
| VOUT[1]_FLD/ CAM_FLD/ CAM_WE/ **GPMC_A[11]**/ UART2_CTS/ GP0[28] | AB23 | O | IPD DVDD_C | VOUT[1], CAMERA_I/F, UART2, GP0 PINCNTL174 DSIS: N/A MM: MUX1 | GPMC Address 11 |
| EMAC[0]_MTXD[4]/ EMAC[1]_RGTXD[2]/ EMAC[1]_RMRXER/ **GPMC_A[11]**/ UART4_RTS | G23 | O | IPD DVDD_GPMC | EMAC[0], EMAC[1], UART4 PINCNTL254 DSIS: N/A MM: MUX0 | |
| VOUT[1]_B_CB_C[0]/ CAM_VS/ **GPMC_A[10]**/ UART2_TXD/ GP0[27] | AD23 | O | IPU DVDD_C | VOUT[1], CAMERA_I/F, UART2, GP0 PINCNTL173 DSIS: N/A MM: MUX1 | GPMC Address 10 |
| EMAC[0]_MTXD[3]/ EMAC[1]_RGTXD[0]/ EMAC[1]_RMRXD[1]/ **GPMC_A[10]**/ UART4_CTS | H23 | O | IPD DVDD_GPMC | EMAC[0], EMAC[1], UART4 PINCNTL253 DSIS: N/A MM: MUX0 | |
| VOUT[1]_B_CB_C[1]/ CAM_HS/ **GPMC_A[9]**/ UART2_RXD/ GP0[26] | AE23 | O | IPD DVDD_C | VOUT[1], CAMERA_I/F, UART2, GP0 PINCNTL172 DSIS: N/A MM: MUX1 | GPMC Address 9 |
| EMAC[0]_MTXD[2]/ EMAC[1]_RGTXCTL/ EMAC[1]_RMRXD[0]/ **GPMC_A[9]**/ UART4_TXD | H22 | O | IPD DVDD_GPMC | EMAC[0], EMAC[1], UART4 PINCNTL252 DSIS: N/A MM: MUX0 | |
| VOUT[1]_R_CR[0]/ CAM_D[0]/ **GPMC_A[8]**/ UART4_RTS/ GP0[25] | AA22 | O | IPD DVDD_C | VOUT[1], CAMERA_I/F, UART4, GP0 PINCNTL171 DSIS: N/A MM: MUX1 | GPMC Address 8 |
| EMAC[0]_MTXD[1]/ EMAC[1]_RGTXD[1]/ **GPMC_A[8]**/ UART4_RXD | H25 | O | IPD DVDD_GPMC | EMAC[0], EMAC[1], UART4 PINCNTL251 DSIS: N/A MM: MUX0 | |


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**Table 4-15. GPMC Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| VOUT[1]_R_CR[1]/ CAM_D[1]/ **GPMC_A[7]**/ UART4_CTS/ GP0[24] | AC19 | O | IPD DVDD_C | VOUT[1], CAMERA_I/F, UART4, GP0 PINCNTL170 DSIS: N/A MM: MUX1 | GPMC Address 7 |
| EMAC[0]_MTXD[0]/ EMAC[1]_RGRXD[3]/ **GPMC_A[7]**/ SPI[2]_D[0] | J24 | O | IPD DVDD_GPMC | EMAC[0], EMAC[1], SPI[2] PINCNTL250 DSIS: N/A MM: MUX0 | |
| VOUT[1]_G_Y_YC[0]/ CAM_D[2]/ **GPMC_A[6]**/ UART4_TXD/ GP0[23] | AC18 | O | IPD DVDD_C | VOUT[1], CAMERA_I/F, UART4, GP0 PINCNTL169 DSIS: N/A MM: MUX1 | GPMC Address 6 |
| EMAC[0]_GMTCLK/ EMAC[1]_RGRXC/ **GPMC_A[6]**/ SPI[2]_D[1] | K23 | O | IPD DVDD_GPMC | EMAC[0], EMAC[1], SPI[2] PINCNTL249 DSIS: N/A MM: MUX0 | |
| VOUT[1]_G_Y_YC[1]/ CAM_D[3]/ **GPMC_A[5]**/ UART4_RXD/ GP0[22] | AD18 | O | IPU DVDD_C | VOUT[1], CAMERA_I/F, UART4, GP0 PINCNTL168 DSIS: N/A MM: MUX1 | GPMC Address 5 |
| EMAC[0]_MRXDV/ EMAC[1]_RGRXD[1]/ **GPMC_A[5]**/ SPI[2]_SCLK | K22 | O | IPD DVDD_GPMC | EMAC[0], EMAC[1], SPI[2] PINCNTL248 DSIS: N/A MM: MUX0 | |
| SD2_DAT[0]/ **GPMC_A[4]**/ GP1[14] | L26 | O | IPU DVDD_GPMCB | SD2, GP1 PINCNTL120 DSIS: N/A MM: MUX1 | GPMC Address 4 |
| EMAC[0]_MRXD[7]/ EMAC[0]_RGTXD[1]/ **GPMC_A[4]**/ SPI[2]_SCS[3] | G27 | O | IPD DVDD_GPMC | EMAC[0], SPI[2] PINCNTL247 DSIS: N/A MM: MUX0 | |
| SD2_DAT[1]_ $\overline{\text{SDIRQ}}$/ **GPMC_A[3]**/ GP1[13] | M24 | O | IPU DVDD_GPMC | SD2, GP1 PINCNTL119 DSIS: N/A MM: MUX1 | GPMC Address 3 |
| EMAC[0]_MRXD[6]/ EMAC[0]_RGTXD[2]/ **GPMC_A[3]**/ UART5_RTS | F28 | O | IPD DVDD_GPMC | EMAC[0], UART5 PINCNTL246 DSIS: N/A MM: MUX0 | |
| SD2_DAT[2]_SD$\overline{\text{RW}}$/ **GPMC_A[2]**/ GP2[6] | K27 | O | IPU DVDD_GPMC | SD2, GP2 PINCNTL118 DSIS: N/A MM: MUX1 | GPMC Address 2 |
| EMAC[0]_MRXD[5]/ EMAC[0]_RGTXD[3]/ **GPMC_A[2]**/ UART5_CTS | H26 | O | IPD DVDD_GPMC | EMAC[0], UART5 PINCNTL245 DSIS: N/A MM: MUX0 | |

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**Table 4-15. GPMC Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| SD2_DAT[3]/ **GPMC_A[1]**/ GP2[5] | J28 | O | IPU DVDD_GPMC | SD2, GP2 PINCNTL117 DSIS: N/A MM: MUX1 | GPMC Address 1 |
| EMAC[0]_MRXD[4]/ EMAC[0]_RGRXD[3]/ **GPMC_A[1]**/ UART5_TXD | T23 | O | IPD DVDD_GPMC | EMAC[0], UART5 PINCNTL244 DSIS: N/A MM: MUX0 | |
| VOUT[1]_B_CB_C[2]/ **GPMC_A[0]**/ HDMI_CEC/ SPI[2]_D[0]/ GP3[30] | AF28 | O | IPU DVDD | VOUT[1], HDMI, SPI[2], GP3 PINCNTL231 DSIS: N/A MM: MUX1 | GPMC Address 0 |
| EMAC[0]_MRXD[3]/ EMAC[1]_RGRXCTL/ GPMC_A[27]/ GPMC_A[26]/ **GPMC_A[0]**/ UART5_RXD | J25 | O | IPD DVDD_GPMC | EMAC[0], EMAC[1], GPMC, UART5 PINCNTL243 DSIS: N/A MM: MUX0 | |


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**Table 4-15. GPMC Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **GPMC_D[15]**/ BTMODE[15] | Y25 | I/O | DIS DVDD_GPMCB | BTMODE PINCNTL104 DSIS: PIN | GPMC Multiplexed Data/Address I/Os. |
| **GPMC_D[14]**/ BTMODE[14] | V24 | I/O | DIS DVDD_GPMCB | BTMODE PINCNTL103 DSIS: PIN | |
| **GPMC_D[13]**/ BTMODE[13] | U23 | I/O | DIS DVDD_GPMCB | BTMODE PINCNTL102 DSIS: PIN | |
| **GPMC_D[12]**/ BTMODE[12] | U24 | I/O | DIS DVDD_GPMCB | BTMODE PINCNTL101 DSIS: PIN | |
| **GPMC_D[11]**/ BTMODE[11] | AA27 | I/O | DIS DVDD_GPMCB | BTMODE PINCNTL100 DSIS: PIN | |
| **GPMC_D[10]**/ BTMODE[10] | Y26 | I/O | DIS DVDD_GPMCB | BTMODE PINCNTL99 DSIS: PIN | |
| **GPMC_D[9]**/ BTMODE[9] | AB28 | I/O | DIS DVDD_GPMCB | BTMODE PINCNTL98 DSIS: PIN | |
| **GPMC_D[8]**/ BTMODE[8] | Y27 | I/O | DIS DVDD_GPMCB | BTMODE PINCNTL97 DSIS: PIN | |
| **GPMC_D[7]**/ BTMODE[7] | V25 | I/O | DIS DVDD_GPMCB | BTMODE PINCNTL96 DSIS: PIN | |
| **GPMC_D[6]**/ BTMODE[6] | U25 | I/O | DIS DVDD_GPMCB | BTMODE PINCNTL95 DSIS: PIN | |
| **GPMC_D[5]**/ BTMODE[5] | AA28 | I/O | DIS DVDD_GPMCB | BTMODE PINCNTL94 DSIS: PIN | |
| **GPMC_D[4]**/ BTMODE[4] | V26 | I/O | DIS DVDD_GPMCB | BTMODE PINCNTL93 DSIS: PIN | |
| **GPMC_D[3]**/ BTMODE[3] | W27 | I/O | DIS DVDD_GPMCB | BTMODE PINCNTL92 DSIS: PIN | |
| **GPMC_D[2]**/ BTMODE[2] | V27 | I/O | DIS DVDD_GPMCB | BTMODE PINCNTL91 DSIS: PIN | |
| **GPMC_D[1]**/ BTMODE[1] | Y28 | I/O | DIS DVDD_GPMCB | BTMODE PINCNTL90 DSIS: PIN | |
| **GPMC_D[0]**/ BTMODE[0] | U26 | I/O | DIS+ DVDD_GPMCB | BTMODE PINCNTL89 DSIS: PIN | |

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### 4.2.10 HDMI

**Table 4-16. HDMI Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| HDMI_CLKP | AG18 | O | – VDDA_HDMI_1P8 | – | HDMI Clock Output. When the HDMI PHY is powered down, these pins should be left unconnected. |
| HDMI_CLKN | AH18 | O | – VDDA_HDMI_1P8 | – | |
| HDMI_DN2 | AH21 | O | – VDDA_HDMI_1P8 | – | HDMI Data 2 output. When the HDMI PHY is powered down, these pins should be left unconnected. |
| HDMI_DP2 | AG21 | O | – VDDA_HDMI_1P8 | – | |
| HDMI_DN1 | AH20 | O | – VDDA_HDMI_1P8 | – | HDMI Data 1 output. When the HDMI PHY is powered down, these pins should be left unconnected. |
| HDMI_DP1 | AG20 | O | – VDDA_HDMI_1P8 | – | |
| HDMI_DN0 | AH19 | O | – VDDA_HDMI_1P8 | – | HDMI Data 0 output. When the HDMI PHY is powered down, these pins should be left unconnected. |
| HDMI_DP0 | AG19 | O | – VDDA_HDMI_1P8 | – | |
| VOUT[1]_G_Y_YC[2]/ GPMC_A[13]/ **HDMI_SCL**/ SPI[2]_SCS[2]/ I2C[2]_SCL/ GP3[20] | AF27 | I/O | IPU DVDD | VOUT[1], GPMCSPI[2], I2C[2], GP3 PINCNTL228 DSIS: 1 MM: MUX1 | HDMI I2C Serial Clock Output |
| I2C[1]_SCL/ **HDMI_SCL** | AF24 | I/O | DVDD | I2C[1] PINCNTL78 DSIS: 1 MM: MUX0 | |
| VOUT[1]_R_CR[3]/ GPMC_A[14]/ **HDMI_SDA**/ SPI[2]_SCLK/ I2C[2]_SDA/ GP3[21] | AG28 | I/O | IPU DVDD | VOUT[1], GPMCSPI[2], I2C[2], GP3 PINCNTL229 DSIS: 1 MM: MUX1 | HDMI I2C Serial Data I/O |
| I2C[1]_SDA/ **HDMI_SDA** | AG24 | I/O | DVDD | I2C[1] PINCNTL79 DSIS: 1 MM: MUX0 | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal


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**Table 4-16. HDMI Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| VOUT[1]_B_CB_C[2]/ GPMC_A[0]/ **HDMI_CEC**/ SPI[2]_D[0]/ GP3[30] | AF28 | I/O | IPU DVDD | VOUT[1], GPMC, SPI[2], GP3 PINCNTL231 DSIS: 1 MM: MUX1 | HDMI Consumer Electronics Control I/O |
| GPMC_A[22]/ SPI[2]_D[1]/ **HDMI_CEC**/ TIM4_IO/ GP1[17] | AB27 | I/O | IPU DVDD_GPMC | GPMC, SPI[2], TIMER4, GP1 PINCNTL111 DSIS: 1 MM: MUX0 | |
| VOUT[1]_R_CR[2]/ GPMC_A[15]/ **HDMI_HPDET**/ SPI[2]_D[1]/ GP3[22] | AE27 | I | IPD DVDD | VOUT[1], GPMCSPI[2], GP3 PINCNTL230 DSIS: 0 MM: MUX1 | HDMI Hot Plug Detect Input. Signals the connection / removal of an HDMI cable at the connector. |
| GPMC_A[23]/ SPI[2]_SCLK/ **HDMI_HPDET**/ TIM5_IO/ GP1[18] | AA26 | I | IPD DVDD_GPMC | GPMC, SPI[2], TIMER5, GP1 PINCNTL112 DSIS: 0 MM: MUX0 | |

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### 4.2.11 I2C

**Table 4-17. I2C Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **I2C[0]** | | | | | |
| I2C[0]_SCL | AC4 | I/O | DVDD | – PINCNTL263 | I2C[0] Clock I/O. For proper device operation, this pin ***must*** be pulled up via external resistor. |
| I2C[0]_SDA | AB6 | I/O | DVDD | – PINCNTL264 | I2C[0] Data I/O. For proper device operation, this pin ***must*** be pulled up via external resistor. |
| **I2C[1]** | | | | | |
| **I2C[1]_SCL**/ HDMI_SCL | AF24 | I/O | DVDD | HDMI PINCNTL78 DSIS: 1 | I2C[1] Clock I/O. For proper device operation in I2C mode, this pin ***must*** be pulled up via external resistor. |
| **I2C[1]_SDA**/ HDMI_SDA | AG24 | I/O | DVDD | HDMI PINCNTL79 DSIS: 1 | I2C[1] Data I/O. For proper device operation in I2C mode, this pin ***must*** be pulled up via external resistor. |
| **I2C[2]** | | | | | |
| VIN[0]A_FLD/ VIN[0]B_VSYNC/ UART5_RXD/ **I2C[2]_SCL**/ GP2[1] | AA20 | I/O | IPU DVDD | VIN[0]A, VIN[0]B,UART5, GP2 PINCNTL136 DSIS: 1 MM: MUX3 | I2C[2] Clock I/O. For proper device operation in I2C mode, this pin ***must*** be pulled up via external resistor. |
| VOUT[1]_G_Y_YC[2]/ GPMC_A[13]/ HDMI_SCL/ SPI[2]_SCS[2]/ **I2C[2]_SCL**/ GP3[20] | AF27 | I/O | IPU DVDD | VOUT[1], GPMC, HDMI, SPI[2], GP3 PINCNTL228 DSIS: 1 MM: MUX2 | |
| VIN[0]A_D[16]/ CAM_D[8]/ **I2C[2]_SCL**/ GP0[10] | AA21 | I/O | IPU DVDD_C | VIN[0]A, CAM I/F, GP0 PINCNTL156 DSIS: 1 MM: MUX1 | |
| UART0_DCD/ UART3_RXD/ SPI[0]_SCS[3]/ **I2C[2]_SCL**/ SD1_POW/ GP1[2] | AH4 | I/O | IPU DVDD | UART0, UART3, SPI[0], SD1, GP1 PINCNTL74 DSIS: 1 MM: MUX0 | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and the Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal


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**Table 4-17. I2C Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| EMAC[0]_MTCLK/<br>EMAC[0]_RGRXC/<br>SPI[3]_SCS[3]/<br>**I2C[2]_SDA**/<br>GP3[23] | L24 | I/O | IPD<br>DVDD_GPMC | EMAC[0], SPI[3], GP3<br>PINCNTL235<br>DSIS: 1<br>MM: MUX3 | I2C[2] Data I/O. For proper device operation in I2C mode, this pin ***must*** be pulled up via external resistor. |
| VOUT[1]_R_CR[3]/<br>GPMC_A[14]/<br>HDMI_SDA/<br>SPI[2]_SCLK/<br>**I2C[2]_SDA**/<br>GP3[21] | AG28 | I/O | IPU<br>DVDD | VOUT[1], GPMC, HDMI, SPI[2], GP3<br>PINCNTL229<br>DSIS: 1<br>MM: MUX2 | |
| VIN[0]A_DE/<br>VIN[0]B_HSYNC/<br>UART5_TXD/<br>**I2C[2]_SDA**/<br>GP2[0] | AE21 | I/O | IPU<br>DVDD | VIN[0]A, VIN[0]B, UART5, GP2<br>PINCNTL135<br>DSIS: 1<br>MM: MUX1 | |
| UART0_DSR/<br>UART3_TXD/<br>SPI[0]_SCS[2]/<br>**I2C[2]_SDA**/<br>SD1_SDWP/<br>GP1[3] | AG4 | I/O | IPU<br>DVDD | UART0, UART3, SPI[0], SD1, GP1<br>PINCNTL75<br>DSIS: 1<br>MM: MUX0 | |
| **I2C3** | | | | | |
| VOUT[1]_B_CB_C[8]/<br>EMAC[1]_MRXD[4]/<br>**I2C[3]_SCL**/<br>GP3[5] | AH26 | I/O | IPD<br>DVDD | VOUT[1], EMAC[1], GP3<br>PINCNTL213<br>DSIS: 1<br>MM: MUX3 | I2C3 Clock I/O. For proper device operation in I2C mode, this pin ***must*** be pulled up via external resistor. |
| VIN[0]A_D[18]/<br>CAM_D[10]/<br>EMAC[1]_RMRXD[1]/<br>**I2C[3]_SCL**/<br>GP0[12] | AF20 | I/O | IPU<br>DVDD_C | VIN[0]A, CAM I/F, EMAC[1], GP0<br>PINCNTL158<br>DSIS: 1<br>MM: MUX2 | |
| DCAN0_RX/<br>UART2_RXD/<br>**I2C[3]_SCL**/<br>GP1[1] | AG6 | I/O | IPU<br>DVDD | DCAN0, UART2, GP1<br>PINCNTL69<br>DSIS: 1<br>MM: MUX1 | |
| MCA[0]_AXR[1]/<br>**I2C[3]_SCL** | J1 | I/O | IPU<br>DVDD | MCA[0]<br>PINCNTL22<br>DSIS: 1<br>MM: MUX0 | |
| VOUT[1]_B_CB_C[9]/<br>EMAC[1]_MRXD[5]/<br>**I2C[3]_SDA**/<br>GP3[6] | AA24 | I/O | IPD<br>DVDD | VOUT[1], EMAC[1], GP3<br>PINCNTL214<br>DSIS: 1<br>MM: MUX3 | I2C3 Data I/O. For proper device operation in I2C mode, this pin ***must*** be pulled up via external resistor. |
| VIN[0]A_D[19]/<br>CAM_D[11]/<br>EMAC[1]_RMRXD[0]/<br>**I2C[3]_SDA**/<br>GP0[13] | AF21 | I/O | IPU<br>DVDD_C | VIN[0]A, CAM I/F, EMAC[1], GP0<br>PINCNTL159<br>DSIS: 1<br>MM: MUX2 | |
| DCAN0_TX/<br>UART2_TXD/<br>**I2C[3]_SDA**/<br>GP1[0] | AH6 | I/O | IPU<br>DVDD | DCAN0, UART2, GP1<br>PINCNTL68<br>DSIS: 1<br>MM: MUX1 | |
| MCA[0]_AXR[2]/<br>**I2C[3]_SDA** | L4 | I/O | IPU<br>DVDD | MCA[0]<br>PINCNTL23<br>DSIS: 1<br>MM: MUX0 | |

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### 4.2.12 McASP

**Table 4-18. McASP0 Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **McASP0** | | | | | |
| **MCA[0]_ACLKR**/ MCA[5]_AXR[2] | K2 | I/O | IPD DVDD | MCA[5] PINCNTL19 DSIS: 0 | McASP0 Receive Bit Clock I/O |
| **MCA[0]_AFSR**/ MCA[5]_AXR[3] | K1 | I/O | IPD DVDD | MCA[5] PINCNTL20 DSIS: 0 | McASP0 Receive Frame Sync I/O |
| MCA[0]_ACLKX | R4 | I/O | IPD DVDD | – PINCNTL17 | McASP0 Transmit Bit Clock I/O |
| AUD_CLKIN0/ MCA[0]_AXR[7]/ **MCA[0]_AHCLKX**/ MCA[3]_AHCLKX/ USB1_DRVVBUS | L5 | I/O | IPD DVDD | AUD_CLKIN0, MCA[0], MCA[3], USB1 PINCNTL14 DSIS: PIN | McASP0 Transmit High-Frequency Master Clock I/O |
| MCA[0]_AFSX | L3 | I/O | IPD DVDD | – PINCNTL18 | McASP0 Transmit Frame Sync I/O |
| AUD_CLKIN2/ **MCA[0]_AXR[9]**/ MCA[2]_AHCLKX/ MCA[5]_AHCLKX/ EDMA_EVT2/ TIM3_IO/ GP0[9] | H1 | I/O | IPD DVDD | AUD_CLKIN2, MCA[1], MCA[4], EDMA, TIMER2, GP0 PINCNTL16 DSIS: PIN MM: MUX1 | McASP0 Transmit/Receive Data I/Os |
| **MCA[0]_AXR[9]**/ MCB_CLKX/ MCB_CLKR | M6 | I/O | IPD DVDD | MCB PINCNTL30 DSIS: PIN MM: MUX0 | |
| AUD_CLKIN1/ **MCA[0]_AXR[8]**/ MCA[1]_AHCLKX/ MCA[4]_AHCLKX/ EDMA_EVT3/ TIM2_IO/ GP0[8] | R5 | I/O | IPD DVDD | AUD_CLKIN1, MCA[1], MCA[4], EDMA, TIMER2, GP0 PINCNTL15 DSIS: PIN MM: MUX1 | |
| **MCA[0]_AXR[8]**/ MCB_FSX/ MCB_FSR | L1 | I/O | IPD DVDD | MCB PINCNTL29 DSIS: PIN MM: MUX0 | |
| AUD_CLKIN0/ **MCA[0]_AXR[7]**/ MCA[0]_AHCLKX/ MCA[3]_AHCLKX/ USB1_DRVVBUS | L5 | I/O | IPD DVDD | AUD_CLKIN0, MCA[0], MCA[3], USB1 PINCNTL14 DSIS: PIN MM: MUX1 | |
| **MCA[0]_AXR[7]**/ MCB_DX | L2 | I/O | IPD DVDD | MCB PINCNTL28 DSIS: PIN MM: MUX0 | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull during and after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal


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**Table 4-18. McASP0 Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **MCA[0]_AXR[6]**/ MCB_DR | M4 | I/O | IPD DVDD | MCB PINCNTL27 DSIS: PIN | McASP0 Transmit/Receive Data I/Os |
| **MCA[0]_AXR[5]**/ MCA[1]_AXR[9] | M3 | I/O | IPD DVDD | MCA[1] PINCNTL26 DSIS: PIN | |
| **MCA[0]_AXR[4]**/ MCA[1]_AXR[8] | R6 | I/O | IPD DVDD | MCA[1] PINCNTL25 DSIS: PIN | |
| **MCA[0]_AXR[3]**/ | M5 | I/O | IPD DVDD | PINCNTL24 DSIS: PIN | |
| **MCA[0]_AXR[2]**/ I2C[3]_SDA | L4 | I/O | IPU DVDD | I2C[3] PINCNTL23 DSIS: PIN | |
| **MCA[0]_AXR[1]**/ I2C[3]_SCL | J1 | I/O | IPU DVDD | I2C[3] PINCNTL22 DSIS: PIN | |
| **MCA[0]_AXR[0]** | J2 | I/O | IPD DVDD | PINCNTL21 DSIS: PIN | |

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## Table 4-19. McASP1 Terminal Functions

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **McASP1** | | | | | |
| **MCA[1]_ACLKR**/ MCA[1]_AXR[4] | M1 | I/O | IPD DVDD | MCA[1] PINCNTL33 DSIS: 0 | McASP1 Receive Bit Clock I/O |
| **MCA[1]_AFSR**/ MCA[1]_AXR[5] | M2 | I/O | IPD DVDD | MCA[1] PINCNTL34 DSIS: 0 | McASP1 Receive Frame Sync I/O |
| MCA[1]_ACLKX | U5 | I/O | IPD DVDD | – PINCNTL31 | McASP1 Transmit Bit Clock I/O |
| AUD_CLKIN1/ MCA[0]_AXR[8]/ **MCA[1]_AHCLKX**/ MCA[4]_AHCLKX/ EDMA_EVT3/ TIM2_IO/ GP0[8] | R5 | I/O | IPD DVDD | AUD_CLKIN1, MCA[0], MCA[4], EDMA, TIMER2, GP0 PINCNTL15 DSIS: PIN | McASP1 Transmit High-Frequency Master Clock I/O |
| MCA[1]_AFSX | V3 | I/O | IPD DVDD | – PINCNTL32 | McASP1 Transmit Frame Sync I/O |
| MCA[3]_AXR[3]/ **MCA[1]_AXR[9]**/ | J6 | I/O | IPD DVDD | MCA[3] PINCNTL50 DSIS: PIN MM: MUX1 | McASP1 Transmit/Receive Data I/Os |
| MCA[0]_AXR[5]/ **MCA[1]_AXR[9]** | M3 | I/O | IPD DVDD | MCA[0] PINCNTL26 DSIS: PIN MM: MUX0 | |
| MCA[3]_AXR[2]/ **MCA[1]_AXR[8]**/ GP0[20] | F2 | I/O | IPD DVDD | MCA[3], GP0 PINCNTL49 DSIS: PIN MM: MUX1 | |
| MCA[0]_AXR[4]/ **MCA[1]_AXR[8]** | R6 | I/O | IPD DVDD | MCA[0] PINCNTL25 DSIS: PIN MM: MUX0 | |
| MCA[2]_AXR[3]/ **MCA[1]_AXR[7]**/ TIM3_IO/ GP0[15] | H2 | I/O | IPD DVDD | MCA[2], TIMER3, GP0 PINCNTL44 DSIS: PIN | |
| MCA[2]_AXR[2]/ **MCA[1]_AXR[6]**/ TIM2_IO/ GP0[14] | V5 | I/O | IPD DVDD | MCA[2], TIMER2, GP0 PINCNTL43 DSIS: PIN | |
| MCA[1]_AFSR/ **MCA[1]_AXR[5]** | M2 | I/O | IPD DVDD | MCA[1] PINCNTL34 DSIS: PIN | |
| MCA[1]_ACLKR/ **MCA[1]_AXR[4]** | M1 | I/O | IPD DVDD | MCA[1] PINCNTL33 DSIS: PIN | |
| **MCA[1]_AXR[3]**/ MCB_CLKR | N6 | I/O | IPD DVDD | MCB PINCNTL38 DSIS: PIN | |
| **MCA[1]_AXR[2]**/ MCB_FSR | R3 | I/O | IPD DVDD | MCB PINCNTL37 DSIS: PIN | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull during and after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal


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**Table 4-19. McASP1 Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **MCA[1]_AXR[1]**/ SD0_DAT[5]/ | T6 | I/O | IPU DVDD | SD0 PINCNTL36 DSIS: PIN | McASP1 Transmit/Receive Data I/Os |
| **MCA[1]_AXR[0]**/ SD0_DAT[4]/ | V4 | I/O | IPU DVDD | SD0 PINCNTL35 DSIS: PIN | |

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**Table 4-20. McASP2 Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **McASP2** | | | | | |
| **MCA[2]_ACLKX**/ GP0[10] | U6 | I/O | IPU DVDD | GP0 PINCNTL39 DSIS: 0 | McASP2 Transmit Bit Clock I/O |
| AUD_CLKIN2/ MCA[0]_AXR[9]/ **MCA[2]_AHCLKX**/ MCA[5]_AHCLKX/ EDMA_EVT2/ TIM3_IO/ GP0[9] | H1 | I/O | IPD DVDD | AUD_CLKIN2, MCA[0], MCA[5], EDMA, TIMER3, GP0 PINCNTL16 DSIS: PIN | McASP2 Transmit High-Frequency Master Clock I/O |
| **MCA[2]_AFSX**/ GP0[11] | AA5 | I/O | IPU DVDD | GP0 PINCNTL40 DSIS: 0 | McASP2 Transmit Frame Sync I/O |
| **MCA[2]_AXR[3]**/ MCA[1]_AXR[7]/ TIM3_IO/ GP0[15] | H2 | I/O | IPD DVDD | MCA[1], TIMER3, GP0 PINCNTL44 DSIS: PIN | McASP2 Transmit/Receive Data I/Os |
| **MCA[2]_AXR[2]**/ MCA[1]_AXR[6]/ TIM2_IO/ GP0[14] | V5 | I/O | IPD DVDD | MCA[1], TIMER2, GP0 PINCNTL43 DSIS: PIN | |
| **MCA[2]_AXR[1]**/ SD0_DAT[7]/ UART5_TXD/ GP0[13] | V6 | I/O | IPU DVDD | SD0, UART5, GP0 PINCNTL42 DSIS: PIN | |
| **MCA[2]_AXR[0]**/ SD0_DAT[6]/ UART5_RXD/ GP0[12] | N2 | I/O | IPU DVDD | SD0, UART5, GP0 PINCNTL41 DSIS: PIN | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull during and after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17,*Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal


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**Table 4-21. McASP3 Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **McASP3** | | | | | |
| **MCA[3]_ACLKX**/ GP0[16] | G6 | I/O | IPD DVDD | GP0 PINCNTL45 DSIS: 0 | McASP3 Transmit Bit Clock I/O |
| AUD_CLKIN0/ MCA[0]_AXR[7]/ MCA[0]_AHCLKX/ **MCA[3]_AHCLKX**/ USB1_DRVVBUS | L5 | I/O | IPD DVDD | AUD_CLKIN0, MCA[0], USB1 PINCNTL14 DSIS: PIN | McASP3 Transmit High-Frequency Master Clock I/O |
| **MCA[3]_AFSX**/ GP0[17] | H4 | I/O | IPD DVDD | GP0 PINCNTL46 DSIS: 0 | McASP3 Transmit Frame Sync I/O |
| **MCA[3]_AXR[3]**/ MCA[1]_AXR[9]/ | J6 | I/O | IPD DVDD | MCA[1] PINCNTL50 DSIS: PIN | McASP3 Transmit/Receive Data I/Os |
| **MCA[3]_AXR[2]**/ MCA[1]_AXR[8]/ GP0[20] | F2 | I/O | IPD DVDD | MCA[1], GP0 PINCNTL49 DSIS: PIN | |
| **MCA[3]_AXR[1]**/ TIM5_IO/ GP0[19] | G2 | I/O | IPD DVDD | TIMER5, GP0 PINCNTL48 DSIS: PIN | |
| **MCA[3]_AXR[0]**/ TIM4_IO/ GP0[18] | G1 | I/O | IPD DVDD | TIMER4, GP0 PINCNTL47 DSIS: PIN | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull before after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal

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**Table 4-22. McASP4 Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **McASP4** | | | | | |
| **MCA[4]_ACLKX**/ GP0[21] | K7 | I/O | IPD DVDD | GP0 PINCNTL51 DSIS: 0 | McASP4 Transmit Bit Clock I/O |
| AUD_CLKIN1/ MCA[0]_AXR[8]/ MCA[1]_AHCLKX/ **MCA[4]_AHCLKX**/ EDMA_EVT3/ TIM2_IO/ GP0[8] | R5 | I/O | IPD DVDD | AUD_CLKIN1, MCA[0], MCA[1], EDMA, TIMER2, GP0 PINCNTL15 DSIS: PIN | McASP4 Transmit High-Frequency Master Clock I/O |
| **MCA[4]_AFSX**/ GP0[22] | H3 | I/O | IPD DVDD | GP0 PINCNTL52 DSIS: 0 | McASP4 Transmit Frame Sync I/O |
| MCA[5]_AXR[1]/ **MCA[4]_AXR[3]**/ TIM7_IO/ GP0[28] | L6 | I/O | IPD DVDD | MCA[5], TIMER7, GP0 PINCNTL58 DSIS: PIN | McASP4 Transmit/Receive Data I/Os |
| MCA[5]_AXR[0]/ **MCA[4]_AXR[2]**/ GP0[27] | L7 | I/O | IPD DVDD | MCA[5], GP0 PINCNTL57 DSIS: PIN | |
| **MCA[4]_AXR[1]**/ TIM6_IO/ GP0[24] | J4 | I/O | IPD DVDD | TIMER6, GP0 PINCNTL54 DSIS: PIN | |
| **MCA[4]_AXR[0]**/ GP0[23] | H6 | I/O | IPD DVDD | GP0 PINCNTL53 DSIS: PIN | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull during and after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal


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**Table 4-23. McASP5 Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **McASP5** | | | | | |
| **MCA[5]_ACLKX**/ GP0[25] | J3 | I/O | IPD DVDD | GP0 PINCNTL55 DSIS: 0 | McASP5 Transmit Bit Clock I/O |
| AUD_CLKIN2/ MCA[0]_AXR[9]/ MCA[2]_AHCLKX/ **MCA[5]_AHCLKX**/ EDMA_EVT2/ TIM3_IO/ GP0[9] | H1 | I/O | IPD DVDD | AUD_CLKIN2, MCA[0], MCA[2], EDMA, TIMER3, GP0 PINCNTL16 DSIS: PIN | McASP5 Transmit High-Frequency Master Clock I/O |
| **MCA[5]_AFSX**/ GP0[26] | H5 | I/O | IPD DVDD | GP0 PINCNTL56 DSIS: 0 | McASP5 Transmit Frame Sync I/O |
| MCA[0]_AFSR/ **MCA[5]_AXR[3]** | K1 | I/O | IPD DVDD | MCA[0] PINCNTL20 DSIS: PIN | McASP5 Transmit/Receive Data I/Os |
| MCA[0]_ACLKR/ **MCA[5]_AXR[2]** | K2 | I/O | IPD DVDD | MCA[0] PINCNTL19 DSIS: PIN | |
| **MCA[5]_AXR[1]**/ MCA[4]_AXR[3]/ TIM7_IO/ GP0[28] | L6 | I/O | IPD DVDD | MCA[4], TIMER7, GP0 PINCNTL58 DSIS: PIN | |
| **MCA[5]_AXR[0]**/ MCA[4]_AXR[2]/ GP0[27] | L7 | I/O | IPD DVDD | MCA[4], GP0 PINCNTL57 DSIS: PIN | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull during and after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal

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### 4.2.13 McBSP

**Table 4-24. McBSP Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **McBSP** | | | | | |
| MCA[0]_AXR[9]/ MCB_CLKX/ **MCB_CLKR** | M6 | I/O | IPD DVDD | MCA[0], MCB PINCNTL30 DSIS: PIN MM: MUX1 | McBSP Receive Clock I/O |
| MCA[1]_AXR[3]/ **MCB_CLKR** | N6 | I/O | IPD DVDD | MCA[1] PINCNTL38 DSIS: PIN MM: MUX0 | |
| MCA[0]_AXR[8]/ MCB_FSX/ **MCB_FSR** | L1 | I/O | IPD DVDD | MCA[0], MCB PINCNTL29 DSIS: PIN MM: MUX1 | McBSP Receive Frame Sync I/O |
| MCA[1]_AXR[2]/ **MCB_FSR** | R3 | I/O | IPD DVDD | MCA[1], MCB PINCNTL37 DSIS: PIN MM: MUX0 | |
| MCA[0]_AXR[6]/ **MCB_DR** | M4 | I/O | IPD DVDD | MCA[0] PINCNTL27 DSIS: PIN | McBSP Receive Data Input |
| MCA[0]_AXR[9]/ **MCB_CLKX**/ MCB_CLKR | M6 | I/O | IPD DVDD | MCA[0], MCB PINCNTL30 DSIS: PIN | McBSP Transmit Clock I/O |
| MCA[0]_AXR[8]/ **MCB_FSX**/ MCB_FSR | L1 | I/O | IPD DVDD | MCA[0], MCB PINCNTL29 DSIS: PIN | McBSP Transmit Frame Sync I/O |
| MCA[0]_AXR[7]/ **MCB_DX** | L2 | I/O | IPD DVDD | MCA[0] PINCNTL28 DSIS: PIN | McBSP Transmit Data Output |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull during and after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal


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### 4.2.14 PCI Express (PCIe)

**Table 4-25. PCI Express (PCIe) Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| PCIE_TXP0 | AD2 | O | _ VDDA_PCIE_1P8 | PCIE Transmit Data Lane 0. When the PCIe SERDES are powered down, these pins should be left unconnected. |
| PCIE_TXN0 | AD1 | O | | |
| PCIE_RXP0 | AC2 | I | _ VDDA_PCIE_1P8 | PCIE Receive Data Lane 0. When the PCIe SERDES are powered down, these pins should be left unconnected. |
| PCIE_RXN0 | AC1 | I | | |
| SERDES_CLKP | AF1 | I | _ SERDES_CLK LDO (internal) | PCIE Serdes Reference Clock Inputs Reference Clock Inputs. When PCI Express is not used, these pins can be left unconnected. |
| SERDES_CLKN | AF2 | I | _ SERDES_CLK LDO (internal) | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal

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### 4.2.15 Reset, Interrupts, and JTAG Interface

**Table 4-26. RESET, Interrupts, and JTAG Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **RESET** | | | | | |
| $\overline{\text{RESET}}$ | J5 | I | IPU DVDD | – PINCNTL260 | Device Reset input |
| $\overline{\text{POR}}$ | F1 | I | – DVDD | – | Power-On Reset input |
| $\overline{\text{RSTOUT_WD_OUT}}$ | K6 | O | DIS DVDD | – PINCNTL262 | Reset output (RSTOUT) or watchdog out (WD_OUT)<br>For more detailed information on $\overline{\text{RSTOUT_WD_OUT}}$ pin behavior, see Section 8.3.14, *$\overline{\text{RSTOUT_WD_OUT}}$ Pin*. |
| **INTERRUPTS** | | | | | |
| $\overline{\text{NMI}}$ | H7 | I | IPU DVDD | – PINCNTL261 | Non-Maskable Interrupt input |
| GP0[31:0] | see Table 4-11 | I/O | see **NOTE** | see Table 4-11 | Interrupt-capable general-purpose I/Os.<br>**NOTE:** All pins are multiplexed with other pin functions. See Table 4-11, GP0 Terminal Functions table for muxing and internal pullup/pulldown/disable details. |
| GP1[31:0] | see Table 4-12 | I/O | see **NOTE** | see Table 4-12 | Interrupt-capable general-purpose I/Os.<br>**NOTE:** All pins are multiplexed with other pin functions. See Table 4-12, GP1 Terminal Functions table for muxing and internal pullup/pulldown/disable details. |
| GP2[31:0] | see Table 4-13 | I/O | see **NOTE** | see Table 4-13 | Interrupt-capable general-purpose I/Os.<br>**NOTE:** All pins are multiplexed with other pin functions. See Table 4-13, GP2 Terminal Functions table for muxing and internal pullup/pulldown/disable details. |
| GP3[31:0] | see Table 4-14 | I/O | see **NOTE** | see Table 4-14 | Interrupt-capable general-purpose I/Os.<br>**NOTE:** All pins are multiplexed with other pin functions. See Table 4-14, GP3 Terminal Functions table for muxing and internal pullup/pulldown/disable details. |
| **JTAG** | | | | | |
| TCLK | W7 | I | IPU DVDD | – | JTAG test clock input |
| RTCK | AD4 | O | IPU/DIS DVDD | – | JTAG return clock output<br>The internal pullup (IPU) is enabled for this pin when the device is in reset and the IPU is disabled (DIS) when reset is released. |
| TDI | Y7 | I | IPU DVDD | – | JTAG test data input |
| TDO | AC5 | O | IPU DVDD | – | JTAG test port data output |
| TMS | AA7 | I | IPU DVDD | – | JTAG test port mode select input. For proper operation, ***do not*** oppose the IPU on this pin. |
| $\overline{\text{TRST}}$ | AA4 | I | IPD DVDD | – | JTAG test port reset input |
| VOUT[0]_R_CR[2]/ **EMU4**/ GP2[26] | AD9 | I/O | IPD DVDD | VOUT[0], GP2 PINCNTL196 DSIS: PIN | Emulator pin 4 |
| VOUT[0]_G_Y_YC[2]/ **EMU3**/ GP2[24] | AH7 | I/O | IPD DVDD | VOUT[0], GP2 PINCNTL188 DSIS: PIN | Emulator pin 3 |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull during and after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal


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**Table 4-26. RESET, Interrupts, and JTAG Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| VOUT[0]_B_CB_C[2]/ **EMU2**/ GP2[22] | AG7 | I/O | IPD DVDD | VOUT[0], GP0 PINCNTL180 DSIS: PIN | Emulator pin 2 |
| EMU1 | AE11 | I/O | IPU DVDD | – | Emulator pin 1 |
| EMU0 | AG8 | I/O | IPU DVDD | – | Emulator pin 0 |

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### 4.2.16 SD Signals (MMC/SD/SDIO)

**Table 4-27. SD0 Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **SD0_CLK**/ GP0[1] | Y6 | O | IPU DVDD_SD | GP0 PINCNTL8 DSIS: 1 | SD0 Clock output |
| **SD0_CMD**/ SD1_CMD/ GP0[2] | N1 | I/O | IPU DVDD_SD | SD1, GP0 PINCNTL9 DSIS: 1 | SD0 Command input/output |
| **SD0_DAT[0]**/ SD1_DAT[4]/ GP0[3] | R7 | I/O | IPU DVDD_SD | SD1, GP0 PINCNTL10 DSIS: PIN | SD0 Data0 I/O. Functions as data bit 0 for 4-/8-bit SD mode and single data bit for 1-bit SD mode. |
| **SD0_DAT[1]_$\overline{\text{SDIRQ}}$**/ SD1_DAT[5]/ GP0[4] | Y5 | I/O | IPU DVDD_SD | SD1, GP0 PINCNTL11 DSIS: PIN | SD0 Data1 I/O. Functions as data bit 1 for 4-/8-bit SD mode and as an IRQ input for 1-bit SD mode. |
| **SD0_DAT[2]_SDR$\overline{\text{W}}$**/ SD1_DAT[6]/ GP0[5] | Y3 | I/O | IPU DVDD_SD | SD1, GP0 PINCNTL12 DSIS: PIN | SD0 Data2 I/O. Functions as data bit 2 for 4-/8-bit SD mode and as a Read Wait input for 1-bit SD mode. |
| **SD0_DAT[3]**/ SD1_DAT[7]/ GP0[6] | Y4 | I/O | IPU DVDD_SD | SD1, GP0 PINCNTL13 DSIS: PIN | SD0 Data3 I/O. Functions as data bit 3 for 4-/8-bit SD mode. |
| MCA[1]_AXR[0]/ **SD0_DAT[4]**/ | V4 | I/O | IPU DVDD | MCA[1] PINCNTL35 DSIS: PIN | SD0 Data4 I/O. Functions as data bit 4 for 8-bit SD mode. |
| MCA[1]_AXR[1]/ **SD0_DAT[5]**/ | T6 | I/O | IPU DVDD | MCA[1] PINCNTL36 DSIS: PIN | SD0 Data5 I/O. Functions as data bit 5 for 8-bit SD mode. |
| MCA[2]_AXR[0]/ **SD0_DAT[6]**/ UART5_RXD/ GP0[12] | N2 | I/O | IPU DVDD | MCA[2], UART5, GP0 PINCNTL41 DSIS: PIN | SD0 Data6 I/O. Functions as data bit 6 for 8-bit SD mode. |
| MCA[2]_AXR[1]/ **SD0_DAT[7]**/ UART5_TXD/ GP0[13] | V6 | I/O | IPU DVDD | MCA[2], UART5, GP0 PINCNTL42 DSIS: PIN | SD0 Data7 I/O. Functions as data bit 7 for 8-bit SD mode. |
| $\overline{\text{UART0_CTS}}$/ UART4_RXD/ $\overline{\text{DCAN1_TX}}$/ $\overline{\text{SPI[1]_SCS[3]}}$/ **SD0_SDCD** | AE6 | I | IPD DVDD | UART0, UART4, DCAN1, SPI[1] PINCNTL72 DSIS: 1 | SD0 Card Detect input |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal


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**Table 4-28. SD1 Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| SD1_CLK | P3 | O | IPU DVDD_SD | – PINCNTL1 DSIS: N/A | SD1 Clock output |
| SD0_CMD/ **SD1_CMD**/ GP0[2] | N1 | I/O | IPU DVDD_SD | SD0, GP0 PINCNTL9 DSIS: N/A MM: MUX1 | SD1 Command input/output |
| **SD1_CMD**/ GP0[0] | P2 | I/O | IPU DVDD_SD | GP1 PINCNTL2 DSIS: N/A MM: MUX0 | |
| SD1_DAT[0] | P1 | I/O | IPU DVDD_SD | – PINCNTL3 | SD1 Data0 I/O. Functions as data bit 0 for 4-/8-bit SD mode and single data bit for 1-bit SD mode. |
| SD1_DAT[1]_$\overline{\text{SDIRQ}}$ | P5 | I/O | IPU DVDD_SD | – PINCNTL4 | SD1 Data1 I/O. Functions as data bit 1 for 4-/8-bit SD mode and as an IRQ input for 1-bit SD mode. |
| SD1_DAT[2]_SDR$\overline{\text{W}}$ | P4 | I/O | IPU DVDD_SD | – PINCNTL5 | SD1 Data2 I/O. Functions as data bit 2 for 4-/8-bit SD mode and as a Read Wait input for 1-bit SD mode. |
| SD1_DAT[3] | P6 | I/O | IPU DVDD_SD | – PINCNTL6 | SD1 Data3 I/O. Functions as data bit 3 for 4-/8-bit SD mode. |
| SD0_DAT[0]/ **SD1_DAT[4]**/ GP0[3] | R7 | I/O | IPU DVDD_SD | SD0, GP0 PINCNTL10 DSIS: PIN | SD1 Data4 I/O. Functions as data bit 4 for 8-bit SD mode. |
| SD0_DAT[1]_$\overline{\text{SDIRQ}}$/ **SD1_DAT[5]**/ GP0[4] | Y5 | I/O | IPU DVDD_SD | SD0, GP0 PINCNTL11 DSIS: PIN | SD1 Data5 I/O. Functions as data bit 5 for 8-bit SD mode. |
| SD0_DAT[2]_SDR$\overline{\text{W}}$/ **SD1_DAT[6]**/ GP0[5] | Y3 | I/O | IPU DVDD_SD | SD0, GP0 PINCNTL12 DSIS: PIN | SD1 Data6 I/O. Functions as data bit 6 for 8-bit SD mode. |
| SD0_DAT[3]/ **SD1_DAT[7]**/ GP0[6] | Y4 | I/O | IPU DVDD_SD | SD0, GP0 PINCNTL13 DSIS: PIN | SD1 Data7 I/O. Functions as data bit 7 for 8-bit SD mode. |
| $\overline{\text{UART0_DCD}}$/ $\overline{\text{UART3_RXD}}$/ $\overline{\text{SPI[0]_SCS[3]}}$/ I2C[2]_SCL/ **SD1_POW**/ GP1[2] | AH4 | O | IPU DVDD | UART0, UART3, SPI[0], I2C[2], GP1 PINCNTL74 DSIS: PIN | SD1 Card Power Enable output |
| $\overline{\text{SPI[0]_SCS[1]}}$/ **SD1_SDCD**/ EDMA_EVT1/ TIM4_IO/ GP1[6] | AE5 | I | IPU DVDD | SPI[0], EDMA, TIM4, GP1 PINCNTL80 DSIS: 1 | SD1 Card Detect input |
| $\overline{\text{UART0_DSR}}$/ $\overline{\text{UART3_TXD}}$/ $\overline{\text{SPI[0]_SCS[2]}}$/ I2C[2]_SDA/ **SD1_SDWP**/ GP1[3] | AG4 | I | IPU DVDD | UART0, UART3, SPI[0], I2C[2], GP1 PINCNTL75 DSIS: 0 | SD1 Card Write Protect input |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal

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**Table 4-29. SD2 Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **SD2_SCLK**/ GP1[15] | M23 | O | IPU DVDD_GPMC | GP1 PINCNTL121 DSIS: N/A | SD2 Clock output |
| $\overline{\text{GPMC_CS[4]}}$/ **SD2_CMD**/ GP1[8] | P25 | I/O | IPU DVDD_GPMC | GPMC, GP1 PINCNTL126 DSIS: N/A | SD2 Command input/output |
| **SD2_DAT[0]**/ GPMC_A[4]/ GP1[14] | L26 | I/O | IPU DVDD_GPMC | GPMC, GP1 PINCNTL120 DSIS: PIN | SD2 Data0 I/O. Functions as data bit 0 for 4-/8-bit SD mode and single data bit for 1-bit SD mode. |
| **SD2_DAT[1]_$\overline{\text{SDIRQ}}$**/ GPMC_A[3]/ GP1[13] | M24 | I/O | IPU DVDD_GPMC | GMPC, GP1 PINCNTL119 DSIS: PIN | SD2 Data1 I/O. Functions as data bit 1 for 4-/8-bit SD mode and as an IRQ input for 1-bit SD mode |
| **SD2_DAT[2]_SDR$\overline{\text{W}}$**/ GPMC_A[2]/ GP2[6] | K27 | I/O | IPU DVDD_GPMC | GPMC, GP2 PINCNTL118 DSIS: PIN | SD2 Data2 I/O. Functions as data bit 2 for 4-/8-bit SD mode and as a Read Wait input for 1-bit SD mode. |
| **SD2_DAT[3]**/ GPMC_A[1]/ GP2[5] | J28 | I/O | IPU DVDD_GPMC | GPMC, GP2 PINCNTL117 DSIS: PIN | SD2 Data3 I/O. Functions as data bit 3 for 4-/8-bit SD mode. |
| **SD2_DAT[4]**/ GPMC_A[27]/ $\overline{\text{GPMC_A[23]}}$/ $\overline{\text{GPMC_CS[7]}}$/ EDMA_EVT0/ TIM7_IO/ GP1[22] | R24 | I/O | IPU DVDD_GPMC | GPMC, EDMA, TIM7, GP1 PINCNTL116 DSIS: PIN | SD2 Data4 I/O. Functions as data bit 4 for 8-bit SD mode. |
| **SD2_DAT[5]**/ GPMC_A[26]/ GPMC_A[22]/ TIM6_IO/ GP1[21] | P22 | I/O | IPU DVDD_GPMC | GPMC, TIM6, GP1 PINCNTL115 DSIS: PIN | SD2 Data5 I/O. Functions as data bit 5 for 8-bit SD mode. |
| **SD2_DAT[6]**/ GPMC_A[25]/ GPMC_A[21]/ UART2_TXD/ GP1[20] | N23 | I/O | IPU DVDD_GPMC | GPMC, UART2, GP1 PINCNTL114 DSIS: PIN | SD2 Data6 I/O. Functions as data bit 6 for 8-bit SD mode. |
| **SD2_DAT[7]**/ GPMC_A[24]/ GPMC_A[20]/ UART2_RXD/ GP1[19] | L25 | I/O | IPU DVDD_GPMC | GPMC, UART2, GP1 PINCNTL113 DSIS: PIN | SD2 Data7 I/O. Functions as data bit 7 for 8-bit SD mode. |
| $\overline{\text{UART0_RTS}}$/ UART4_TXD/ $\overline{\text{DCAN1_RX}}$/ $\overline{\text{SPI[1]_SCS[2]}}$/ **SD2_SDCD** | AF5 | I | IPD DVDD | UART0, UART4, DCAN1, SPI[1] PINCNTL73 DSIS: 1 | SD2 Card Detect input. |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull during and after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal


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### 4.2.17 SPI

**Table 4-30. SPI 0 Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| SPI[0]_SCLK | AC7 | I/O | IPU DVDD | – PINCNTL82 | SPI Clock I/O |
| UART0_DCD/ UART3_RXD/ **SPI[0]_SCS[3]**/ I2C[2]_SCL/ SD1_POW/ GP1[2] | AH4 | I/O | IPU DVDD | UART0, UART3, I2C[2], SD1, GP1 PINCNTL74 DSIS: PIN | SPI Chip Select I/O |
| UART0_DSR/ UART3_TXD/ **SPI[0]_SCS[2]**/ I2C[2]_SDA/ SD1_SDWP/ GP1[3] | AG4 | I/O | IPU DVDD | UART0, UART3, I2C[2], SD1, GP1 PINCNTL75 DSIS: PIN | |
| **SPI[0]_SCS[1]**/ SD1_SDCD/ EDMA_EVT1/ TIM4_IO/ GP1[6] | AE5 | I/O | IPU DVDD | SD1, EDMA, TIMER4, GP1 PINCNTL80 DSIS: PIN | |
| **SPI[0]_SCS[0]** | AD6 | I/O | IPU DVDD | – PINCNTL81 | |
| SPI[0]_D[1] | AF3 | I/O | IPU DVDD | – PINCNTL83 | SPI Data I/O. Can be configured as either MISO or MOSI |
| SPI[0]_D[0] | AE3 | I/O | IPU DVDD | – PINCNTL84 | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull during and after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal

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**Table 4-31. SPI 1 Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **SPI[1]_SCLK**/ GP1[17] | AC3 | I/O | IPU DVDD | GP1 PINCNTL86 DSIS: PIN | SPI Clock I/O |
| $\overline{\text{UART0_CTS}}$/ UART4_RXD/ DCAN1_TX/ $\overline{\textbf{SPI[1]_SCS[3]}}$/ SD0_SDCD | AE6 | I/O | IPU DVDD | UART0, UART4, DCAN1, SD0 PINCNTL72 DSIS: PIN | SPI Chip Select I/O |
| $\overline{\text{UART0_RTS}}$/ UART4_TXD/ DCAN1_RX/ $\overline{\textbf{SPI[1]_SCS[2]}}$/ SD2_SDCD | AF5 | I/O | IPU DVDD | UART0, UART4, DCAN1, SD2 PINCNTL73 DSIS: PIN | |
| DEVOSC_WAKE/ $\overline{\textbf{SPI[1]_SCS[1]}}$/ TIM5_IO/ GP1[7] | W6 | I/O | IPU DVDD_SD | DEVOSC, TIMER5, GP1 PINCNTL7 DSIS: PIN | |
| $\overline{\textbf{SPI[1]_SCS[0]}}$/ GP1[16] | AD3 | I/O | IPU DVDD | GP1 PINCNTL85 DSIS: PIN | |
| **SPI[1]_D[1]**/ GP1[18] | AA3 | I/O | IPU DVDD | GP1 PINCNTL87 DSIS: PIN | SPI Data I/O. Can be configured as either MISO or MOSI |
| **SPI[1]_D[0]**/ GP1[26] | AA6 | I/O | IPU DVDD | GP1 PINCNTL88 DSIS: PIN | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull during and after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal


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**Table 4-32. SPI 2 Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| EMAC[0]_MRXDV/ EMAC[1]_RGRXD[1]/ GPMC_A[5]/ **SPI[2]_SCLK** | K22 | I/O | IPD DVDD_GPMC | EMAC[0], EMAC[1], GPMC PINCNTL248 DSIS: 1 MM: MUX2 | SPI Clock I/O |
| VOUT[1]_R_CR[3]/ GPMC_A[14]/ HDMI_SDA/ **SPI[2]_SCLK**/ I2C[2]_SDA/ GP3[21] | AG28 | I/O | IPU DVDD | VOUT[1], GPMC, HDMI, I2C[2], GP3 PINCNTL229 DSIS: 1 MM: MUX1 | |
| GPMC_A[23]/ **SPI[2]_SCLK**/ HDMI_HPDET/ TIM5_IO/ GP1[18] | AA26 | I/O | IPD DVDD_GPMC | GPMC, HDMI, TIMER5, GP1 PINCNTL112 DSIS: 1 MM: MUX0 | |
| EMAC[0]_MRXD[7]/ EMAC[0]_RGTXD[1]/ GPMC_A[4]/ **SPI[2]_SCS[3]**/ | G27 | I/O | IPD DVDD_GPMC | EMAC[0], GPMC PINCNTL247 DSIS: 1 | SPI Chip Select I/O |
| VOUT[1]_G_Y_YC[2]/ GPMC_A[13]/ HDMI_SCL/ **SPI[2]_SCS[2]**/ I2C[2]_SCL/ GP3[20] | AF27 | I/O | IPU DVDD | VOUT[1], HDMI, I2C[2], GP3 PINCNTL228 DSIS: 1 | |
| GPMC_A[20]/ **SPI[2]_SCS[1]**/ GP1[15] | AD28 | I/O | IPU DVDD_GPMC | GPMC, GP1 PINCNTL109 DSIS: 1 | |
| GPMC_CS[3]/ **SPI[2]_SCS[0]**/ GP1[26] | P26 | I/O | IPU DVDD_GPMC | GPMC, GP1 PINCNTL125 DSIS: 1 | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull during and after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal

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**Table 4-32. SPI 2 Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| EMAC[0]_GMTCLK/ EMAC[1]_RGRXC/ GPMC_A[6]/ **SPI[2]_D[1]** | K23 | I/O | IPD DVDD_GPMC | EMAC[0], EMAC[1], GPMC PINCNTL249 DSIS: PIN MM: MUX2 | SPI Data I/O. Can be configured as either MISO or MOSI |
| VOUT[1]_R_CR[2]/ GPMC_A[15]/ HDMI_HPDET/ **SPI[2]_D[1]**/ GP3[22] | AE27 | I/O | IPD DVDD | VOUT[1], GPMC, HDMI, GP3 PINCNTL230 DSIS: PIN MM: MUX1 | |
| GPMC_A[22]/ **SPI[2]_D[1]**/ HDMI_CEC/ TIM4_IO/ GP1[17] | AB27 | I/O | IPU DVDD_GPMC | GPMC, HDMI, TIMER 4, GP1 PINCNTL111 DSIS: PIN MM: MUX0 | |
| EMAC[0]_MTXD[0]/ EMAC[1]_RGRXD[3]/ GPMC_A[7]/ **SPI[2]_D[0]** | J24 | I/O | IPD DVDD_GPMC | EMAC[0], EMAC[1], GPMC PINCNTL250 DSIS: PIN MM: MUX2 | |
| VOUT[1]_B_CB_C[2]/ GPMC_A[0]/ HDMI_CEC/ **SPI[2]_D[0]**/ GP3[30] | AF28 | I/O | IPU DVDD | VOUT[1], GPMC, HDMI, GP3 PINCNTL231 DSIS: PIN MM: MUX1 | |
| GPMC_A[21]/ **SPI[2]_D[0]**/ GP1[16] | AC28 | I/O | IPD DVDD_GPMC | GPMC, GP1 PINCNTL110 DSIS: PIN MM: MUX0 | |


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**Table 4-33. SPI 3 Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| VOUT[0]_AVID/ VOUT[0]_FLD/ **SPI[3]_SCLK**/ TIM7_IO/ GP2[21] | AA10 | I/O | IPD DVDD | VOUT[0], TIMER 7, GP2 PINCNTL179 DSIS: 1 MM: MUX2 | SPI Clock I/O |
| VOUT[1]_R_CR[5]/ EMAC[1]_MTXD[4]/ **SPI[3]_SCLK**/ GP3[15] | AC26 | I/O | IPD DVDD | VOUT[0], EMAC[1], GP3 PINCNTL223 DSIS: 1 MM: MUX1 | |
| VIN[0]A_D[21]/ CAM_D[13]/ EMAC[1]_RMTXD[0]/ **SPI[3]_SCLK**/ GP0[15] | AE18 | I/O | IPD DVDD_C | VIN[0]A, CAMERA_I/F, EMAC[1], GP0 PINCNTL161 DSIS: 1 MM: MUX0 | |
| EMAC[0]_MTCLK/ EMAC[0]_RGRXC/ **SPI[3]_SCS[3]**/ I2C[2]_SDA/ GP3[23] | L24 | I/O | IPD DVDD | EMAC[0], I2C[2], GP3 PINCNTL235 DSIS: 1 | SPI Chip Select I/O |
| EMAC[0]_MRCLK/ EMAC[0]_RGTXC/ EMAC[0]_RMCRSDV/ **SPI[3]_SCS[2]**/ GP3[27] | H27 | I/O | IPD DVDD_GPMC | EMAC[0], GP3 PINCNTL239 DSIS: 1 | |
| VOUT[1]_R_CR[4]/ EMAC[1]_MTXD[3]/ **SPI[3]_SCS[1]**/ GP3[14] | AG27 | I/O | IPD DVDD | VOUT[1]. EMAC[1], GP3 PINCNTL222 DSIS: 1 | |
| VIN[0]A_D[20]/ CAM_D[12]/ EMAC[1]_RMCRSDV/ **SPI[3]_SCS[0]**/ GP0[14] | AC17 | I/O | IPD DVDD_C | VIN[0]A, CAMERA,_I/F, EMAC[1]_RM, GP0 PINCNTL160 DSIS: 1 | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull during and after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal

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**Table 4-33. SPI 3 Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| VOUT[1]_HSYNC/ EMAC[1]_MCOL/ **SPI[3]_D[1]**/ UART3_RTS/ GP2[29] | AC24 | I/O | IPD DVDD | VOUT[1], EMAC[1], UART3, GP2 PINCNTL205 DSIS: PIN MM: MUX2 | SPI Data I/O. Can be configured as either MISO or MOSI |
| VOUT[1]_R_CR[6]/ EMAC[1]_MTXD[5]/ **SPI[3]_D[1]**/ GP3[16] | AA25 | I/O | IPD DVDD | VOUT[1], EMAC[1], GP3 PINCNTL224 DSIS: PIN MM: MUX1 | |
| VIN[0]A_D[22]/ CAM_D[14]/ EMAC[1]_RMTXD[1]/ **SPI[3]_D[1]**/ GP0[16] | AC21 | I/O | IPD DVDD_C | VIN[0]A, CAMERA_I/F, EMAC[1]_RM, GP0 PINCNTL162 DSIS: PIN MM: MUX0 | |
| VOUT[1]_VSYNC/ EMAC[1]_MCRS/ **SPI[3]_D[0]**/ UART3_CTS/ GP2[30] | AA23 | I/O | IPD DVDD | VOUT[1], EMAC[1], UART3, GP2 PINCNTL206 DSIS: PIN MM: MUX2 | |
| VOUT[1]_R_CR[7]/ EMAC[1]_MTXD[6]/ **SPI[3]_D[0]**/ GP3[17] | V22 | I/O | IPD DVDD | VOUT[1], EMAC[1], GP3 PINCNTL225 DSIS: PIN MM: MUX1 | |
| VIN[0]A_D[23]/ CAM_D[15]/ EMAC[1]_RMTXEN/ **SPI[3]_D[0]**/ GP0[17] | AC16 | I/O | IPD DVDD_C | VIN[0]A, CAMERA_I/F, EMAC[1], GP0 PINCNTL163 DSIS: PIN MM: MUX0 | |


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### 4.2.18 Oscillator/PLL, Audio Reference Clocks, and Clock Generator

**Table 4-34. Oscillator/PLL, Audio Reference Clocks, and Clock Generator Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **CLOCK GENERATOR** | | | | | |
| VIN[0]A_D[12]_BD[4]/ **CLKOUT1**/ GP2[17] | AG17 | I/O | IPD DVDD | VIN[0]A, GP2 PINCNTL152 DSIS: PIN | Device Clock output 1. Can be used as a system clock for other devices. |
| GPMC_CLK/ GPMC_CS[5]/ GPMC_WAIT[1]/ **CLKOUT1**/ EDMA_EVT3/ TIM4_IO/ GP1[27] | R26 | O | IPU DVDD_GPMC | GPMC, EDMA, TIM4, GP1 PINCNTL127 DSIS: N/A | |
| VIN[0]B_CLK/ **CLKOUT0**/ GP1[9] | AE17 | I/O | IPD DVDD | VIN[0]B, GP1 PINCNTL134 DSIS: PIN | Device Clock output 0. Can be used as a system clock for other devices. |
| CLKIN32/ **CLKOUT0**/ TIM3_IO/ GP3[31] | J7 | O | IPD DVDD | CLKIN32, TIM3, GP3 PINCNTL259 DSIS: N/A | |
| **OSCILLATOR/PLL** | | | | | |
| DEVOSC_MXI/ DEV_CLKIN | AH2 | A I | – VDDA_1P8 | – | Device Crystal input. Crystal connection to internal oscillator for system clock. Functions as DEV_CLKIN clock input when an ***external*** oscillator is used. |
| DEVOSC_MXO | AH3 | A O | – VDDA_1P8 | – | Device Crystal output. Crystal connection to internal oscillator for system clock. When device oscillator is BYPASSED, leave this pin unconnected. |
| VSSA_DEVOSC | AG3 | GND | | | Supply Ground for DEV Oscillator. If the internal oscillator is bypassed, DEVOSC_VSS should be connected to ground (VSS). |
| AUXOSC_MXI/ AUX_CLKIN | R1 | A I | – VDDA_1P8 | – | Auxiliary Crystal input [Optional Audio/Video Reference Crystal Input]. Crystal connection to internal oscillator for auxiliary clock. Functions as AUX_CLKIN clock input when an external oscillator is used. |
| AUXOSC_MXO | T1 | A O | – VDDA_1P8 | – | Auxiliary Crystal output [Optional Audio/Video Reference Crystal Output]. When auxiliary oscillator is BYPASSED, leave this pin unconnected. |
| VSSA_AUXOSC | R2 | GND | | | Supply Ground for AUX Oscillator. If the internal oscillator is bypassed, AUXOSC_VSS should be connected to ground (VSS). |
| **CLKIN32**/ CLKOUT0/ TIM3_IO/ GP3[31] | J7 | I | IPD DVDD | CLKOUT0, TIMER 3, GP3 PINCNTL259 DSIS: PIN | RTC Clock input. Optional 32.768 KHz clock for RTC reference. |
| **DEVOSC_WAKE**/ SPI[1]_SCS[1]/ TIM5_IO/ GP1[7] | W6 | I | IPU DVDD_SD | SPI[1], TIMER 5, GP1 PINCNTL7 DSIS: 1 | Oscillator Wake-up input. |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull during and after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal

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**Table 4-34. Oscillator/PLL, Audio Reference Clocks, and Clock Generator Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **AUDIO REFERENCE CLOCKS** | | | | | |
| **AUD_CLKIN2**/ MCA[0]_AXR[9]/ MCA[2]_AHCLKX/ MCA[5]_AHCLKX/ EDMA_EVT2/ TIM3_IO/ GP0[9] | H1 | I | IPD DVDD | MCA[0], MCA[2], MCA[5], EDMA, TIMER 3, GP0 PINCNTL16 DSIS: PIN | Audio Reference Clock 2 for Audio Peripherals. |
| **AUD_CLKIN1**/ MCA[0]_AXR[8]/ MCA[1]_AHCLKX/ MCA[4]_AHCLKX/ EDMA_EVT3/ TIM2_IO/ GP0[8] | R5 | I | IPD DVDD | MCA[0], MCA[1], MCA[4], EDMA, TIMER 2, GP0 PINCNTL15 DSIS: PIN | Audio Reference Clock 1 for Audio Peripherals. |
| **AUD_CLKIN0**/ MCA[0]_AXR[7]/ MCA[0]_AHCLKX/ MCA[3]_AHCLKX/USB1_DRVVBUS | L5 | I | IPD DVDD | MCA[0], MCA[3], USB1 PINCNTL14 DSIS: PIN | Audio Reference Clock 0 for Audio Peripherals. |


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### 4.2.19 Timer

**Table 4-35. Timer Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **Timers 8- and Watchdog Timer 0** | | | | | |
| **Timer 8 Timer1** | | | | | |
| There are no external pins for these timers. | | | | | |
| **Timers TCLKIN** | | | | | |
| **TCLKIN**/ GP0[30] | T2 | I | IPD DVDD | GP0 PINCNTL60 DSIS: 0 | Timer external clock input |
| **Timer 7** | | | | | |
| GPMC_$\overline{BE[1]}$/ GPMC_A[24]/ EDMA_EVT1/ **TIM7_IO**/ GP1[30] | V28 | I/O | IPD DVDD_GPMC | GPMC, EDMA, GP1 PINCNTL132 DSIS: PIN MM: MUX3 | Timer 7 capture event input or PWM output |
| SD2_DAT4 GPMC_A[27]/ GPMC_A[23]/ GPMC_CS[7]/ EDMA_EVT0/ **TIM7_IO**/ GP1[22] | R24 | I/O | IPU DVDD_GPMC | SD2, GPMC, EDMA, GP1 PINCNTL116 DSIS: PIN MM: MUX2 | |
| VOUT[0]_AVID/ VOUT[0]_FLD/ SPI[3]_SCLK/ **TIM7_IO**/ GP2[21] | AA10 | I/O | IPD DVDD | VOUT[0], SPI[3], GP2 PINCNTL179 DSIS: PIN MM: MUX1 | |
| MCA[5]_AXR[1]/ MCA[4]_AXR[3]/ **TIM7_IO**/ GP0[28] | L6 | I/O | IPD DVDD | MCA[5], MCA[4], GP0 PINCNTL58 DSIS: PIN MM: MUX0 | |
| **Timer 6** | | | | | |
| GPMC_$\overline{BE[0]}$_CLE/ GPMC_A[25]/ EDMA_EVT2/ **TIM6_IO**/ GP1[29] | U27 | I/O | IPD DVDD_GPMC | GPMC, EDMA, GP1 PINCNTL131 DSIS: PIN MM: MUX3 | Timer 6 capture event input or PWM output |
| SD2_DAT[5]/ GPMC_A[26]/ GPMC_A[22]/ **TIM6_IO**/ GP1[21] | P22 | I/O | IPU DVDD_GPMC | SD2, GPMC, GP1 PINCNTL115 DSIS: PIN MM: MUX2 | |
| VOUT[1]_AVID/ EMAC[1]_MRXER/ UART4_RTS/ **TIM6_IO**/ GP2[31] | Y22 | I/O | IPD DVDD | VOUT[1], EMAC[1], UART4, GP2 PINCNTL207 DSIS: PIN MM: MUX1 | |
| MCA[4]_AXR[1]/ **TIM6_IO**/ GP0[24] | J4 | I/O | IPD DVDD | MCA[4], GP0 PINCNTL54 DSIS: PIN MM: MUX0 | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal

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**Table 4-35. Timer Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **Timer 5** | | | | | |
| GPMC_ADV_ALE/ GPMC_CS[6]/ **TIM5_IO**/ GP1[28] | M26 | I/O | IPU DVDD_GPMC | GPMC, GP1 PINCNTL128 DSIS: PIN MM: MUX3 | Timer 5 capture event input or PWM output |
| GPMC_A[23]/ SPI[2]_SCLK/ HDMI_HPDET/ **TIM5_IO**/ GP1[18] | AA26 | I/O | IPD DVDD_GPMC | GPMC, SPI[2], HDMI, GP1 PINCNTL112 DSIS: PIN MM: MUX2 | |
| DEVOSC_WAKE/ SPI[1]_SCS[1]/ **TIM5_IO**/ GP1[7] | W6 | I/O | IPU DVDD_SD | OSC, SPI[1], GP1 PINCNTL7 DSIS: PIN MM: MUX1 | |
| MCA[3]_AXR[1]/ **TIM5_IO**/ GP0[19] | G2 | I/O | IPD DVDD | MCA[3], GP0 PINCNTL48 DSIS: PIN MM: MUX0 | |
| **Timer 4** | | | | | |
| GPMC_CLK/ GPMC_CS[5]/ GPMC_WAIT[1]/ CLKOUT1/ EDMA_EVT3/ **TIM4_IO**/ GP1[27] | R26 | I/O | IPU DVDD_GPMC | GPMC, CLKOUT1, EDMA, GP1 PINCNTL127 DSIS: PIN MM: MUX3 | Timer 4 capture event input or PWM output |
| GPMC_A[22]/ SPI[2]_D[1]/ HDMI_CEC/ **TIM4_IO**/ GP1[17] | AB27 | I/O | IPU DVDD_GPMC | GPMC, SPI[2], HDMI, GP1 PINCNTL111 DSIS: PIN MM: MUX2 | |
| SPI[0]_SCS[1]/ SD1_SDCD/ EDMA_EVT1/ **TIM4_IO**/ GP1[6] | AE5 | I/O | IPU DVDD | SPI[0], SD1, EDMA, GP1 PINCNTL80 DSIS: PIN MM: MUX1 | |
| MCA[3]_AXR[0]/ **TIM4_IO**/ GP0[18] | G1 | I/O | IPD DVDD | MCA[3], GP0 PINCNTL47 DSIS: PIN MM: MUX0 | |


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**Table 4-35. Timer Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE[1] | OTHER[2] [3] | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **Timer 3** | | | | | |
| CLKIN32/ CLKOUT0/ **TIM3_IO**/ GP3[31] | J7 | I/O | IPD DVDD | CLKIN32, CLKOUT, GP3 PINCNTL259 DSIS: PIN MM: MUX3 | Timer 3 capture event input or PWM output |
| GPMC_A[19]/ **TIM3_IO**/ GP1[14] | AC27 | I/O | IPD DVDD_GPMC | GPMC, GP1 PINCNTL108 DSIS: PIN MM: MUX2 | |
| AUD_CLKIN2/ MCA[0]_AXR[9]/ MCA[2]_AHCLKX/ MCA[5]_AHCLKX/ EDMA_EVT2/ **TIM3_IO**/ GP0[9] | H1 | I/O | IPD DVDD | AUD_CLKIN2, MCA[0], MCA[2]. MCA[5], EDMA, GP0 PINCNTL16 DSIS: PIN MM: MUX1 | |
| MCA[2]_AXR[3]/ MCA[1]_AXR[7]/ **TIM3_IO**/ GP0[15] | H2 | I/O | IPD DVDD | MCA[2], MCA[1], GP0 PINCNTL44 DSIS: PIN MM: MUX0 | |
| **Timer 2** | | | | | |
| EMAC_RMREFCLK/ **TIM2_IO**/ GP1[10] | J27 | I/O | IPD DVDD_GPMC | EMAC, GP1 PINCNTL232 DSIS: PIN MM: MUX3 | Timer 2 capture event input or PWM output |
| GPMC_A[18]/ **TIM2_IO**/ GP0[13] | AE28 | I/O | IPD DVDD_GPMC | GPMC, GP0 PINCNTL107 DSIS: PIN MM: MUX2 | |
| AUD_CLKIN1/ MCA[0]_AXR[8]/ MCA[1]_AHCLKX/ MCA[4]_AHCLKX/ EDMA_EVT3/ **TIM2_IO**/ GP0[8] | R5 | I/O | IPD DVDD | AUD_CLKIN1, MCA[0], MCA[1], MCA[4], EDMA, GP0 PINCNTL15 DSIS: PIN MM: MUX1 | |
| MCA[2]_AXR[2]/ MCA[1]_AXR[6]/ **TIM2_IO**/ GP0[14] | V5 | I/O | IPD DVDD | MCA[2], MCA[1], GP0 PINCNTL43 DSIS: PIN MM: MUX0 | |
| **Watchdog Timer 0** | | | | | |
| $\overline{\text{RSTOUT_WD_OUT}}$ | | O | DIS DVDD | – PINCNTL262 | Watchdog timer 0 event output |

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### 4.2.20 UART

**Table 4-36. UART0 Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **UART0** | | | | | |
| UART0_RXD | AH5 | I | IPU DVDD | – PINCNTL70 DSIS: PIN | UART0 Receive Data Input. Functions as IrDA receive input in IrDA modes and CIR receive input in CIR mode. |
| UART0_TXD | AG5 | O | IPU DVDD | – PINCNTL71 DSIS: PIN | UART0 Transmit Data Output. Functions as CIR transmit output in CIR mode. |
| **UART0_RTS**/ UART4_TXD/ DCAN1_RX/ SPI[1]_SCS[2]/ SD2_SDCD | AF5 | O | IPU DVDD | UART4, DCAN1, SPI[1], SD2 PINCNTL73 DSIS: PIN | UART0 Request to Send Output. Indicates module is ready to receive data. Functions as transmit data output in IrDA modes. |
| **UART0_CTS**/ UART4_RXD/ DCAN1_TX/ SPI[1]_SCS[3]/ SD0_SDCD | AE6 | I/O | IPU DVDD | UART4, DCAN1, SPI[1], SD0 PINCNTL72 DSIS: 1 | UART0 Clear to Send Input. Functions as SD transceiver control output in IrDA and CIR modes. |
| **UART0_DTR**/ UART3_CTS/ UART1_TXD/ GP1[4] | AG2 | O | IPU DVDD | UART3, UART1, GP1 PINCNTL76 DSIS: PIN | UART0 Data Terminal Ready Output |
| **UART0_DSR**/ UART3_TXD/ SPI[0]_SCS[2]/ I2C[2]_SDA/ SD1_SDWP/ GP1[3] | AG4 | I | IPU DVDD | UART3, SPI[0], I2C[2], SD1, GP1 PINCNTL75 DSIS: 1 | UART0 Data Set Ready Input |
| **UART0_DCD**/ UART3_RXD/ SPI[0]_SCS[3]/ I2C[2]_SCL/ SD1_POW/ GP1[2] | AH4 | I | IPU DVDD | UART3, SPI[0], I2C[2], SD1, GP1 PINCNTL74 DSIS: 1 | UART0 Data Carrier Detect Input |
| **UART0_RIN**/ UART3_RTS/ UART1_RXD/ GP1[5] | AF4 | I | IPU DVDD | UART3, UART1, GP1 PINCNTL77 DSIS: 1 | UART0 Ring Indicator Input |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal


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**Table 4-37. UART1 Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **UART1** | | | | | |
| EMAC[0]_MTXD[5]/ EMAC[1]_RGTXC/ EMAC[1]_RMCRSDV/ GPMC_A[12]/ **UART1_RXD** | F27 | I | IPD DVDD_GPMC | EMAC[0], EMAC[1], GPMC PINCNTL255 DSIS: 1 MM: MUX1 | UART1 Receive Data Input. Functions as IrDA receive input in IrDA modes and CIR receive input in CIR mode. |
| UART0_RIN/ UART3_RTS/ **UART1_RXD**/ GP1[5] | AF4 | I | IPU DVDD | UART0, UART3, GP1 PINCNTL77 DSIS: 1 MM: MUX0 | |
| EMAC[0]_MTXD[6]/ EMAC[1]_RGRXD[0]/ EMAC[1]_RMTXD[0]/ GPMC_A[13]/ **UART1_TXD** | J22 | O | IPD DVDD_GPMC | EMAC[0], EMAC[1], GPMC PINCNTL256 DSIS: PIN MM: MUX1 | UART1 Transmit Data Output. Functions as CIR transmit output in CIR mode. |
| UART0_DTR/ UART3_CTS/ **UART1_TXD**/ GP1[4] | AG2 | O | IPU DVDD | UART0, UART3, GP1 PINCNTL76 DSIS: PIN MM: MUX0 | |
| EMAC[0]_MTXEN/ EMAC[1]_RGRXD[2]/ EMAC[1]_RMTXEN/ GPMC_A[15]/ **UART1_RTS** | J23 | O | IPD DVDD_GPMC | EMAC[0], EMAC[1], GPMC PINCNTL258 DSIS: PIN | UART1 Request to Send Output. Indicates module is ready to receive data. Functions as transmit data output in IrDA modes. |
| EMAC[0]_MTXD[7]/ EMAC[1]_RGTXD[3]/ EMAC[1]_RMTXD[1]/ GPMC_A[14]/ **UART1_CTS** | H24 | I/O | IPD DVDD_GPMC | EMCA[0], EMAC[1], GPMC PINCNTL257 DSIS: 1 | UART1 Clear to Send Input. Functions as SD transceiver control output in IrDA and CIR modes. |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal

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**Table 4-38. UART2 Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **UART2** | | | | | |
| SD2_DAT[7]/ GPMC_A[24]/ GPMC_A[20]/ **UART2_RXD**/ GP1[19] | L25 | I | IPU DVDD_GPMC | SD2, GPMC, GP1 PINCNTL113 DSIS: 1 MM: MUX3 | UART2 Receive Data Input. Functions as IrDA receive input in IrDA modes and CIR receive input in CIR mode. |
| DCAN0_RX/ **UART2_RXD**/ I2C[3]_SCL/ GP1[1] | AG6 | I | IPU DVDD | DCAN0, I2C[3], GP1 PINCNTL69 DSIS: 1 MM: MUX2 | |
| **UART2_RXD**/ GP0[29] | U4 | I | IPD DVDD | GP0 PINCNTL59 DSIS: 1 MM: MUX1 | |
| VOUT[1]_B_CB_C[1]/ CAM_HS/ GPMC_A[9]/ **UART2_RXD**/ GP0[26] | AE23 | I | IPD DVDD_C | VOUT[1], CAMERA_I/F, GPMC, GP0 PINCNTL172 DSIS: 1 MM: MUX0 | |
| SD2_DAT[6]/ GPMC_A[25]/ GPMC_A[21]/ **UART2_TXD**/ GP1[20] | N23 | O | IPU DVDD_GPMC | SD2, GPMC, GP1 PINCNTL114 DSIS: PIN MM: MUX3 | UART2 Transmit Data Output. Functions as CIR transmit output in CIR mode. |
| DCAN0_TX/ **UART2_TXD**/ I2C[3]_SDA/ GP1[0] | AH6 | O | IPU DVDD | DCAN0, I2C[3], GP1 PINCNTL68 DSIS: PIN MM: MUX2 | |
| **UART2_TXD**/ GP0[31] | U3 | O | IPD DVDD | GP0 PINCNTL61 DSIS: PIN MM: MUX1 | |
| VOUT[1]_B_CB_C[0]/ CAM_VS/ GPMC_A[10]/ **UART2_TXD**/ GP0[27] | AD23 | O | IPU DVDD_C | VOUT[1], CAMERA_I/F, GPMC, GP0 PINCNTL173 DSIS: PIN MM: MUX0 | |
| VOUT[0]_FLD/ CAM_PCLK/ GPMC_A[12]/ **UART2_RTS**/ GP2[2] | AF18 | O | IPD DVDD_C | VOUT[0], CAMERA_I/F, GPMC, GP2 PINCNTL175 DSIS: PIN | UART2 Request to Send Output. Indicates module is ready to receive data. Functions as transmit data output in IrDA modes. |
| VOUT[1]_FLD/ CAM_FLD/ CAM_WE/ GPMC_A[11]/ **UART2_CTS**/ GP0[28] | AB23 | I/O | IPD DVDD_C | VOUT[1], CAMERA_I/F, GPMC, GP0 PINCNTL174 DSIS: 1 | UART2 Clear to Send Input. Functions as SD transceiver control output in IrDA and CIR modes. |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal


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**Table 4-39. UART3 Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **UART3** | | | | | |
| VOUT[1]_B_CB_C[6]/ EMAC[1]_MRXD[2]/ **UART3_RXD**/ GP3[3] | AD25 | I | IPD DVDD | VOUT[1], EMAC[1], GP3 PINCNTL211 DSIS: 1 MM: MUX1 | UART3 Receive Data Input. Functions as IrDA receive input in IrDA modes and CIR receive input in CIR mode. |
| UART0_DCD/ **UART3_RXD**/ SPI[0]_SCS[3]/ I2C[2]_SCL/ SD1_POW/ GP1[2] | AH4 | I | IPU DVDD | UART0, SPI[0], I2C[2], SD1, GP1 PINCNTL74 DSIS: 1 MM: MUX0 | |
| VOUT[1]_B_CB_C[7]/ EMAC[1]_MRXD[3]/ **UART3_TXD**/ GP3[4] | AC25 | O | IPD DVDD | VOUT[1], EMAC[1], GP3 PINCNTL212 DSIS: PIN MM: MUX1 | UART3 Transmit Data Output. Functions as CIR transmit output in CIR mode. |
| UART0_DSR/ **UART3_TXD**/ SPI[0]_SCS[2]/ I2C[2]_SDA/ SD1_SDWP/ GP1[3] | AG4 | O | IPU DVDD | UART0, SPI[0], I2C[2], SD1, GP1 PINCNTL75 DSIS: PIN MM: MUX0 | |
| VOUT[1]_HSYNC/ EMAC[1]_MCOL/ SPI[3]_D[1]/ **UART3_RTS**/ GP2[29] | AC24 | O | IPD DVDD | VOUT[1], EMAC[1], SPI[3], GP2 PINCNTL205 DSIS: PIN MM: MUX1 | UART3 Request to Send Output. Indicates module is ready to receive data. Functions as transmit data output in IrDA modes. |
| UART0_RIN/ **UART3_RTS**/ UART1_RXD/ GP1[5] | AF4 | O | IPU DVDD | UART0, UART1, GP1 PINCNTL77 DSIS: PIN MM: MUX0 | |
| VOUT[1]_VSYNC/ EMAC[1]_MCRS/ SPI[3]_D[0]/ **UART3_CTS**/ GP2[30] | AA23 | I/O | IPD DVDD | VOUT[1], EMAC[1], SPI[3], GP2 PINCNTL206 DSIS: 1 MM: MUX1 | UART3 Clear to Send Input. Functions as SD transceiver control output in IrDA and CIR modes. |
| UART0_DTR/ **UART3_CTS**/ UART1_TXD/ GP1[4] | AG2 | I/O | IPU DVDD | UART3, UART1, GP1 PINCNTL76 DSIS: 1 MM: MUX0 | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal

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**Table 4-40. UART4 Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **UART4** | | | | | |
| UART0_CTS/ **UART4_RXD**/ DCAN1_TX/ SPI[1]_SCS[3]/ SD0_SDCD | AE6 | I | IPU DVDD | UART0, DCAN1, SPI[1], SD0 PINCNTL72 DSIS: 1 MM: MUX3 | UART4 Receive Data Input. Functions as IrDA receive input in IrDA modes and CIR receive input in CIR mode. |
| VOUT[1]_B_CB_C[4]/ EMAC[1]_MRXD[0]/ **UART4_RXD**/ GP3[1] | AG25 | I | IPD DVDD | VOUT[1], EMAC[1], GP3 PINCNTL209 DSIS: 1 MM: MUX2 | |
| EMAC[0]_MTXD[1]/ EMAC[1]_RGTXD[1]/ GPMC_A[8]/ **UART4_RXD** | H25 | I | IPD DVDD_GPMC | EMAC[0], EMAC[1], GPMC PINCNTL251 DSIS: 1 MM: MUX1 | |
| VOUT[1]_G_Y_YC[1]/ CAM_D[3]/ GPMC_A[5]/ **UART4_RXD**/ GP0[22] | AD18 | I | IPU DVDD_C | VOUT[1], CAMERA_I/F, GPMC, GP0 PINCNTL168 DSIS: 1 MM: MUX0 | |
| UART0_RTS/ **UART4_TXD**/ DCAN1_RX/ SPI[1]_SCS[2]/ SD2_SDCD | AF5 | O | IPU DVDD | UART0, DCAN1, SPI[1], SD2 PINCNTL73 DSIS: PIN MM: MUX3 | UART4 Transmit Data Output. Functions as CIR transmit output in CIR mode. |
| VOUT[1]_B_CB_C[5]/ EMAC[1]_MRXD[1]/ **UART4_TXD**/ GP3[2] | AF25 | O | IPD DVDD | VOUT[1], EMAC[1], GP3 PINCNTL210 DSIS: PIN MM: MUX2 | |
| EMAC[0]_MTXD[2]/ EMAC[1]_RGTXCTL/ EMAC[1]_RMRXD[0]/ GPMC_A[9]/ **UART4_TXD** | H22 | O | IPD DVDD_GPMC | EMAC[0], EMAC[1], GPMC PINCNTL252 DSIS: PIN MM: MUX1 | |
| VOUT[1]_G_Y_YC[0]/ CAM_D[2]/ GPMC_A[6]/ **UART4_TXD**/ GP0[23] | AC18 | O | IPD DVDD_C | VOUT[1], CAMERA_I/F, GPMC, GP0 PINCNTL169 DSIS: PIN MM: MUX0 | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal


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**Table 4-40. UART4 Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| VOUT[1]_AVID/ EMAC[1]_MRXER/ **UART4_RTS**/ TIM6_IO/ GP2[31] | Y22 | O | IPD DVDD | VOUT[1], EMAC[1], TIMER6, GP2 PINCNTL207 DSIS: PIN MM: MUX2 | UART4 Request to Send Output. Indicates module is ready to receive data. Functions as transmit data output in IrDA modes. |
| EMAC[0]_MTXD[4]/ EMAC[1]_RGTXD[2]/ EMAC[1]_RMRXER/ GPMC_A[11]/ **UART4_RTS** | G23 | O | IPD DVDD_GPMC | EMAC[0], EMAC[1], GPMC PINCNTL254 DSIS: PIN MM: MUX1 | |
| VOUT[1]_R_CR[0]/ CAM_D[0]/ GPMC_A[8]/ **UART4_RTS**/ GP0[25] | AA22 | O | IPD DVDD_C | VOUT[1], CAMERA_I/F, GPMC, GP0 PINCNTL171 DSIS: PIN MM: MUX0 | |
| VOUT[1]_B_CB_C[3]/ EMAC[1]_MRCLK/ **UART4_CTS**/ GP3[0] | AH25 | I/O | IPD DVDD | VOUT[1], EMAC[1], GP3 PINCNTL208 DSIS: 1 MM: MUX2 | UART4 Clear to Send Input. Functions as SD transceiver control output in IrDA and CIR modes. |
| EMAC[0]_MTXD[3]/ EMAC[1]_RGTXD[0]/ EMAC[1]_RMRXD[1]/ GPMC_A[10]/ **UART4_CTS** | H23 | I/O | IPD DVDD_GPMC | EMAC[0], EMAC[1], GPMC PINCNTL253 DSIS: 1 MM: MUX1 | |
| VOUT[1]_R_CR[1]/ CAM_D[1]/ GPMC_A[7]/ **UART4_CTS**/ GP0[24] | AC19 | I/O | IPD DVDD_C | VOUT[1], CAMERA_I/F, GPMC, GP0 PINCNTL170 DSIS: 1 MM: MUX0 | |

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**Table 4-41. UART5 Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **UART5** | | | | | |
| MCA[2]_AXR[0]/ SD0_DAT[6]/ **UART5_RXD**/ GP0[12] | N2 | I | IPU DVDD | MCA[2], SD0, GP0 PINCNTL41 DSIS: 1 MM: MUX3 | UART5 Receive Data Input. Functions as IrDA receive input in IrDA modes and CIR receive input in CIR mode. |
| VOUT[1]_R_CR[8]/ EMAC[1]_MTXD[7]/ **UART5_RXD**/ GP3[18] | W23 | I | IPD DVDD | VOUT[1], EMAC[1], GP3 PINCNTL226 DSIS: 1 MM: MUX2 | |
| VIN[0]A_FLD/ VIN[0]B_VSYNC/ **UART5_RXD**/ I2C[2]_SCL/ GP2[1] | AA20 | I | IPU DVDD | VIN[0]A, I2C[2], GP2 PINCNTL136 DSIS: 1 MM: MUX1 | |
| EMAC[0]_MRXD[3]/ EMAC[1]_RGRXCTL / GPMC_A[27]/ GPMC_A[26]/ GPMC_A[0]/ **UART5_RXD** | J25 | I | IPD DVDD_GPMC | EMAC[0], EMAC[1], GPMC PINCNTL243 DSIS: 1 MM: MUX0 | |
| MCA[2]_AXR[1]/ SD0_DAT[7]/ **UART5_TXD**/ GP0[13] | V6 | O | IPU DVDD | MCA[2], SD0, GP0 PINCNTL42 DSIS: PIN MM: MUX3 | UART5 Transmit Data Output. Functions as CIR transmit output in CIR mode. |
| VOUT[1]_R_CR[9]/ EMAC[1]_MTXEN/ **UART5_TXD**/ GP3[19] | Y24 | O | IPD DVDD | VOUT[1], EMAC[1], GP3 PINCNTL227 DSIS: PIN MM: MUX2 | |
| VIN[0]A_DE/ VIN[0]B_HSYNC/ **UART5_TXD**/ I2C[2]_SDA/ GP2[0] | AE21 | O | IPU DVDD | VIN[0]A, I2C[2], GP0 PINCNTL135 DSIS: PIN MM: MUX1 | |
| EMAC[0]_MRXD[4]/ EMAC[0]_RGRXD[3] / GPMC_A[1]/ **UART5_TXD** | T23 | O | IPD DVDD_GPMC | EMAC[0], GPMC PINCNTL244 DSIS: PIN MM: MUX0 | |
| VIN[0]A_HSYNC/ **UART5_RTS**/ GP2[3] | AC20 | O | IPU DVDD | VIN[0]A, GP2 PINCNTL138 DSIS: PIN MM: MUX1 | UART5 Request to Send Output. Indicates module is ready to receive data. Functions as transmit data output in IrDA modes. |
| EMAC[0]_MRXD[6]/ EMAC[0]_RGTXD[2] / GPMC_A[3]/ **UART5_RTS** | F28 | O | IPD DVDD_GPMC | EMAC[0], GPMC PINCNTL246 DSIS: PIN MM: MUX0 | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal


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**Table 4-41. UART5 Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| VIN[0]A_VSYNC/ **UART5_CTS**/ GP2[4] | AD20 | I/O | IPU DVDD | VIN[0]A, GP2 PINCNTL139 DSIS: 1 MM: MUX1 | UART5 Clear to Send Input. Functions as SD transceiver control output in IrDA and CIR modes. |
| EMAC[0]_MRXD[5]/ EMAC[0]_RGTXD[3] / GPMC_A[2]/ **UART5_CTS** | H26 | I/O | IPD DVDD_GPMC | EMAC[0], GPMC PINCNTL245 DSIS: 1 MM: MUX0 | |

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### 4.2.21 USB

**Table 4-42. USB Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **USB0** | | | | | |
| USB0_DP | AG11 | A I/O | – VDDA_USB_3P3 | – | USB0 bidirectional data differential signal pair [plus/minus]. |
| USB0_DM | AH11 | A I/O | – VDDA_USB_3P3 | – | When the USB0 PHY is powered down, these pins should be left unconnected. |
| USB0_ID | AG10 | A I | – VDDA_USB_3P3 | – | USB0 OTG identification input.<br>When the USB0 PHY is powered down, this pin should be left unconnected. |
| USB0_CE | AH10 | A O | – VDDA_USB_3P3 | – | USB0 charger enable.<br>When the USB0 PHY is powered down, this pin should be left unconnected. |
| USB0_VBUSIN | AG12 | A I | – VDDA_USB_3P3 | – | 5-V USB0 VBUS comparator input.<br>This analog input pin senses the level of the USB VBUS voltage and should connect directly to the USB VBUS voltage. When the USB0 PHY is powered down, this pin should be left unconnected. |
| **USB0_DRVVBUS**/ GP0[7] | AF11 | O | IPD DVDD | GP0 PINCNTL270 DSIS: N/A | When this pin is used as USB0_DRVVBUS and the USB0 Controller is operating as a Host, this signal is used by the USB0 Controller to enable the external VBUS charge pump.<br>When the USB0 PHY is powered down, this pin should be left unconnected. |
| **USB1** | | | | | |
| USB1_DP | AG13 | A I/O | – VDDA_USB_3P3 | – | USB1 bidirectional data differential signal pair [plus/minus]. |
| USB1_DM | AH13 | A I/O | – VDDA_USB_3P3 | – | When the USB1 PHY is powered down, these pins should be left unconnected. |
| USB1_ID | AH12 | A I | – VDDA_USB_3P3 | – | USB1 OTG identification input.<br>When the USB1 PHY is powered down, this pin should be left unconnected. |
| USB1_CE | AH14 | A O | – VDDA_USB_3P3 | – | USB1 charger enable.<br>When the USB1 PHY is powered down, this pin should be left unconnected. |
| USB1_VBUSIN | AG14 | A I | – VDDA_USB_3P3 | – | 5-V USB1 VBUS comparator input.<br>This analog input pin senses the level of the USB VBUS voltage and should connect directly to the USB VBUS voltage. When the USB1 PHY is powered down, this pin should be left unconnected. |
| AUD_CLKIN0/ MCA[0]_AXR[7]/ MCA[0]_AHCLKX/ MCA[3]_AHCLKX/ **USB1_DRVVBUS** | L5 | O | IPD DVDD | AUD_CLKIN0, MCA[0], MCA[3], PINCNTL14 DSIS: N/A | When this pin is used as USB1_DRVVBUS and the USB1 Controller is operating as a Host, this signal is used by the USB1 Controller to enable the external VBUS charge pump.<br>When the USB1 PHY is powered down, this pin should be left unconnected. |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal


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### 4.2.22 Video Input (Digital)

**Table 4-43. Video Input 0 (Digital) Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **Video Input 0 (Digital)** | | | | | |
| **VIN[0]B_CLK**/ CLKOUT0/ GP1[9] | AE17 | I | IPD DVDD | CLKOUT0, GP1 PINCNTL134 DSIS: 0 | Video Input 0 Port B Clock input. Input clock for 8-bit Port B video capture. This signal is not used in 16-bit and 24-bit capture modes. |
| **VIN[0]A_CLK**/ GP2[2] | AB20 | I | IPD DVDD | GP2 PINCNTL137 DSIS: 0 | Video Input 0 Port A Clock input. Input clock for 8-bit , 16-bit, or 24-bit Port A video capture. |
| **VIN[0]A_D[23]**/ CAM_D[15]/ EMAC[1]_RMTXEN/ SPI[3]_D[0]/ GP0[17] | AC16 | I | IPD DVDD_C | CAM_IF, EMAC[1]_RM, SPI[3], GP0 PINCNTL163 DSIS: PIN | Video Input 0 Data inputs. For 16-bit capture, D[7:0] are Cb/Cr and [15:8] are Y Port A inputs. For 8-bit capture, D[7:0] are Port A YCbCr data inputs and D[15:8] are Port B YCbCr data inputs. For RGB capture, D[23:16] are R, D[15:8] are G, and D[7:0] are B data inputs. |
| **VIN[0]A_D[22]**/ CAM_D[14]/ EMAC[1]_RMTXD[1]/ SPI[3]_D[1]/ GP0[16] | AC21 | I | IPD DVDD_C | CAM_IF, EMAC[1]_RM, SPI[3], GP0 PINCNTL162 DSIS: PIN | |
| **VIN[0]A_D[21]**/ CAM_D[13]/ EMAC[1]_RMTXD[0]/ SPI[3]_SCLK/ GP0[15] | AE18 | I | IPD DVDD_C | CAM_IF, EMAC[1]_RM, SPI[3], GP0 PINCNTL161 DSIS: PIN | |
| **VIN[0]A_D[20]**/ CAM_D[12]/ EMAC[1]_RMCRSDV/ SPI[3]_SCS[0]/ GP0[14] | AC17 | I | IPD DVDD_C | CAM_IF, EMAC[1]_RM, SPI[3], GP0 PINCNTL160 DSIS: PIN | |
| **VIN[0]A_D[19]**/ CAM_D[11]/ EMAC[1]_RMRXD[0]/ I2C[3]_SDA/ GP0[13] | AF21 | I | IPU DVDD_C | CAM_IF, EMAC[1]_RM, I2C[3], GP0 PINCNTL159 DSIS: PIN | |
| **VIN[0]A_D[18]**/ CAM_D[10]/ EMAC[1]_RMRXD[1]/ I2C[3]_SCL/ GP0[12] | AF20 | I | IPU DVDD_C | CAM_IF, EMAC[1]_RM, I2C[3], GP0 PINCNTL158 DSIS: PIN | |
| **VIN[0]A_D[17]**/ CAM_D[9]/ EMAC[1]_RMRXER/ GP0[11] | AB21 | I | IPD DVDD_C | CAM_IF, EMAC[1]_RM, I2C[3], GP0 PINCNTL157 DSIS: PIN | |
| **VIN[0]A_D[16]**/ CAM_D[8]/ I2C[2]_SCL/ GP0[10] | AA21 | I | IPU DVDD_C | CAM_IF, I2C[3], GP0 PINCNTL156 DSIS: PIN | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal.

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**Table 4-43. Video Input 0 (Digital) Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **VIN[0]A_D[15]_BD[7]**/ CAM_SHUTTER/ GP2[20] | AC14 | I | IPD DVDD | CAM_IF, GP2 PINCNTL155 DSIS: PIN | Video Input 0 Data inputs. For 16-bit capture, D[7:0] are Cb/Cr and [15:8] are Y Port A inputs. For 8-bit capture, D[7:0] are Port A YCbCr data inputs and D[15:8] are Port B YCbCr data inputs. For RGB capture, D[23:16] are R, D[15:8] are G, and D[7:0] are B data inputs. |
| **VIN[0]A_D[14]_BD[6]**/ CAM_STROBE/ GP2[19] | AC12 | I | IPD DVDD | CAM_IF, GP2 PINCNTL154 DSIS: PIN | |
| **VIN[0]A_D[13]_BD[5]**/ CAM_RESET/ GP2[18] | AF17 | I | IPD DVDD | CAM_IF, GP2 PINCNTL153 DSIS: PIN | |
| **VIN[0]A_D[12]_BD[4]**/ CLKOUT1/ GP2[17] | AG17 | I | IPD DVDD | CLKOUT1, GP2 PINCNTL152 DSIS: PIN | |
| **VIN[0]A_D[11]_BD[3]**/ CAM_WE/ GP2[16] | AH17 | I | IPD DVDD | CAM_IF, GP2 PINCNTL151 DSIS: PIN | |
| **VIN[0]A_D[10]_BD[2]**/ GP2[15] | AH9 | I | IPD DVDD | GP2 PINCNTL150 DSIS: PIN | |
| **VIN[0]A_D[9]_BD[1]**/ GP2[14] | AG9 | I | IPD DVDD | GP2 PINCNTL149 DSIS: PIN | |
| **VIN[0]A_D[8]_BD[0]**/ GP2[13] | AB15 | I | IPD DVDD | GP2 PINCNTL148 DSIS: PIN | |
| **VIN[0]A_D[7]**/ GP2[12] | AA11 | I | IPD DVDD | GP2 PINCNTL147 DSIS: PIN | Video Input 0 Data inputs. For 16-bit capture, D[7:0] are Cb/Cr and [15:8] are Y Port A inputs. For 8-bit capture, D[7:0] are Port A YCbCr data inputs and D[15:8] are Port B YCbCr data inputs. For RGB capture, D[23:16] are R, D[15:8] are G, and D[7:0] are B data inputs. |
| **VIN[0]A_D[6]**/ GP2[11] | AH16 | I | IPD DVDD | GP2 PINCNTL146 DSIS: PIN | |
| **VIN[0]A_D[5]**/ GP2[10] | AG16 | I | IPD DVDD | GP2 PINCNTL145 DSIS: PIN | |
| **VIN[0]A_D[4]**/ GP2[9] | AH8 | I | IPD DVDD | GP2 PINCNTL144 DSIS: PIN | |
| **VIN[0]A_D[3]**/ GP2[8] | AE12 | I | IPD DVDD | GP2 PINCNTL143 DSIS: PIN | |
| **VIN[0]A_D[2]**/ GP2[7] | AC9 | I | IPD DVDD | GP2 PINCNTL142 DSIS: PIN | |
| **VIN[0]A_D[1]**/ GP1[12] | AB11 | I | IPD DVDD | GP1 PINCNTL141 DSIS: PIN | |
| **VIN[0]A_D[0]**/ GP1[11] | AF9 | I | IPD DVDD | GP1 PINCNTL140 DSIS: PIN | |
| VIN[0]A_DE/ **VIN[0]B_HSYNC**/ UART5_TXD/ I2C[2]_SDA/ GP2[0] | AE21 | I | IPU DVDD | VIN[0]A, UART5, I2C[2], GP2 PINCNTL135 DSIS: 0 | Video Input 0 Port B Horizontal Sync input. Discrete horizontal synchronization signal for Port B 8-bit YCbCr capture without embedded syncs (“BT.601” modes). Not used in RGB or 16-bit YCbCr capture modes |
| **VIN[0]A_HSYNC**/ UART5_RTS/ GP2[3] | AC20 | I | IPU DVDD | UART5, GP2 PINCNTL138 DSIS: 0 | Video Input 0 Port A Horizontal Sync0 input. Discrete horizontal synchronization signal for Port A RGB capture mode or YCbCr capture without embedded syncs (“BT.601” modes). |


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**Table 4-43. Video Input 0 (Digital) Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| VIN[0]A_FLD/ **VIN[0]B_VSYNC**/ UART5_RXD/ I2C[2]_SCL/ GP2[1] | AA20 | I | IPU DVDD | VIN[0]A, UART5, I2C[2], GP2 PINCNTL136 DSIS:0 | Video Input 0 Port B Vertical Sync1 input. Discrete vertical synchronization signal for Port B 8-bit YCbCr capture without embedded syncs (“BT.601” modes). Not used in RGB or 16-bit YCbCr capture modes. |
| **VIN[0]A_VSYNC**/ UART5_CTS/ GP2[4] | AD20 | I | IPU DVDD | UART5, GP2 PINCNTL139 DSIS: 0 | Video Input 0 Port A Vertical Sync0 input. Discrete vertical synchronization signal for Port A RGB capture mode or YCbCr capture without embedded syncs (“BT.601” modes). |
| **VIN[0]B_FLD**/ CAM_D[4]/ GP0[21] | AD17 | I | IPU DVDD_C | CAMERA_I/F, GP0 PINCNTL167 DSIS: 0 | Video Input 0 Port B Field ID input. Discrete field identification signal for Port B 8-bit YCbCr capture without embedded syncs (“BT.601” modes). Not used in RGB or 16-bit YCbCr capture modes. |
| **VIN[0]A_FLD**/ CAM_D[5]/ GP0[20] | AC22 | I | IPU DVDD_C | CAMERA_I/F, GP0 PINCNTL166 DSIS: 0 MM: MUX1 | Video Input 0 Port A Field ID input. Discrete field identification signal for Port A RGB capture mode or YCbCr capture without embedded syncs (“BT.601” modes). |
| **VIN[0]A_FLD**/ VIN[0]B_VSYNC/ UART5_RXD/ I2C[2]_SCL/ GP2[1] | AA20 | I | IPU DVDD | VIN[0]B, UART5, I2C[2], GP2 PINCNTL136 DSIS: 0 MM: MUX0 | |
| **VIN[0]B_DE**/ CAM_D[6]/ GP0[19] | AC15 | I | IPU DVDD_C | CAMERA_I/F, GP0 PINCNTL165 DSIS: 0 | Video Input 0 Port B Data Enable input. Discrete data valid signal for Port B RGB capture mode or YCbCr capture without embedded syncs (“BT.601” modes). |
| **VIN[0]A_DE**/ CAM_D[7]/ GP0[18] | AB17 | I | IPU DVDD_C | CAMERA_I/F, GP0 PINCNTL164 DSIS: 0 MM: MUX1 | Video Input 0 Port A Data Enable input. Discrete data valid signal for Port A RGB capture mode or YCbCr capture without embedded syncs ("BT.601" modes). |
| **VIN[0]A_DE**/ VIN[0]B_HSYNC/ UART5_TXD/ I2C[2]_SDA/ GP2[0] | AE21 | I | IPU DVDD | VIN[0]B, UART5, I2C[2], GP2 PINCNTL135 DSIS: 0 MM: MUX0 | |

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### 4.2.23 Video Output (Digital)

**Table 4-44. Video Output 0 (Digital) Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **Video Output 0** | | | | | |
| VOUT[0]_CLK | AD12 | O | IPD DVDD | – PINCNTL176 | Video Output Clock output. |
| VOUT[0]_G_Y_YC[9] | AF14 | O | IPD DVDD | – PINCNTL195 | Video Output Data. These signals represent the 8 MSBs of G/Y/YC video data. For RGB mode they are green data bits, for YUV444 mode they are Y data bits, for Y/C mode they are Y (Luma) data bits and for BT.656 mode they are multiplexed Y/Cb/Cr (Luma and Chroma) data bits. |
| VOUT[0]_G_Y_YC[8] | AE14 | O | IPD DVDD | – PINCNTL194 | |
| VOUT[0]_G_Y_YC[7] | AD14 | O | IPD DVDD | – PINCNTL193 | |
| VOUT[0]_G_Y_YC[6] | AA8 | O | IPD DVDD | – PINCNTL192 | |
| VOUT[0]_G_Y_YC[5] | AB12 | O | IPD DVDD | – PINCNTL191 | |
| VOUT[0]_G_Y_YC[4] | AB8 | O | IPD DVDD | – PINCNTL190 | |
| VOUT[0]_G_Y_YC[3]/ GP2[25] | AH15 | O | IPD DVDD | GP2 PINCNTL189 DSIS: PIN | |
| **VOUT[0]_G_Y_YC[2]**/ EMU3/ GP2[24] | AH7 | O | IPD DVDD | EMU, GP2 PINCNTL188 DSIS: PIN | |
| VOUT[0]_B_CB_C[9] | AG15 | O | IPD DVDD | – PINCNTL187 | Video Output Data. These signals represent the 8 MSBs of B/CB/C video data. For RGB mode they are blue data bits, for YUV444 mode they are Cb (Chroma) data bits, for Y/C mode they are multiplexed Cb/Cr (Chroma) data bits and for BT.656 mode they are unused. |
| VOUT[0]_B_CB_C[8] | AF15 | O | IPD DVDD | – PINCNTL186 | |
| VOUT[0]_B_CB_C[7] | AB10 | O | IPD DVDD | – PINCNTL185 | |
| VOUT[0]_B_CB_C[6] | AC10 | O | IPD DVDD | – PINCNTL184 | |
| VOUT[0]_B_CB_C[5] | AD15 | O | IPD DVDD | – PINCNTL183 | |
| VOUT[0]_B_CB_C[4] | AD11 | O | IPD DVDD | – PINCNTL182 | |
| **VOUT[0]_B_CB_C[3]**/ GP2[23] | AE15 | O | IPD DVDD | GP2 PINCNTL181 DSIS: PIN | |
| **VOUT[0]_B_CB_C[2]**/ EMU2/ GP2[22] | AG7 | O | IPD DVDD | EMU2, GP2 PINCNTL180 DSIS: PIN | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal


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**Table 4-44. Video Output 0 (Digital) Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| VOUT[0]_R_CR[9]/ | AC13 | O | IPD DVDD | – PINCNTL203 | Video Output Data. These signals represent the 8 MSBs of R/CR video data. For RGB mode they are red data bits, for YUV444 mode they are Cr (Chroma) data bits, for Y/C mode and BT.656 modes they are unused. |
| VOUT[0]_R_CR[8]/ | AE8 | O | IPD DVDD | – PINCNTL202 | |
| VOUT[0]_R_CR[7]/ | AF12 | O | IPD DVDD | – PINCNTL201 | |
| VOUT[0]_R_CR[6]/ | AF6 | O | IPD DVDD | – PINCNTL200 | |
| VOUT[0]_R_CR[5]/ | AF8 | O | IPD DVDD | – PINCNTL199 | |
| VOUT[0]_R_CR[4]/ | AA9 | O | IPD DVDD | – PINCNTL198 | |
| **VOUT[0]_R_CR[3]**/ GP2[27] | AB9 | O | IPD DVDD | GP2 PINCNTL197 DSIS: PIN | |
| **VOUT[0]_R_CR[2]**/ EMU4/ GP2[26] | AD9 | O | IPD DVDD | EMU4, GP2 PINCNTL196 DSIS: PIN | |
| VOUT[0]_VSYNC | AB13 | O | IPD DVDD | – PINCNTL178 | Video Output Vertical Sync output. This is the discrete vertical synchronization output. This signal is not used for embedded sync modes. |
| VOUT[0]_HSYNC | AC11 | O | IPD DVDD | – PINCNTL177 | Video Output Horizontal Sync output. This is the discrete horizontal synchronization output. This signal is not used for embedded sync modes. |
| **VOUT[0]_FLD**/ CAM_PCLK/ GPMC_A[12]/ UART2_RTS/ GP2[2] | AF18 | O | IPD DVDD_C | CAMERA_I/F, GPMC, UART2, GP2 PINCNTL175 DSIS: N/A MM: MUX1 | Video Output Field ID output. This is the discrete field identification output. This signal is not used for embedded sync modes. |
| VOUT[0]_AVID/ **VOUT[0]_FLD**/ SPI[3]_SCLK/ TIM7_IO/ GP2[21] | AA10 | O | IPD DVDD | VOUT[0], SPI[3], TIMER7, GP2 PINCNTL179 DSIS: N/A MM: MUX0 | |
| **VOUT[0]_AVID**/ VOUT[0]_FLD/ SPI[3]_SCLK/ TIM7_IO/ GP2[21] | AA10 | O | IPD DVDD | VOUT[0], SPI[3], TIMER7, GP2 PINCNTL179 DSIS: N/A | Video Output Active Video output. This is the discrete active video indicator output. This signal is not used for embedded sync modes. |

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## Table 4-45. Video Output 1 Terminal Functions

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **Video Output 1** | | | | | |
| **VOUT[1]_CLK**/ EMAC[1]_MTCLK/ GP2[28] | AE24 | O | IPD DVDD | EMAC[1], GP2 PINCNTL204 DSIS: N/A | Video Output Clock output |
| **VOUT[1]_G_Y_YC[9]**/ EMAC[1]_MTXD[2]/ GP3[13] | AD26 | O | IPD DVDD | EMAC[1], GP3 PINCNTL221 DSIS: N/A | Video Output Data. These signals represent the 8 MSBs of G/Y/YC video data. For RGB mode they are green data bits, for YUV444 mode they are Y data bits, for Y/C mode they are Y (Luma) data bits and for BT.656 mode they are multiplexed Y/Cb/Cr (Luma and Chroma) data bits. |
| **VOUT[1]_G_Y_YC[8]**/ EMAC[1]_MTXD[1]/ GP3[12] | AE26 | O | IPD DVDD | EMAC[1], GP3 PINCNTL220 DSIS: N/A | |
| **VOUT[1]_G_Y_YC[7]**/ EMAC[1]_MTXD[0]/ GP3[11] | AF26 | O | IPD DVDD | EMAC[1], GP3 PINCNTL219 DSIS: N/A | |
| **VOUT[1]_G_Y_YC[6]**/ EMAC[1]_GMTCLK/ GP3[10] | AH27 | O | IPD DVDD | EMAC[1], GP3 PINCNTL218 DSIS: N/A | |
| **VOUT[1]_G_Y_YC[5]**/ EMAC[1]_MRXDV/ GP3[9] | AG26 | O | IPD DVDD | EMAC[1], GP3 PINCNTL217 DSIS: N/A | Video Output Data. These signals represent the 8 MSBs of G/Y/YC video data. For RGB mode they are green data bits, for YUV444 mode they are Y data bits, for Y/C mode they are Y (Luma) data bits and for BT.656 mode they are multiplexed Y/Cb/Cr (Luma and Chroma) data bits. |
| **VOUT[1]_G_Y_YC[4]**/ EMAC[1]_MRXD[7]/ GP3[8] | W22 | O | IPD DVDD | EMAC[1], GP3 PINCNTL216 DSIS: N/A | |
| **VOUT[1]_G_Y_YC[3]** EMAC[1]_MRXD[6]/ GP3[7] | Y23 | O | IPD DVDD | EMAC[1], GP3 PINCNTL215 DSIS: N/A | |
| **VOUT[1]_G_Y_YC[2]**/ GPMC_A[13]/ HDMI_SCL/ SPI[2]_SCS[2]/ I2C[2]_SCL/ GP3[20] | AF27 | O | IPU DVDD | GPMC, HDMI, SPI[2], I2C[2], GP3 PINCNTL228 DSIS: N/A | |
| **VOUT[1]_G_Y_YC[1]**/ CAM_D[3]/ GPMC_A[5]/ UART4_RXD/ GP0[22] | AD18 | O | IPU DVDD_C | CAMERA_I/F, GPMC, UART4, GP0 PINCNTL168 DSIS: N/A | Video Output Data. These signals represent the 2 LSBs of G/Y/YC video data for 10-bit, 20-bit, and 30-bit video modes (VOUT[1] only). For RGB mode they are green data bits, for YUV444 mode they are Y data bits, for Y/C mode they are Y (Luma) data bits and for BT-656 mode they are multiplexed Y/Cb/Cr (Luma and Chroma) data bits. These signals are not used in 8/16/24-bit modes. |
| **VOUT[1]_G_Y_YC[0]**/ CAM_D[2]/ GPMC_A[6]/ UART4_TXD/ GP0[23] | AC18 | O | IPD DVDD_C | CAMERA_I/F, GPMC, UART4, GP0 PINCNTL169 DSIS: N/A | |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal


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**Table 4-45. Video Output 1 Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **VOUT[1]_B_CB_C[9]**/ EMAC[1]_MRXD[5]/ I2C[3]_SDA/ GP3[6] | AA24 | O | IPD DVDD | EMAC[1], I2C[3], GP3 PINCNTL214 DSIS: N/A | Video Output Data. These signals represent the 8 MSBs of B/CB/C video data. For RGB mode they are blue data bits, for YUV444 mode they are Cb (Chroma) data bits, for Y/C mode they are multiplexed Cb/Cr (Luma) data bits, and for BT.656 mode they are not used. |
| **VOUT[1]_B_CB_C[8]**/ EMAC[1]_MRXD[4]/ I2C[3]_SCL/ GP3[5] | AH26 | O | IPD DVDD | EMAC[1], I2C[3], GP3 PINCNTL213 DSIS: N/A | |
| **VOUT[1]_B_CB_C[7]**/ EMAC[1]_MRXD[3]/ UART3_TXD/ GP3[4] | AC25 | O | IPD DVDD | EMAC[1], UART3, GP3 PINCNTL212 DSIS: N/A | |
| **VOUT[1]_B_CB_C[6]**/ EMAC[1]_MRXD[2]/ UART3_RXD/ GP3[3] | AD25 | O | IPD DVDD | EMAC[1], UART3, GP3 PINCNTL211 DSIS: N/A | |
| **VOUT[1]_B_CB_C[5]**/ EMAC[1]_MRXD[1]/ UART4_TXD/ GP3[2] | AF25 | O | IPD DVDD | EMAC[1], UART4, GP3 PINCNTL210 DSIS: N/A | Video Output Data. These signals represent the 8 MSBs of B/CB/C video data. For RGB mode they are blue data bits, for YUV444 mode they are Cb (Chroma) data bits, for Y/C mode they are multiplexed Cb/Cr (Luma) data bits, and for BT.656 mode they are not used. |
| **VOUT[1]_B_CB_C[4]**/ EMAC[1]_MRXD[0]/ UART4_RXD/ GP3[1] | AG25 | O | IPD DVDD | EMAC[1], UART4, GP3 PINCNTL209 DSIS: N/A | |
| **VOUT[1]_B_CB_C[3]**/ EMAC[1]_MRCLK/ UART4_CTS/ GP3[0] | AH25 | O | IPD DVDD | EMAC[1], UART4, GP3 PINCNTL208 DSIS: N/A | |
| **VOUT[1]_B_CB_C[2]**/ GPMC_A[0]/ HDMI_CEC/ SPI[2]_D[0]/ GP3[30] | AF28 | O | IPU DVDD | GPMC, HDMI, SPI[2], GP3 PINCNTL231 DSIS: N/A | |
| **VOUT[1]_B_CB_C[1]**/ CAM_HS/ GPMC_A[9]/ UART2_RXD/ GP0[26] | AE23 | O | IPD DVDD_C | CAMERA_I/F, GPMC, UART2, GP0 PINCNTL172 DSIS: N/A | Video Output Data. These signals represent the 2 LSBs of B/CB/C video data for 20-bit, and 30-bit video modes. For RGB mode they are blue data bits, for YUV444 mode they are Cb (Chroma) data bits, for Y/C mode they are multiplexed Cb/Cr (Chroma) data bits and for BT.656 mode they are unused. These signals are not used in 16/24-bit modes. |
| **VOUT[1]_B_CB_C[0]**/ CAM_VS/ GPMC_A[10]/ UART2_TXD/ GP0[27] | AD23 | O | IPU DVDD_C | CAMERA_I/F, GPMC, UART2, GP0 PINCNTL173 DSIS: N/A | |
| **VOUT[1]_R_CR[9]**/ EMAC[1]_MTXEN/ UART5_TXD/ GP3[19] | Y24 | O | IPD DVDD | EMAC[1], UART5, GP3 PINCNTL227 DSIS: N/A | Video Output Data. These signals represent the 8 MSBs of R/CR video data. For RGB mode they are red data bits, for YUV444 mode they are Cr (Chroma) data bits, for Y/C mode and BT.656 mode they are not used. |
| **VOUT[1]_R_CR[8]**/ EMAC[1]_MTXD[7]/ UART5_RXD/ GP3[18] | W23 | O | IPD DVDD | EMAC[1], UART5, GP3 PINCNTL226 DSIS: N/A | |
| **VOUT[1]_R_CR[7]**/ EMAC[1]_MTXD[6]/ SPI[3]_D[0]/ GP3[17] | V22 | O | IPD DVDD | EMAC[1], SPI[3], GP3 PINCNTL225 DSIS: N/A | |
| **VOUT[1]_R_CR[6]**/ EMAC[1]_MTXD[5]/ SPI[3]_D[1]/ GP3[16] | AA25 | O | IPD DVDD | EMAC[1], SPI[3], GP3 PINCNTL224 DSIS: N/A | |

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**Table 4-45. Video Output 1 Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | OTHER(2) (3) | MUXED | DESCRIPTION |
|---|---|---|---|---|---|
| **VOUT[1]_R_CR[5]**/ EMAC[1]_MTXD[4]/ SPI[3]_SCLK/ GP3[15] | AC26 | O | IPD DVDD | EMAC[1], SPI[3], GP3 PINCNTL223 DSIS: N/A | Video Output Data. These signals represent the 8 MSBs of R/CR video data. For RGB mode they are red data bits, for YUV444 mode they are Cr (Chroma) data bits, for Y/C mode and BT.656 mode they are not used. |
| **VOUT[1]_R_CR[4]**/ EMAC[1]_MTXD[3]/ SPI[3]_SCS[1]/ GP3[14] | AG27 | O | IPD DVDD | EMAC[1], SPI[3], GP3 PINCNTL222 DSIS: N/A | |
| **VOUT[1]_R_CR[3]**/ GPMC_A[14]/ HDMI_SDA/ SPI[2]_SCLK/ I2C[2]_SDA/ GP3[21] | AG28 | O | IPU DVDD | GPMC, HDMI, SPI[2], I2C[2], GP3 PINCNTL229 DSIS: N/A | |
| **VOUT[1]_R_CR[2]**/ GPMC_A[15]/ HDMI_HPDET/ SPI[2]_D[1]/ GP3[22] | AE27 | O | IPU DVDD | GPMC, HDMI, SPI[2], I2C[2], GP3 PINCNTL230 DSIS: N/A | |
| **VOUT[1]_R_CR[1]**/ CAM_D[1]/ GPMC_A[7]/ UART4_CTS/ GP0[24] | AC19 | O | IPD DVDD_C | CAMERA_I/F, GPMC, UART4, GP0 PINCNTL170 DSIS: N/A | Video Output Data. These signals represent the 2 LSBs of R/CR video data for 30-bit video modes. For RGB mode they are red data bits, for YUV444 mode they are Cr (Chroma) data bits, for Y/C mode and BT.656 modes they are not used. These signals are not used in 24-bit mode. |
| **VOUT[1]_R_CR[0]**/ CAM_D[0]/ GPMC_A[8]/ UART4_RTS/ GP0[25] | AA22 | O | IPD DVDD_C | CAMERA_I/F, GPMC, UART4, GP0 PINCNTL171 DSIS: N/A | |
| **VOUT[1]_VSYNC**/ EMAC[1]_MCRS/ SPI[3]_D[0]/ UART3_CTS/ GP2[30] | AA23 | O | IPD DVDD | EMAC[1], SPI[3], UART3, GP2 PINCNTL206 DSIS: N/A | Video Output Vertical Sync output. This is the discrete vertical synchronization output. This signal is not used for embedded sync modes |
| **VOUT[1]_HSYNC**/ EMAC[1]_MCOL/ SPI[3]_D[1]/ UART3_RTS/ GP2[29] | AC24 | O | IPD DVDD | EMAC[1], SPI[3], UART3, GP2 PINCNTL205 DSIS: N/A | Video Output Horizontal Sync output. This is the discrete horizontal synchronization output. This signal is not used for embedded sync modes. |
| **VOUT[1]_FLD**/ CAM_FLD/ CAM_WE/ GPMC_A[11]/ UART2_CTS/ GP0[28] | AB23 | O | IPD DVDD_C | CAMERA_I/F, GPMC, UART2, GP0 PINCNTL174 DSIS: N/A | Video Output Field ID output. This is the discrete field identification output. This signal is not used for embedded sync modes. |
| **VOUT[1]_AVID**/ EMAC[1]_MRXER/ UART4_RTS/ TIM6_IO/ GP2[31] | Y22 | O | IPD DVDD | EMAC[1], UART4, TIMER6, GP2 PINCNTL207 DSIS: N/A | Video Output Active Video output. This is the discrete active video indicator output. This signal is not used for embedded sync modes. |


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### 4.2.24 Video Output (Analog, TV)

**Table 4-46. Video Outupt (Analog, TV) Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER(2) (3) | DESCRIPTION |
|---|---|---|---|---|
| **VIDEO INTERFACES (TV)** | | | | |
| TV_OUT0 | AH24 | O | VDDA_VDAC_1P8 | Composite/S-Video (Luminance) Amplifier Output.<br>In **Normal mode** (internal amplifier used), this pin drives the 75-Ω TV load. An external resistor (Rout) should be connected between this pin and the TV_VFB0 pin and be placed as close to the pins as possible. The nominal value of Rout is 2700 Ω.<br>In **TVOUT Bypass mode** (internal amplifier *not* used), this pin is *not* used.<br>When this pin is not used or the TV output is powered-down, this pin should be left unconnected. |
| TV_OUT1 | AH22 | O | VDDA_VDAC_1P8 | S-Video (Chrominance) Amplifier Output.<br>In **Normal mode** (internal amplifier used), this pin drives the 75-Ω TV load.<br>An external resistor (Rout) should be connected between this pin and the TV_VFB1 pin and be placed as close to the pins as possible. The nominal value of Rout is 2700 Ω.<br>In **TVOUT Bypass mode** (internal amplifier *not* used), this pin is *not* used.<br>When this pin is not used or the TV output is powered-down, this pin should be left unconnected. |
| TV_VFB0 | AG23 | A O | VDDA_VDAC_1P8 | Composite/S-Video (Luminance) Feedback.<br>In **Normal mode** (internal amplifier used), this pin acts as the buffer feedback node.<br>An external resistor (Rout) should be connected between this pin and the TV_OUT0 pin.<br>In **TVOUT Bypass mode** (internal amplifier *not* used), this pin acts as the direct Video DAC output and should be connected to ground through a load resistor (Rload) and to an external video amplifier. The nominal value of Rload is 1500 Ω.<br>When this pin is **not used** or the TV output is powered-down, this pin should be left unconnected. |
| TV_VFB1 | AG22 | A O | VDDA_VDAC_1P8 | S-Video (Chrominance) Feedback.<br>In **Normal mode** (internal amplifier used), this pin acts as the buffer feedback node.<br>An external resistor (Rout) should be connected between this pin and the TV_OUT1 pin.<br>In **TVOUT Bypass mode** (internal amplifier not used), it acts as the direct Video DAC output and should be connected to ground through a load resistor (Rload) and to an external video amplifier. The nominal value of Rload is 1500 Ω.<br>When this pin is **not used** or the TV output is powered-down, this pin should be left unconnected. |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State
(2) IPD = Internal Pulldown Active, IPU = Internal Pullup Active, DIS = Internal Pull Disabled. This represents the default state of the Internal Pull after Reset. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see Section 5.5.1, *Pullup/Pulldown Resistors* and Section 8.3.17, *Pin Behaviors at Reset*.
(3) Specifies the operating I/O supply voltage for each signal

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**Table 4-46. Video Outupt (Analog, TV) Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE[1] | OTHER[2] [3] | DESCRIPTION |
|---|---|---|---|---|
| TV_RSET | AH23 | A | _ VDDA_VDAC_1P8 | TV Input Reference Current Setting.<br>An external resistor (Rset) should be connected between this pin and VSSA_VDAC to set the reference current of the video DAC. The value of the resistor depends on the mode of operation.<br>In **Normal mode** (internal amplifier used), the nominal value for Rset is 4700 Ω.<br>In **TVOUT Bypass mode** (internal amplifier *not* used), the nominal value for Rset is 10000 Ω.<br>When the TV output is **not used**, this pin should be connected to ground (VSS). |


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### 4.2.25 Reserved Pins

**Table 4-47. Reserved Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER | DESCRIPTION |
|---|---|---|---|---|
| RSV1 | AD8 | O | | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV2 | U8 | O | | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV3 | V8 | O | | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV4 | Y14 | I | | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV5 | AC8 | I | | |
| RSV16 | U1 | I | | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV17 | U2 | I | | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV23 | AB1 | O | | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV24 | AB2 | O | | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV25 | AA2 | I | | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV26 | AA1 | I | | Reserved. (Leave unconnected, ***do not*** connect to power or ground.) |
| RSV27 | T10 | S | | Reserved. For proper device operation, this pin **must always** be tied directly to a 1-µF capacitor to ground (VSS). |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State

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### 4.2.26 Supply Voltages

**Table 4-48. Supply Voltages Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER | DESCRIPTION |
|---|---|---|---|---|
| VREFSSTL_DDR[0] | G15 | S | | Reference Power Supply DDR[0] |
| VREFSSTL_DDR[1] | G14 | S | | Reference Power Supply DDR[1] |
| CVDD | K9, K12, K18, L15, L17, L19, M16, M18, N17, N19, P12, P14, P16, R15, R17, R19, T12, U11, U13, U17, U19, W11 | S | | Variable Voltage Supply for the CORE_L Core Logic Voltage Domain<br>For actual voltage supply ranges, see Section 7.2, *Recommended Operating Conditions*. |
| CVDD_ARM | T14, T15, T16, U15, U16, V15, V16 | S | | Variable Voltage Supply for the ARM_L Core Logic Voltage Domain<br>For actual voltage supply ranges, see Section 7.2, *Recommended Operating Conditions*. |
| CVDD_DSP | K10, L9, L10, L11, L12, M10, M12, N9 | S | | Variable Voltage Supply for the DSP_L Core Logic Voltage Domain<br>For actual voltage supply ranges, see Section 7.2, *Recommended Operating Conditions*. |
| DVDD | M8, N7, P8, T7, U21, U22, V20,Y11, Y16, AA15, AA17, AB14, AB16 | S | | 3.3 V/1.8 V Power Supply for General I/Os |
| DVDD_GPMC | K20, L21, M20 | S | | 3.3 V/1.8 V Power Supply for GPMC I/Os (that is, GPMC, SD2, and so forth) |
| DVDD_GPMCB | P20, T20 | S | | 3.3 V/1.8 V Power Supply for GPMCB I/Os |
| DVDD_SD | P7, P9 | S | | 3.3 V/1.8 V Power Supply for MMC/SD/SDIO I/Os (specifically, SD0, SD1, and pin W6) |
| DVDD_DDR[0] | E20, E21, G16, H16, H17, J15, J16, J17, J18 | S | | 1.5 V/1.8 V Power Supply for DDR[0] I/Os |
| DVDD_DDR[1] | E8, E9, G13, H12, H13, H14, J10, J11, J13 | S | | 1.5 V/1.8 V Power Supply for DDR[1] I/Os |
| DVDD_M | R10 | S | | 1.8 V Power Supply . For proper device operation, this pin ***must*** always be connected to a 1.8-V Power Supply. |
| DVDD_C | W19, W20 | S | | 3.3 V/1.8 V Power Supply for Camera I/F I/Os |
| VDDA_ARMPLL_1P8 | R13 | S | | 1.8 V Analog Power Supply for PLL_ARM |
| VDDA_DSPPLL_1P8 | P11 | S | | 1.8 V Analog Power Supply for PLL_DSP |
| VDDA_VID0PLL_1P8 | AB18 | S | | 1.8 V Analog Power Supply for PLL_VIDEO0 |
| VDDA_VID1PLL_1P8 | AA18 | S | | 1.8 V Analog Power Supply for PLL_VIDEO1 |
| VDDA_AUDIOPLL_1P8 | R18 | S | | 1.8 V Analog Power Supply for PLL_AUDIO |
| VDDA_DDRPLL_1P8 | H15 | S | | 1.8 V Analog Power Supply for PLL_DDR |
| VDDA_L3PLL_1P8 | N18 | S | | 1.8 V Analog Power Supply for PLL_L3, PLL_HDVPSS, and PLL_MEDIACTL |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State


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**Table 4-48. Supply Voltages Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER | DESCRIPTION |
|---|---|---|---|---|
| VDDA_PCIE_1P8 | W9, W10 | S | | 1.8 V Analog Power Supply for PCIe.<br>For proper device operation, this pin ***must*** always be connected to a 1.8-V Power Supply, even if the PCIe is not being used. |
| VDDA_CSI2_1P8 | M22 | S | | 1.8 V Analog Power Supply for CSI2.<br>For proper device operation, this pin ***must*** always be connected to a 1.8-V Power Supply, even if the CSI2 is not being used. |
| VDDA_HDMI_1P8 | W18 | S | | 1.8 V Analog Power Supply for HDMI.<br>For proper device operation, this pin ***must*** always be connected to a 1.8-V Power Supply, even if the HDMI is not being used. |
| VDDA_USB0_1P8 | AA12 | S | | 1.8 V Analog Power Supply for USB0.<br>For proper device operation, this pin ***must*** always be connected to a 1.8-V Power Supply, even if the USB0 is not being used. |
| VDDA_USB1_1P8 | W13 | S | | 1.8 V Analog Power Supply for USB1.<br>For proper device operation, this pin ***must*** always be connected to a 1.8-V Power Supply, even if the USB1 is not being used. |
| VDDA_VDAC_1P8 | AB19 | S | | 1.8 V Reference Power Supply for VDAC.<br>For proper device operation, this pin ***must*** always be connected to a 1.8-V Power Supply, even if the VDAC is not being used. |
| VDDA_USB_3P3 | AA13 | S | | 3.3 V Analog Power Supply for USB0 and USB1.<br>For proper device operation, this pin ***must*** always be connected to a 3.3-V Power Supply, even if USB0 and USB1 are not being used. |
| VDDA_1P8 | L20, M7, R20, U7, U9, U10, V10, W15, Y13 | S | | 1.8 V Power Supply for on-chip LDOs and I/O biasing |
| LDOCAP_ARM | W14 | A | | ARM Cortex-A8 VBB LDO output.<br>This pin must always be connected via a 1-uF capacitor to VSS. |
| LDOCAP_ARMRAM | V14 | A | | ARM Cortex-A8 RAM LDO output.<br>This pin must always be connected via a 1-uF capacitor to VSS. |
| LDOCAP_RAM0 | P18 | A | | CORE RAM0 LDO output.<br>This pin must always be connected via a 1-uF capacitor to VSS. |
| LDOCAP_RAM1 | R11 | A | | CORE RAM1 LDO output.<br>This pin must always be connected via a 1-uF capacitor to VSS. |
| LDOCAP_RAM2 | L18 | A | | CORE RAM2 LDO output.<br>This pin must always be connected via a 1-uF capacitor to VSS. |
| LDOCAP_DSP | P10 | A | | C674x DSP VBB LDO output.<br>This pin must always be connected via a 1-uF capacitor to VSS. |
| LDOCAP_DSPRAM | M11 | A | | C674x DSP RAM LDO output.<br>This pin must always be connected via a 1-uF capacitor to VSS. |
| LDOCAP_HDVICP | N10 | A | | HDVICP2 VBB LDO output.<br>This pin must always be connected via a 1-uF capacitor to VSS. |
| LDOCAP_HDVICPRAM | N11 | A | | HDVICP2 RAM LDO output.<br>This pin must always be connected via a 1-uF capacitor to VSS. |
| LDOCAP_SERDESCLK | T11 | A | | SERDES_CLKP/N Pins LDO output.<br>This pin must always be connected via a 1-uF capacitor to VSS. |

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### 4.2.27 Ground Pins (VSS)

**Table 4-49. Ground Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | OTHER | DESCRIPTION |
|---|---|---|---|---|
| VSS | A1, A12, A17, A28, D9, D20, J12, J14, J19, K11, K13, K14, K15, K16, K17, K19, L8, L13, L16, L22, M9, M15, M17, M19, M21, N8, N12, N15, N16, N20, N21, P13, P15, P17, P19, P21, R8, R9, R12, R14, R16, R21, R22, T8, T9, T13, T17, T18, T19, T21, T22, U12, U14, U18, U20, V7, V9, V11, V17, V19, V21, W12, W16, W17, Y1, Y2, Y10, Y12, Y15, Y17, Y18, Y19, AA14, AA16, AD21, AE1, AE2, AE9, AE20, AF23, AG1, AH1, AH28 | GND | | Ground (GND) |
| VSSA_VDAC | AA19 | GND | | Analog GND for VDAC.<br>For proper device operation, this pin *must* always be connected to ground, even if the VDAC is not being used. |
| VSSA_CSI2 | N22 | GND | | Analog GND for CSI2.<br>For proper device operation, this pin *must* always be connected to ground, even if the CSI2 is not being used. |
| VSSA_HDMI | V18 | GND | | Analog GND for HDMI<br>For proper device operation, this pin *must* always be connected to ground, even if the HDMI is not being used. |
| VSSA_USB | V12, V13 | GND | | Analog GND for USB0 and USB1.<br>For proper device operation, this pin *must* always be connected to ground, even if USB0 and USB1 are not being used. |
| VSSA_DEVOSC | AG3 | GND | | Ground for Device Oscillator |
| VSSA_AUXOSC | R2 | GND | | Ground for Auxiliary Oscillator |

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, MM = Multi Muxed, DSIS = De-selected Input State


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# 5 Device Configurations

## 5.1 Control Module Registers

## 5.2 Boot Modes

The state of the device after boot is determined by sampling the input states of the BTMODE[15:0] pins when device reset ($\overline{\text{POR}}$ or $\overline{\text{RESET}}$) is de-asserted. The sampled values are latched into the CONTROL_STATUS register, which is part of the Control Module. The BTMODE[15:11] values determine the following system boot settings:

- $\overline{\text{RSTOUT_WD_OUT}}$ Control
- GPMC CS0 Default Data Bus Width, Wait Enable, and Address/Data Multiplexing

For additional details on BTMODE[15:11] pin functions, see Table 4-1, *Boot Configuration Terminal Functions*.

The BTMODE[4:0] values determine the boot mode order according to Table 5-1, *Boot Mode Order*. The 1st boot mode listed for each BTMODE[4:0] configuration is executed as the primary boot mode. If the primary boot mode fails, the 2nd, 3rd, and 4th boot modes are executed in that order until a successful boot is completed.

The BTMODE[7:5] pins are RESERVED and should be pulled down as indicated inTable 4-1, *Boot Configuration Terminal Functions*.

When the EMAC bootmode is selected (see Table 5-1), the sampled value from BTMODE[9:8] pins are used to determine the Ethernet PHY Mode selection (see Table 5-7).

When the XIP (MUX0), XIP (MUX1), XIP w/ WAiT (MUX0) or XIP w/ WAiT (MUX1) bootmode is selected (see Table 5-1), the sampled value from BTMODE[10] pin is used to select between GPMC pin muxing options shown in Table 5-2, *XIP (on GPMC) Boot Options [Muxed or Non-Muxed]*.

For more detailed information on booting the device, see the *ROM Code Memory and Peripheral Booting* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

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**Table 5-1. Boot Mode Order**

| BTMODE[4:0] | 1st | 2nd | 3rd | 4th |
|---|---|---|---|---|
| 00000 | RESERVED | RESERVED | RESERVED | RESERVED |
| 00001 | UART | XIP w/WAIT (MUX0)(1)(2) | MMC | SPI |
| 00010 | UART | SPI | NAND | NANDI2C |
| 00011 | UART | SPI | XIP (MUX0)(1)(2) | MMC |
| 00100 | EMAC(3) | SPI | NAND | NANDI2C |
| 00101 | RESERVED | RESERVED | RESERVED | RESERVED |
| 00110 | RESERVED | RESERVED | RESERVED | RESERVED |
| 00111 | EMAC(3) | MMC | SPI | XIP (MUX1)(1)(2) |
| 01000 | PCIE_32(4) | RESERVED | RESERVED | RESERVED |
| 01001 | PCIE_64(4) | RESERVED | RESERVED | RESERVED |
| 01010 | RESERVED | RESERVED | RESERVED | RESERVED |
| 01011 | RESERVED | RESERVED | RESERVED | RESERVED |
| 01100 | RESERVED | RESERVED | RESERVED | RESERVED |
| 01101 | RESERVED | RESERVED | RESERVED | RESERVED |
| 01110 | RESERVED | RESERVED | RESERVED | RESERVED |
| 01111 | Fast XIP (MUX0)(1) | UART | EMAC(3) | PCIE_64(4) |
| 10000 | XIP (MUX1)(1)(2) | UART | EMAC(3) | MMC |
| 10001 | XIP w/WAIT (MUX1)(1)(2) | UART | EMAC(3) | MMC |
| 10010 | NAND | NANDI2C | SPI | UART |
| 10011 | NAND | NANDI2C | MMC | UART |
| 10100 | NAND | NANDI2C | SPI | EMAC(3) |
| 10101 | NANDI2C | MMC | EMAC(3) | UART |
| 10110 | SPI | MMC | UART | EMAC(3) |
| 10111 | MMC | SPI | UART | EMAC(3) |
| 11000 | SPI | MMC | PCIE_32(4) | RESERVED |
| 11001 | SPI | MMC | PCIE_64(4) | RESERVED |
| 11010 | XIP (MUX0)(1)(2) | UART | SPI | MMC |
| 11011 | XIP w/WAIT (MUX0)(1)(2) | UART | SPI | MMC |
| 11100 | RESERVED | RESERVED | RESERVED | RESERVED |
| 11101 | RESERVED | RESERVED | RESERVED | RESERVED |
| 11110 | RESERVED | RESERVED | RESERVED | RESERVED |
| 11111 | Fast XIP (MUX0)(1) | EMAC(3) | UART | PCIE_32(4) |

(1) GPMC CS0 eXecute In Place (XIP) boot for NOR/OneNAND/ROM. MUX0/1 refers to the multiplexing option for the GPMC_A[12:0] pins. For more detailed information on booting the device, including which pins are used for each boot mode, see the *ROM Code Memory and Peripheral Booting* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

(2) When the XIP (MUX0), XIP (MUX1), XIP w/ WAiT (MUX0) or XIP w/ WAiT (MUX1) bootmode is selected, the sampled value from BTMODE[10] pin is used to select between GPMC pin configuration options shown in Table 5-2, *XIP (on GPMC) Boot Options*.

(3) When the EMAC bootmode is selected, the sampled value from BTMODE[9:8] pins are used to determine the Ethernet PHY Mode Selection (see Table 5-7).

(4) When the PCIe bootmode is selected (PCIE_32 or PCI_64), the sampled value from BTMODE[15:12] pins are used to determine the addressing options. For more detailed information on the PCIe addressing options, see the *ROM Code Memory and Peripheral Booting* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

### 5.2.1 XIP (NOR) Boot Options

Table 5-2 shows the XIP (NOR) boot mode GPMC pin configuration options (Option A: BTMODE[10] = 0 and Option B: BTMODE[10] = 1). For Option B, the pull state on select pins is reconfigured to IPD and remains IPD after boot until the user software reconfigures it.


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## Table 5-2. XIP (on GPMC) Boot Options

| SIGNAL NAME | PIN NO. | OTHER CONDITIONS | CONTROLLED I/O FUNCTION DURING XIP (NOR) BOOT | | | |
|---|---|---|---|---|---|---|
| | | | BTMODE[10] = 0 [OPTION A] | | BTMODE[10] = 1 [OPTION B] | |
| | | | PIN FUNCTION | PULL STATE | PIN FUNCTION | PULL STATE |
| GPMC_CS[0]/* | T28 | | GPMC_CS[0] | IPU | GPMC_CS[0] | IPU |
| GPMC_ADV_ALE/* | M26 | BTMODE[14:13] = 01b or 10b (Mux) | GPMC_ADV_ALE | IPU | GPMC_ADV_ALE | IPU |
| | | BTMODE[14:13] = 00b (Non-Mux) | | | Default | |
| GPMC_OE_RE | T27 | | GPMC_OE_RE | IPU | GPMC_OE_RE | IPU |
| GPMC_BE[0]_CLE/GPMC_A[25]/* | U27 | | GPMC_BE[0]_CLE | IPD | Default | IPD |
| GPMC_BE[1]/GPMC_A[24]/* | V28 | | Default | IPD | Default | IPD |
| GPMC_WE | U28 | | GPMC_WE | IPU | GPMC_WE | IPU |
| GPMC_WAIT[0]/GPMC_A[26]/* | W28 | BTMODE[15] = 1b (WAIT Used/Enabled) | GPMC_WAIT[0] | IPU | GPMC_WAIT[0] | IPU |
| | | BTMODE[15] = 0b (WAIT Not Used/Disabled) | | | Default | IPD(1) |
| GPMC_CLK/* | R26 | | GPMC_CLK | IPU | Default | IPU |
| GPMC_D[15:0]/* | Y25,V24,U23,U24,AA27,Y26,AB28,Y27,V25,U25,AA28,V26,W27,V27,Y28,U26 | | GPMC_D[15:0] | Off | GPMC_D[15:0] | Off |
| */GPMC_A[27]/GPMC_A[26]/GPMC_A[0]/* | J25 | BTMODE[12] = 0b (8-bit Mode) | GPMC_A[0] | IPD | GPMC_A[0] | IPD |
| | | BTMODE[12] = 1b (16-bit Mode) | | | Default | |
| */GPMC_A[1:12]/* (M0) | T23,H26,F28,G27,K22,K23,J24,H25,H22,H23,G23,F27 | XIP_MUX0 Mode | GPMC_A[1:12] | IPD | GPMC_A[1:12] | IPD |
| | | XIP_MUX1 Mode | Default | IPD | Default | IPD |
| */GPMC_A[1:12]/* (M1) | J28,K27,M24,L26,AD18,AC18,AC19,AA22,AE23,AD23,AB23,AF18 | XIP_MUX0 Mode | Default | Default | Default | Default |
| | | XIP_MUX1 Mode | GPMC_A[1:12] | Default | GPMC_A[1:12] | Default |
| */GPMC_A[13:15]/* (M0) | J22,H24,J23 | | Default | IPD | Default | IPD |
| */GPMC_A[0]/* (M1) | AF28 | BTMODE[12] = 0b (8-bit Mode) | Default | IPU | Default | IPU |
| | | BTMODE[12] = 1b (16-bit Mode) | | | | |
| */GPMC_A[13]/* (M1) | AF27 | BTMODE[14:13] = 01b or 10b (Mux) | Default | IPU | Default | IPU |
| | | BTMODE[14:13] = 00b (Non-Mux) | | | | IPD(1) |
| */GPMC_A[14]/* (M1) | AG28 | BTMODE[14:13] = 01b or 10b (Mux) | Default | IPU | Default | IPU |
| | | BTMODE[14:13] = 00b (Non-Mux) | | | | IPD(1) |
| */GPMC_A[15]/* (M1) | AE27 | | Default | IPD | Default | IPD |
| GPMC_A[16:19]/* | AD27,V23,AE28,AC27 | | Default | IPD | Default | IPD |
| GPMC_A[20] (M0) | AD28 | | Default | IPU | Default | IPD(1) |
| GPMC_A[21] (M0) | AC28 | | Default | IPD | Default | IPD |
| GPMC_A[22] (M0) | AB27 | | Default | IPU | Default | IPD(1) |
| GPMC_A[23] (M0) | AA26 | | Default | IPD | Default | IPD |

(1) After initial power-up the internal pullup (IPU) will be at its default configuration of IPU. During the boot ROM execution, the pull state is reconfigured to IPD and it remains IPD after boot until the user software reconfigures it.

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**Table 5-2. XIP (on GPMC) Boot Options (continued)**

| SIGNAL NAME | PIN NO. | OTHER CONDITIONS | CONTROLLED I/O FUNCTION DURING XIP (NOR) BOOT | | | |
|---|---|---|---|---|---|---|
| | | | BTMODE[10] = 0 [OPTION A] | | BTMODE[10] = 1 [OPTION B] | |
| | | | PIN FUNCTION | PULL STATE | PIN FUNCTION | PULL STATE |
| */GPMC_A[24]/GPMC_A[20]/* | L25 | | Default | IPU | Default | IPD(1) |
| */GPMC_A[25]/GPMC_A[21]/* | N23 | | Default | IPU | Default | IPD(1) |
| */GPMC_A[26]/GPMC_A[22]/* | P22 | | Default | IPU | Default | IPD(1) |
| */GPMC_A[27]/GPMC_A[23]/* | R24 | | Default | IPU | Default | IPU |
| GPMC_A[24] (M1) | M25 | | Default | IPU | Default | IPU |
| GPMC_A[25] (M1) | K28 | | Default | IPU | Default | IPU |


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### 5.2.2 NAND Flash Boot

Table 5-3 lists the device pins that are configured by the ROM for the NAND Flash boot mode.

NOTE: Table 5-3 lists the configuration of the GPMC_CLK pin (pin mux and pull state) in NAND bootmodes.

The NAND flash memory is not XIP and requires shadowing before the code can be executed.

**Table 5-3. Pins Used in NAND FLASH Bootmode**

| SIGNAL NAME | PIN NO. | TYPE | OTHER CONDITIONS |
|---|---|---|---|
| GPMC_CS[0]/* | T28 | O | BTMODE[12] = 0b (8-bit Mode) BTMODE[12] = 1b (16-bit Mode) BTMODE[14:13] = 00b (GPMC CS0 not muxed) BTMODE[15] = 0b (wait disabled) |
| GPMC_ADV_ALE/* | M26 | O | |
| GPMC_OE_RE | T27 | O | |
| GPMC_BE[0]_CLE/GPMC_A[25]/* | U27 | O | |
| GPMC_BE[1]/GPMC_A[24]/* | V28 | O | |
| GPMC_WE | U28 | O | |
| GPMC_WAIT[0]/GPMC_A[26]/*(1) | W28 | I | |
| GPMC_CLK/* | R26 | O | |
| GPMC_D[15:0]/* | Y25,V24,U23,U24, AA27,Y26,AB28,Y27, V25,U25,AA28,V26 ,W27,V27,Y28,U26 | I/O | |

(1) GPMC_CLK/* is not configured in BTMODE[10] = 1 [OPTION B]

### 5.2.3 NAND I2C Boot (I2C EEPROM)

Table 5-4 lists the device pins that are configured by the ROM for the NAND I2C boot mode.

**Table 5-4. Pins Used in NAND I2C Bootmode**

| SIGNAL NAME | PIN NO. | TYPE |
|---|---|---|
| I2C[0]_SCL | AC4 | I/O |
| I2C[0]_SDA | AB6 | I/O |

### 5.2.4 MMC/SD Cards Boot

Table 5-5 lists the device pins that are configured by the ROM for the MMC/SD boot mode.

**Table 5-5. Pins Used in MMC/SD Bootmode**

| SIGNAL NAME | PIN NO. | TYPE |
|---|---|---|
| SD1_CLK | P3 | O |
| SD1_CMD/GP0[0] [MUX0] | P2 | O |
| SD1_DAT[0] | P1 | I/O |
| SD1_DAT[1]_SDIRQ | P5 | I/O |
| SD_DAT[2]_SDRW | P4 | I/O |
| SD1_DAT[3] | P6 | I/O |

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### 5.2.5 SPI Boot

Table 5-6 lists the device pins that are configured by the ROM for the SPI boot mode.

**Table 5-6. Pins Used in SPI Bootmode**

| SIGNAL NAME | PIN NO. | TYPE |
|---|---|---|
| $\overline{\text{SPI[0]_SCS[0]}}$ | AD6 | I/O |
| SPI[0]_D[0] (MISO) | AE3 | I/O |
| SPI[0]_D[1] (MOSI) | AF3 | I/O |
| SPI[0]_SCLK | AC7 | I/O |

### 5.2.6 Ethernet PHY Mode Selection

When the EMAC bootmode is selected, via the BTMODE[4:0] pins (see Table 5-1), Table 5-7 shows the sampled value of BTMODE[9:8] pins and the Ethernet PHY Mode selection.

Table 5-8 shows the signal names (pin functions) and the associated pin numbers selected in each particular EMAC mode.

**Table 5-7. EMAC PHY Mode Selection**

| BTMODE[9:8] | ETHERNET PHY MODE SELECTION |
|---|---|
| 00b | MII |
| 01b | RMII |
| 10b | RGMII |
| 11b | RESERVED |

**Table 5-8. Pins Used in EMAC[0] MII/GMII, RGMII, and RMII Boot Modes**

| PIN NO. | SIGNAL NAMES | | | | | |
|---|---|---|---|---|---|---|
| | MII/GMII | TYPE | RGMII | TYPE | RMII | TYPE |
| J27 | DEFAULT | | DEFAULT | | EMAC_RMREFCLK | Output only |
| L23 | EMAC[0]_MCOL | I | EMAC[0]_RGRXCTL | I | EMAC[0]_RMRXD[0] | I |
| R25 | EMAC[0]_MCRS | I | EMAC[0]_RGRXD[2] | I | EMAC[0]_RMRXD[1] | I |
| K23 | EMAC[0]_GMTCLK | O | DEFAULT | | DEFAULT | |
| H27 | EMAC[0]_MRCLK | I | EMAC[0]_RGTXC | O | EMC[0]_RMCRSDV | I |
| G28 | EMAC[0]_MRXD[0] | I | EMAC[0]_RGTXD[0] | O | EMAC[0]_RMTXD[0] | O |
| P23 | EMAC[0]_MRXD[1] | I | EMAC[0]_RGRXD[0] | I | EMAC[0]_RMTXD[1] | O |
| R23 | EMAC[0]_MRXD[2] | I | EMAC[0]_RGRXD[1] | I | EMAC[0]_RMTXEN | O |
| J25 | EMAC[0]_MRXD[3] | I | DEFAULT | | DEFAULT | |
| T23 | EMAC[0]_MRXD[4] | I | EMAC[0]_RGRXD[3] | I | DEFAULT | |
| H26 | EMAC[0]_MRXD[5] | I | EMAC[0]_RGTXD[3] | O | DEFAULT | |
| F28 | EMAC[0]_MRXD[6] | I | EMAC[0]_RGTXD[2] | O | DEFAULT | |
| G27 | EMAC[0]_MRXD[7] | I | EMAC[0]_RGTXD[1] | O | DEFAULT | |
| K22 | EMAC[0]_MRXDV | I | DEFAULT | | DEFAULT | |
| J26 | EMAC[0]_MRXER | I | EMAC[0]_RGTXCTL | O | EMAC[0]_RMRXER | I |
| L24 | EMAC[0]_MTCLK | I | EMAC[0]_RGRXC | I | DEFAULT | |
| J24 | EMAC[0]_MTXD[0] | O | DEFAULT | | DEFAULT | |
| H25 | EMAC[0]_MTXD[1] | O | DEFAULT | | DEFAULT | |
| H22 | EMAC[0]_MTXD[2] | O | DEFAULT | | DEFAULT | |


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**Table 5-8. Pins Used in EMAC[0] MII/GMII, RGMII, and RMII Boot Modes (continued)**

| PIN NO. | SIGNAL NAMES | | | | | |
|---|---|---|---|---|---|---|
| | MII/GMII | TYPE | RGMII | TYPE | RMII | TYPE |
| H23 | EMAC[0]_MTXD[3] | O | DEFAULT | | DEFAULT | |
| G23 | EMAC[0]_MTXD[4] | O | DEFAULT | | DEFAULT | |
| F27 | EMAC[0]_MTXD[5] | O | DEFAULT | | DEFAULT | |
| J22 | EMAC[0]_MTXD[6] | O | DEFAULT | | DEFAULT | |
| H24 | EMAC[0]_MTXD[7] | O | DEFAULT | | DEFAULT | |
| J23 | EMAC[0]_MTXEN | O | DEFAULT | | DEFAULT | |
| H28 | MDCLK | O | MDCLK | O | MDCLK | O |
| P24 | MDIO | I/O | MDIO | I/O | MDIO | I/O |

### 5.2.7 PCIe Bootmode (PCIE_32 and PCIE_64)

Table 5-9 lists the device pins that are configured by the ROM for the PCIe boot mode.

**Table 5-9. Pins Used in PCIe Bootmode**

| SIGNAL NAME | PIN NO. | TYPE |
|---|---|---|
| PCIE_TXP0 | AD2 | O |
| PCIE_TXN0 | AD1 | O |
| PCIE_RXP0 | AC2 | I |
| PCIE_RXN0 | AC1 | I |
| SERDES_CLKIP | AF1 | I |
| SERDES_CLKN | AF2 | I |

### 5.2.8 UART Bootmode

Table 5-10 lists the device pins that are configured by the ROM for the UART boot mode.

**Table 5-10. Pins Used in UART Bootmode**

| SIGNAL NAME | PIN NO. | TYPE |
|---|---|---|
| UART0_RXD | AH5 | I |
| UART0_TXD | AG5 | O |

## 5.3 Pin Multiplexing Control

Device level pin multiplexing is controlled on a pin-by-pin basis by the MUXMODE bits of the PINCNTL1 – PINCNTL270 registers in the Control Module.

Pin multiplexing selects which one of several peripheral pin functions controls the pin's I/O buffer output data values. Table 5-11 shows the peripheral pin functions associated with each MUXMODE setting for all multiplexed pins. The default pin multiplexing control for almost every pin is to select MUXMODE = 0x0, in which case the pin's I/O buffer is 3-stated.

In most cases, the input from each pin is routed to all of the peripherals that share the pin, regardless of the MUXMODE setting. However, in some cases a constant "0" or "1" value is routed to the associated peripheral when its peripheral function is not selected to control any output pin. For more details on the De-Selected Input State (DSIS), see the "MUXED" columns of each Terminal Functions table (Section 4.2, *Terminal Functions*).

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Some peripheral pin functions can be routed to more than one device pin. These types of peripheral pin functions are called Multimuxed (MM) and may have different Switching Characteristics and Timing Requirements for each device pin option. The Multimuxed peripheral pin functions are labeled as "MM" in Terminal Functions tables in Section 4.2, *Terminal Functions* and the associated timings for each MM pin option are in Section 9, *Peripheral Information and Timings*.

For more detailed information on the Pin Control 1 through Pin Control 270 (PINCNTLx) registers breakout, see Figure 5-1 and Table 5-11. For the register reset values of each PINCNTLx register, see Table 5-13, *PINCNTLx Registers MUXMODE Functions*.

**Figure 5-1. PINCNTL1 – PINCNTL270 (PINCNTLx) Registers Breakout**

| 31 | 24 | 23 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|
| RESERVED | | RESERVED | | RSV | RXACTIVE | PLLTYPESEL | PLLUDEN |
| R - 0000 0000 | | R - 0000 | | R/W (see Table 5-13 for register reset value) | | | |

| 15 | 8 | 7 | 0 |
|---|---|---|---|
| RESERVED | | MUXMODE[7:0] (see Table 5-13) | |
| R - 0000 0000 | | R/W - 0000 0000 | |

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

**Table 5-11. PINCNTL1 – PINCNTL270 (PINCNTLx) Registers Bit Descriptions**

| Bit | Field | Description | Comments |
|---|---|---|---|
| 31:20 | RESERVED | Reserved. Read only, writes have no effect. | For PINCNTLx register reset value examples, see Table 5-12, *PNICNTLx Register Reset Value Examples*.<br>For the full register reset values of all PINCNTLx registers, see Table 5-13, *PINCNTLx Registers MUXMODE Functions*. |
| 19 | RSV | Reserved. This bit ***must*** always be written with the reset (default) value.<br>(See Table 5-13 for full register reset value) | |
| 18 | RXACTIVE | Receiver Enable<br>0 = Receiver Disabled<br>1 = Receiver Enabled | |
| 17 | PLLTYPSEL | Pullup/Pulldown Type Selection bit<br>0 = Pulldown (PD) selected<br>1 = Pullup (PU) selected | |
| 16 | PLLUDEN | Pullup/Pulldown Enable bit<br>0 = PU/PD enabled<br>1 = PU/PD disabled | |
| 15:8 | RESERVED | Reserved. Read only, writes have no effect. | |
| 7:0 | MUXMODE[7:0] | MUXMODE Selection bits<br>These bits select the multiplexed mode pin function settings (seeTable 5-13, *PINCNTLx Registers MUXMODE Functions*). A value of zero results in the pin being tri-stated. Non-zero values other than those shown in Table 5-13 are Reserved. | |


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## Table 5-12. PINCNTLx Register Reset Value Examples

| HEX ADDRESS RANGE | PINCNTLx REGISTER NAME | Bits 31:24 | Bits 23:20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 | Bits 15:8 | Bits 7:0 | REGISTER RESET VALUE |
|---|---|---|---|---|---|---|---|---|---|---|
| | | RESERVED | RESERVED | RSV | RSV | PLLTYPESEL | PLLUDEN | RESERVED | MUXMODE[7:0] | |
| 0x4814 0800 | PINCNTL1 | 00h | 0h | 0 | 1 | 1 | 0 | 00h | 00h | 0x0006 0000 |
| 0x4814 0804 | PINCNTL2 | 00h | 0h | 1 | 1 | 1 | 0 | 00h | 00h | 0x000E 0000 |
| 0x4814 0808 | PINCNTL3 | 00h | 0h | 1 | 1 | 1 | 0 | 00h | 00h | 0x000E 0000 |
| | | | | … | | | | | | |
| 0x4814 0C34 | PINCNTL270 | 00h | 0h | 1 | 1 | 0 | 0 | 00h | 00h | 0x000C 0000 |

(1) "(M0)" represents multimuxed option "0" for this pin function, "(M1)" represents multimuxed option "1" for this pin function, ... etc.

(2) Within this MUXMODE setting, EMAC[x] GMII or RGMII pin functions are selected via the RGMII0_EN and/or RGMII1_EN bits (8 and 9, respectively) in the GMII_SEL register [0x4814_0650] of the Control Module. "0" = GMII (default) and "1" = RGMII.

## Table 5-13. PINCNTLx Registers MUXMODE Functions

| HEX ADDRESS | REGISTER NAME | PIN NO. | REGISTER RESET VALUE | MUXMODE[7:0] SETTINGS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 0x1 | 0x2 | 0x4 | 0x8 | 0x10 | 0x20 | 0x40 | 0x80 |
| 0x4814 0800 | PINCNTL1 | P3 | 0x0006 0000 | SD1_CLK | | | | | | | |
| 0x4814 0804 | PINCNTL2 | P2 | 0x000E 0000 | SD1_CMD(M0) | | | | | | | GP0[0] |
| 0x4814 0808 | PINCNTL3 | P1 | 0x000E 0000 | SD1_DAT[0] | | | | | | | |
| 0x4814 080C | PINCNTL4 | P5 | 0x000E 0000 | SD1_DAT[1]_$\overline{\text{SDIRQ}}$ | | | | | | | |
| 0x4814 0810 | PINCNTL5 | P4 | 0x000E 0000 | SD1_DAT[2]_SDR$\overline{\text{W}}$ | | | | | | | |
| 0x4814 0814 | PINCNTL6 | P6 | 0x000E 0000 | SD1_DAT[3] | | | | | | | |
| 0x4814 0818 | PINCNTL7 | W6 | 0x000E 0000 | DEVOSC_WAKE | $\overline{\text{SPI[1]_SCS[1]}}$ | | | | | TIM5_IO(M1) | GP1[7](M0) |
| 0x4814 081C | PINCNTL8 | Y6 | 0x0006 0000 | SD0_CLK | | | | | | | GP0[1] |
| 0x4814 0820 | PINCNTL9 | N1 | 0x000E 0000 | SD0_CMD | SD1_CMD(M1) | | | | | | GP0[2] |
| 0x4814 0824 | PINCNTL10 | R7 | 0x000E 0000 | SD0_DAT[0] | SD1_DAT[4] | | | | | | GP0[3] |
| 0x4814 0828 | PINCNTL11 | Y5 | 0x000E 0000 | SD0_DAT[1]_$\overline{\text{SDIRQ}}$ | SD1_DAT[5] | | | | | | GP0[4] |
| 0x4814 082C | PINCNTL12 | Y3 | 0x000E 0000 | SD0_DAT[2]_SDR$\overline{\text{W}}$ | SD1_DAT[6] | | | | | | GP0[5] |
| 0x4814 0830 | PINCNTL13 | Y4 | 0x000E 0000 | SD0_DAT[3] | SD1_DAT[7] | | | | | | GP0[6] |
| 0x4814 0834 | PINCNTL14 | L5 | 0x000C 0000 | AUD_CLKIN0 | MCA[0]_AXR[7](M1) | MCA[0]_AHCLKX | MCA[3]_AHCLKX | | | | USB1_DRVVBUS |
| 0x4814 0838 | PINCNTL15 | R5 | 0x000C 0000 | AUD_CLKIN1 | MCA[0]_AXR[8](M1) | MCA[1]_AHCLKX | MCA[4]_AHCLKX | | EDMA_EVT3(M1) | TIM2_IO(M1) | GP0[8] |
| 0x4814 083C | PINCNTL16 | H1 | 0x000C 0000 | AUD_CLKIN2 | MCA[0]_AXR[9](M1) | MCA[2]_AHCLKX | MCA[5]_AHCLKX | | EDMA_EVT2(M1) | TIM3_IO(M1) | GP0[9] |
| 0x4814 0840 | PINCNTL17 | R4 | 0x0004 0000 | MCA[0]_ACLKX | | | | | | | |
| 0x4814 0844 | PINCNTL18 | L3 | 0x000C 0000 | MCA[0]_AFSX | | | | | | | |
| 0x4814 0848 | PINCNTL19 | K2 | 0x0004 0000 | MCA[0]_ACLKR | MCA[5]_AXR[2] | | | | | | |
| 0x4814 084C | PINCNTL20 | K1 | 0x000C 0000 | MCA[0]_AFSR | MCA[5]_AXR[3] | | | | | | |

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## Table 5-13. PINCNTLx Registers MUXMODE Functions (continued)

| HEX ADDRESS | REGISTER NAME | PIN NO. | REGISTER RESET VALUE | MUXMODE[7:0] SETTINGS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 0x1 | 0x2 | 0x4 | 0x8 | 0x10 | 0x20 | 0x40 | 0x80 |
| 0x4814 0850 | PINCNTL21 | J2 | 0x000C 0000 | MCA[0]_AXR[0] | | | | | | | |
| 0x4814 0854 | PINCNTL22 | J1 | 0x000E 0000 | MCA[0]_AXR[1] | | | | | I2C[3]_SCL(M0) | | |
| 0x4814 0858 | PINCNTL23 | L4 | 0x000E 0000 | MCA[0]_AXR[2] | | | | | I2C[3]_SDA(M0) | | |
| 0x4814 085C | PINCNTL24 | M5 | 0x000C 0000 | MCA[0]_AXR[3] | | | | | | | |
| 0x4814 0860 | PINCNTL25 | R6 | 0x000C 0000 | MCA[0]_AXR[4] | MCA[1]_AXR[8](M0) | | | | | | |
| 0x4814 0864 | PINCNTL26 | M3 | 0x000C 0000 | MCA[0]_AXR[5] | MCA[1]_AXR[9](M0) | | | | | | |
| 0x4814 0868 | PINCNTL27 | M4 | 0x000C 0000 | MCA[0]_AXR[6] | MCB_DR | | | | | | |
| 0x4814 086C | PINCNTL28 | L2 | 0x000C 0000 | MCA[0]_AXR[7](M0) | MCB_DX | | | | | | |
| 0x4814 0870 | PINCNTL29 | L1 | 0x000C 0000 | MCA[0]_AXR[8](M0) | MCB_FSX | MCB_FSR(M1) | | | | | |
| 0x4814 0874 | PINCNTL30 | M6 | 0x000C 0000 | MCA[0]_AXR[9](M0) | MCB_CLKX | MCB_CLKR(M1) | | | | | |
| 0x4814 0878 | PINCNTL31 | U5 | 0x0004 0000 | MCA[1]_ACLKX | | | | | | | |
| 0x4814 087C | PINCNTL32 | V3 | 0x000C 0000 | MCA[1]_AFSX | | | | | | | |
| 0x4814 0880 | PINCNTL33 | M1 | 0x0004 0000 | MCA[1]_ACLKR | MCA[1]_AXR[4] | | | | | | |
| 0x4814 0884 | PINCNTL34 | M2 | 0x000C 0000 | MCA[1]_AFSR | MCA[1]_AXR[5] | | | | | | |
| 0x4814 0888 | PINCNTL35 | V4 | 0x000E 0000 | MCA[1]_AXR[0] | SD0_DAT[4] | | | | | | |
| 0x4814 088C | PINCNTL36 | T6 | 0x000E 0000 | MCA[1]_AXR[1] | SD0_DAT[5] | | | | | | |
| 0x4814 0890 | PINCNTL37 | R3 | 0x000C 0000 | MCA[1]_AXR[2] | MCB_FSR(M0) | | | | | | |
| 0x4814 0894 | PINCNTL38 | N6 | 0x000C 0000 | MCA[1]_AXR[3] | MCB_CLKR(M0) | | | | | | |
| 0x4814 0898 | PINCNTL39 | U6 | 0x0006 0000 | MCA[2]_ACLKX | | | | | | | GP0[10](M1) |
| 0x4814 089C | PINCNTL40 | AA5 | 0x000E 0000 | MCA[2]_AFSX | | | | | | | GP0[11](M1) |
| 0x4814 08A0 | PINCNTL41 | N2 | 0x000E 0000 | MCA[2]_AXR[0] | SD0_DAT[6] | | | | UART5_RXD(M3) | | GP0[12](M1) |
| 0x4814 08A4 | PINCNTL42 | V6 | 0x000E 0000 | MCA[2]_AXR[1] | SD0_DAT[7] | | | | UART5_TXD(M3) | | GP0[13](M1) |
| 0x4814 08A8 | PINCNTL43 | V5 | 0x000C 0000 | MCA[2]_AXR[2] | MCA[1]_AXR[6] | | | | | TIM2_IO(M0) | GP0[14](M1) |
| 0x4814 08AC | PINCNTL44 | H2 | 0x000C 0000 | MCA[2]_AXR[3] | MCA[1]_AXR[7] | | | | | TIM3_IO(M0) | GP0[15](M1) |
| 0x4814 08B0 | PINCNTL45 | G6 | 0x0004 0000 | MCA[3]_ACLKX | | | | | | | GP0[16](M1) |
| 0x4814 08B4 | PINCNTL46 | H4 | 0x000C 0000 | MCA[3]_AFSX | | | | | | | GP0[17](M1) |
| 0x4814 08B8 | PINCNTL47 | G1 | 0x000C 0000 | MCA[3]_AXR[0] | | | | | | TIM4_IO(M0) | GP0[18](M1) |
| 0x4814 08BC | PINCNTL48 | G2 | 0x000C 0000 | MCA[3]_AXR[1] | | | | | | TIM5_IO(M0) | GP0[19](M1) |
| 0x4814 08C0 | PINCNTL49 | F2 | 0x000C 0000 | MCA[3]_AXR[2] | MCA[1]_AXR[8](M1) | | | | | | GP0[20](M1) |
| 0x4814 08C4 | PINCNTL50 | J6 | 0x000C 0000 | MCA[3]_AXR[3] | MCA[1]_AXR[9](M1) | | | | | | |
| 0x4814 08C8 | PINCNTL51 | K7 | 0x0004 0000 | MCA[4]_ACLKX | | | | | | | GP0[21](M1) |
| 0x4814 08CC | PINCNTL52 | H3 | 0x000C 0000 | MCA[4]_AFSX | | | | | | | GP0[22](M1) |
| 0x4814 08D0 | PINCNTL53 | H6 | 0x000C 0000 | MCA[4]_AXR[0] | | | | | | | GP0[23](M1) |
| 0x4814 08D4 | PINCNTL54 | J4 | 0x000C 0000 | MCA[4]_AXR[1] | | | | | | TIM6_IO(M0) | GP0[24](M1) |


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## Table 5-13. PINCNTLx Registers MUXMODE Functions (continued)

| HEX ADDRESS | REGISTER NAME | PIN NO. | REGISTER RESET VALUE | MUXMODE[7:0] SETTINGS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 0x1 | 0x2 | 0x4 | 0x8 | 0x10 | 0x20 | 0x40 | 0x80 |
| 0x4814 08D8 | PINCNTL55 | J3 | 0x000C 0000 | MCA[5]_ACLKX | | | | | | | GP0[25](M1) |
| 0x4814 08DC | PINCNTL56 | H5 | 0x000C 0000 | MCA[5]_AFSX | | | | | | | GP0[26](M1) |
| 0x4814 08E0 | PINCNTL57 | L7 | 0x000C 0000 | MCA[5]_AXR[0] | MCA[4]_AXR[2] | | | | | | GP0[27](M1) |
| 0x4814 08E4 | PINCNTL58 | L6 | 0x000C 0000 | MCA[5]_AXR[1] | MCA[4]_AXR[3] | | | | | TIM7_IO(M0) | GP0[28](M1) |
| 0x4814 08E8 | PINCNTL59 | U4 | 0x0004 0000 | | | | UART2_RXD(M1) | | | | GP0[29] |
| 0x4814 08EC | PINCNTL60 | T2 | 0x0004 0000 | | | | TCLKIN | | | | GP0[30] |
| 0x4814 08F0 | PINCNTL61 | U3 | 0x000C 0000 | | | | UART2_TXD(M1) | | | | GP0[31] |
| 0x4814 08F4 | PINCNTL62 | W1 | 0x000C 0000 | | | | | | | | GP1[7](M1) |
| 0x4814 08F8 | PINCNTL63 | W2 | 0x000E 0000 | | | | | | | | GP1[8](M1) |
| 0x4814 08FC | PINCNTL64 | V1 | 0x000C 0000 | | | | | | | | GP1[9](M1) |
| 0x4814 0900 | PINCNTL65 | V2 | 0x000E 0000 | | | | | | | | GP1[10](M1) |
| 0x4814 0904 | PINCNTL66 | – | 0x000C 0000 | Reserved. ***Do Not*** Program this Register. | | | | | | | |
| 0x4814 0908 | PINCNTL67 | – | 0x000E 0000 | Reserved. ***Do Not*** Program this Register. | | | | | | | |
| 0x4814 090C | PINCNTL68 | AH6 | 0x000E 0000 | DCAN0_TX | UART2_TXD(M2) | | | | I2C[3]_SDA(M1) | | GP1[0] |
| 0x4814 0910 | PINCNTL69 | AG6 | 0x000E 0000 | DCAN0_RX | UART2_RXD(M2) | | | | I2C[3]_SCL(M1) | | GP1[1] |
| 0x4814 0914 | PINCNTL70 | AH5 | 0x000E 0000 | UART0_RXD | | | | | | | |
| 0x4814 0918 | PINCNTL71 | AG5 | 0x000E 0000 | UART0_TXD | | | | | | | |
| 0x4814 091C | PINCNTL72 | AE6 | 0x000E 0000 | $\overline{\text{UART0_CTS}}$ | UART4_RXD(M3) | | DCAN1_TX | $\overline{\text{SPI[1]_SCS[3]}}$ | | SD0_SDCD | |
| 0x4814 0920 | PINCNTL73 | AF5 | 0x000E 0000 | $\overline{\text{UART0_RTS}}$ | UART4_TXD(M3) | | DCAN1_RX | $\overline{\text{SPI[1]_SCS[2]}}$ | | SD2_SDCD | |
| 0x4814 0924 | PINCNTL74 | AH4 | 0x000E 0000 | $\overline{\text{UART0_DCD}}$ | UART3_RXD(M0) | | | $\overline{\text{SPI[0]_SCS[3]}}$ | I2C[2]_SCL(M0) | SD1_POW | GP1[2] |
| 0x4814 0928 | PINCNTL75 | AG4 | 0x000E 0000 | $\overline{\text{UART0_DSR}}$ | UART3_TXD(M0) | | | $\overline{\text{SPI[0]_SCS[2]}}$ | I2C[2]_SDA(M0) | SD1_SDWP | GP1[3] |
| 0x4814 092C | PINCNTL76 | AG2 | 0x000E 0000 | $\overline{\text{UART0_DTR}}$ | $\overline{\text{UART3_CTS}}$(M0) | UART1_TXD(M0) | | | | | GP1[4] |
| 0x4814 0930 | PINCNTL77 | AF4 | 0x000E 0000 | UART0_RIN | $\overline{\text{UART3_RTS}}$(M0) | UART1_RXD(M0) | | | | | GP1[5] |
| 0x4814 0934 | PINCNTL78 | AF24 | 0x000E 0000 | I2C[1]_SCL | HDMI_SCL(M0) | | | | | | |
| 0x4814 0938 | PINCNTL79 | AG24 | 0x000E 0000 | I2C[1]_SDA | HDMI_SDA(M0) | | | | | | |
| 0x4814 093C | PINCNTL80 | AE5 | 0x0006 0000 | $\overline{\text{SPI[0]_SCS[1]}}$ | SD1_SDCD | | | | EDMA_EVT1(M1) | TIM4_IO(M1) | GP1[6] |
| 0x4814 0940 | PINCNTL81 | AD6 | 0x0006 0000 | $\overline{\text{SPI[0]_SCS[0]}}$ | | | | | | | |
| 0x4814 0944 | PINCNTL82 | AC7 | 0x0006 0000 | SPI[0]_SCLK | | | | | | | |
| 0x4814 0948 | PINCNTL83 | AF3 | 0x0006 0000 | SPI[0]_D[1] | | | | | | | |
| 0x4814 094C | PINCNTL84 | AE3 | 0x0006 0000 | SPI[0]_D[0] | | | | | | | |
| 0x4814 0950 | PINCNTL85 | AD3 | 0x0006 0000 | $\overline{\text{SPI[1]_SCS[0]}}$ | | | | | | | GP1[16](M1) |
| 0x4814 0954 | PINCNTL86 | AC3 | 0x0006 0000 | SPI[1]_SCLK | | | | | | | GP1[17](M1) |
| 0x4814 0958 | PINCNTL87 | AA3 | 0x0006 0000 | SPI[1]_D[1] | | | | | | | GP1[18](M1) |
| 0x4814 095C | PINCNTL88 | AA6 | 0x0006 0000 | SPI[1]_D[0] | | | | | | | GP1[26](M1) |

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## Table 5-13. PINCNTLx Registers MUXMODE Functions (continued)

| HEX ADDRESS | REGISTER NAME | PIN NO. | REGISTER RESET VALUE | MUXMODE[7:0] SETTINGS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 0x1 | 0x2 | 0x4 | 0x8 | 0x10 | 0x20 | 0x40 | 0x80 |
| 0x4814 0960 | PINCNTL89 | U26 | 0x0005 0000 | GPMC_D[0] | | | | | | | BTMODE[0] |
| 0x4814 0964 | PINCNTL90 | Y28 | 0x0005 0000 | GPMC_D[1] | | | | | | | BTMODE[1] |
| 0x4814 0968 | PINCNTL91 | V27 | 0x0005 0000 | GPMC_D[2] | | | | | | | BTMODE[2] |
| 0x4814 096C | PINCNTL92 | W27 | 0x0005 0000 | GPMC_D[3] | | | | | | | BTMODE[3] |
| 0x4814 0970 | PINCNTL93 | V26 | 0x0005 0000 | GPMC_D[4] | | | | | | | BTMODE[4] |
| 0x4814 0974 | PINCNTL94 | AA28 | 0x0005 0000 | GPMC_D[5] | | | | | | | BTMODE[5] |
| 0x4814 0978 | PINCNTL95 | U25 | 0x0005 0000 | GPMC_D[6] | | | | | | | BTMODE[6] |
| 0x4814 097C | PINCNTL96 | V25 | 0x0005 0000 | GPMC_D[7] | | | | | | | BTMODE[7] |
| 0x4814 0980 | PINCNTL97 | Y27 | 0x0005 0000 | GPMC_D[8] | | | | | | | BTMODE[8] |
| 0x4814 0984 | PINCNTL98 | AB28 | 0x0005 0000 | GPMC_D[9] | | | | | | | BTMODE[9] |
| 0x4814 0988 | PINCNTL99 | Y26 | 0x0005 0000 | GPMC_D[10] | | | | | | | BTMODE[10] |
| 0x4814 098C | PINCNTL100 | AA27 | 0x0005 0000 | GPMC_D[11] | | | | | | | BTMODE[11] |
| 0x4814 0990 | PINCNTL101 | U24 | 0x0005 0000 | GPMC_D[12] | | | | | | | BTMODE[12] |
| 0x4814 0994 | PINCNTL102 | U23 | 0x0005 0000 | GPMC_D[13] | | | | | | | BTMODE[13] |
| 0x4814 0998 | PINCNTL103 | V24 | 0x0005 0000 | GPMC_D[14] | | | | | | | BTMODE[14] |
| 0x4814 099C | PINCNTL104 | Y25 | 0x0005 0000 | GPMC_D[15] | | | | | | | BTMODE[15] |
| 0x4814 09A0 | PINCNTL105 | AD27 | 0x0004 0000 | GPMC_A[16] | | | | | | | GP2[5](M0) |
| 0x4814 09A4 | PINCNTL106 | V23 | 0x0004 0000 | GPMC_A[17] | | | | | | | GP2[6](M0) |
| 0x4814 09A8 | PINCNTL107 | AE28 | 0x0004 0000 | GPMC_A[18] | | | | | | TIM2_IO(M2) | GP1[13](M0) |
| 0x4814 09AC | PINCNTL108 | AC27 | 0x0004 0000 | GPMC_A[19] | | | | | | TIM3_IO(M2) | GP1[14](M0) |
| 0x4814 09B0 | PINCNTL109 | AD28 | 0x0006 0000 | GPMC_A[20](M0) | | SPI[2]_SCS[1] | | | | | GP1[15](M0) |
| 0x4814 09B4 | PINCNTL110 | AC28 | 0x0004 0000 | GPMC_A[21](M0) | | SPI[2]_D[0](M0) | | | | | GP1[16](M0) |
| 0x4814 09B8 | PINCNTL111 | AB27 | 0x0006 0000 | GPMC_A[22](M0) | | SPI[2]_D[1](M0) | | HDMI_CEC(M0) | | TIM4_IO(M2) | GP1[17](M0) |
| 0x4814 09BC | PINCNTL112 | AA26 | 0x0004 0000 | GPMC_A[23](M0) | | SPI[2]_SCLK(M0) | | HDMI_HPDET(M0) | | TIM5_IO(M2) | GP1[18](M0) |
| 0x4814 09C0 | PINCNTL113 | L25 | 0x0006 0000 | SD2_DAT[7] | GPMC_A[24](M0) | GPMC_A[20](M1) | | | UART2_RXD(M3) | | GP1[19] |
| 0x4814 09C4 | PINCNTL114 | N23 | 0x0006 0000 | SD2_DAT[6] | GPMC_A[25](M0) | GPMC_A[21](M1) | | | UART2_TXD(M3) | | GP1[20] |
| 0x4814 09C8 | PINCNTL115 | P22 | 0x0006 0000 | SD2_DAT[5] | GPMC_A[26](M0) | GPMC_A[22](M1) | | | | TIM6_IO(M2) | GP1[21] |
| 0x4814 09CC | PINCNTL116 | R24 | 0x0006 0000 | SD2_DAT[4] | GPMC_A[27](M0) | GPMC_A[23](M1) | GPMC_CS[7] | | EDMA_EVT0(M1) | TIM7_IO(M2) | GP1[22] |
| 0x4814 09D0 | PINCNTL117 | J28 | 0x0006 0000 | SD2_DAT[3] | GPMC_A[1](M1) | | | | | | GP2[5](M1) |
| 0x4814 09D4 | PINCNTL118 | K27 | 0x0006 0000 | SD2_DAT[2]_SDRW | GPMC_A[2](M1) | | | | | | GP2[6](M1) |
| 0x4814 09D8 | PINCNTL119 | M24 | 0x0006 0000 | SD2_DAT[1]_SDIRQ | GPMC_A[3](M1) | | | | | | GP1[13](M1) |
| 0x4814 09DC | PINCNTL120 | L26 | 0x0006 0000 | SD2_DAT[0] | GPMC_A[4](M1) | | | | | | GP1[14](M1) |
| 0x4814 09E0 | PINCNTL121 | M23 | 0x0006 0000 | SD2_CLK | | | | | | | GP1[15](M1) |
| 0x4814 09E4 | PINCNTL122 | T28 | 0x0006 0000 | GPMC_CS[0] | | | | | | | GP1[23] |
| 0x4814 09E8 | PINCNTL123 | K28 | 0x0006 0000 | GPMC_CS[1] | GPMC_A[25](M1) | | | | | | GP1[24] |


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## Table 5-13. PINCNTLx Registers MUXMODE Functions (continued)

| HEX ADDRESS | REGISTER NAME | PIN NO. | REGISTER RESET VALUE | MUXMODE[7:0] SETTINGS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 0x1 | 0x2 | 0x4 | 0x8 | 0x10 | 0x20 | 0x40 | 0x80 |
| 0x4814 09EC | PINCNTL124 | M25 | 0x0006 0000 | GPMC_CS[2] | GPMC_A[24](M1) | | | | | | GP1[25] |
| 0x4814 09F0 | PINCNTL125 | P26 | 0x0006 0000 | GPMC_CS[3] | | SPI[2]_SCS[0] | | | | | GP1[26](M0) |
| 0x4814 09F4 | PINCNTL126 | P25 | 0x0006 0000 | GPMC_CS[4] | SD2_CMD | | | | | | GP1[8](M0) |
| 0x4814 09F8 | PINCNTL127 | R26 | 0x0006 0000 | GPMC_CLK | GPMC_CS[5] | | GPMC_WAIT[1] | CLKOUT1 | EDMA_EVT3(M0) | TIM4_IO(M3) | GP1[27] |
| 0x4814 09FC | PINCNTL128 | M26 | 0x0006 0000 | GPMC_ADV_ALE | GPMC_CS[6] | | | | | TIM5_IO(M3) | GP1[28] |
| 0x4814 0A00 | PINCNTL129 | T27 | 0x0006 0000 | GPMC_OE_RE | | | | | | | |
| 0x4814 0A04 | PINCNTL130 | U28 | 0x0006 0000 | GPMC_WE | | | | | | | |
| 0x4814 0A08 | PINCNTL131 | U27 | 0x0004 0000 | GPMC_BE[0]_CLE | GPMC_A[25](M2) | | | | EDMA_EVT2(M0) | TIM6_IO(M3) | GP1[29] |
| 0x4814 0A0C | PINCNTL132 | V28 | 0x0004 0000 | GPMC_BE[1] | GPMC_A[24](M2) | | | | EDMA_EVT1(M0) | TIM7_IO(M3) | GP1[30] |
| 0x4814 0A10 | PINCNTL133 | W28 | 0x0006 0000 | GPMC_WAIT[0] | GPMC_A[26](M2) | | | | EDMA_EVT0(M0) | | GP1[31] |
| 0x4814 0A14 | PINCNTL134 | AE17 | 0x0004 0000 | VIN[0]B_CLK | | | | | CLKOUT0 | | GP1[9](M0) |
| 0x4814 0A18 | PINCNTL135 | AE21 | 0x000E 0000 | VIN[0]A_DE(M0) | | | | VIN[0]B_HSYNC | UART5_TXD(M1) | I2C[2]_SDA(M1) | GP2[0] |
| 0x4814 0A1C | PINCNTL136 | AA20 | 0x000E 0000 | VIN[0]A_FLD(M0) | | | | VIN[0]B_VSYNC | UART5_RXD(M1) | I2C[2]_SCL(M3) | GP2[1] |
| 0x4814 0A20 | PINCNTL137 | AB20 | 0x000C 0000 | VIN[0]A_CLK | | | | | | | GP2[2](M1) |
| 0x4814 0A24 | PINCNTL138 | AC20 | 0x000E 0000 | VIN[0]A_HSYNC | | | | | UART5_RTS(M1) | | GP2[3] |
| 0x4814 0A28 | PINCNTL139 | AD20 | 0x000E 0000 | VIN[0]A_VSYNC | | | | | UART5_CTS(M1) | | GP2[4] |
| 0x4814 0A2C | PINCNTL140 | AF9 | 0x000C 0000 | VIN[0]A_D[0] | | | | | | | GP1[11](M1) |
| 0x4814 0A30 | PINCNTL141 | AB11 | 0x000C 0000 | VIN[0]A_D[1] | | | | | | | GP1[12](M1) |
| 0x4814 0A34 | PINCNTL142 | AC9 | 0x000C 0000 | VIN[0]A_D[2] | | | | | | | GP2[7] |
| 0x4814 0A38 | PINCNTL143 | AE12 | 0x000C 0000 | VIN[0]A_D[3] | | | | | | | GP2[8] |
| 0x4814 0A3C | PINCNTL144 | AH8 | 0x000C 0000 | VIN[0]A_D[4] | | | | | | | GP2[9] |
| 0x4814 0A40 | PINCNTL145 | AG16 | 0x000C 0000 | VIN[0]A_D[5] | | | | | | | GP2[10] |
| 0x4814 0A44 | PINCNTL146 | AH16 | 0x000C 0000 | VIN[0]A_D[6] | | | | | | | GP2[11] |
| 0x4814 0A48 | PINCNTL147 | AA11 | 0x000C 0000 | VIN[0]A_D[7] | | | | | | | GP2[12] |
| 0x4814 0A4C | PINCNTL148 | AB15 | 0x000C 0000 | VIN[0]A_D[8]_BD[0] | | | | | | | GP2[13] |
| 0x4814 0A50 | PINCNTL149 | AG9 | 0x000C 0000 | VIN[0]A_D[9]_BD[1] | | | | | | | GP2[14] |
| 0x4814 0A54 | PINCNTL150 | AH9 | 0x000C 0000 | VIN[0]A_D[10]_BD[2] | | | | | | | GP2[15] |
| 0x4814 0A58 | PINCNTL151 | AH17 | 0x000C 0000 | VIN[0]A_D[11]_BD[3] | | | | | CAM_WE(M1) | | GP2[16] |
| 0x4814 0A5C | PINCNTL152 | AG17 | 0x0004 0000 | VIN[0]A_D[12]_BD[4] | | | | | CLKOUT1 | | GP2[17] |
| 0x4814 0A60 | PINCNTL153 | AF17 | 0x000C 0000 | VIN[0]A_D[13]_BD[5] | | | | | CAM_RESET | | GP2[18] |
| 0x4814 0A64 | PINCNTL154 | AC12 | 0x000C 0000 | VIN[0]A_D[14]_BD[6] | | | | | CAM_STROBE | | GP2[19] |
| 0x4814 0A68 | PINCNTL155 | AC14 | 0x000C 0000 | VIN[0]A_D[15]_BD[7] | | | | | CAM_SHUTTER | | GP2[20] |
| 0x4814 0A6C | PINCNTL156 | AA21 | 0x000E 0000 | VIN[0]A_D[16] | CAM_D[8] | | | | I2C[2]_SCL(M1) | | GP0[10](M0) |
| 0x4814 0A70 | PINCNTL157 | AB21 | 0x000C 0000 | VIN[0]A_D[17] | CAM_D[9] | | EMAC[1]_RMRXER(M1) | | | | GP0[11](M0) |

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## Table 5-13. PINCNTLx Registers MUXMODE Functions (continued)

| HEX ADDRESS | REGISTER NAME | PIN NO. | REGISTER RESET VALUE | MUXMODE[7:0] SETTINGS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 0x1 | 0x2 | 0x4 | 0x8 | 0x10 | 0x20 | 0x40 | 0x80 |
| 0x4814 0A74 | PINCNTL158 | AF20 | 0x000E 0000 | VIN[0]A_D[18] | CAM_D[10] | | EMAC[1]_RMRXD[1](M1) | | I2C[3]_SCL(M2) | | GP0[12](M0) |
| 0x4814 0A78 | PINCNTL159 | AF21 | 0x000E 0000 | VIN[0]A_D[19] | CAM_D[11] | | EMAC[1]_RMRXD[0](M1) | | I2C[3]_SDA(M2) | | GP0[13](M0) |
| 0x4814 0A7C | PINCNTL160 | AC17 | 0x000C 0000 | VIN[0]A_D[20] | CAM_D[12] | | EMAC[1]_RMCRSDV(M1) | | $\overline{\text{SPI[3]_SCS[0]}}$ | | GP0[14](M0) |
| 0x4814 0A80 | PINCNTL161 | AE18 | 0x0004 0000 | VIN[0]A_D[21] | CAM_D[13] | | EMAC[1]_RMTXD[0](M1) | | SPI[3]_SCLK(M0) | | GP0[15](M0) |
| 0x4814 0A84 | PINCNTL162 | AC21 | 0x0004 0000 | VIN[0]A_D[22] | CAM_D[14] | | EMAC[1]_RMTXD[1](M1) | | SPI[3]_D[1](M0) | | GP0[16](M0) |
| 0x4814 0A88 | PINCNTL163 | AC16 | 0x0004 0000 | VIN[0]A_D[23] | CAM_D[15] | | EMAC[1]_RMTXEN(M1) | | SPI[3]_D[0](M0) | | GP0[17](M0) |
| 0x4814 0A8C | PINCNTL164 | AB17 | 0x0006 0000 | VIN[0]A_DE(M1) | CAM_D[7] | | | | | | GP0[18](M0) |
| 0x4814 0A90 | PINCNTL165 | AC15 | 0x0006 0000 | VIN[0]B_DE | CAM_D[6] | | | | | | GP0[19](M0) |
| 0x4814 0A94 | PINCNTL166 | AC22 | 0x0006 0000 | VIN[0]A_FLD(M1) | CAM_D[5] | | | | | | GP0[20](M0) |
| 0x4814 0A98 | PINCNTL167 | AD17 | 0x0006 0000 | VIN[0]B_FLD | CAM_D[4] | | | | | | GP0[21](M0) |
| 0x4814 0A9C | PINCNTL168 | AD18 | 0x0006 0000 | VOUT[1]_G_Y_YC[1] | CAM_D[3] | | | GPMC_A[5](M1) | UART4_RXD(M0) | | GP0[22](M0) |
| 0x4814 0AA0 | PINCNTL169 | AC18 | 0x0004 0000 | VOUT[1]_G_Y_YC[0] | CAM_D[2] | | | GPMC_A[6](M1) | UART4_TXD(M0) | | GP0[23](M0) |
| 0x4814 0AA4 | PINCNTL170 | AC19 | 0x0004 0000 | VOUT[1]_R_CR[1] | CAM_D[1] | | | GPMC_A[7](M1) | $\overline{\text{UART4_CTS}}$(M0) | | GP0[24](M0) |
| 0x4814 0AA8 | PINCNTL171 | AA22 | 0x0004 0000 | VOUT[1]_R_CR[0] | CAM_D[0] | | | GPMC_A[8](M1) | $\overline{\text{UART4_RTS}}$(M0) | | GP0[25](M0) |
| 0x4814 0AAC | PINCNTL172 | AE23 | 0x0004 0000 | VOUT[1]_B_CB_C[1] | CAM_HS | | | GPMC_A[9](M1) | UART2_RXD(M0) | | GP0[26](M0) |
| 0x4814 0AB0 | PINCNTL173 | AD23 | 0x0006 0000 | VOUT[1]_B_CB_C[0] | CAM_VS | | | GPMC_A[10](M1) | UART2_TXD(M0) | | GP0[27](M0) |
| 0x4814 0AB4 | PINCNTL174 | AB23 | 0x0004 0000 | VOUT[1]_FLD | CAM_FLD | $\overline{\text{CAM_WE}}$(M0) | | GPMC_A[11](M1) | $\overline{\text{UART2_CTS}}$ | | GP0[28](M0) |
| 0x4814 0AB8 | PINCNTL175 | AF18 | 0x0004 0000 | VOUT[0]_FLD(M1) | CAM_PCLK | | | GPMC_A[12](M1) | $\overline{\text{UART2_RTS}}$ | | GP2[2](M0) |
| 0x4814 0ABC | PINCNTL176 | AD12 | 0x000C 0000 | VOUT[0]_CLK | | | | | | | |
| 0x4814 0AC0 | PINCNTL177 | AC11 | 0x000C 0000 | VOUT[0]_HSYNC | | | | | | | |
| 0x4814 0AC4 | PINCNTL178 | AB13 | 0x000C 0000 | VOUT[0]_VSYNC | | | | | | | |
| 0x4814 0AC8 | PINCNTL179 | AA10 | 0x000C 0000 | VOUT[0]_AVID | VOUT[0]_FLD(M0) | | | SPI[3]_SCLK(M2) | | TIM7_IO(M1) | GP2[21] |
| 0x4814 0ACC | PINCNTL180 | AG7 | 0x000C 0000 Reset by GCR Only | VOUT[0]_B_CB_C[2] | EMU2 | | | | | | GP2[22] |
| 0x4814 0AD0 | PINCNTL181 | AE15 | 0x000C 0000 | VOUT[0]_B_CB_C[3] | | | | | | | GP2[23] |
| 0x4814 0AD4 | PINCNTL182 | AD11 | 0x000C 0000 | VOUT[0]_B_CB_C[4] | | | | | | | |
| 0x4814 0AD8 | PINCNTL183 | AD15 | 0x000C 0000 | VOUT[0]_B_CB_C[5] | | | | | | | |
| 0x4814 0ADC | PINCNTL184 | AC10 | 0x000C 0000 | VOUT[0]_B_CB_C[6] | | | | | | | |
| 0x4814 0AE0 | PINCNTL185 | AB10 | 0x000C 0000 | VOUT[0]_B_CB_C[7] | | | | | | | |
| 0x4814 0AE4 | PINCNTL186 | AF15 | 0x000C 0000 | VOUT[0]_B_CB_C[8] | | | | | | | |


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## Table 5-13. PINCNTLx Registers MUXMODE Functions (continued)

| HEX ADDRESS | REGISTER NAME | PIN NO. | REGISTER RESET VALUE | MUXMODE[7:0] SETTINGS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 0x1 | 0x2 | 0x4 | 0x8 | 0x10 | 0x20 | 0x40 | 0x80 |
| 0x4814 0AE8 | PINCNTL187 | AG15 | 0x000C 0000 | VOUT[0]_B_CB_C[9] | | | | | | | |
| 0x4814 0AEC | PINCNTL188 | AH7 | 0x000C 0000 Reset by GCR Only | VOUT[0]_G_Y_YC[2] | EMU3 | | | | | | GP2[24] |
| 0x4814 0AF0 | PINCNTL189 | AH15 | 0x000C 0000 | VOUT[0]_G_Y_YC[3] | | | | | | | GP2[25] |
| 0x4814 0AF4 | PINCNTL190 | AB8 | 0x000C 0000 | VOUT[0]_G_Y_YC[4] | | | | | | | |
| 0x4814 0AF8 | PINCNTL191 | AB12 | 0x000C 0000 | VOUT[0]_G_Y_YC[5] | | | | | | | |
| 0x4814 0AFC | PINCNTL192 | AA8 | 0x000C 0000 | VOUT[0]_G_Y_YC[6] | | | | | | | |
| 0x48140B00 | PINCNTL193 | AD14 | 0x000C 0000 | VOUT[0]_G_Y_YC[7] | | | | | | | |
| 0x48140B04 | PINCNTL194 | AE14 | 0x000C 0000 | VOUT[0]_G_Y_YC[8] | | | | | | | |
| 0x48140B08 | PINCNTL195 | AF14 | 0x000C 0000 | VOUT[0]_G_Y_YC[9] | | | | | | | |
| 0x48140B0C | PINCNTL196 | AD9 | 0x000C 0000 Reset by GCR Only | VOUT[0]_R_CR[2] | EMU4 | | | | | | GP2[26] |
| 0x4814 0B10 | PINCNTL197 | AB9 | 0x000C 0000 | VOUT[0]_R_CR[3] | | | | | | | GP2[27] |
| 0x4814 0B14 | PINCNTL198 | AA9 | 0x000C 0000 | VOUT[0]_R_CR[4] | | | | | | | |
| 0x4814 0B18 | PINCNTL199 | AF8 | 0x000C 0000 | VOUT[0]_R_CR[5] | | | | | | | |
| 0x4814 0B1C | PINCNTL200 | AF6 | 0x000C 0000 | VOUT[0]_R_CR[6] | | | | | | | |
| 0x4814 0B20 | PINCNTL201 | AF12 | 0x000C 0000 | VOUT[0]_R_CR[7] | | | | | | | |
| 0x4814 0B24 | PINCNTL202 | AE8 | 0x000C 0000 | VOUT[0]_R_CR[8] | | | | | | | |
| 0x4814 0B28 | PINCNTL203 | AC13 | 0x000C 0000 | VOUT[0]_R_CR[9] | | | | | | | |
| 0x4814 0B2C | PINCNTL204 | AE24 | 0x0004 0000 | VOUT[1]_CLK | EMAC[1]_MTCLK | | | | | | GP2[28] |
| 0x4814 0B30 | PINCNTL205 | AC24 | 0x0004 0000 | VOUT[1]_HSYNC | EMAC[1]_MCOL | | | SPI[3]_D[1](M2) | $\overline{\text{UART3_RTS}}$(M1) | | GP2[29] |
| 0x4814 0B34 | PINCNTL206 | AA23 | 0x0004 0000 | VOUT[1]_VSYNC | EMAC[1]_MCRS | | | SPI[3]_D[0](M2) | $\overline{\text{UART3_CTS}}$(M1) | | GP2[30] |
| 0x4814 0B38 | PINCNTL207 | Y22 | 0x0004 0000 | VOUT[1]_AVID | EMAC[1]_MRXER | | | | $\overline{\text{UART4_RTS}}$(M2) | TIM6_IO(M1) | GP2[31] |
| 0x4814 0B3C | PINCNTL208 | AH25 | 0x0004 0000 | VOUT[1]_B_CB_C[3] | EMAC[1]_MRCLK | | | | $\overline{\text{UART4_CTS}}$(M2) | | GP3[0] |
| 0x4814 0B40 | PINCNTL209 | AG25 | 0x0004 0000 | VOUT[1]_B_CB_C[4] | EMAC[1]_MRXD[0] | | | | UART4_RXD(M2) | | GP3[1] |
| 0x4814 0B44 | PINCNTL210 | AF25 | 0x0004 0000 | VOUT[1]_B_CB_C[5] | EMAC[1]_MRXD[1] | | | | UART4_TXD(M2) | | GP3[2] |
| 0x4814 0B48 | PINCNTL211 | AD25 | 0x0004 0000 | VOUT[1]_B_CB_C[6] | EMAC[1]_MRXD[2] | | | | UART3_RXD(M1) | | GP3[3] |
| 0x48140B4C | PINCNTL212 | AC25 | 0x0004 0000 | VOUT[1]_B_CB_C[7] | EMAC[1]_MRXD[3] | | | | UART3_TXD(M1) | | GP3[4] |
| 0x4814 0B50 | PINCNTL213 | AH26 | 0x0004 0000 | VOUT[1]_B_CB_C[8] | EMAC[1]_MRXD[4] | | | | I2C[3]_SCL(M3) | | GP3[5] |
| 0x4814 0B54 | PINCNTL214 | AA24 | 0x0004 0000 | VOUT[1]_B_CB_C[9] | EMAC[1]_MRXD[5] | | | | I2C[3]_SDA(M3) | | GP3[6] |
| 0x4814 0B58 | PINCNTL215 | Y23 | 0x0004 0000 | VOUT[1]_G_Y_YC[3] | EMAC[1]_MRXD[6] | | | | | | GP3[7] |
| 0x4814 0B5C | PINCNTL216 | W22 | 0x0004 0000 | VOUT[1]_G_Y_YC[4] | EMAC[1]_MRXD[7] | | | | | | GP3[8] |
| 0x4814 0B60 | PINCNTL217 | AG26 | 0x0004 0000 | VOUT[1]_G_Y_YC[5] | EMAC[1]_MRXDV | | | | | | GP3[9] |
| 0x4814 0B64 | PINCNTL218 | AH27 | 0x0004 0000 | VOUT[1]_G_Y_YC[6] | EMAC[1]_GMTCLK | | | | | | GP3[10] |
| 0x4814 0B68 | PINCNTL219 | AF26 | 0x0004 0000 | VOUT[1]_G_Y_YC[7] | EMAC[1]_MTXD[0] | | | | | | GP3[11] |
| 0x4814 0B6C | PINCNTL220 | AE26 | 0x0004 0000 | VOUT[1]_G_Y_YC[8] | EMAC[1]_MTXD[1] | | | | | | GP3[12] |

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## Table 5-13. PINCNTLx Registers MUXMODE Functions (continued)

| HEX ADDRESS | REGISTER NAME | PIN NO. | REGISTER RESET VALUE | MUXMODE[7:0] SETTINGS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 0x1 | 0x2 | 0x4 | 0x8 | 0x10 | 0x20 | 0x40 | 0x80 |
| 0x4814 0B70 | PINCNTL221 | AD26 | 0x0004 0000 | VOUT[1]_G_Y_YC[9] | EMAC[1]_MTXD[2] | | | | | | GP3[13] |
| 0x4814 0B74 | PINCNTL222 | AG27 | 0x0004 0000 | VOUT[1]_R_CR[4] | EMAC[1]_MTXD[3] | | | | SPI[3]_SCS[1] | | GP3[14] |
| 0x4814 0B78 | PINCNTL223 | AC26 | 0x0004 0000 | VOUT[1]_R_CR[5] | EMAC[1]_MTXD[4] | | | | SPI[3]_SCLK(M1) | | GP3[15] |
| 0x4814 0B7C | PINCNTL224 | AA25 | 0x0004 0000 | VOUT[1]_R_CR[6] | EMAC[1]_MTXD[5] | | | | SPI[3]_D[1](M1) | | GP3[16] |
| 0x4814 0B80 | PINCNTL225 | V22 | 0x0004 0000 | VOUT[1]_R_CR[7] | EMAC[1]_MTXD[6] | | | | SPI[3]_D[0](M1) | | GP3[17] |
| 0x4814 0B84 | PINCNTL226 | W23 | 0x0004 0000 | VOUT[1]_R_CR[8] | EMAC[1]_MTXD[7] | | | | UART5_RXD(M2) | | GP3[18] |
| 0x4814 0B88 | PINCNTL227 | Y24 | 0x0004 0000 | VOUT[1]_R_CR[9] | EMAC[1]_MTXEN | | | | UART5_TXD(M2) | | GP3[19] |
| 0x4814 0B8C | PINCNTL228 | AF27 | 0x0006 0000 | VOUT[1]_G_Y_YC[2] | GPMC_A[13](M1) | | | HDMI_SCL(M1) | SPI[2]_SCS[2] | I2C[2]_SCL(M2) | GP3[20] |
| 0x4814 0B90 | PINCNTL229 | AG28 | 0x0006 0000 | VOUT[1]_R_CR[3] | GPMC_A[14](M1) | | | HDMI_SDA(M1) | SPI[2]_SCLK(M1) | I2C[2]_SDA(M2) | GP3[21] |
| 0x4814 0B94 | PINCNTL230 | AE27 | 0x0004 0000 | VOUT[1]_R_CR[2] | GPMC_A[15](M1) | | | HDMI_HPDET(M1) | SPI[2]_D[1](M1) | | GP3[22] |
| 0x4814 0B98 | PINCNTL231 | AF28 | 0x0006 0000 | VOUT[1]_B_CB_C[2] | GPMC_A[0](M1) | | | HDMI_CEC(M1) | SPI[2]_D[0](M1) | | GP3[30](M1) |
| 0x4814 0B9C | PINCNTL232 | J27 | 0x0004 0000 | EMAC_RMREFCLK | | | | | | TIM2_IO(M3) | GP1[10](M0) |
| 0x4814 0BA0 | PINCNTL233 | H28 | 0x000E 0000 | MDCLK | | | | | | | GP1[11](M0) |
| 0x4814 0BA4 | PINCNTL234 | P24 | 0x000E 0000 | MDIO | | | | | | | GP1[12](M0) |
| 0x4814 0BA8 | PINCNTL235 | L24 | 0x000C 0000 | EMAC[0]_MTCLK/ EMAC[0]_RGRXC | | | | | SPI[3]_SCS[3] | I2C[2]_SDA(M3) | GP3[23] |
| 0x4814 0BAC | PINCNTL236 | L23 | 0x000C 0000 | EMAC[0]_MCOL/ EMAC[0]_RGRXCTL | | EMAC[0]_RMRXD[0] | | | | | GP3[24] |
| 0x4814 0BB0 | PINCNTL237 | R25 | 0x000C 0000 | EMAC[0]_MCRS/ EMAC[0]_RGRXD[2] | | EMAC[0]_RMRXD[1] | | | | | GP3[25] |
| 0x4814 0BB4 | PINCNTL238 | J26 | 0x000C 0000 | EMAC[0]_MRXER/ EMAC[0]_RGTXCTL | | EMAC[0]_RMRXER | | | | | GP3[26] |
| 0x4814 0BB8 | PINCNTL239 | H27 | 0x000C 0000 | EMAC[0]_MRCLK/ EMAC[0]_RGTXC | | EMAC[0]_RMCRSDV | | | SPI[3]_SCS[2] | | GP3[27] |
| 0x4814 0BBC | PINCNTL240 | G28 | 0x0004 0000 | EMAC[0]_MRXD[0]/ EMAC[0]_RGTXD[0] | | EMAC[0]_RMTXD[0] | | | | | GP3[28] |
| 0x4814 0BC0 | PINCNTL241 | P23 | 0x0004 0000 | EMAC[0]_MRXD[1]/ EMAC[0]_RGRXD[0] | | EMAC[0]_RMTXD[1] | | | | | GP3[29] |
| 0x4814 0BC4 | PINCNTL242 | R23 | 0x0004 0000 | EMAC[0]_MRXD[2]/ EMAC[0]_RGRXD[1] | | EMAC[0]_RMTXEN | | | | | GP3[30](M0) |
| 0x4814 0BC8 | PINCNTL243 | J25 | 0x0004 0000 | EMAC[0]_MRXD[3]/ EMAC[1]_RGRXCTL | | GPMC_A[27](M1) | GPMC_A[26](M1) | GPMC_A[0](M0) | UART5_RXD(M0) | | |
| 0x4814 0BCC | PINCNTL244 | T23 | 0x0004 0000 | EMAC[0]_MRXD[4]/ EMAC[0]_RGRXD[3] | | | | GPMC_A[1](M0) | UART5_TXD(M0) | | |
| 0x4814 0BD0 | PINCNTL245 | H26 | 0x0004 0000 | EMAC[0]_MRXD[5]/ EMAC[0]_RGTXD[3] | | | | GPMC_A[2](M0) | UART5_CTS(M0) | | |
| 0x4814 0BD4 | PINCNTL246 | F28 | 0x0004 0000 | EMAC[0]_MRXD[6]/ EMAC[0]_RGTXD[2] | | | | GPMC_A[3](M0) | UART5_RTS(M0) | | |
| 0x4814 0BD8 | PINCNTL247 | G27 | 0x0004 0000 | EMAC[0]_MRXD[7]/ EMAC[0]_RGTXD[1] | | | | GPMC_A[4](M0) | SPI[2]_SCS[3] | | |


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## Table 5-13. PINCNTLx Registers MUXMODE Functions (continued)

| HEX ADDRESS | REGISTER NAME | PIN NO. | REGISTER RESET VALUE | MUXMODE[7:0] SETTINGS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 0x1 | 0x2 | 0x4 | 0x8 | 0x10 | 0x20 | 0x40 | 0x80 |
| 0x4814 0BDC | PINCNTL248 | K22 | 0x0004 0000 | EMAC[0]_MRXDV/ EMAC[1]_RGRXD[1] | | | | GPMC_A[5](M0) | SPI[2]_SCLK(M2) | | |
| 0x4814 0BE0 | PINCNTL249 | K23 | 0x0004 0000 | EMAC[0]_GMTCLK/ EMAC[1]_RGRXC | | | | GPMC_A[6](M0) | SPI[2]_D[1](M2) | | |
| 0x4814 0BE4 | PINCNTL250 | J24 | 0x0004 0000 | EMAC[0]_MTXD[0]/ EMAC[1]_RGRXD[3] | | | | GPMC_A[7](M0) | SPI[2]_D[0](M2) | | |
| 0x4814 0BE8 | PINCNTL251 | H25 | 0x0004 0000 | EMAC[0]_MTXD[1]/ EMAC[1]_RGTXD[1] | | | | GPMC_A[8](M0) | UART4_RXD(M1) | | |
| 0x4814 0BEC | PINCNTL252 | H22 | 0x0004 0000 | EMAC[0]_MTXD[2]/ EMAC[1]_RGTXCTL | EMAC[1]_RMRXD[0](M0) | | | GPMC_A[9](M0) | UART4_TXD(M1) | | |
| 0x4814 0BF0 | PINCNTL253 | H23 | 0x0004 0000 | EMAC[0]_MTXD[3]/ EMAC[1]_RGTXD[0] | EMAC[1]_RMRXD[1](M0) | | | GPMC_A[10](M0) | $\overline{\text{UART4_CTS}}$(M1) | | |
| 0x4814 0BF4 | PINCNTL254 | G23 | 0x0004 0000 | EMAC[0]_MTXD[4]/ EMAC[1]_RGTXD[2] | EMAC[1]_RMRXER | | | GPMC_A[11](M0) | $\overline{\text{UART4_RTS}}$(M1) | | |
| 0x4814 0BF8 | PINCNTL255 | F27 | 0x0004 0000 | EMAC[0]_MTXD[5]/ EMAC[1]_RGTXC | EMAC[1]_RMCRSDV(M0) | | | GPMC_A[12](M0) | UART1_RXD(M1) | | |
| 0x4814 0BFC | PINCNTL256 | J22 | 0x0004 0000 | EMAC[0]_MTXD[6]/ EMAC[1]_RGRXD[0] | EMAC[1]_RMTXD[0](M0) | | | GPMC_A[13](M0) | UART1_TXD(M1) | | |
| 0x4814 0C00 | PINCNTL257 | H24 | 0x0004 0000 | EMAC[0]_MTXD[7]/ EMAC[1]_RGTXD[3] | EMAC[1]_RMTXD[1](M0) | | | GPMC_A[14](M0) | $\overline{\text{UART1_CTS}}$ | | |
| 0x4814 0C04 | PINCNTL258 | J23 | 0x0004 0000 | EMAC[0]_MTXEN/ EMAC[1]_RGRXD[2] | EMAC[1]_RMTXEN(M0) | | | GPMC_A[15](M0) | $\overline{\text{UART1_RTS}}$ | | |
| 0x4814 0C08 | PINCNTL259 | J7 | 0x0004 0000 | CLKIN32 | | CLKOUT0 | | | | TIM3_IO(M3) | GP3[31] |
| 0x4814 0C0C | PINCNTL260 | J5 | 0x000E 0000 | $\overline{\text{RESET}}$ | | | | | | | |
| 0x4814 0C10 | PINCNTL261 | H7 | 0x000E 0000 | $\overline{\text{NMI}}$ | | | | | | | |
| 0x4814 0C14 | PINCNTL262 | K6 | 0x0005 0000 | $\overline{\text{RSTOUT_WD_OUT}}$ | | | | | | | |
| 0x4814 0C18 | PINCNTL263 | AC4 | 0x000D 0000 | I2C[0]_SCL | | | | | | | |
| 0x4814 0C1C | PINCNTL264 | AB6 | 0x000D 0000 | I2C[0]_SDA | | | | | | | |
| 0x4814 0C20 | PINCNTL265 | – | Undetermined | Reserved. ***Do Not*** Program this Register. | | | | | | | |
| 0x4814 0C24 | PINCNTL266 | – | Undetermined | Reserved. ***Do Not*** Program this Register. | | | | | | | |
| 0x4814 0C28 | PINCNTL267 | – | Undetermined | Reserved. ***Do Not*** Program this Register. | | | | | | | |
| 0x4814 0C2C | PINCNTL268 | – | Undetermined | Reserved. ***Do Not*** Program this Register. | | | | | | | |
| 0x4814 0C30 | PINCNTL269 | – | Undetermined | Reserved. ***Do Not*** Program this Register. | | | | | | | |
| 0x4814 0C34 | PINCNTL270 | AF11 | 0x000C 0000 | USB0_DRVVBUS | GP0[7] | | | | | | |

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## 5.4 Handling Unused Pins

When device signal pins are unused in the system, they can be left unconnected unless otherwise noted in the Terminal Functions tables (see Section 4.2). For unused input pins, the internal pull resistor should be enabled, or an external pull resistor should be used, to prevent floating inputs. Unless otherwise noted, all supply pins must always be connected to the correct voltage, even when their associated signal pins are unused.

## 5.5 DeBugging Considerations

### *5.5.1 Pullup/Pulldown Resistors*

Proper board design should ensure that input pins to the TMS320DM8127 DaVinci™ Digital Media Processsors device always be at a valid logic level and not floating. This may be achieved via pullup/pulldown resistors. The device features internal pullup (IPU) and internal pulldown (IPD) resistors on most pins to eliminate the need, unless otherwise noted, for external pullup/pulldown resistors.

An external pullup/pulldown resistor needs to be used in the following situations:

- *Boot Configuration Pins*: If the pin is both routed out and 3-stated (not driven), an external pullup/pulldown resistor is ***strongly recommended***, even if the IPU/IPD matches the desired value/state.
- *Other Input Pins*: If the IPU/IPD *does not* match the desired value/state, use an external pullup/pulldown resistor to pull the signal to the opposite rail.

For the boot configuration pins (listed in Table 4-1, *Boot Configuration Terminal Functions*), if they are both routed out and 3-stated (not driven), it is ***strongly recommended*** that an external pullup/pulldown resistor be implemented. Although, internal pullup/pulldown resistors exist on these pins and they may match the desired configuration value, providing external connectivity can help ensure that valid logic levels are latched on these device boot configuration pins. In addition, applying external pullup/pulldown resistors on the boot and configuration pins adds convenience to the user in debugging and flexibility in switching operating modes.

Tips for choosing an external pullup/pulldown resistor:

- Consider the total amount of current that may pass through the pullup or pulldown resistor. Make sure to include the leakage currents of all the devices connected to the net, as well as any internal pullup or pulldown resistors.
- Decide a target value for the net. For a pulldown resistor, this should be below the lowest $V_{IL}$ level of all inputs connected to the net. For a pullup resistor, this should be above the highest $V_{IH}$ level of all inputs on the net. A reasonable choice would be to target the $V_{OL}$ or $V_{OH}$ levels for the logic family of the limiting device; which, by definition, have margin to the $V_{IL}$ and $V_{IH}$ levels.
- Select a pullup/pulldown resistor with the largest possible value; but, which can still ensure that the net will reach the target pulled value when maximum current from all devices on the net is flowing through the resistor. The current to be considered includes leakage current plus, any other internal and external pullup/pulldown resistors on the net.
- For bidirectional nets, there is an additional consideration which sets a lower limit on the resistance value of the external resistor. Verify that the resistance is small enough that the weakest output buffer can drive the net to the opposite logic level (including margin).
- Remember to include tolerances when selecting the resistor value.
- For pullup resistors, also remember to include tolerances on the $DV_{DD}$ rail.

For most systems, a 1-kΩ resistor can be used to oppose the IPU/IPD while meeting the above criteria. Users should confirm this resistor value is correct for their specific application.

For most systems, a 20-kΩ resistor can be used to compliment the IPU/IPD on the boot and configuration pins while meeting the above criteria. Users should confirm this resistor value is correct for their specific application.


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For most systems, a 20-kΩ resistor can also be used as an external PU/PD on the pins that have IPUs/IPDs disabled and require an external PU/PD resistor while still meeting the above criteria. Users should confirm this resistor value is correct for their specific application.

For more detailed information on input current ($I_I$), and the low-/high-level input voltages ($V_{IL}$ and $V_{IH}$) for the device, see Section 7.4, *Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature*.

For the internal pullup/pulldown resistors for all device pins, see the peripheral/system-specific terminal functions table.

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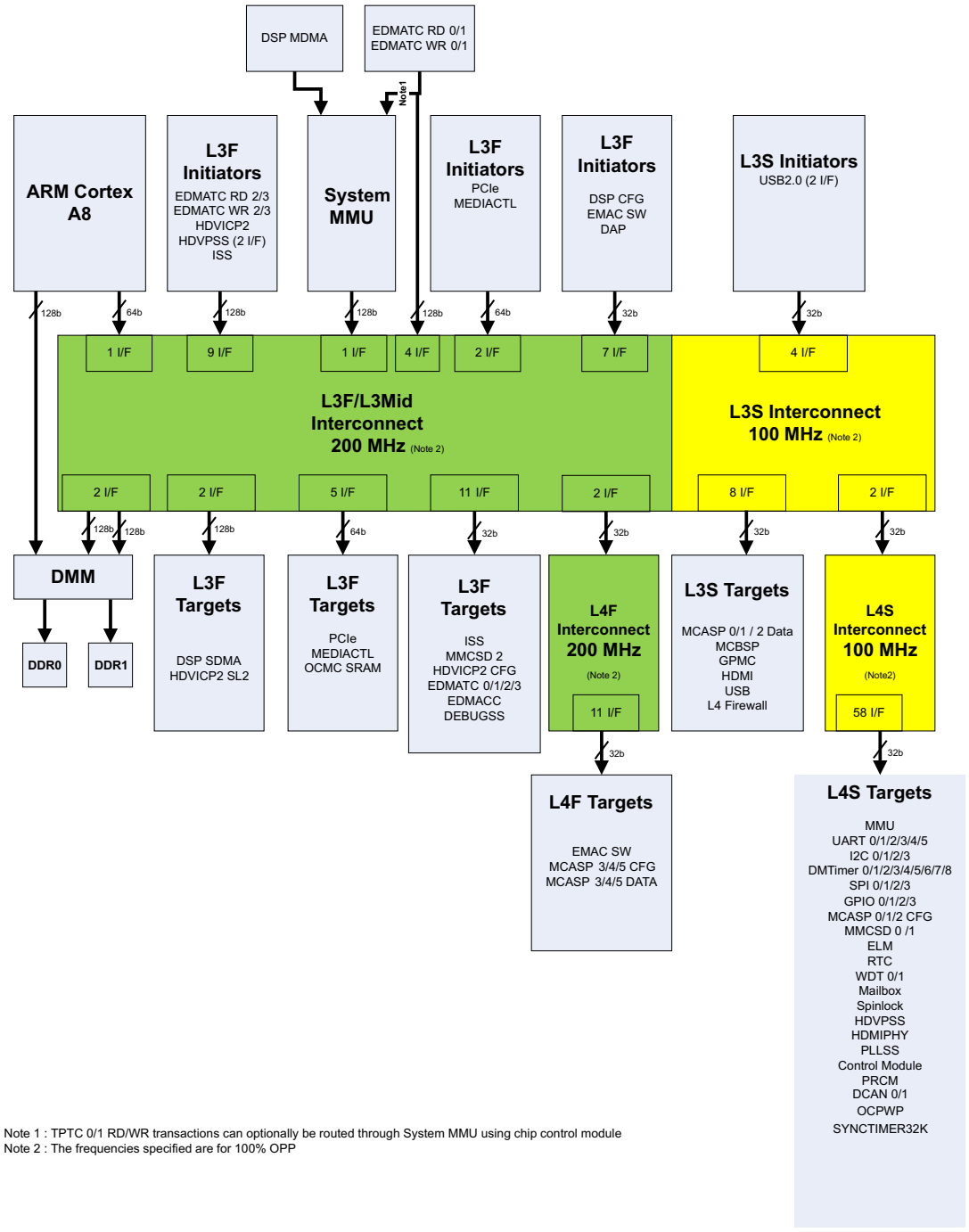
# 6 System Interconnect

The device's various processors, subsystems, and peripherals are interconnected through a switch fabric architecture. The switch fabric is composed of an L3 and L4 interconnect, a switched central resource (SCR), and multiple bridges (for an overview, see Figure 6-1). Not all Initiators in the switch fabric are connected to all Target peripherals. The supported initiator and target connections are designated by a "X" in Table 6-1, *Target/Initiator Connectivity*.

For more detailed information on the device System Interconnect Architecture, see the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).




Note 1 : TPTC 0/1 RD/WR transactions can optionally be routed through System MMU using chip control module
Note 2 : The frequencies specified are for 100% OPP

**Figure 6-1. System Interconnect**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## Table 6-1. L3 Master/Slave Connectivity(1)

(1) X = Connection exists.
S = Selectable path based on thirty-third address bit from control module register for System MMU accessible targets. Non-System MMU accessible targets (such as, C674x SDMA) will always be direct mapped.

| | SLAVES | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MASTERS | System MMU | EDMA DMM Tiler/Lisa0 | EDMA DMM Tiler/Lisa1 | EDMA DMM ELLA | HDVICP2 SL2 | HDVICP2 Hst | Media Controller | GPMC | C674x SDMA | PCIe Gen2 Slave | McASP 0/1/2 | McBSP | HDMI 1.3 Tx Audio | L4 HS Periph Port 0 | L4 HS Periph Port 1 | L4 Std Periph Port 0 | L4 Std Periph Port 1 | L3 Registers | EDMA TPTC0 - 3 CFG | EDMA TPCC | OCMC RAM | L4 Firewall | USB2.0 CFG | Imaging SS | SD2 |
| ARM M1 (128-bit) | | | | X | | | | | | | | | | | | | | | | | | | | | |
| ARM M2 (64-bit) | | | X | | X | X | X | X | X | X | X | X | X | X | | X | | X | X | X | X | X | X | X | X |
| C674x MDMA | X | | | | | | | | | | | | | | | | | | | | | | | | |
| System MMU | | | X | | | | | X | | X | X | X | | X | | X | | | | X | X | | | | |
| C674x CFG | | | | | | | | | | | | | | X | | X | | | X | X | | | X | | |
| HDVICP2 VDMA | | X | | | | | | | | | | | | | | | | | | | X | | | | |
| HDVPSS Mstr0 | | X | | | X | | | | X | | | | | | | | | | | | X | | | | |
| HDVPSS Mstr1 | | | X | | X | | | | X | | | | | | | | | | | | X | | | | |
| EMAC SW | | X | | | X | | | | X | | | | | | | | | | | | X | | | | |
| USB2.0 DMA | | X | | | X | | | | X | | | | | | | | | | | | | | | | |
| USB2.0 Queue Mgr | | X | | | X | | | X | X | | | | | | | | | | | | X | | | | |
| PCIe Gen2 | | X | | | X | X | X | X | X | | X | X | X | | X | | X | | X | X | X | | X | X | X |
| Media Controller | | X | | | X | X | | X | X | X | X | X | X | X | | X | | | X | X | X | | X | | X |
| DAP | | X | | | X | X | X | X | X | X | X | X | X | | X | | X | X | X | X | X | X | X | | |
| EDMA TPTC0 RD | S | X | | | X | X | X | X | X | X | X | X | X | | X | | X | | | X | X | | X | X | X |
| EDMA TPTC0 WR | S | | X | | X | X | X | X | X | X | X | X | X | | X | | X | | | X | X | | X | X | X |
| EDMA TPTC1 RD | S | | X | | X | X | X | X | X | X | X | X | X | X | | X | | | | X | X | | X | X | X |
| EDMA TPTC1 WR | S | X | | | X | X | X | X | X | X | X | X | X | X | | X | | | | X | X | | X | X | X |
| EDMA TPTC2 RD | | | X | | X | X | X | X | X | X | X | X | X | | X | | X | | | X | X | | X | X | X |
| EDMA TPTC2 WR | | X | | | X | X | X | X | X | X | X | X | X | | X | | X | | | X | X | | X | X | X |
| EDMA TPTC3 RD | | X | | | X | X | X | X | X | X | X | X | X | X | | X | | | | X | X | | X | X | X |
| EDMA TPTC3 WR | | | X | | X | X | X | X | X | X | X | X | X | X | | X | | | | X | X | | X | X | X |
| ISS | | | X | | X | | | | X | | | | | | | | | | | | X | | | | |

The L4 interconnect is a non-blocking peripheral interconnect that provides low-latency access to a large number of low-bandwidth, physically-dispersed target cores. The L4 can handle incoming traffic from up to four initiators and can distribute those communication requests to and collect related responses from up to 63 targets.

The device provides two interfaces with L3 interconnect for high-speed peripheraland standard peripheral.

**Table 6-2. L4 Peripheral Conn0ectivity(1)**

| L4 PERIPHERALS | MASTERS | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | ARM Cortex-A8 M2 (64-bit) | EDMA TPTC0 | EDMA TPTC1 | EDMA TPTC2 | EDMA TPTC3 | C674x CONFIG | System MMU | PCIe |
| **L4 Fast Peripherals Port 0/1** | | | | | | | | |
| EMAC SW | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 | Port1 |
| McASP3 CFG | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 | Port1 |
| McASP4 CFG | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 | Port1 |
| McASP5 CFG | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 | Port1 |
| McASP3 DATA | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 | Port1 |
| McASP4 DATA | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 | Port1 |
| McASP5 DATA | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 | Port1 |
| **L4 Slow Peripherals Port 0/1** | | | | | | | | |
| I2C0 | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 | Port1 |
| I2C1 | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 | Port1 |
| I2C2 | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 | Port1 |
| I2C3 | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 | Port1 |
| SPI0 | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 | Port1 |
| SPI1 | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 | Port1 |
| SPI2 | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 | Port1 |
| SPI3 | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 | Port1 |
| UART0 | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 | Port1 |
| UART1 | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 | Port1 |
| UART2 | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 | Port1 |
| UART3 | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 | Port1 |
| UART4 | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 | Port1 |
| UART5 | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 | Port1 |
| Timer1 | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 | Port1 |
| Timer2 | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 | Port1 |
| Timer3 | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 | Port1 |
| Timer4 | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 | Port1 |
| Timer5 | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 | Port1 |
| Timer6 | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 | Port1 |
| Timer7 | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 | Port1 |
| Timer8 | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 | Port1 |
| GPIO0 | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 | Port1 |
| GPIO1 | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 | Port1 |
| MMC/SD0/SDIO | Port0 | Port1 | Port0 | Port1 | Port0 | | | Port1 |
| MMC/SD1/SDIO | Port0 | Port1 | Port0 | Port1 | Port0 | | | Port1 |
| MMC/SD2/SDIO | Port0 | Port1 | Port0 | Port1 | Port0 | | | Port1 |
| WDT0 | Port0 | Port1 | Port0 | Port1 | Port0 | | | Port1 |
| RTC | Port0 | Port1 | Port0 | Port1 | Port0 | | | Port1 |
| System MMU | Port0 | Port1 | Port0 | Port1 | Port0 | | | Port1 |

(1) X, Port0, Port1 = Connection exists.


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**Table 6-2. L4 Peripheral Conn0ectivity[(1)] (continued)**

| L4 PERIPHERALS | MASTERS | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | ARM Cortex-A8 M2 (64-bit) | EDMA TPTC0 | EDMA TPTC1 | EDMA TPTC2 | EDMA TPTC3 | C674x CONFIG | System MMU | PCIe |
| Mailbox | Port0 | | | | | Port0 | Port0 | |
| Spinlock | Port0 | | | | | Port0 | Port0 | |
| HDVPSS | Port0 | Port1 | Port0 | Port1 | Port0 | | | Port1 |
| PLLSS | Port0 | | | | | | | Port1 |
| Control/Top Regs (Control Module) | Port0 | | | | | | | Port1 |
| PRCM | Port0 | | | | | | | Port1 |
| ELM | Port0 | | | | | | | Port1 |
| HDMIPHY | Port0 | | | | | | | Port1 |
| DCAN0 | Port0 | Port1 | Port0 | Port1 | Port0 | | | Port1 |
| DCAN1 | Port0 | Port1 | Port0 | Port1 | Port0 | | | Port1 |
| OCPWP | Port0 | | | | | | | Port0 |
| McASP0 CFG | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 | Port1 |
| McASP1 CFG | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 | Port1 |
| McASP2 CFG | Port0 | Port1 | Port0 | Port1 | Port0 | Port0 | Port0 | Port1 |
| SYNCTIMER32K | Port0 | Port1 | Port0 | Port1 | Port0 | | | Port1 |

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# 7 Device Operating Conditions

## 7.1 Absolute Maximum Ratings (1)(2)

| | | |
|---|---|---|
| Supply voltage ranges (Steady State): | Core (CVDD, CVDD_ARM, CVDD_DSP, CVDD_HDVICP) | -0.3 V to 1.5 V |
| | I/O, 1.8 V (DVDD_M, DVDD_DDR[0], DVDD_DDR[1], VDDA_1P8, VDDA_ARMPLL_1P8, VDDA_DSPPLL_1P8, VDDA_VID0PLL_1P8, VDDA_VID1PLL_1P8, VDDA_AUDIOPLL_1P8, VDDA_DDRPLL_1P8, VDDA_L3PLL_1P8, VDDA_PCIE_1P8, VDDA_CSI2_1P8, VDDA_HDMI_1P8, VDDA_USB0_1P8, VDDA_USB1_1P8, VDDA_VDAC_1P8) | -0.3 V to 2.1 V |
| | I/O 3.3 V (DVDD, DVDD_GPMC, DVDD_GPMCB, DVDD_SD, DVDD_C) | -0.3 V to 4.0 V |
| | DDR Reference Voltage (VREFSSTL_DDR[0], VREFSSTL_DDR[1]) | -0.3 V to 1.1 V |
| Input and Output voltage ranges: | V I/O, 1.5-V pins (Steady State) | -0.3 V to DVDD_DDR[x] + 0.3 V |
| | V I/O, 1.8-V pins (Steady State) | -0.3 V to DVDD + 0.3 V<br>-0.3 V to DVDD_x + 0.3 V |
| | V I/O, 3.3-V pins (Steady State) | -0.3 V to DVDD + 0.3 V<br>-0.3 V to DVDD_x + 0.3 V |
| Operating junction temperature range, $T_J$: | Commercial Temperature | 0°C to 90°C |
| | Industrial | -40°C to 90°C |
| | Extended | -40°C to 105°C |
| Storage temperature range, $T_{stg}$: | | -55°C to 150°C |
| Latch-up Performance: | I-test: Silicon Revision 3.0, All I/O pins (3) | ±100 mA |
| | I-test: Silicon Revision 2.1, All I/O pins (3) | ±70 mA |
| | Over-Voltage Test, All Supply pins (4) | 1.5xVddmax V |
| Electrostatic Discharge (ESD) Performance: | ESD-HBM (Human Body Model) (5) | ±1000 V |
| | ESD-CDM (Charged-Device Model) (6) | ±250 V |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to their associated VSS or VSSA_x.
(3) Pins stressed per JEDEC JESD78 at 90°C (Class II) and passed with specified I/O pin injection current and clamp voltage of 1.5 times maximum recommended I/O voltage and negative 0.5 times maximum recommended I/O voltage.
(4) Supplies stressed per JEDEC JESD78 at 90°C (Class II) and passed specified voltage injection.
(5) Level listed is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 500-V HBM is possible if necessary precautions are taken. Pins listed as 1000 V may actually have higher performance.
(6) Level listed is the passing level per EIA-JEDEC JESD22-C101E. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 250-V CDM is possible if necessary precautions are taken. Pins listed as 250 V may actually have higher performance.


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## 7.2 Recommended Operating Conditions

| PARAMETER | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| CVDD | Supply voltage, Core (Scalable) DVFS only, No AVS | 166% OPP | 1.28 | 1.35 | 1.42 | V |
| | | 120% OPP | 1.14 | 1.20 | 1.26 | |
| | | 100% OPP | 1.05 | 1.10 | 1.16 | |
| CVDD_ARM | Supply voltage, Core ARM (Scalable) DVFS only, No AVS | 166% OPP | 1.28 | 1.35 | 1.42 | V |
| | | 120% OPP | 1.14 | 1.20 | 1.26 | |
| | | 100% OPP | 1.05 | 1.10 | 1.16 | |
| CVDD_DSP | Supply voltage, Core, DSP (Scalable) DVFS only, No AVS | 166% OPP | 1.28 | 1.35 | 1.42 | V |
| | | 120% OPP | 1.14 | 1.20 | 1.26 | |
| | | 100% OPP | 1.05 | 1.10 | 1.16 | |
| CVDD_HDVICP | Supply voltage, Core, HDVICP2 (Scalable) DVFS only, No AVS | 166% OPP | 1.28 | 1.35 | 1.42 | V |
| | | 120% OPP | 1.14 | 1.20 | 1.26 | |
| | | 100% OPP | 1.05 | 1.10 | 1.16 | |
| DVDD | Supply voltage, I/O, standard pins(1) | 3.3 V | 3.14 | 3.3 | 3.47 | V |
| | | 1.8 V | 1.71 | 1.8 | 1.89 | |
| DVDD_GPMC | Supply voltage, I/O, GPMC pin group | 3.3 V | 3.14 | 3.3 | 3.47 | V |
| | | 1.8 V | 1.71 | 1.8 | 1.89 | |
| DVDD_GPMCB | Supply voltage, I/O, GPMCB pin group | 3.3 V | 3.14 | 3.3 | 3.47 | V |
| | | 1.8 V | 1.71 | 1.8 | 1.89 | |
| DVDD_SD | Supply voltage, I/O, SD pin group | 3.3 V | 3.14 | 3.3 | 3.47 | V |
| | | 1.8 V | 1.71 | 1.8 | 1.89 | |
| DVDD_C | Supply voltage, I/O, C pin group | 3.3 V | 3.14 | 3.3 | 3.47 | V |
| | | 1.8 V | 1.71 | 1.8 | 1.89 | |
| DVDD_M | Supply voltage, I/O, M pin group | 1.8 V | 1.71 | 1.8 | 1.89 | V |
| DVDD_DDR[0] DVDD_DDR[1] | Supply voltage, I/O, DDR[0] and DDR[1] | DDR2 | 1.71 | 1.8 | 1.89 | V |
| | | DDR3 mode | 1.43 | 1.5 | 1.58 | |
| VDDA_USB_3P3 | Supply voltage, I/O, Analog, USB 3.3 V | | 3.14 | 3.3 | 3.47 | V |
| VDDA_1P8 VDDA_x_1P8 | Supply Voltage, I/O, Analog, (VDDA_1P8, VDDA_ARMPLL_1P8, VDDA_DSPPLL_1P8, VDDA_VID0PLL_1P8, VDDA_VID1PLL_1P8, VDDA_AUDIOPLL_1P8, VDDA_DDRPLL_1P8, VDDA_L3PLL_1P8, VDDA_PCIE_1P8, VDDA_CSI2_1P8, VDDA_HDMI_1P8, VDDA_USB0_1P8, VDDA_USB1_1P8, VDDA_VDAC_1P8) **Note:** CSI2, HDMI, USB0/1, and VDAC relative to their respective VSSA. | | 1.71 | 1.8 | 1.89 | V |
| VSS | Supply Ground (VSS, VSSA_CSI2, VSSA_HDMI, VSSA_USB, VSSA_VDAC, VSSA_DEVOSC(2), VSSA_AUXOSC(2)) | | | 0 | | V |
| $V_{REFSSTL_DDR[x]}$ | IO Reference Voltage, (VREFSSTL_DDR[0], VREFSSTL_DDR[1]) | | 0.49 * DVDD_DDR[x] | 0.50 * DVDD_DDR[x] | 0.51 * DVDD_DDR[x] | V |
| USBx_VBUSIN | USBx VBUS Comparator Input | | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High-level input voltage, LVCMOS (JTAG[TCK] pins), 3.3 V(1) | | 2 | | | V |
| | High-level input voltage, JTAG[TCK], 3.3 V | | 2.15 | | | V |
| | High-level input voltage, JTAG[TCK], 1.8 V | | 1.45 | | | V |
| | High-level input voltage, I2C (I2C[0] and I2C[1]) | | 0.7DVDD | | | V |
| | High-level input voltage, LVCMOS(1), 1.8 V | | 0.65DVDDx | | | V |

(1) LVCMOS pins are all I/O pins powered by DVDD, DVDD_GPMC, DVDD_GPMCB, DVDD_SD, DVDD_C supplies except for I2C[0] and I2C[1] pins.
(2) When using the internal Oscillators, the oscillator grounds (VSSA_DEVOSC, VSSA_AUXOSC) must be kept separate from other grounds and connected directly to the crystal load capacitor ground.

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## Recommended Operating Conditions *(continued)*

| PARAMETER | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Low-level input voltage, LVCMOS(1), 3.3 V | | | | 0.8 | V |
| | Low-level input voltage, JTAG[TCK] | | | | 0.45 | V |
| | Low-level input voltage, I2C (I2C[0] and I2C[1]) | | | | 0.3DVDDx | V |
| | Low-level input voltage, LVCMOS(1), 1.8 V | | | | 0.35DVDDx | V |
| $I_{OH}$ | High-level output current | 6 mA I/O buffers | | | -6 | mA |
| | | DDR[0], DDR[1] buffers @ 50-Ω impedance setting | | | -8 | mA |
| $I_{OL}$ | Low-level output current | 6 mA I/O buffers | | | 6 | mA |
| | | DDR[0], DDR[1] buffers @ 50-Ω impedance setting | | | 8 | mA |
| $V_{ID}$ | Differential input voltage (SERDES_CLKN/P), [AC coupled] | | 0.250 | | 2.0 | V |
| $t_t$ | Transition time, 10% - 90%, All inputs (unless otherwise specified in the *Electrical Data/Timing* sections of each peripheral) | | | | 0.25P or 10(3) | ns |
| $T_J$ | Operating junction temperature range(4) | Commercial Temperature (default) | 0 | | 90 | °C |
| | | Industrial | -40 | | 90 | °C |
| | | Extended | -40 | | 105 | °C |

(3) Whichever is smaller. P = the period of the applied signal. Maintaining transition times as fast as possible is recommended to improve noise immunity on input signals.
(4) For more detailed information on estimating junction temps within systems, see the *IC Package Thermal Metrics* Application Report (Literature Number: SPRA953).

## 7.3 Power-On Hours (POH)

The POH information in Table 7-1 is provided solely for convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI Semiconductor Products. To avoid significant device degradation, the device POH must be limited to those shown in Table 7-1.

**Table 7-1. Power-On Hour Limits**

| Operating Condition | Nominal CVDD Voltage (V) | Junction Temperature ($T_j$) | Lifetime POH(1) |
|---|---|---|---|
| 100% OPP | 1.1 | -40 to 105 °C | 100K |
| 120% OPP | 1.2 | -40 to 105 °C | 100K |
| 166% OPP | 1.35 | -40 to 105 °C | 49K |

(1) POH represent device operation under the specified nominal conditions continuously for the duration of the calculated lifetime.

Logic functions and parameter values are not ensured out of the range specified in Section 7.2, Recommended Operating Conditions.

The above notations cannot be deemed a warranty or deemed to extend or modify the warranty under TI's standard terms and conditions for semiconductor products.


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## 7.4 Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature (Unless Otherwise Noted)

| PARAMETER | | TEST CONDITIONS(1) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Low/Full speed: USB_DM and USB_DP | | 2.8 | | VDD_USB_3P3 | V |
| | High speed: USB_DM and USB_DP | | 360 | | 440 | mV |
| | High-level output voltage, LVCMOS(2) (3.3-V I/O) | 3.3 V, DVDDx = MIN, $I_{OH}$ = MAX | 2.4 | | | V |
| | High-level output voltage, LVCMOS(2) (1.8-V I/O) | 1.8 V, DVDDx = MIN, $I_{OH}$ = MAX | 1.26 | | | V |
| $V_{OL}$ | Low/Full speed: USB_DM and USB_DP | | 0.0 | | 0.3 | V |
| | High speed: USB_DM and USB_DP | | -10 | | 10 | mV |
| | Low-level output voltage, LVCMOS(2) (3.3-V I/O) | 3.3 V, DVDDx = MAX, $I_{OL}$ = MAX | | | 0.4 | V |
| | Low-level output voltage, LVCMOS(2) (1.8-V I/O) | 1.8 V, DVDDx = MAX, $I_{OL}$ = MAX | | | 0.4 | V |
| | Low-level output voltage, I2C (I2C[0], I2C[1]) | 1.8/3.3 V, $I_{OL}$ = 4mA | | | 0.4 | V |
| | LDOs (applies to all LDOCAP_x pins) | | | | 1.5 | V |
| $I_I$(3) | Input current, LVCMOS(2), 3.3 V mode | 0 < $V_I$ < DVDDx, 3.3 V pull disabled | -20 | | 20 | µA |
| | | 0 < $V_I$ < DVDDx, 3.3 V pulldown enabled(4) | 20 | 100 | 300 | µA |
| | | 0 < $V_I$ < DVDDx, 3.3 V pullup enabled(4) | -20 | -100 | -300 | µA |
| | Input current, LVCMOS(2), 1.8 V mode | 0 < $V_I$ < DVDDx, 1.8 V pull disabled | -5 | | 5 | µA |
| | | 0 < $V_I$ < DVDDx, 1.8 V pulldown enabled(4) | 50 | 100 | 200 | µA |
| | | 0 < $V_I$ < DVDDx, 1.8 V pullup enabled(4) | -50 | -100 | -200 | µA |
| | Input current, I2C (I2C[0], I2C[1]) | 3.3 V mode | -20 | | 20 | µA |
| | | 1.8 V mode | -5 | | 5 | µA |
| $I_{OZ}$(5) | I/O Off-state output current | 3.3 V mode, pull enabled | -300 | | 300 | µA |
| | | 3.3 V mode, pull disabled | -20 | | 20 | µA |
| | | 1.8 V mode, pull enabled | -200 | | 200 | µA |
| | | 1.8 V mode, pull disabled | -5 | | 5 | µA |
| $I_{CDD}$ | Core (CVDD) supply current (scalable) | | see note (6) | | | mA |
| ICVDD_ARM | ARM Core Current (Scalable) | | see note (6) | | | mA |
| ICVDD_DSP | DSP Core Current (Scalable) | | see note (6) | | | mA |
| ICVDD_HDVICP | HDVICP2 Core Current (Scalable) | | see note (6) | | | mA |

(1) For test conditions shown as MIN, MAX, or TYP, use the appropriate value specified in the recommended operating conditions table.
(2) LVCMOS pins are all I/O pins powered by DVDD, DVDD_GPMC, DVDD_GPMCB, DVDD_SD, DVDD_C supplies except for I2C[0] and I2C[1] pins.
(3) $I_I$ applies to input-only pins and bi-directional pins. For input-only pins, $I_I$ indicates the input leakage current. For bi-directional pins, $I_I$ indicates the input leakage current and off-state (Hi-Z) output leakage current.
(4) Applies only to pins with an internal pullup (IPU) or pulldown (IPD) resistor.
(5) $I_{OZ}$ applies to output-only pins, indicating off-state (Hi-Z) output leakage current.
(6) The actual current draw varies across manufacturing processes and is highly application-dependent. For more details on core and I/O activity, as well as information relevant to board power supply design, see the *TMS320DM814x/AM387x Power Estimation Spreadsheet* Application Report (Literature Number: SPRABO3). To determine the worst-case power consumption values, use the *TMS320DM814x/AM387x Power Estimation Spreadsheet* Application Report.

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## Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature (Unless Otherwise Noted) *(continued)*

| PARAMETER | | TEST CONDITIONS[1] | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{DDD}$ | 3.3-V I/O (DVDD, DVDD_GPMC, DVDD_GPMCB, DVDD_SD, DVDD_C, VDDA_USB_3P3) supply current | | | see note [6] | | mA |
| | 1.8-V I/O (DVDD, DVDD_GPMC, DVDD_GPMCB, DVDD_SD, DVDD_C DVDD_M, DVDD_DDR[0], DVDD_DDR[1] [for DDR2], VDDA_x_1P8) supply current | | | see note [6] | | mA |
| | 1.5-V I/O (DVDD_DDR[0], DVDD_DDR[1] [for DDR3 SDRAM]) supply current | | | see note [6] | | mA |
| $C_I$ | Input capacitance LVCMOS[2] | | | | 12 | pF |
| $C_o$ | Output capacitance LVCMOS[2] | | | | 12 | pF |


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# 8 Power, Reset, Clocking, and Interrupts

## 8.1 Power, Reset and Clock Management (PRCM) Module

The PRCM module is the centralized management module for the power, reset, and clock control signals of the device. The PRCM interfaces with all the components on the device for power, clock, and reset management through power-control signals. The PRCM module inTiming Requirements for AUD_CLKINxtegrates enhanced features to allow the device to adapt energy consumption dynamically, according to changing application and performance requirements. The innovative hardware architecture allows a substantial reduction in leakage current.

The PRCM module is composed of two main entities:

- Power reset manager (PRM): Handles the power, reset, wake-up management, and system clock source control (oscillator)
- Clock manager (CM): Handles the clock generation, distribution, and management.

For more details on the PRCM, see the *Power, Reset, and Clock Management (PRCM) Module* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

## 8.2 Power

### *8.2.1 Voltage and Power Domains*

Every Module within the device belongs to a Core Logic Voltage Domain, Memory Voltage Domain, and a Power Domain (see Table 8-1).

**Table 8-1. Voltage and Power Domains**

| CORE LOGIC VOLTAGE DOMAIN | MEMORY VOLTAGE DOMAIN | POWER DOMAIN | MODULES |
|---|---|---|---|
| ARM_L | ARM_M | ALWAYS ON | ARM Cortex-A8 Subsystem |
| CORE_L | CORE_M | | DMM, EDMA, ELM, DDR0, EMAC Switch, GPIO Banks 0/1/2/3,GPMC, I2C0/1/2, IPC, MCASP0/1, OCMC SRAM, PCIE, PRCM, RTC, SPI01/2/3, Timer1/2/3/4/5/6/7/8, UART0/1/2/3/4/5, USB0/1, WDT0, System Interconnect, JTAG, Media Controller, ISS (except for ISP, FACEDETECT, CSI2) |
| | | ISP | ISP, FACEDETECT, CSI2 |
| | | HDVPSS | HDVPSS, HDMI, SD-DAC |
| DSP_L | DSP_M | DSP | C674x DSP and L2 SRAM |

#### 8.2.1.1 Core Logic Voltage Domains

The device contains four Core Logic Voltage Domains. These domains define groups of Modules that share the same supply voltage for their core logic. Each Core Logic Voltage Domain is powered by a dedicated supply voltage rail. Table 8-2 shows the mapping between the Core Logic Voltage Domains and their associated supply pins.

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**Table 8-2. Core Logic Voltage Domains and Supply Pin Associations**

| CORE LOGIC VOLTAGE DOMAIN | SUPPLY PIN NAME |
|---|---|
| ARM_L | CVDD_ARM |
| CORE_L | CVDD |
| DSP_L | CVDD_DSP |
| HDVICP_L | CVDD_HDVICP |

**Note:** A regulated supply voltage ***must*** be supplied to each Core Logic Voltage Domain at all times, regardless of the Core Logic Power Domain states.

#### 8.2.1.2 Memory Voltage Domains

The SRAM within each Device Module is assigned to one of four Memory Voltage Domains. The voltage of each Memory Voltage Domain is independently controlled by internal LDO regulators, which are supplied by the VDDA_1P8 pins.

The voltage level output by each of these LDO regulators is controlled through software by programming the RAMLDO_CTRLx registers in the Control Module. The Memory Voltage Domain voltage must be programmed based on the Core Logic Voltage Domain voltage for that domain (that is, the corresponding Core Logic Voltage Domain for the ARM_M Voltage Domain is ARM_C, and so on). Table 8-3 shows the Memory Voltage Domain voltage requirements.

**Table 8-3. Memory Voltage Domain LDO Requirements**

| CORE LOGIC VOLTAGE DOMAIN VOLTAGE (V) | MEMORY VOLTAGE DOMAIN VOLTAGE (V) |
|---|---|
| 0.83 – 1.20 | 1.20 |

#### 8.2.1.3 Power Domains

The device contains six Power Domains which supply power to both the Core Logic and SRAM within their associated modules. Each Power Domain, except for the ALWAYS ON domain, has an internal power switch that can completely remove power from that domain. All power switches are turned "OFF" by default after reset, and software can individually turn them "ON/OFF" via Control Module registers.

*Note:* All Modules within a Power Domain are unavailable when the domain is powered "OFF". For instructions on powering "ON/OFF" the Power domains, see the *Power, Reset, and Clock Management (PRCM) Module* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

### *8.2.2 SmartReflex [Not Supported]*

The device contains SmartReflex modules that help to minimize power consumption on the Core Logic Voltage Domains by using external variable-voltage power supplies. Based on the device process, temperature, and desired performance, the SmartReflex modules advise the host processor to raise or lower the supply voltage to each domain for minimal power consumption.

The communication link between the host processor and the external regulators is a system-level decision and can be accomplished using GPIOs, I2C, SPI, or other methods. The following sections briefly describe the two major techniques employed by SmartReflex: Dynamic Voltage Frequency Scaling (DVFS) and Adaptive Voltage Scaling (AVS).


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### 8.2.2.1 Dynamic Voltage Frequency Scaling (DVFS)

Each device Core Logic Voltage Domain can be run independently at one of several Operating Performance Points (OPPs). An OPP for a specific Core Logic Voltage Domain is defined by: (1) maximum frequencies of operation for Modules within the Domain and (2) an associated supply voltage range. Trading off power versus performance, OPPs with lower maximum frequencies also have lower voltage ranges for power savings.

The OPP for a domain can be changed in real-time without requiring a reset. This feature is called Dynamic Voltage Frequency Scaling (DVFS). Table 8-4 contains a list of voltage ranges and maximum module frequencies for the OPPs of each Core Logic Voltage Domain.

**Table 8-4. Device Operating Points (OPPs)(1)**

| | | CORE LOGIC VOLTAGE DOMAINS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | ARM | DSP | HDVICP | CORE | | | | |
| DEVICE(2) | OPP | Cortex A8 (MHz) | DSP (MHz) | HDVICP2 (MHz) | HDVPSS (MHz) | ISS (MHz) | Media Ctlr. (MHz) | L3/L4, Core (MHz) | DDR (MHz)(3) |
| CYEx0 | 100% (1.1 V) | 600 | 500 | 266 | 200 | 400 | 200 | 200 | 400 |
| | 120% (1.2 V) | 720 | 600 | 306 | 200 | 400 | 200 | 220 | 400 |
| CYEx1 | 120% (1.2 V) | 720 | 600 | 306 | 220 | 480 | 240 | 220 | 400 |
| | 166% (1.35 V) | – | – | 410 | – | – | – | – | – |
| CYEx2 | 120% (1.2 V) | 720 | 600 | 306 | 220 | 480 | 240 | 220 | 400 |
| | 166% (1.35 V) | 1000 | 700 | 410 | 220 | 480 | 240 | 220 | 533 |
| CYEx3 | 120% (1.2 V) | 720 | 600 | 306 | 220 | 480 | 240 | 220 | 400 |
| | 166% (1.35 V) | 1000 | 750 | 450 | 220 | 560 | 280 | 220 | 533 |

(1) Not all devices support all OPP frequencies.
(2) CYE denotes the device mechanical package designator, "x" denotes the device temperature range, and 0,1,2, or 3 denotes the device speed range. For more detailed information on the DM8127 device nomenclature breakout, see Figure 10-1, *Device Nomenclature*.
(3) All DDR access ***must*** be suspended prior to changing the DDR frequency of operation.

Although the OPP for each Core Logic Voltage Domain is independently selectable, not all combinations of OPPs are supported. Table 8-5 marks the supported ARM, DSP, and HDVICP2 OPPs for a given CORE OPP.

**Table 8-5. Supported OPP Combinations(1)(2)(3)**

| | ARM | | | DSP | | | HDVICP2 | | |
|---|---|---|---|---|---|---|---|---|---|
| CORE | OPP166 | OPP120 | OPP100 | OPP166 | OPP120 | OPP100 | OPP166 | OPP120 | OPP100 |
| OPP166 | X | | | X | | | X | | |
| OPP120 | X | X | | X | X | | X | X | |
| OPP100 | | X | X | | X | X | | X | X |

(1) "X" denotes supported combinations.
(2) The maximum voltage differences between CVDD and any other CVDD_x voltage domain **must** be < 150 mV.
(3) The CYEx1 devices only support OPP120 for CORE, ARM, and DSP, and either OPP120 or OPP166 for HDVICP2. For the OPPs supported by each device speed range, see Table 8-4.

### 8.2.2.2 Adaptive Voltage Scaling [Not Supported]

As mentioned in Section 8.2.2.1, *Dynamic Voltage Frequency Scaling (DVFS)* above, every OPP has an associated voltage range. Based on the silicon process, temperature, and chosen OPP, the SmartReflex modules guide software in adjusting the Core Logic Voltage Domain supply voltages within these ranges. This technique is called Adaptive Voltage Scaling (AVS). AVS occurs continuously and in real-time, helping to minimize power consumption in response to changing operating conditions.

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### 8.2.3 Memory Power Management

To reduce SRAM leakage, many SRAM blocks can be switched from ACTIVE mode to SHUTDOWN mode. When SRAM is put in SHUTDOWN mode, the voltage supplied to it is automatically removed and all data in that SRAM is lost.

All SRAM located in a switchable power domain (all domains except ALWAYS_ON) automatically enters SHUTDOWN mode whenever its associated power domain goes into the "OFF" state. The SRAM returns to the ACTIVE state when the corresponding Power Domain returns to the "ON" state.

In addition, the following SRAM within the ALWAYS_ON Power Domain can also be independently put into SHUTDOWN by programming the x_MEM_PWRDN registers in the Control Module:

- Media Controller SRAM
- OCMC SRAM

For detailed instructions on powering up/down the various device SRAM, see the *Control Module* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

### 8.2.4 SERDES_CLKP and SERDES_CLKN LDO

The SERDES_CLKP and SERDES_CLKN input buffers are powered by an internal LDO which is programmed through the REFCLK_LJCBLDO_CTRL register in the Control Module.

For more information on programming the SERDES_CLKP and SERDES_CLKN LDO, see *PCI Express (PCIe) Module* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8

### 8.2.5 Dual Voltage I/Os

The device supports dual voltages on some of its I/Os. These I/Os are partitioned into the following groups, and each group has its own dedicated supply pins: DVDD, DVDD_GPMC, DVDD_C, and DVDD_SD. The supply voltage for each group can be independently powered with either 1.8 V or 3.3 V.

For the mapping between pins and power groups, see Section 4.2, *Terminal Functions* of the datasheet.

In addition, the I/O voltage on each DDR interface is independently selectable between either 1.5 V or 1.8 V to support various DDR device types. The I/O supplies for each DDR interface are separate and isolated to allow populating different memory types on each interface.

### 8.2.6 I/O Power-Down Modes

On the device, there are power-down modes available for the following PHYs:

- Video DAC
- DDR
- USB
- HDMI
- CSI2
- PCIE

When a PHY controller is in a power domain that is to be turned "OFF", software must configure the corresponding PHY into power-down mode, prior to putting the power domain in the "OFF" state.


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### 8.2.7 Standby Mode

The device supports Low-Power Standby Mode as described below.

**Standby Mode** is defined as a state in which:

- All switchable power domains are in "OFF" state
- The ARM Cortex-A8 is executing an IDLE loop at its lowest frequency of operation
- All functional blocks not needed for a given application are clock gated

For detailed instructions on entering and exiting from Standby Mode see the *Power, Reset, and Clock Management (PRCM) Module* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

### 8.2.8 Supply Sequencing

The device power supplies are organized into four Supply Sequencing Groups:

1. All CVDD supplies (CVDD, CVDD_x)
2. All 1.5-/1.8-V DVDD_DDR[x] Supplies (1.5 V for DDR3, 1.8 V for DDR2)
3. All 1.8-V Supplies (DVDD_x, DVDD_M, VDDA_x_1P8, VDDA_1P8)
4. All 3.3-V Supplies (DVDD, DVDD_x, DVDD_C, VDDA_x_3P3)

To ensure proper device operation, a specific power-up and power-down sequence must be followed. Some TI power-supply devices include features that facilitate these power sequencing requirements — for example, TI's TPS659113 integrated PMIC. For more information on TI power supplies and their features, visit www.ti.com/processorpower.

For more detailed information on the actual power supply names and their descriptions, see Table 4-48, *Supply Voltages Terminal Functions*.

#### 8.2.8.1 Power-Up Sequence

For proper device operation, the following power-up sequence in Table 8-6 and ***must*** be followed.

**Table 8-6. Power-Up Sequence Ramping Values**

| NO. | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|
| 1 | 1.8 V and DVDD_DDR[x] supplies stable to 3.3 V supplies ramp start | 0 | | ms |
| 2 | 1.8 V supplies to 1.5-/1.8- V DVDD_DDR[x] supplies | 0 (1) | | ms |
| 3 | 1.8 V supplies stable to CVDD, CVDD_x variable supplies ramp start | 0 (1) | | ms |
| 13 | CVDD variable supply ramp start to CVDD_x variable supplies ramp start | 0 | | ms |
| 4 | All supplies valid to power-on-reset ($\overline{\text{POR}}$ high) | 4 096 | | Master Clocks |

(1) The 1.8 V supplies ***must*** be ≥ 1.5-/1.8-V DVDD_DDR[x] supplies.

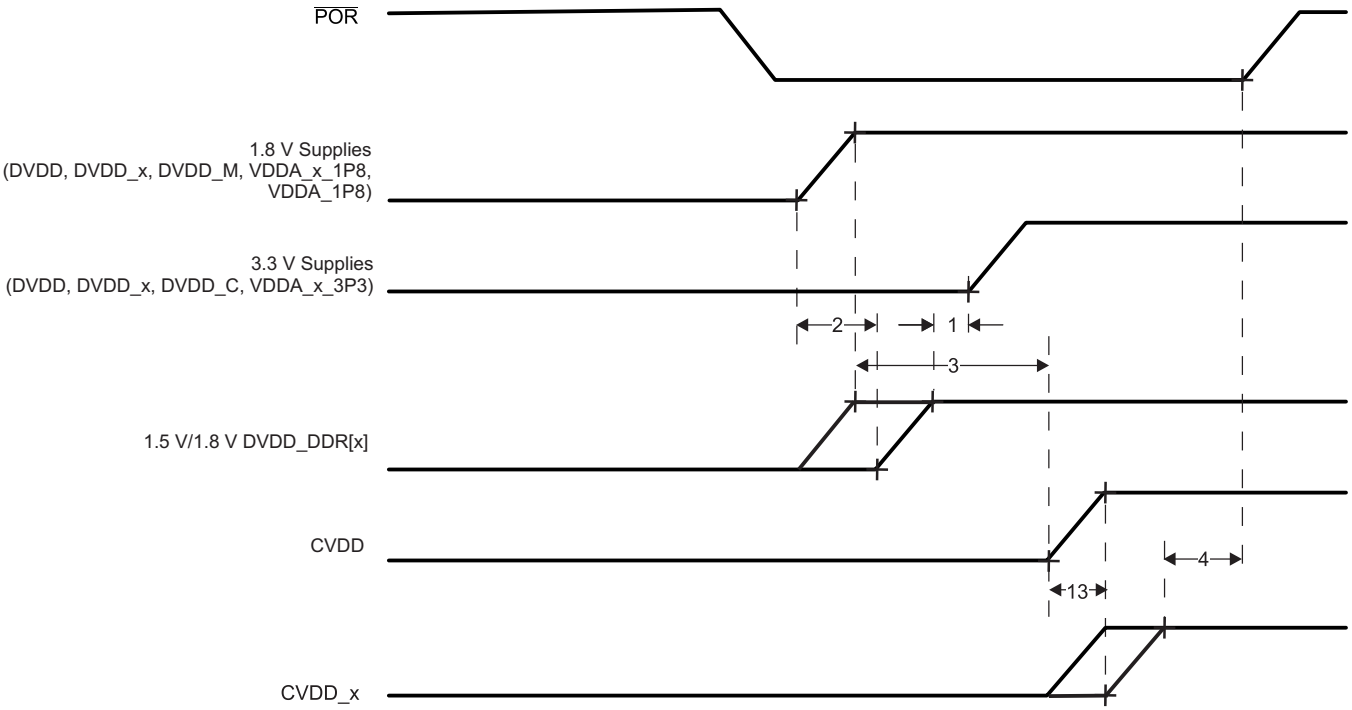


**Figure 8-1. Power-Up Sequence**

### 8.2.8.2 Power-Down Sequence

For proper device operation, the following power-down sequence in Table 8-7 and Figure 8-2 ***must*** be followed. Ramping down all supplies at the same time is allowed, provided the requirements in Table 8-7 are met.

**Table 8-7. Power-Down Sequence Ramping Values**

| NO. | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|
| 8 | CVDD, CVDD_x variable supply to 1.8 V supplies | See (1) | See (1) | ms |
| 9 | 1.5-/1.8-V DVDD_DDR[x] supplies to 1.8 V supplies | See (1) | See (1) | ms |
| 10 | 3.3 V supplies to 1.8 V supplies | See (2) | See (2) | ms |
| 14 | CVDD_x variable supplies ramp-down start to CVDD variable supply ramp-down start | 0 | | ms |

(1) The 1.5-/1.8-V DVDD_DDR[x] and CVDD, CVDD_x variable supplies can be powered down prior to or simultaneously with the 1.8-V supplies.
(2) The 3.3 V supplies ***must*** never be more than 2 V above the 1.8 V supplies (see Figure 8-3).


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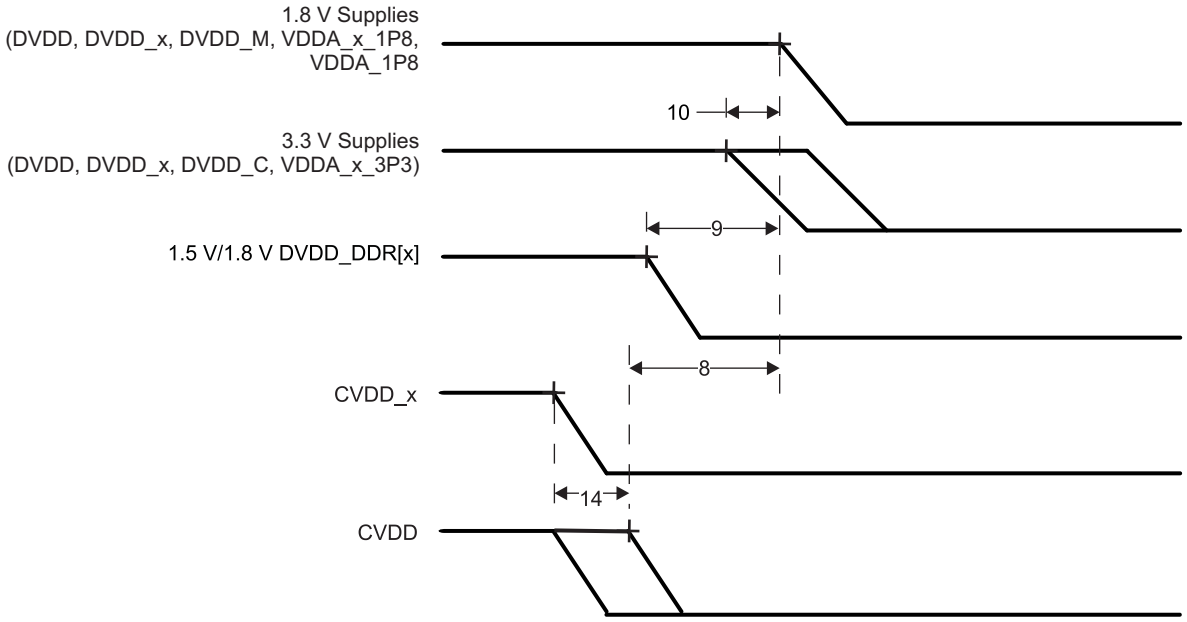


**Figure 8-2. Power-Down Sequence**

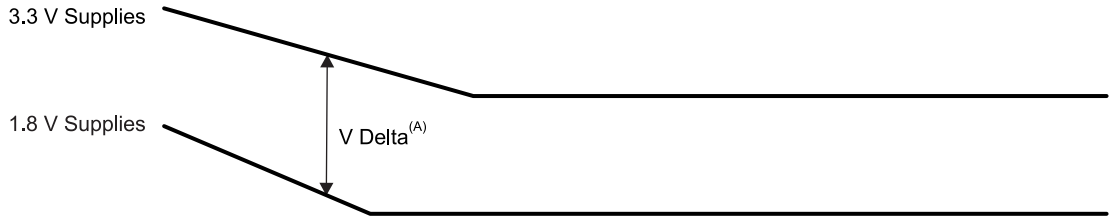


**Figure 8-3. 1.8 V Supplies Falling Before 3.3 V Supplies Delta**

### *8.2.9 Power-Supply Decoupling*

#### 8.2.9.1 Analog and PLL

PLL and Analog supplies benefit from filters or ferrite beads to keep the noise from causing problems. The minimum recommendation is a ferrite bead along with at least one capacitor on the device side of the bead. An additional recommendation is to add one capacitor just before the bead to form a Pi filter. The filter needs to be as close as possible to the device pin, with the device side capacitor being the most important component to be close to the device pin. PLL pins close together can be combined on the same supply, but analog pins should all have their own filters. PLL pins farther away from each other may need their own filtered supply.

#### 8.2.9.2 Digital

Recommended capacitors for power supply decoupling are all 0.1uF in the smallest body size that can be used. Capacitors are more effective in the smallest physical size to limit lead inductance. For example, 0201 sized capacitors are better than 0402 sized capacitors, and so on. TI recommends using capacitors no larger than 0402. Place at least one capacitor for every two power pins. For those power pins that have only one pin, a capacitor is still required. Place one bulk (10 uF or larger) capacitor for every 10 or so power pins as closely as possible to the chip. These larger caps do not need to be under the chip footprint.

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Pay special attention not to put so much capacitance on the supply that it slows the start-up voltage ramp enough to change the power sequencing order. Also be sure to verify that the main chip reset is low until after all supplies are at their correct voltage and stable.

DDR peripheral related supply capacitor numbers are provided in Section 9.13, *DDR2/DDR3 Memory Controller*.


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## 8.3 Reset

### 8.3.1 System-Level Reset Sources

The device has several types of system-level resets. Table 8-8 lists these reset types, along with the reset initiator, and the effects of each reset on the device.

**Table 8-8. System-Level Reset Types**

| TYPE | INITIATOR | RESETS ALL MODULES, EXCLUDING EMAC SWITCH, EMULATION, PLL AND CLOCK CONFIG | RESETS EMAC SWITCH | RESETS EMULATION | PLL AND CLOCK CONFIG | LATCHES BOOT PINS | ASSERTS RSTOUT_WD_OUT PIN |
|---|---|---|---|---|---|---|---|
| Power-on Reset (POR) | POR pin | Yes | Yes | Yes | Yes | Yes | Optional(1)(2) |
| External Warm Reset | RESET pin | Yes | Optional(3) | No | No | Yes | Optional(1)(2) |
| Emulation Warm Reset | On-Chip Emulation Logic | Yes | Optional(3) | No | No | No | Optional(1) |
| Watchdog Reset | Watchdog Timer | Yes | Optional(3) | No | No | No | Yes |
| Software Global Cold Reset | Software | Yes | Optional(3) | Yes | Yes | No | Optional(1) |
| Software Global Warm Reset | Software | Yes | Optional(3) | No | No | No | Optional(1) |
| Test Reset | TRST pin | No | No | Yes | No | No | No |

(1) RSTOUT_WD_OUT pin asserted only if BTMODE[11] was latched as "0" when coming out of reset.
(2) While POR and/or RESET is asserted, the RSTOUT_WD_OUT pin is 3-stated and the internal pull resistor is disabled; therefore, an external pullup/pulldown can be used to set the state of this pin (high/low) while POR and/or RESET is asserted. For more detailed information on external PUs/PDs, see Section 5.5.1, *Pullup/Pulldown Resistors*.
(3) EMAC Switch is NOT reset when the ISO_CONTROL bit in the RESET_ISO Control Module register is set to "1".

### 8.3.2 Power-on Reset (POR pin)

Power-on Reset (POR) is initiated by the POR pin and is used to reset the entire chip, including the Test and Emulation logic, and the EMAC Switch. POR is also referred to as a cold reset since it is required to be asserted when the device goes through a power-up cycle. However, a device power-up cycle is not required to initiate a Power-on Reset.

The following sequence ***must*** be followed during a Power-on Reset:

1. Wait for the power supplies to reach normal operating conditions while keeping the POR pin asserted.
2. Wait for the input clock sources DEV_CLKIN, AUX_CLKIN, and SERDES_CLKN/P to be stable (if used by the system) while keeping the POR pin asserted (low).
3. Once the power supplies and the input clock sources are stable, the POR pin must remain asserted (low) [see Section 8.3.18, *Reset Electrical Data/Timing*]. Within the low period of the POR pin, the following happens:
   (a) All pins except Emulation pins enter a Hi-Z mode and the associated pulls, if applicable, will be enabled.
   (b) The PRCM asserts reset to all modules within the device.
   (c) The PRCM begins propagating these clocks to the chip with the PLLs in BYPASS mode.
4. The POR pin may now be de-asserted (driven high). When the POR pin is de-asserted (high):
   (a) The BTMODE[15:0] pins are latched.
   (b) Reset to the ARM Cortex-A8 and Modules without a local processor is de-asserted.
   (c) RSTOUT_WD_OUT is briefly asserted if BTMODE[11] was latched as "0".
   (d) The clock, reset, and power-down state of each peripheral is determined by the default settings of the PRCM.
   (e) The ARM Cortex-A8 begins executing from the Boot ROM.

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### 8.3.3 External Warm Reset ($\overline{\text{RESET}}$ pin)

An external warm reset is activated by driving the $\overline{\text{RESET}}$ pin active-low. This resets everything in the device, except for the Test and Emulation logic, and the EMAC Switch (optional). An emulator session stays alive during warm reset.

The following sequence ***must*** be followed during a warm reset:

1. Power supplies and input clock sources should already be stable.
2. The $\overline{\text{RESET}}$ pin must be asserted (low)[see Section 8.3.18, *Reset Electrical Data/Timing*]. Within the low period of the $\overline{\text{RESET}}$ pin, the following happens:
   (a) All pins, except Test and Emulation pins, enter a Hi-Z mode and the associated pulls, if applicable, will be enabled.
   (b) The PRCM asserts reset to all modules within the device, except for the Test and Emulation logic, EMAC Switch (optional), PLL, and Clock configuration.
3. The $\overline{\text{RESET}}$ pin may now be de-asserted (driven high). When the $\overline{\text{RESET}}$ pin is de-asserted (high):
   (a) The BTMODE[15:0] pins are latched.
   (b) Reset to the ARM Cortex-A8 and modules without a local processor is de-asserted, with the exception of Test and Emulation logic, EMAC Switch (optional), PLL, and Clock configuration.
   (c) $\overline{\text{RSTOUT_WD_OUT}}$ is asserted [see Section 8.3.18, *Reset Electrical Data/Timing*], if BTMODE[11] was latched as "0".
   (d) The clock, reset, and power-down state of each peripheral is determined by the default settings of the PRCM.
   (e) The ARM Cortex-A8 begins executing from the Boot ROM.

### 8.3.4 Emulation Warm Reset

An Emulation Warm Reset is activated by the on-chip Emulation Module and has the same effect and requirements as an External Warm Reset ($\overline{\text{RESET}}$), with the following exceptions:

- BTMODE[15:0] pins are not re-latched
- $\overline{\text{RSTOUT_WD_OUT}}$ is not 3-stated and is actively driven based on the value previously latched on the BTMODE[11] pin.

The emulator initiates an Emulation Warm Reset via the ICEPICK module. To invoke the Emulation Warm Reset via the ICEPICK module, the user can perform the following from the Code Composer Studio™ IDE menu: Target -> Reset -> System Reset.

### 8.3.5 Watchdog Reset

A Watchdog Reset is initiated when the Watchdog Timer counter reaches zero and has the same effect and requirements as an External Warm Reset ($\overline{\text{RESET}}$ pin), with the following exceptions:

- BTMODE[15:0] pins are not re-latched
- $\overline{\text{RSTOUT_WD_OUT}}$ is not 3-stated and is actively driven based on the value previously latched on the BTMODE[11] pin.

In addition, a Watchdog Reset always results in $\overline{\text{RSTOUT_WD_OUT}}$ being asserted, regardless of whether the BTMODE[11] pin was latched as "0" or "1".

### 8.3.6 Software Global Cold Reset

A Software Global Cold Reset is initiated under software control and has the same effect and requirements as a $\overline{\text{POR}}$ Reset, with the following exceptions:

- BTMODE[15:0] pins are not re-latched and EMAC Switch (optional) is not reset
- $\overline{\text{RSTOUT_WD_OUT}}$ is not 3-stated and is actively driven based on the value previously latched on the BTMODE[11] pin.


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Software initiates a Software Global Cold Reset by writing a "1" to the RST_GLOBAL_COLD_SW bit in the PRM_RSTCTRL register in the PRCM.

For more detailed information on the PRM_RSTCTRL register, see the PRCM Registers section of the *Power, Reset, and Clock Management (PRCM) Module* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

### 8.3.7 Software Global Warm Reset

A Software Global Warm Reset is initiated under software control and has the same effect and requirements as a External Warm Reset ($\overline{\text{RESET}}$ pin), with the following exceptions:

- BTMODE[15:0] pins are not re-latched
- $\overline{\text{RSTOUT_WD_OUT}}$ is not 3-stated and is actively driven based on the value previously latched on the BTMODE[11] pin.

Software initiates a Software Global Warm Reset by writing a "1" to the RST_GLOBAL_WARM_SW bit in the PRM_RSTCTRL register in the PRCM.

For more detailed information on the PRM_RSTCTRL register, see the PRCM Registers section of the *Power, Reset, and Clock Management (PRCM) Module* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

### 8.3.8 Test Reset ($\overline{\text{TRST}}$ pin)

A Test Reset is activated by the emulator asserting the $\overline{\text{TRST}}$ pin. The only effect a Test Reset has is to reset the Test and Emulation Logic.

### 8.3.9 Local Reset

The Local Reset for various Modules within the device is controlled by programming the PRCM and/or the Peripheral Module's internal registers. Only the associated Module is reset when a Local Reset is asserted, leaving the rest of the device unaffected.

For more details on Peripheral Local Resets, see the Reset Management section of the *Power, Reset, and Clock Management (PRCM) Module* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

### 8.3.10 Reset Priority

If any of the above reset sources occur simultaneously, the device only processes the highest-priority reset request. The reset request priorities, from high-to-low, are as follows:

1. Power-on Reset ($\overline{\text{POR}}$)
2. Test Reset ($\overline{\text{TRST}}$)
3. External Warm Reset ($\overline{\text{RESET}}$ pin)
4. Emulation Warm Resets
5. Watchdog Reset
6. Software Global Cold/Warm Resets

### 8.3.11 Reset Status Register

The Reset Status Register (PRM_RSTST) contains information about the last reset that occurred in the system. For more information on this register, see the *Power, Reset, and Clock Management (PRCM) Module* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

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### 8.3.12 PCIE Reset Isolation

The device supports reset isolation for the PCI Express (PCIE) module. This means that the PCI Express Subsystem can be reset without resetting the rest of the device.

When the devcie is a PCI Express Root Complex (RC), the PCIE Subsystem can be reset by software through the PRCM. Software should ensure that there are no ongoing PCIE transactions before asserting this reset by first taking the PCIE Subsystem into the IDLE state. After bringing the PCIE Subsystem out of reset, bus enumeration should be performed again and should treat all Endpoints (EP) as if they had just been connected.

When the device is a PCI Express Endpoint (EP), the PCIE Subsystem will generate an interrupt when an in-band reset is received. Software should process this interrupt by putting the PCIE Subsystem in the IDLE state and then asserting the PCIE local reset through the PRCM.

All device level resets mentioned in the previous sections, except Test Reset, will also reset the PCIE Subsystem. Therefore, the PCIE peripheral should issue a Hot Reset to all downstream devices and re-enumerate the bus upon coming out of reset.

For more detailed information on reset isolation procedures, see the PCIe Reset Isolation section of the *Power, Reset, and Clock Management (PRCM) Module* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

### 8.3.13 EMAC Switch Reset Isolation

The device supports reset isolation for the Ethernet Switch (EMAC Switch). This allows the device to undergo all resets listed in Section 8.3.1, *System-Level Reset Sources*, with the exception of $\overline{\text{POR}}$ Reset, without disrupting the Ethernet Switch or the traffic being routed through the switch during the reset condition. The following reset types can optionally provide an EMAC Switch reset isolation by setting the ISO_CONTROL bit in the RESET_ISO Control Module register to a "1":

- External Warm Reset
- Emulation Warm Reset
- Watchdog Reset
- Software Global Cold Reset
- Software Global Warm Reset

When one of above resets occurs and the Ethernet Switch (EMAC Switch) is programmed to be isolated:

- The switch function of the EMAC Switch and the PLL, which provides the reference clocks to the EMAC Switch, will not be reset.
- Several Control Module registers are not reset. For more details, see the description of the RESET_ISO register in the *Control Module* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).
- The pin multiplexing of some of the EMAC Switch pins is unaffected. For more details, see the description of the RESET_ISO register in the *Control Module* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

The EMAC Switch is always reset when:

- One of the above resets occurs and the Ethernet Switch is programmed to be “not isolated”
- A $\overline{\text{POR}}$ Reset occurs


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### 8.3.14 RSTOUT_WD_OUT Pin

The RSTOUT_WD_OUT pin reflects device reset status and is de-asserted (high) when the device is out reset. This output will always be asserted when a Watchdog Timer reset (Watchdog Reset) occurs. In addition, this output is always 3-stated and the internal pull resistor is disabled on this pin while POR and/or RESET is asserted; therefore, an external pullup/pulldown can be used to set the state of this pin (high/low) while POR and/or RESET is asserted. For more detailed information on external PUs/PDs, see Section 5.5.1, *Pullup/Pulldown Resistors*.

If the BTMODE[11] pin is latched as a "0" at the rising edge of POR or RESET, then RSTOUT_WD_OUT is also asserted when any of the below resets occur:

- Power-On Reset (asserted after the BTMODE[11] pin is latched)
- External Warm Reset (asserted after the BTMODE[11] pin is latched)
- Emulation Warm Reset
- Software Global Cold/Warm Reset

The RSTOUT_WD_OUT pin remains asserted until the PRCM releases the host ARM Cortex-A8 processor for reset.

### 8.3.15 Effect of Reset on Emulation and Trace

The device Emulation and Trace Logic will only be reset by the following sources:

- Power-On Reset
- Software Global Cold Reset
- Test Reset

Other than these three reset types, none of the other resets will affect the Emulation and Trace Logic. However, the multiplexing of the EMU[4:2] pins is reset by all system reset types except Test Reset.

### 8.3.16 Reset During Power Domain Switching

Each Power Domain has a dedicated Warm Reset and Cold Reset. Warm Reset for a Power Domain is asserted under either of the following two conditions:

1. An External Warm Reset, Emulation Warm Reset, or Software Global Warm Reset occurs
2. When that Power Domain switches from the "ON" state to the "OFF" state

Cold Reset for a Power Domain is asserted under either of the following two conditions:

1. Power-On Reset or Software Global Cold Reset occurs
2. When that Power Domain switches from the "OFF" state to the "ON" state

### 8.3.17 Pin Behaviors at Reset

When any reset, other than Test Reset, (all described in Section 8.3.1, *System-Level Reset Sources*) is asserted, all device I/O pins are reset into a Hi-Z state except for:

- Emulation Pins. These pins are only put into a Hi-Z state when Test Reset (TRST) is asserted.
- EMAC Switch Pins. These pins are always put into a Hi-Z state during Power-On Reset. However, some EMAC Switch pins will ***not*** be put into a Hi-Z state during the other reset modes when the ISO_CONTROL bit in the RESET_ISO register of the Control Module is programmed as a "1". For more details, see the description of the RESET_ISO register in the *Control Module* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).
- RSTOUT_WD_OUT Pin during any reset types except for POR and RESET. For more detailed information on RSTOUT_WD_OUT pin behavior, see Section 8.3.14, *RSTOUT_WD_OUT Pin*.

- DDR[0]/[1] Address/Control Pins (CLK, $\overline{CLK}$, CKE, $\overline{WE}$, $\overline{CS[1]}/[0]$, $\overline{RAS}$, $\overline{CAS}$, $\overline{ODT[1]}/[0]$, RST, BA[2:0], A[14:0]). These pins are 3-stated during reset. However, these pins are then driven to the same value as their internal pull resistor reset value when reset is released (For the direction of the internal pull during reset, see the DDR[0]/[1] Terminal Functions tables in the Section 4.2.5, *DDR2/DDR3 Memory Controller* of this document).

In addition, the PINCNTL registers, which control pin multiplexing, enabling the IPUs/IPDs, and enabling the receiver, are reset to their default state. Again, enabling the EMAC Switch reset isolation prevents some PINCNTL registers from being reset.

For details on EMAC Switch reset isolation, see the descriptions of the RESET_ISO register and the PINCNTL registers in the *Control Module* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

Internal pull-up/down (IPU/IPD) resistors are enabled during and immediately after reset as described in Section 4.2, *Terminal Functions* of this document.

**NOTE**

Upon coming out of reset, the ARM Cortex-A8 starts executing code from the internal Boot ROM. The Boot ROM code modifies the PINCNTLx registers to configure the associated pins for the chosen primary and backup Bootmodes. For more details on the Boot ROM effects on pin multiplexing, see the *ROM Code Memory and Peripheral Booting* and *Control Module* chapters of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

### 8.3.18 Reset Electrical Data/Timing

**Table 8-9. Timing Requirements for Reset (see Figure 8-4 and Figure 8-5)**

| NO. | | | | OPP100 | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| 1 | $t_{w(RESET)}$ | Pulse duration, $\overline{POR}$ low or $\overline{RESET}$ low | | 12P[1] | | ns |
| 2 | $t_{su(BOOT)}$ | Setup time, BTMODE[15:0] pins valid before $\overline{POR}$ high or $\overline{RESET}$ high | $\overline{POR}$ | 2P[2] | | ns |
| | | | $\overline{RESET}$ | 2P[2] | | ns |
| 3 | $t_{h(BOOT)}$ | Hold time, BTMODE[15:0] pins valid after $\overline{POR}$ high or $\overline{RESET}$ high | | 0 | | ns |

(1) The device clock source ***must*** be stable and at a valid frequency prior to meeting the $t_{w(RESET)}$ requirement.
(2) P = 1/(DEV Clock) frequency in ns.

**Table 8-10. Switching Characteristics Over Recommended Operating Conditions During Reset (see Figure 8-5)**

| NO. | PARAMETER | | | OPP100 | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| 4 | $t_{d(RSTL-IORST)}$ | Delay time, $\overline{RESET}$ low or $\overline{POR}$ low to all I/Os entering their reset state | | | 14 | ns |
| 5 | $t_{d(RSTH-IOFUNC)}$ | Delay time, $\overline{RESET}$ high or $\overline{POR}$ high to all I/Os exiting their reset state | | | 14 | ns |
| 6 | $t_{d(RSTH-RSTOUTH)}$ | Delay time, $\overline{RESET}$ high to $\overline{RSTOUT_WD_OUT}$ high[1][2] | $\overline{RESET}$ assertion $t_{w(RESET)}$ ≥ 30P | 0 | 2P | ns |
| | | | $\overline{RESET}$ assertion $t_{w(RESET)}$ < 30P | 0 | 32P - $t_{w(RESET)}$ | ns |
| 7 | $t_{d(PORH-RSTOUTH)}$ | Delay time, $\overline{POR}$ high to $\overline{RSTOUT_WD_OUT}$ high[1][2] | | 0 | 12500P | ns |
| 8 | $t_{d(RSTL-RSTOUTZ)}$ | Delay time, $\overline{RESET}$ low to $\overline{RSTOUT_WD_OUT}$ Hi-Z[1][2] | | 0 | 2P | ns |

(1) For more detailed information on $\overline{RSTOUT_WD_OUT}$ pin behavior, see Section 8.3.14, *$\overline{RSTOUT_WD_OUT}$ Pin*.
(2) P = 1/(DEV Clock) frequency in ns.


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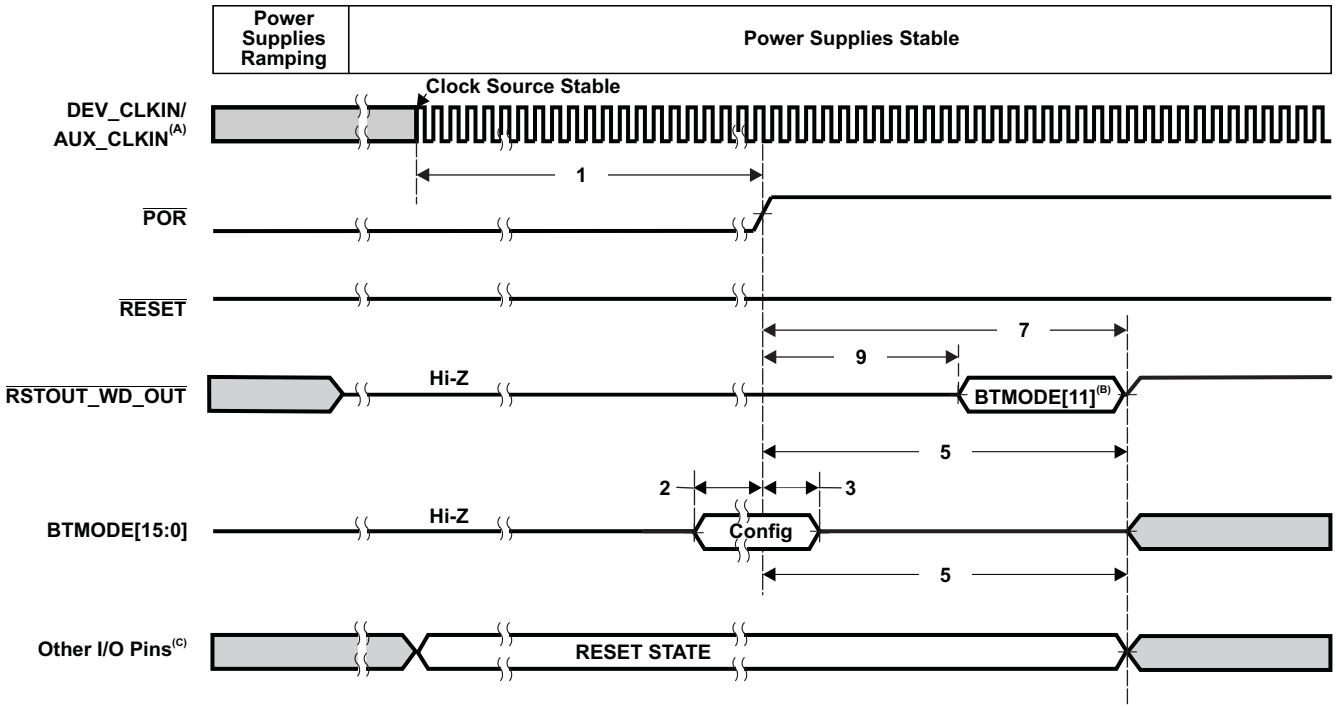
**Table 8-10. Switching Characteristics Over Recommended Operating Conditions During Reset (see Figure 8-5) (continued)**

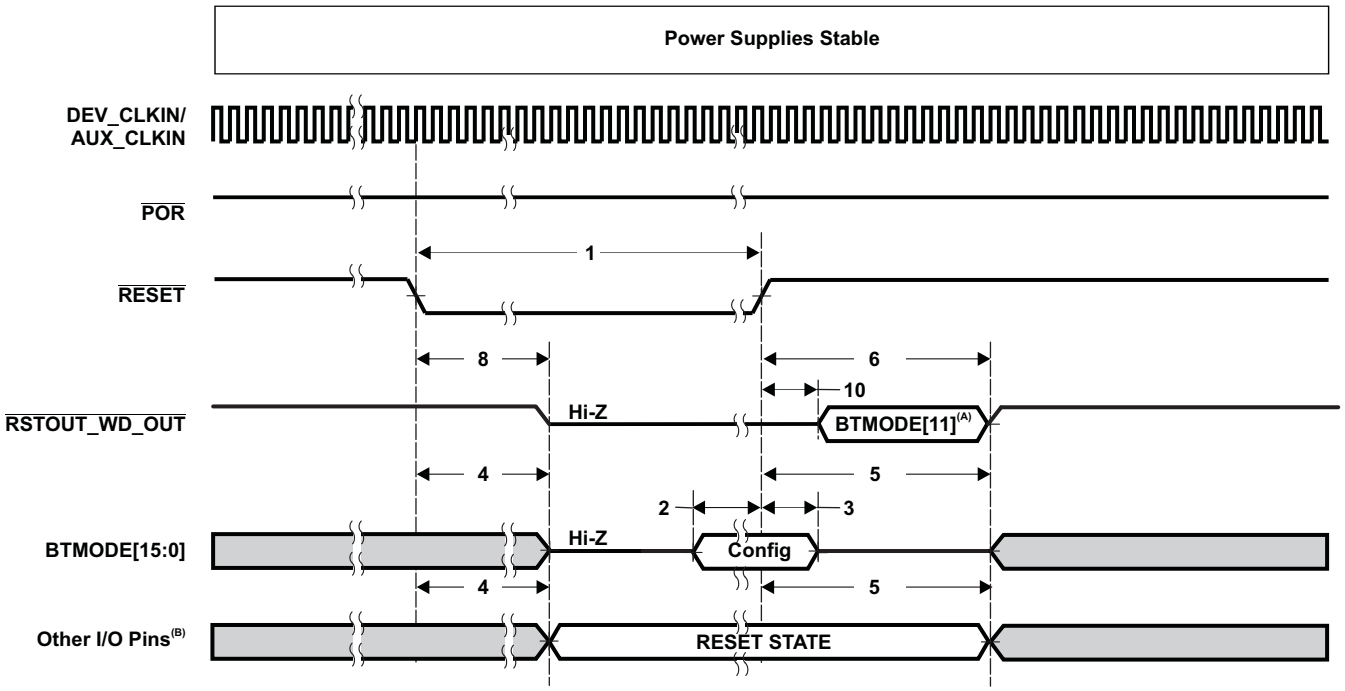
| NO. | PARAMETER | | OPP100 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 9 | $t_{d(PORH-RSTOUTL)}$ | Delay time, $\overline{POR}$ high to $\overline{RSTOUT_WD_OUT}$ driven based on latched BTMODE[11] value(1)(2) | 0 | 2P | ns |
| 10 | $t_{d(RSTH-RSTOUTD)}$ | Delay time, $\overline{RESET}$ high to $\overline{RSTOUT_WD_OUT}$ driven based on latched BTMODE[11] value(1)(2) | 0 | 2P | ns |

Figure 8-4 shows the Power-Up Timing. Figure 8-5 shows the Warm Reset ($\overline{RESET}$) Timing. Max Reset Timing is identical to Warm Reset Timing, except the BTMODE[15:0] pins are ***not*** re-latched.




A. Power supplies and DEV_CLKIN/AUX_CLKIN must be stable before the start of $t_{w(RESET)}$.
B. $\overline{RSTOUT_WD_OUT}$ only asserted if BTMODE[11] was latched as a "0" when coming out of reset.
C. For more detailed information on the RESET STATE of each pin, see Section 8.3.17, *Pin Behaviors at Reset*. Also see Section 4.2, *Terminal Functions* for the IPU/IPD settings during reset.

**Figure 8-4. Power-Up Timing**




A. RSTOUT_WD_OUT only asserted if BTMODE[11] was latched as a "0" when coming out of reset.

B. For more detailed information on the RESET STATE of each pin, see Section 8.3.17, *Pin Behaviors at Reset*. Also see Section 4.2, *Terminal Functions* for the IPU/IPD settings during reset.

**Figure 8-5. Warm Reset (RESET) Timing**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## 8.4 Clocking

The device clocks are generated from several reference clocks that are fed to on-chip PLLs and dividers (both inside and outside of the PRCM Module). Figure 8-6 shows a high-level overview of the device system clocking structure (Note: to reduce complexity, not all clocking connections are shown). For detailed information on the device clocks, see the Clock Generation and Management section of the *Power, Reset, and Clock Management (PRCM) Module* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

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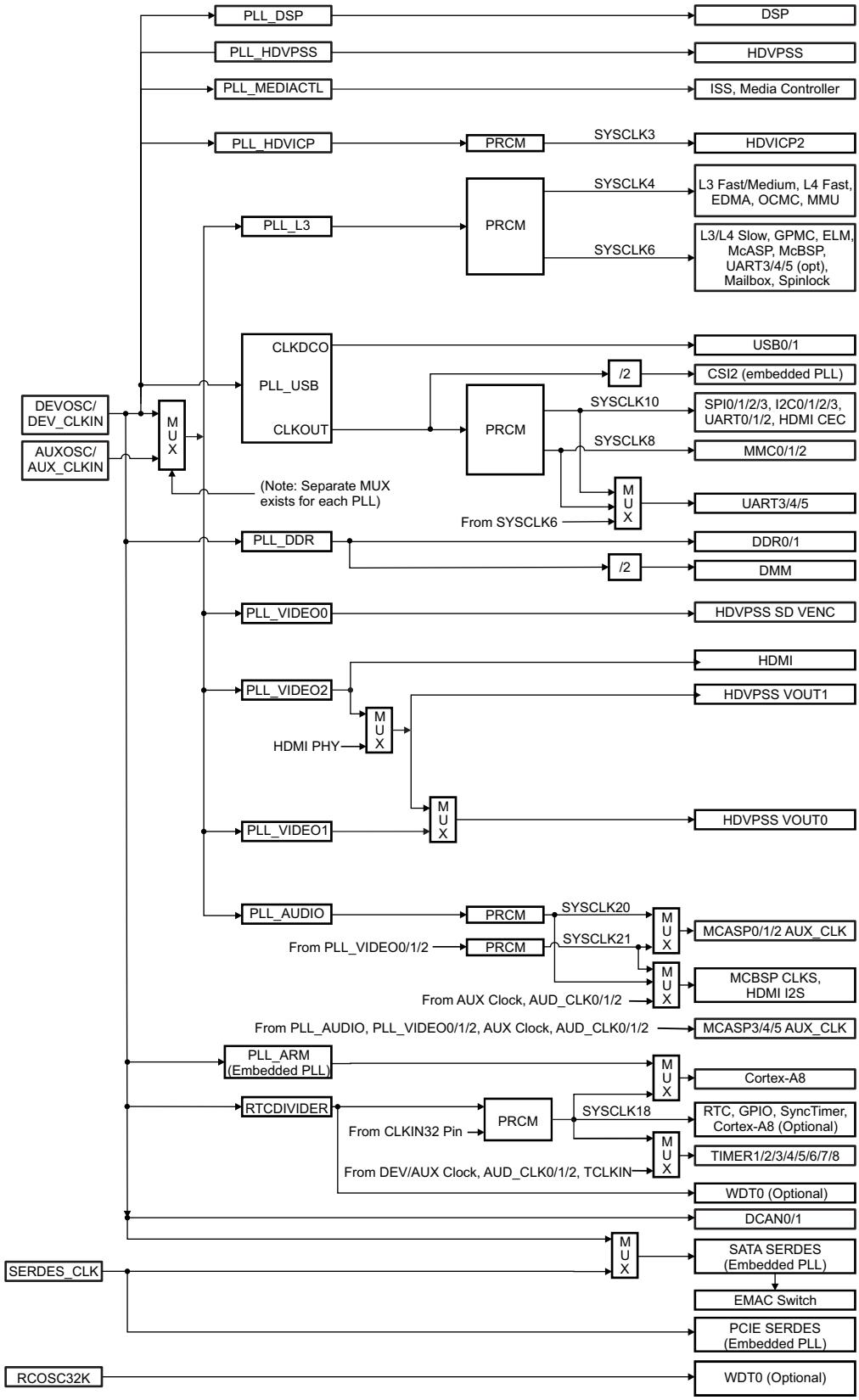


**Figure 8-6. System Clocking Overview**


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### 8.4.1 Device (DEV) and Auxiliary (AUX) Clock Inputs

The device provides two clock inputs, Device (DEVOSC_MXI/DEV_CLKIN) and Auxiliary (AUXOSC_MXI/AUX_CLKIN). The Device (DEV) clock is used to generate the majority of the internal reference clocks, while the Auxiliary (AUX) clock can optionally be used as a source for the Audio and/or Video PLLs.

The DEV and AUX clocks can be sourced in two ways:

1. Using an external crystal in conjunction with the internal oscillator *or*
2. Using an external 1.8-V LVCMOS-compatible clock input

**Note:** The external crystals used with the internal oscillators ***must*** operate in fundamental parallel resonant mode *only*. There is no overtone support.

The DEV Clock should in most cases be 20 MHz. However, it can optionally range anywhere from 20 - 30 MHz if the following are true:

- The DEV Clock is not used to source the EMAC switch reference clock
- A precise 32768-Hz clock is not needed for Real-Time Clock functionality
- If the boot mode is FAST XIP

The AUX Clock is optional and can range from 20-30 MHz. AUX Clock can be used to source the Audio and/or Video PLLs when a very precise audio or video frequency is required.

#### 8.4.1.1 Using the Internal Oscillators

When the internal oscillators are used to generate the DEV and AUX clocks, external crystals are required to be connected across the DEVOSC or AUXOSC oscillator MXI and MXO pins, along with two load capacitors (see Figure 8-7 and Figure 8-8). The external crystal load capacitors should also be connected to the associated oscillator ground pin (VSSA_DEVOSC or VSSA_AUXOSC). The capacitors should ***not*** be connected to board ground (VSS).

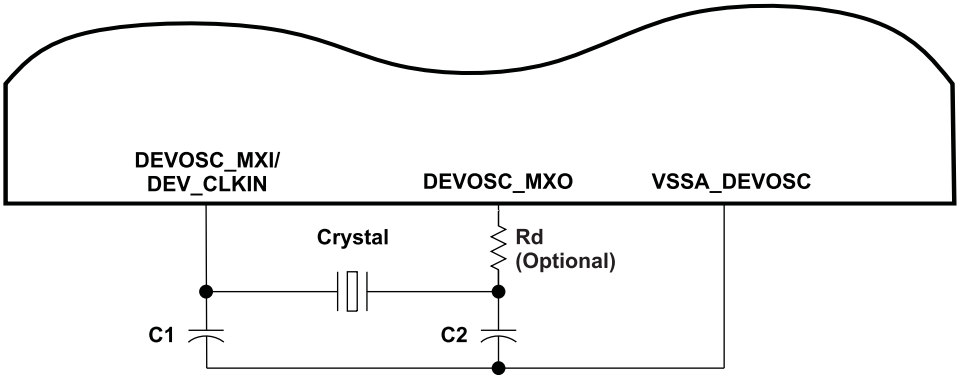


**Figure 8-7. Device Oscillator**

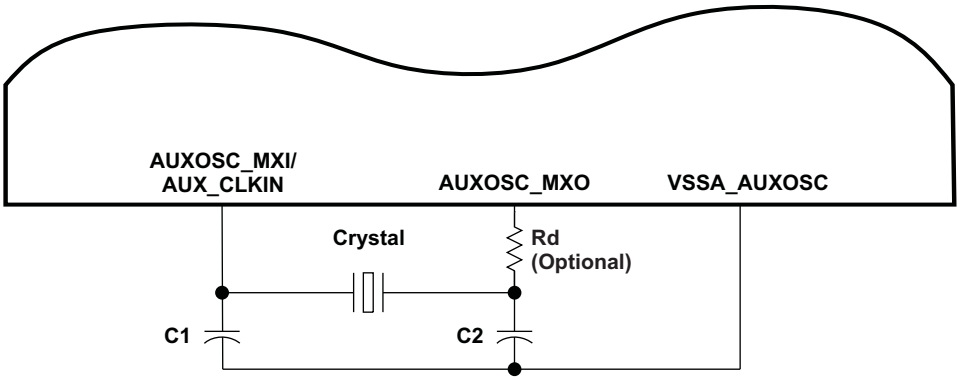


**Figure 8-8. Auxiliary Oscillator**

The load capacitors, C1 and C2 in the above pictures, should be chosen such that the below equation is satisfied. CL in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator MXI, MXO, and VSS pins.

$$C_L = \frac{C_1 C_2}{(C_1 + C_2)}$$

**Table 8-11. Input Requirements for Crystal Circuit on the Device Oscillator (DEVOSC)**

| PARAMETER | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Start-up time (from power up until oscillating at stable frequency) | | | | 4 | ms |
| | Crystal Oscillation frequency(1) | | 20 | 20 | 30 | MHz |
| | Parallel Load Capacitance (C1 and C2) | | 12 | | 24 | pF |
| | Crystal ESR | | | | 50 | Ω |
| | Crystal Shunt Capacitance | | | | 5 | pF |
| | Crystal Oscillation Mode | | | Fundamental Only | | n/a |
| | Crystal Frequency Stability | If Ethernet not used | | | ±200 | ppm |
| | | If MII ***is*** used and RGMII, RMII not used | | | ±100 | |
| | | If RGMII, or RMII used | | | ±50 | |

(1) 20-MHz DEV clock is required for all bootmodes other than Fast XIP. For more detailed information on boot modes, see the *ROM Code Memory and Peripheral Booting* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

**Table 8-12. Input Requirements for Crystal Circuit on the Auxiliary Oscillator (AUXOSC)**

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| | Start-up time (from power up until oscillating at stable frequency) | | 4 | ms |
| | Crystal Oscillation frequency | 20 | 30 | MHz |
| | Parallel Load Capacitance (C1 and C2) | 12 | 24 | pF |
| | Crystal ESR | | 50 | Ω |
| | Crystal Shunt Capacitance | | 5 | pF |
| | Crystal Oscillation Mode | Fundamental Only | | n/a |
| | Crystal Frequency stability(1) | | ±50 | ppm |

(1) Applies only when sourcing the HDMI or HDVPSS DAC clocks from the AUXOSC


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#### 8.4.1.2 Using a 1.8V LVCMOS-Compatible Clock Input

A 1.8-V LVCMOS-Compatible Clock Input can be used instead of the internal oscillators as the DEV and AUX clock inputs to the system. The external connections to support this are shown in Figure 8-9 and Figure 8-10. The DEV_CLKIN and AUX_CLKIN pins are connected to the 1.8-V LVCMOS-Compatible clock sources. The DEV_MXO and AUX_MXO pins are left unconnected. The VSSA_DEVOSC and VSSA_AUXOSC pins are connected to board ground (VSS).

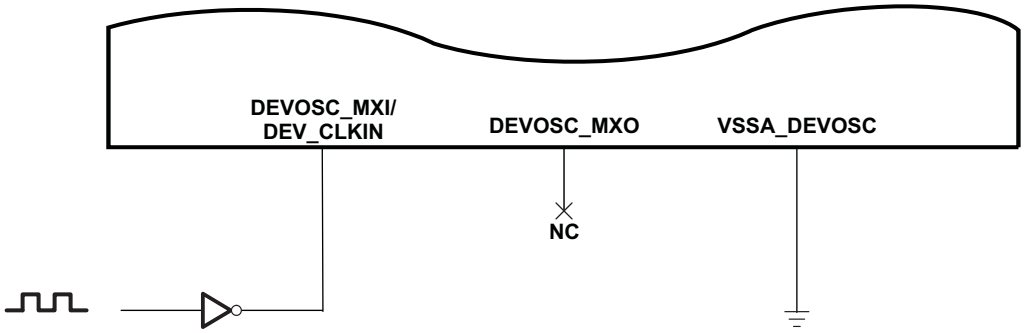


**Figure 8-9. 1.8-V LVCMOS-Compatible Clock Input (DEV_OSC)**

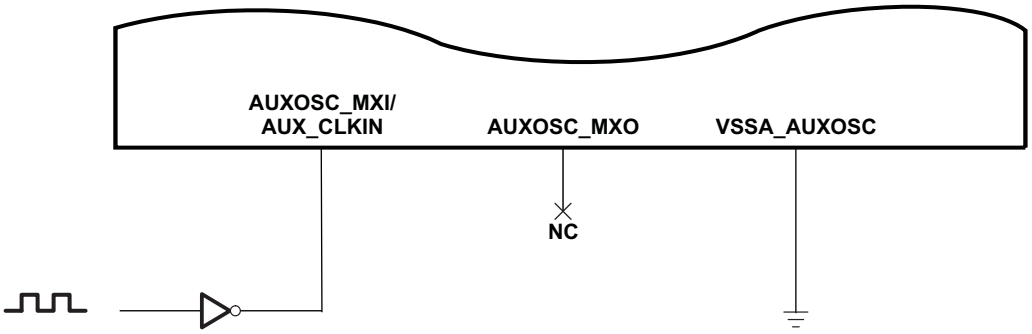


**Figure 8-10. 1.8-V LVCMOS-Compatible Clock Input (AUX_OSC)**

The clock source ***must*** meet the DEVOSC_MXI/DEV_CLKIN timing requirements shown in Table 8-15, *Timing Requirements for DEVOSC_MXI/DEV_CLKIN*.

The clock source must meet the AUXOSC_MXI/AUX_CLKIN timing requirements shown in Table 8-16, *Timing Requirements for AUXOSC_MXI/AUX_CLKIN*.

### *8.4.2 SERDES_CLKN/P Input Clock*

A high-quality, low-jitter differential clock source is required for the PCIE PHY. The clock is required to be AC coupled to the SERDES_CLKP and SERDES_CLKN device pins according to the specifications in Table 8-13. Both the clock source and the coupling capacitors should be placed physically as close to the processor as possible. In addition, make sure to follow any PCB routing and termination recommendations that the clock source manufacturer recommends.

**Table 8-13. SERDES_CLKN/P AC Coupling Capacitors Recommendations**

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| | SERDES_CLKN/P AC coupling capacitor value | 0.24 | 0.27 | 1.0 | nF |
| | SERDES_CLKN/P AC coupling capacitor package size(1)(2) | | 0402 | 0603 | EIA |

(1) L x W, 10 Mil units, that is, a 0402 is a 40 x 20 Mil surface mount capacitor.
(2) The physical size of the capacitor should be as small as practical. Use the same size on both lines in each pair placed side-by-side.

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The differential clock source is required to meet the REFCLK AC Specifications outlined in the *PCI EXPRESS CARD ELECTROMECHANICAL SPECIFICATION, REV. 2.0*, at the input to the AC coupling capacitors.

In addition, LVDS clock sources that are compliant to the above specification, but with the following exceptions, are also acceptable:

**Table 8-14. Acceptable Exceptions to the REFCLK AC Specifications for LVDS Clock Sources**

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IH}$ | Differential High-Level Input Voltage | 125 | 1000 | mV |
| $V_{IL}$ | Differential Low-Level Input Voltage | -1000 | -125 | mV |

### 8.4.3 AUD_CLKINx Input Clocks

External clock inputs can optionally be provided at the AUD_CLKIN0/1/2 pins to serve as a reference clocks for the following modules:

- McASP3/4/5
- McBSP
- TIMER1/2/3/4/5/6/7/8

### 8.4.4 CLKIN32 Input Clock

An external 32768-Hz clock input can optionally be provided at the CLKIN32 pin to serve as a reference clock in place of the RTCDIVIDER clock for the following Modules:

- RTC
- GPIO0/1/2/3
- TIMER1/2/3/4/5/6/7/8
- ARM Cortex-A8
- SYNCTIMER

The CLKIN32 source must meet the timing requirements shown in Table 8-18.

### 8.4.5 External Input Clocks

There are three pins referred to as AUD_CLKIN0,1,2 which are used as optional sources for HDMI I2S, McASP, McBSP and TIMER1-8. The maximum IO pin frequency for these three input clocks is 50MHz.

### 8.4.6 Output Clocks Select Logic

The device includes two selectable general-purpose clock outputs (CLKOUT0 and CLKOUT1). The source for these output clocks is controlled by the CLKOUT_MUX register in the Control Module (see Figure 8-11).


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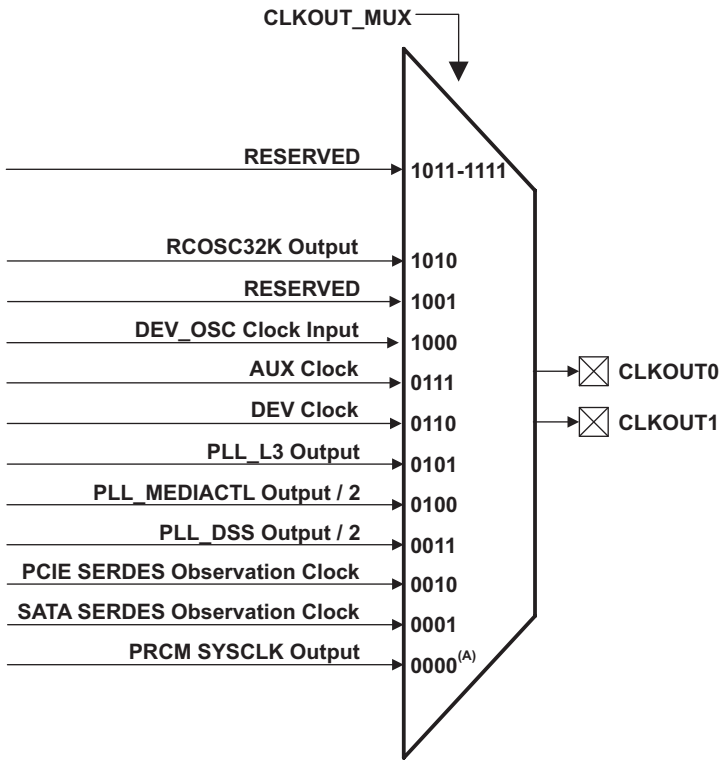


A. Muxed output of DEVOSC clock, USBPLL clock output, VIDEO0 PLL Clock output, and RTC DIVIDER output.

**Figure 8-11. CLKOUTx Source Selection Logic**

For detailed information on the CLKOUTx switching characteristics, see Table 8-19.

### 8.4.7 Input/Output Clocks Electrical Data/Timing

**Note:** If an external clock oscillator is used, a single clean power supply should be used to power both the device and the external clock oscillator circuit.

**Table 8-15. Timing Requirements for DEVOSC_MXI/DEV_CLKIN(1) (2) (3)(see Figure 8-12)**

| NO. | | | | OPP100 | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | NOM | MAX | |
| 1 | $t_{c(DMXI)}$ | Cycle time, DEVOSC_MXI/DEV_CLKIN | | 33.$\overline{33}$ | 50 | 50 | ns |
| 2 | $t_{w(DMXIH)}$ | Pulse duration, DEVOSC_MXI/DEV_CLKIN high | | 0.45C | | 0.55C | ns |
| 3 | $t_{w(DMXIL)}$ | Pulse duration, DEVOSC_MXI/DEV_CLKIN low | | 0.45C | | 0.55C | ns |
| 4 | $t_{t(DMXI)}$ | Transition time, DEVOSC_MXI/DEV_CLKIN | | | | 7 | ns |
| 5 | $t_{J(DMXI)}$ | Period jitter, DEVOSC_MXI/DEV_CLKIN | | | | 0.02C | ns |
| | | Frequency Stability | If Ethernet not used | | | ±200 | ppm |
| | | | If MII is used and RGMII, RMII not used | | | ±100 | |
| | | | If RGMII, or RMII used | | | ±50 | |

(1) The DEVOSC_MXI/DEV_CLKIN frequency and PLL settings should be chosen such that the resulting SYSCLKs and Module Clocks are within the specific ranges shown in the Section 8.4.9, *SYSCLKs* and Section 8.4.10, *Module Clocks*.
(2) The reference points for the rise and fall transitions are measured at $V_{IL}$ MAX and $V_{IH}$ MIN.
(3) C = DEV_CLKIN cycle time in ns. For example, when DEVOSC_MXI/DEV_CLKIN frequency is 20 MHz, use C = 50 ns.

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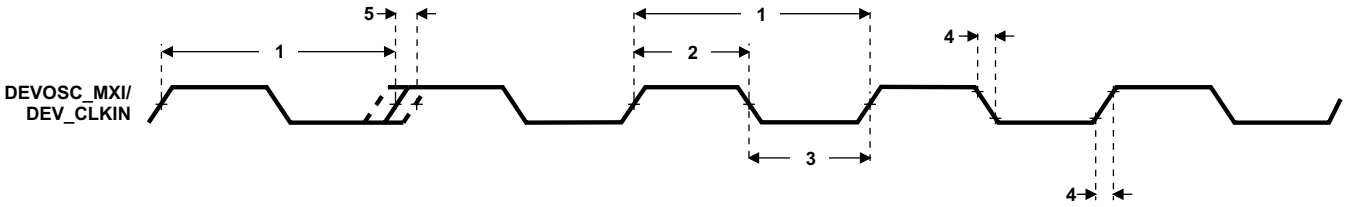


**Figure 8-12. DEV_MXI/DEV_CLKIN Timing**


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**Table 8-16. Timing Requirements for AUX_MXI/AUX_CLKIN (1) (2) (see Figure 8-13)**

| NO. | | | OPP100 | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | |
| 1 | $t_{c(AMXI)}$ | Cycle time, AUXOSC_MXI/AUX_CLKIN | $33.\overline{3}$ | 50 | 50 | ns |
| 2 | $t_{w(AMXIH)}$ | Pulse duration, AUXOSC_MXI/AUX_CLKIN high | 0.45C | | 0.55C | ns |
| 3 | $t_{w(AMXIL)}$ | Pulse duration, AUXOSC_MXI/AUX_CLKIN low | 0.45C | | 0.55C | ns |
| 4 | $t_{t(AMXI)}$ | Transition time, AUXOSC_MXI/AUX_CLKIN | | | 7 | ns |
| 5 | $t_{J(AMXI)}$ | Period jitter, AUXOSC_MXI/AUX_CLKIN | | | 0.02C | ns |
| 6 | $S_f$ | Frequency stability, AUXOSC_MXI/AUX_CLKIN (3) | | | ± 50 | ppm |

(1) The reference points for the rise and fall transitions are measured at $V_{IL}$ MAX and $V_{IH}$ MIN.
(2) C = AUX_CLKIN cycle time in ns. For example, when AUXOSC_MXI/AUX_CLKIN frequency is 20 MHz, use C = 50 ns.
(3) Applies only when sourcing the HDMI or HDVPSS DAC clocks from the AUXOSC.

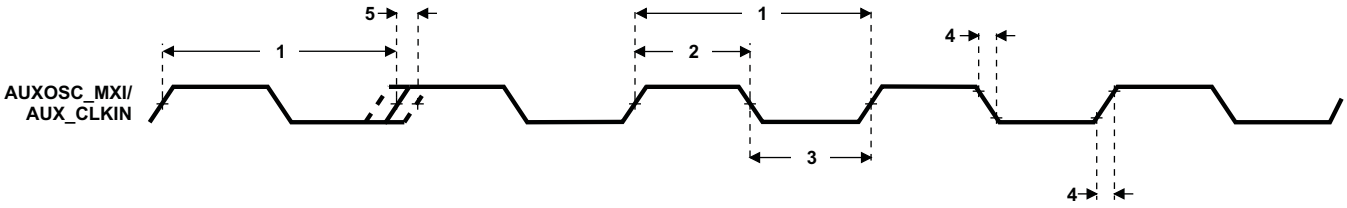


**Figure 8-13. AUX_MXI/AUX_CLKIN Timing**

**Table 8-17. Timing Requirements for AUD_CLKINx (1) (see Figure 8-14)**

| NO. | | | OPP100/120/166 | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | |
| 1 | $t_{c(AUD_CLKINx)}$ | Cycle time, AUD_CLKINx | 20 | | | ns |
| 2 | $t_{w(AUD_CLKINxH)}$ | Cycle time, AUD_CLKINx | 0.45A | | 0.55 A | ns |
| 3 | $t_{w(AUD_CLKINxL)}$ | Cycle time, AUD_CLKINx | 0.45A | | 0.55 A | ns |

(1) A = AUD_CLKINx cycle time in ns.

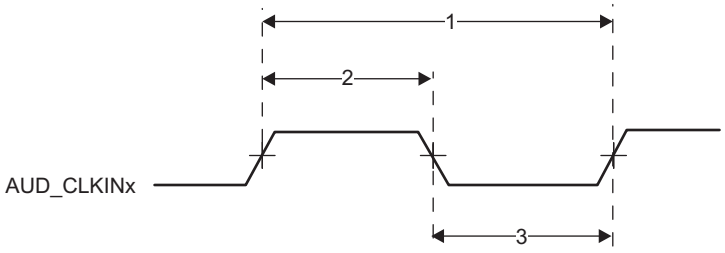


**Figure 8-14. AUD_CLKINx Timing**


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**Table 8-18. Timing Requirements for CLKIN32 (1)(2) (see Figure 8-15)**

| NO. | | | OPP100 | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | |
| 1 | $t_{c(CLKIN32)}$ | Cycle time, CLKIN32 | 1/32768 | | | s |
| 2 | $t_{w(CLKIN32H)}$ | Pulse duration, CLKIN32 high | 0.45C | | 0.55C | ns |
| 3 | $t_{w(CKIN32L)}$ | Pulse duration, CLKIN32 low | 0.45C | | 0.55C | ns |
| 4 | $t_{t(CLKIN32)}$ | Transition time, CLKIN32 | | | 7 | ns |
| 5 | $t_{J(CLKIN32)}$ | Period jitter, CLKIN32 | | | 0.02C | ns |

(1) The reference points for the rise and fall transitions are measured at $V_{IL}$ MAX and $V_{IH}$ MIN.
(2) C = CLKIN32 cycle time in ns. For example, when CLKIN32 frequency is 32768 Hz, use C = 1/32768 s.

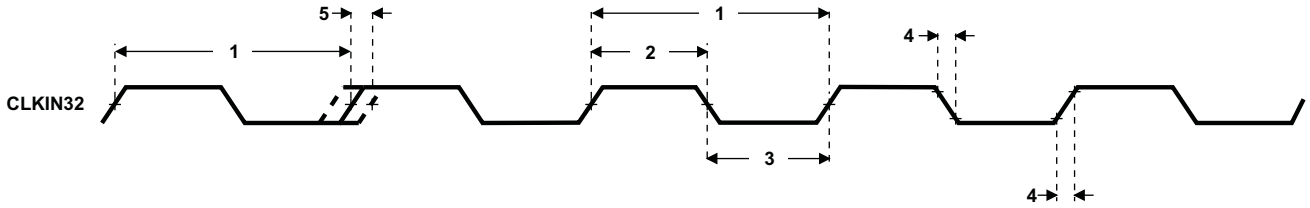


**Figure 8-15. CLKIN32 Timing**

**Table 8-19. Switching Characteristics Over Recommended Operating Conditions for CLKOUTx (CLKOUT0 and CLKOUT1)(1) (2) (see Figure 8-16)**

| NO. | PARAMETER | | OPP100 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{c(CLKOUTx)}$ | Cycle time, CLKOUTx | 5 | | ns |
| 2 | $t_{w(CLKOUTxH)}$ | Pulse duration, CLKOUTx high | 0.45P | 0.55P | ns |
| 3 | $t_{w(CLKOUTxL)}$ | Pulse duration, CLKOUTx low | 0.45P | 0.55P | ns |
| 4 | $t_{t(CLKOUTx)}$ | Transition time, CLKOUTx | | 0.05P | ns |

(1) The reference points for the rise and fall transitions are measured at $V_{OL}$ MAX and $V_{OH}$ MIN.
(2) P = 1/CLKOUTx clock frequency in nanoseconds (ns). For example, when CLKOUTx frequency is 200 MHz, use P = 5 ns.

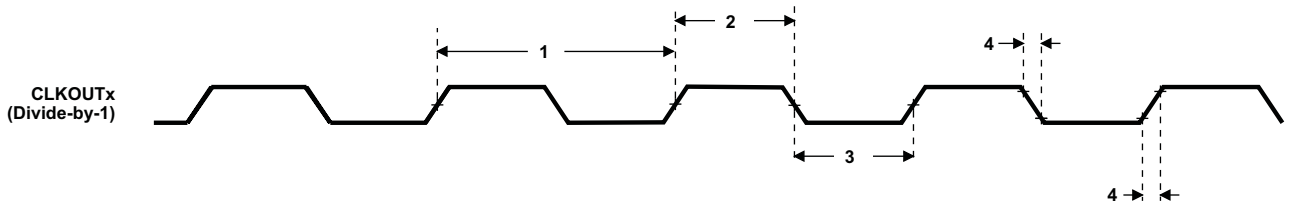


**Figure 8-16. CLKOUTx Timing**

### 8.4.8 PLLs

The device contains 12 top-level PLLs, and 4 embedded PLLs (within the ) that provide clocks to different parts of the system. Figure 8-17 and Figure 8-18 show simplified block diagrams of the Top-Level PLL and PLL_ARM. In addition, see the System Clocking Overview (Figure 8-6) for a high-level view of the device clock architecture including the PLL reference clock sources and connections.

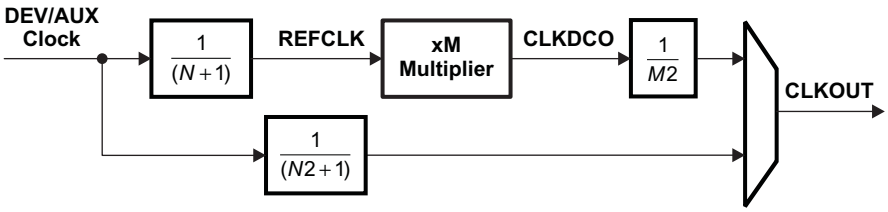


**Figure 8-17. Top-Level PLL Simplified Block Diagram**

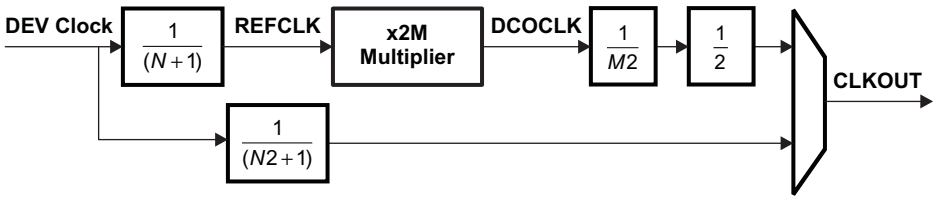


**Figure 8-18. PLL_ARM Simplified Block Diagram**

The reference clock for most of the PLLs comes from the DEV input clock, with select PLLs also having the option to use the AUX input clock as a reference. Also, each PLL supports a Bypass mode in which the reference clock can be directly passed to the PLL CLKOUT through a divider. All device PLL's will come-up in Bypass mode after reset.

For details on programming the device PLLs, see the *Control Module* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).


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#### 8.4.8.1 PLL Power Supply Filtering

The device PLLs are supplied externally via the VDDA_**x**PLL_1P8 power-supply pins (where "**x**" represents ARM, VID0, VID1, AUDIO, DDR, and/or L3). External filtering must be added on the PLL supply pins to ensure that the requirements in Table 8-20 are met.

**Table 8-20. PLL Power Supply Requirements**

| PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|
| Dynamic noise at VDDA_**x**PLL_1P8 pins | | 50 | mV p-p |

#### 8.4.8.2 PLL Multipliers and Dividers

The Top-Level and PLL_ARM PLLs support the internal multiplier and divider values shown in Table 8-21, *Top-Level PLL Multiplier and Divider Limits* and Table 8-22, *PLL_ARM Multiplier and Divider Limits*. The PLLs must be programmed to conform to the various REFCLK, CLKDCO, DCOCLK, and CLKOUT limits described in Section 8.4.8.3, *PLL Frequency Limits*.

**Table 8-21. Top-Level PLL Multiplier and Divider Limits**

| PARAMETER | MIN | MAX |
|---|---|---|
| N Pre-Divider | 0 | 255 |
| PLL Multiplier (M) | 2 | 4095(1) |
| M2 Post Divider | 1 | 127 |
| N2 Bypass Divider | 0 | 15 |

(1) The PLL Multiplier supports fractional values (up to 18-bits of fraction) except when the PLL Multiplier is > 4093.

**Table 8-22. PLL_ARM Multiplier and Divider Limits**

| PARAMETER | MIN | MAX |
|---|---|---|
| N Pre-Divider | 0 | 127 |
| PLL Multiplier (M)(1) | 2 | 2047(2) |
| M2 Post Divider | 1 | 31 |
| N2 Bypass Divider | 0 | 15 |

(1) This parameter describes the limits on the programmable multiplier value M. The multiplication factor for the PLL_ARM is equal to 2 * M (also see Figure 8-18).
(2) The PLL Multiplier supports fractional values (up to 18-bits of fraction) except when the PLL Multiplier is < 20 OR > 2045.

#### 8.4.8.3 PLL Frequency Limits

Each PLL supports a minimum and maximum operating frequency for its REFCLK, CKLDCO, and CLKOUT values. The PLLs must be configured not to exceed any of the constraints placed on these values shown in Table 8-23 through Table 8-25. Care must be taken to stay within these limits when selecting external clock input frequencies, internal divider values, and PLL multiply ratios. In addition, limits shown in these tables may be further restricted by the clock frequency limitations of the device modules using these clocks. For more detailed information on the SYSCLK and Module Clock frequency limits, see Section 8.4.9, *SYSCLKs* and Section 8.4.10, *Module Clocks*.

**Table 8-23. Top-Level PLL Frequency Ranges (ALL OPPs)**

| CLOCK | MIN | MAX | UNIT |
|---|---|---|---|
| REFCLK | 0.5 | 2.5 | MHz |
| CLKDCO (HS1)(1) | 1000 | 2000 | MHz |
| CLKDCO (HS2)(2) | 500 | 1000 | MHz |

(1) The PLL has two modes of operation: HS1 and HS2. The mode of operation should be set, according to the desired CLKDCO frequency, by programming the SELFREQDCO field of the ADPLLLJx_CLKCTRL registers in the Control Module.
(2) CLKDCO of the PLL_USB is used undivided by the USB modules; therefore, CLKDCO for the PLL_USB PLL must be programmed to 960 MHz for proper operation.

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**Table 8-23. Top-Level PLL Frequency Ranges (ALL OPPs) (continued)**

| CLOCK | MIN | MAX | UNIT |
|---|---|---|---|
| CLKOUT | see Table 8-25 | see Table 8-25 | MHz |

**Table 8-24. ARM Cortex-A8 Embedded PLL (PLL_ARM) Frequency Ranges (ALL OPPs)**

| CLOCK | MIN | MAX | UNIT |
|---|---|---|---|
| REFCLK | 0.032 | 52 | MHz |
| DCOCLK | 20 | 2000 | MHz |
| CLKOUT | see Table 8-25 | see Table 8-25 | MHz |

**Table 8-25. PLL CLKOUT Frequency Ranges**

| PLL | OPP100 | | UNIT |
|---|---|---|---|
| | MIN | MAX | |
| PLL_ARM | 10 | 600 | MHz |
| PLL_DSP | 10 | 500 | MHz |
| PLL_HDVICP | 10 | 266 | MHz |
| PLL_L3 | 10 | 200 | MHz |
| PLL_DDR | 10 | 400 | MHz |
| PLL_HDVPSS | 10 | 200 | MHz |
| PLL_AUDIO | 10 | 200 | MHz |
| PLL_MEDIACTL | 10 | 400 | MHz |
| PLL_USB | 10(1) | 960 | MHz |
| PLL_VIDEO0 | 10 | 200 | MHz |
| PLL_VIDEO1 | 10 | 200 | MHz |
| PLL_VIDEO2 | 10 | 200 | MHz |

(1) When the USB is used, PLL_USB **must** be fixed at 960 MHz.

### 8.4.8.4 PLL Register Descriptions

The PLL Control Registers reside in the Control Module and are listed in Section 5.1, *Control Module* of this datasheet.


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### 8.4.9 SYSCLKs

In some cases, the system clock inputs and PLL outputs are sent to the PRCM Module for division and multiplexing before being routed to the various device Modules. These clock outputs from the PRCM Module are called SYSCLKs. Table Table 8-26 lists the device SYSCLKs along with their maximum supported clock frequencies. In addition, limits shown in these tables may be further restricted by the clock frequency limitations of the device modules using these clocks. For more details on Module Clock frequency limits, see Section 8.4.10 *Module Clocks*.

**Table 8-26. Maximum SYSCLK Clock Frequencies(1)**

| SYSCLK | MAX CLOCK FREQUENCY OPP100 (MHz) |
|---|---|
| SYSCLK1 | RSV |
| SYSCLK2 | RSV |
| SYSCLK3 | 266 |
| SYSCLK4 | 200 |
| SYSCLK5 | RSV |
| SYSCLK6 | 100 |
| SYSCLK7 | RSV |
| SYSCLK8 | 192 |
| SYSCLK9 | RSV |
| SYSCLK10 | 48 |
| SYSCLK11 | RSV |
| SYSCLK12 | RSV |
| SYSCLK13 | RSV |
| SYSCLK14 | 27 |
| SYSCLK15 | RSV |
| SYSCLK16 | 27 |
| SYSCLK17 | RSV |
| SYSCLK18 | 0.032768 |
| SYSCLK19 | 192 |
| SYSCLK20 | 192 |
| SYSCLK21 | 192 |
| SYSCLK22 | RSV |
| SYSCLK23 | 200 |

(1) The maximum frequencies listed in this table are valid for OPP100. Some of these frequencies have higher maximum values when OPP120 or OPP166 is used, see Table 8-4

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### 8.4.10 Module Clocks

Device Modules either receive their clock directly from an external clock input, directly from a PLL, or from a PRCM SYSCLK output. Table 8-27 lists the clock source options for each Module on this device, along with the maximum frequency that Module can accept. To ensure proper Module functionality, the device PLLs and dividers **must** be programmed not to exceed the maximum frequencies listed in this table.

**Table 8-27. Maximum Module Clock Frequencies(1)**

| MODULE | CLOCK SOURCES | MAX FREQUENCY OPP100 (MHz) |
|---|---|---|
| Cortex-A8 | PLL_ARM<br>SYSCLK18 | 600 |
| CSI2 | PLL_USB / 10 | Fixed 96 |
| DCAN0/1 | DEV Clock | 30 |
| DDR0 | PLL_DDR | 400 |
| DMM | PLL_DDR/2 | 200 |
| DSP | PLL_DSP | 500 |
| System MMU | SYSCLK4 | 200 |
| EDMA | SYSCLK4 | 200 |
| EMAC Switch (GMII) | SATA SERDES | Fixed 125 |
| EMAC Switch (RGMII) | PLL_VIDEO0<br>PLL_VIDEO1<br>PLL_VIDEO02<br>PLL_L3 | Fixed 250 |
| EMAC Switch (RMII and MII) | SATA SERDES<br>EMAC_RMREFCLK Pin | Fixed 50 |
| Face Detect | SYSCLK4 | 200 |
| GPIO | SYSCLK6 | 100 |
| GPIO Debounce | SYSCLK18 | Fixed 0.032768 |
| GPMC | SYSCLK6 | 100 |
| HDMI | PLL_VIDEO2 | 186 |
| HDMI CEC | SYSCLK10 | Fixed 48 |
| HDMI I2S | SYSCLK20<br>SYSCLK21<br>AUD_CLK0/1/2<br>AUX Clock | 50 |
| HDVICP2 | SYSCLK3 | 266 |
| HDVPSS | PLL_HDVPSS | 200 |
| HDVPSS VOUT1 | PLL_VIDEO2<br>HDMI PHY | 186 |
| HDVPSS VOUT0 | PLL_VIDEO1<br>PLL_VIDEO2 | 165 |
| HDVPSS SD VENC | PLL_VIDEO0 | Fixed 54 |
| I2C0/1/2 | SYSCLK10 | 48 |
| ISS | PLL_ MEDIACTL | 400 |
| L3 Fast | SYSCLK4 | 200 |
| L3 Medium | SYSCLK4 | 200 |
| L3 Slow | SYSCLK6 | 100 |
| L4 Fast | SYSCLK4 | 200 |
| L4 Slow | SYSCLK6 | 100 |
| Mailbox | SYSCLK6 | 100 |
| McASP | SYSCLK6 | 100 |

(1) The maximum frequencies listed in this table are valid for OPP100. Some of these frequencies have higher maximum values when OPP120 or OPP166 is used, see Table 8-4


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**Table 8-27. Maximum Module Clock Frequencies[(1)] (continued)**

| MODULE | CLOCK SOURCES | MAX FREQUENCY OPP100 (MHz) |
|---|---|---|
| McASP0/1 AUX_CLK | SYSCLK20<br>SYSCLK21 | 192 |
| McASP3/4/5 AUX_CLK | PLL_AUDIO<br>PLL_VIDEO0/1/2<br>AUD_CLK0/1/2<br>AUX Clock | 192 |
| Media Controller | PLL_MEDIACTL/2 | 200 |
| OCMC RAM | SYSCLK4 | 200 |
| PCIe SERDES | SERDES_CLKx Pins | 100 |
| SATA SERDES | DEV Clock<br>SERDES_CLKx Pins | 20 or 100 |
| SPI0/1 | SYSCLK10 | 48 |
| Spinlock | SYSCLK6 | 100 |
| Sync Timer | SYSCLK18 | Fixed 0.032768 |
| TIMER1/2/3/4/5/6/7/8 | SYSCLK18<br>DEV Clock<br>AUX Clock<br>AUD_CLK0/1/2<br>TCLKIN | 30 |
| UART0/1/2 | SYSCLK10 | 48 |
| UART3 | SYSCLK6<br>SYSCLK8<br>SYSCLK10 | 192 |
| USB | PLL_USB CLKDCO | Fixed 960 |
| WDT0 | RTCDIVIDER<br>RCOSC32K | Fixed 0.032768 |

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## 8.5 Interrupts

The device has a large number of interrupts to service the needs of its many peripherals and subsystems. The ARM Cortex-A8 and Media Controller are capable of servicing these interrupts. The following sections list the device interrupt mapping and multiplexing schemes.

### *8.5.1 ARM Cortex-A8 Interrupts*

The ARM Cortex-A8 Interrupt Controller (AINTC) is responsible for prioritizing all service requests from the System peripherals and generating either IRQs or FIQs to the Cortex-A8. The AINTC has the capability to handle up to 128 requests, and the priority of the interrupt inputs are programmable. Table 8-28 lists the interrupt sources for the AINTC.

Note: For General-Purpose devices, the AINTC does not support the generation of FIQs to the ARM processor.

For more details on ARM Cortex-A8 interrupt control, see the ARM Interrupt Controller (AINTC) chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

**Table 8-28. ARM Cortex-A8 Interrupt Controller (AINTC) Interrupt Sources**

| Cortex-A8 INTERRUPT NUMBER | ACRONYM | SOURCE |
|---|---|---|
| 0 | EMUINT | Cortex-A8 Emulation |
| 1 | COMMTX | Cortex-A8 Emulation |
| 2 | COMMRX | Cortex-A8 Emulation |
| 3 | BENCH | Cortex-A8 Emulation |
| 4 | ELM_IRQ | ELM |
| 5 | | |
| 6 | | |
| 7 | NMI | NMIn Pin |
| 8 | | |
| 9 | L3DEBUG | L3 Interconnect |
| 10 | L3APPINT | L3 Interconnect |
| 11 | TINT8 | TIMER8 |
| 12 | EDMACOMPINT | EDMA CC Completion |
| 13 | EDMAMPERR | EDMA Memory Protection Error |
| 14 | EDMAERRINT | EDMA CC Error |
| 15 | WDTINT0 | Watchdog Timer 0 |
| 16 | – | Reserved |
| 17 | USBSSINT | USB Subsystem |
| 18 | USBINT0 | USB0 |
| 19 | USBINT1 | USB1 |
| 20-27 | – | Reserved |
| 28 | SDINT1 | MMC/SD1 |
| 29 | SDINT2 | MMC/SD2 |
| 30 | I2CINT2 | I2C2 |
| 31 | I2CINT3 | I2C3 |
| 32 | GPIOINT2A | GPIO2 A |
| 33 | GPIOINT2B | GPIO2 B |
| 34 | USBWAKEUP | USB Subsystem Wakeup |
| 35 | PCIeWAKEUP | PCIe Wakeup |
| 36 | DSSINT | HDVPSS |


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**Table 8-28. ARM Cortex-A8 Interrupt Controller (AINTC) Interrupt Sources (continued)**

| Cortex-A8 INTERRUPT NUMBER | ACRONYM | SOURCE |
|---|---|---|
| 38 | HDMIINT | HDMI |
| 39 | ISS_IRQ_5 | ISS |
| 40 | 3PGSWRXTHR0 | EMAC Switch RX Threshold |
| 41 | 3PGSWRXINT0 | EMAC Switch Receive |
| 42 | 3PGSWTXINT0 | EMAC Switch Transmit |
| 43 | 3PGSWMISC0 | EMAC Switch Miscellaneous |
| 44 | UARTINT3 | UART3 |
| 45 | UARTINT4 | UART4 |
| 46 | UARTINT5 | UART5 |
| 47 | FDIF_IRQ3 | Face Detect |
| 48 | PCIINT0 | PCIe |
| 49 | PCIINT1 | PCIe |
| 50 | PCIINT2 | PCIe |
| 51 | PCIINT3 | PCIe |
| 52 | DCAN0_INT0 | DCAN0 |
| 53 | DCAN0_INT1 | DCAN0 |
| 54 | DCAN0_PARITY | DCAN0 Parity |
| 55 | DCAN1_INT0 | DCAN1 |
| 56 | DCAN1_INT1 | DCAN1 |
| 57 | DCAN1_PARITY | DCAN1 Parity |
| 58-61 | – | Reserved |
| 62 | GPIOINT3A | GPIO3 |
| 63 | GPIOINT3B | GPIO3 |
| 64 | SDINT0 | MMC/SD0 |
| 65 | SPIINT0 | SPI0 |
| 66 | - | Reserved |
| 67 | TINT1 | TIMER1 |
| 68 | TINT2 | TIMER2 |
| 69 | TINT3 | TIMER3 |
| 70 | I2CINT0 | I2C0 |
| 71 | I2CINT1 | I2C1 |
| 72 | UARTINT0 | UART0 |
| 73 | UARTINT1 | UART1 |
| 74 | UARTINT2 | UART2 |
| 75 | RTCINT | RTC |
| 76 | RTCALARMINT | RTC Alarm |
| 77 | MBINT | Mailbox |
| 78 | – | Reserved |
| 79 | PLLINT | PLL Recalculation Interrupt |
| 80 | MCATXINT0 | McASP0 Transmit |
| 81 | MCARXINT0 | McASP0 Receive |
| 82 | MCATXINT1 | McASP1 Transmit |
| 83 | MCARXINT1 | McASP1 Receive |
| 84 | MCATXINT2 | McASP2 Transmit |
| 85 | MCARXINT2 | McASP2 Receive |
| 86 | MCBSPINT | McBSP |
| 87 | – | Reserved |

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**Table 8-28. ARM Cortex-A8 Interrupt Controller (AINTC) Interrupt Sources (continued)**

| Cortex-A8 INTERRUPT NUMBER | ACRONYM | SOURCE |
|---|---|---|
| 88 | – | Reserved |
| 91 | – | Reserved |
| 92 | TINT4 | TIMER4 |
| 93 | TINT5 | TIMER5 |
| 94 | TINT6 | TIMER6 |
| 95 | TINT7 | TIMER7 |
| 96 | GPIOINT0A | GPIO0 |
| 97 | GPIOINT0B | GPIO0 |
| 98 | GPIOINT1A | GPIO1 |
| 99 | GPIOINT1B | GPIO1 |
| 100 | GPMCINT | GPMC |
| 101 | DDRERR0 | DDR0 |
| 102 | DDRERR1 | DDR1 |
| 103 | HDVICPCONT1SYNC | HDVICP2 |
| 104 | HDVICPCONT2SYNC | HDVICP2 |
| 105 | MCATXINT3 | McASP3 Transmit |
| 106 | MCARXINT3 | McASP3 Receive |
| 107 | IVA0MBOXINT | HDVICP2 Mailbox |
| 108 | MCATXINT4 | McASP4 Transmit |
| 109 | MCARXINT4 | McASP4 Receive |
| 110 | MCATXINT5 | McASP5 Transmit |
| 111 | MCARXINT5 | McASP5 Receive |
| 112 | TCERRINT0 | EDMA TC 0 Error |
| 113 | TCERRINT1 | EDMA TC 1 Error |
| 114 | TCERRINT2 | EDMA TC 2 Error |
| 115 | TCERRINT3 | EDMA TC 3 Error |
| 116-119 | – | Reserved |
| 122 | MMUINT | System MMU |
| 123 | MCMMUINT | Media Controller |
| 124 | DMMINT | DMM |
| 125 | SPIINT1 | SPI1 |
| 126 | SPIINT2 | SPI2 |
| 127 | SPIINT3 | SPI3 |


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### 8.5.2 C674x DSP Interrupts

The C674x DSP interrupt controller combines up to 128 device events into 12 prioritized interrupts presented to the CPU. The default sources of the 128 device events are shown in Table 8-29. In addition, device events 15 through 95 can alternatively be sourced from one of the 24 Multiplexed device events shown in Table 8-30. The DSP_INTMUX_x registers in the Control Module are used to select between the default event and the multiplexed event. The interrupt controller also controls the generation of the CPU exceptions, NMI, and emulation interrupts.

**Table 8-29. Default C674x Event Sources**

| C674x DEFAULT EVENT NUMBER | ACRONYM | SOURCE |
|---|---|---|
| 0 | EVT0 | C674x Interrupt Controller 0 |
| 1 | EVT1 | C674x Interrupt Controller 1 |
| 2 | EVT2 | C674x Interrupt Controller 2 |
| 3 | EVT3 | C674x Interrupt Controller 3 |
| 4 | - | Reserved |
| 5 | - | Reserved |
| 6 | - | Reserved |
| 7 | - | Reserved |
| 8 | - | Reserved |
| 9 | EMU_DTDMA | C674x-ECM |
| 10 | | |
| 11 | EMU_RTDXRX | C674x-RTDX |
| 12 | EMU_RTDXTX | C674x-RTDX |
| 13 | IDMAINT0 | C674x-ECM |
| 14 | C674x | C674x-ECM |
| 15 | SDINT0 | MMC/SD0 |
| 16 | SPIINT0 | SPI0 |
| 17 | – | Reserved |
| 18 | ELM_IRQ | ELM |
| 19 | – | Reserved |
| 20 | EDMAINT | EDMA CC |
| 21 | EDMAERRINT | EDMA CC Error |
| 22 | TCERRINT0 | EDMA TC0 Error |
| 23 | ISS_IRQ4 | ISS |
| 24 | – | Reserved |
| 25 | – | Reserved |
| 26 | – | Reserved |
| 27 | TCERRINT1 | EDMA TC1 Error |
| 28 | TCERRINT2 | EDMA TC2 Error |
| 29 | TCERRINT3 | EDMA TC3 Error |
| 30 | SDINT1 | MMC/SD1 |
| 31 | SDINT2 | MMC/SD2 |
| 32 | 3PGSWRXTHR0 | EMAC Switch RX Threshold |
| 33 | 3PGSWRXINT0 | EMAC Switch RX |
| 34 | 3PGSWTXINT0 | EMAC Switch TX |
| 35 | 3PGSWMISC0 | EMAC Switch Miscellaneous |
| 36 | PCIINT0 | PCIe |
| 37 | PCIINT1 | PCIe |
| 38 | PCIINT2 | PCIe |

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**Table 8-29. Default C674x Event Sources (continued)**

| C674x DEFAULT EVENT NUMBER | ACRONYM | SOURCE |
|---|---|---|
| 39 | PCIINT3 | PCIe |
| 40 | DSSINT | DSS |
| 41 | HDMIINT | HDMI |
| 42 | – | Reserved |
| 46 | FDIF_IRQ3 | Face Detect |
| 47-48 | - | Reserved |
| 49 | TINT1 | TIMER1 |
| 50 | TINT2 | TIMER2 |
| 51 | TINT3 | TIMER3 |
| 52 | TINT4 | TIMER4 |
| 53 | TINT5 | TIMER5 |
| 54 | TINT6 | TIMER6 |
| 55 | TINT7 | TIMER7 |
| 56 | MBINT | Mailbox |
| 57 | GPIOINT3A | GPIO3 |
| 58 | I2CINT0 | I2C0 |
| 59 | I2CINT1 | I2C1 |
| 60 | UARTINT0 | UART0 |
| 61 | UARTINT1 | UART1 |
| 62 | UARTINT2 | UART2 |
| 63 | GPIOINT3B | GPIO3 |
| 64 | GPIOINT0A | GPIO0 |
| 65 | GPIOINT0B | GPIO0 |
| 66 | GPIOINT1A | GPIO1 |
| 67 | GPIOINT1B | GPIO1 |
| 68 | GPIOINT2A | GPIO2 |
| 69 | GPIOINT2B | GPIO2 |
| 70 | MCATXINT0 | McASP0 Transmit |
| 71 | MCARXINT0 | McASP0 Receive |
| 72 | MCATXINT1 | McASP1 Transmit |
| 73 | MCARXINT1 | McASP1 Receive |
| 74 | MCATXINT2 | McASP2 Transmit |
| 75 | MCARXINT2 | McASP2 Receive |
| 76 | MCBSPINT | McBSP |
| 77 | UARTINT3 | UART3 |
| 78 | UARTINT4 | UART4 |
| 79 | UARTINT5 | UART5 |
| 80 | MCATXINT3 | McASP3 Transmit |
| 81 | MCARXINT3 | McASP3 Receive |
| 82 | MCATXINT4 | McASP4 Transmit |
| 83 | MCARXINT4 | McASP4 Receive |
| 84 | MCATXINT5 | McASP5 Transmit |
| 85 | MCARXINT5 | McASP5 Receive |
| 86 | SPIINT1 | SPI1 |
| 87 | SPIINT2 | SPI2 |
| 88 | SPIINT3 | SPI3 |
| 89 | I2CINT2 | I2C2 |


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**Table 8-29. Default C674x Event Sources (continued)**

| C674x DEFAULT EVENT NUMBER | ACRONYM | SOURCE |
|---|---|---|
| 90 | HDVICPCONT1SYNC | HDVICP2 |
| 91 | HDVICPCONT2SYNC | HDVICP2 |
| 92 | I2CINT3 | I2C3 |
| 93 | MMUINT | System MMU |
| 94 | HDVICPMBOXINT | HDVICP2 Mailbox |
| 95 | GPMCINT | GPMC |
| 96 | INTERR | C674x-Int Ctl |
| 97 | EMC_IDMAERR | C674x-EMC |
| 98 | - | Reserved |
| 99 | - | Reserved |
| 100 | EFIINTA | C674x-EFIA |
| 101 | EFIINTB | C674x-EFIB |
| 102 | - | Reserved |
| 103 | - | Reserved |
| 104 | - | Reserved |
| 105 | - | Reserved |
| 106 | - | Reserved |
| 107 | - | Reserved |
| 108 | - | Reserved |
| 109 | - | Reserved |
| 110 | - | Reserved |
| 111 | - | Reserved |
| 112 | - | Reserved |
| 113 | PMC_ED | C674x-PMC |
| 114 | - | Reserved |
| 115 | - | Reserved |
| 116 | UMC_ED1 | C674x-UMC |
| 117 | UMC_ED2 | C674x-UMC |
| 118 | PDC_INT | C674x-PDC |
| 119 | SYS_CMPA | C674x-SYS |
| 120 | PMC_CMPA | C674x-PMC |
| 121 | PMC_DMPA | C674x-PMC |
| 122 | DMC_CMPA | C674x-DMC |
| 123 | DMC_DMPA | C674x-DMC |
| 124 | UMC_CMPA | C674x-UMC |
| 125 | UMC_DMPA | C674x-UMC |
| 126 | EMC_CMPA | C674x-EMC |
| 127 | EMC_BUSERR | C674x-EMC |

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**Table 8-30. Multiplexed C674x Event Sources**

| C674x MULTIPLEXED EVENT NUMBER | ACRONYM | SOURCE |
|---|---|---|
| 0 | - | Default Event |
| 1 | DCAN0_INT0 | DCAN0 |
| 2 | DCAN0_INT1 | DCAN0 |
| 3 | DCAN1_PARITY | DCAN0 Parity |
| 4 | DCAN1_INT0 | DCAN1 |
| 5 | DCAN1_INT1 | DCAN1 |
| 6 | DCAN1_PARITY | DCAN1 Parity |
| 7 | – | Reserved |
| 8 | – | Reserved |
| 9 | – | Reserved |
| 10 | - | Reserved |
| 11 | L3DEBUG | L3 Interconnect |
| 12 | L3APPINT | L3 Interconnect |
| 13 | EDMAMPERR | EDMA Memory Protection Error |
| 14 | TINT8 | TIMER8 |
| 15 | WDTINT0 | Watchdog Timer 0 |
| 16 | USBSSINT | USB Subsystem |
| 17 | USBINT0 | USB0 |
| 18 | USBINT1 | USB1 |
| 19 | RTCINT | RTC |
| 20 | RTCALARMINT | RTC Alarm |
| 21 | - | Reserved |
| 22 | - | Reserved |
| 23 | DDRERR0 | DDR0 |


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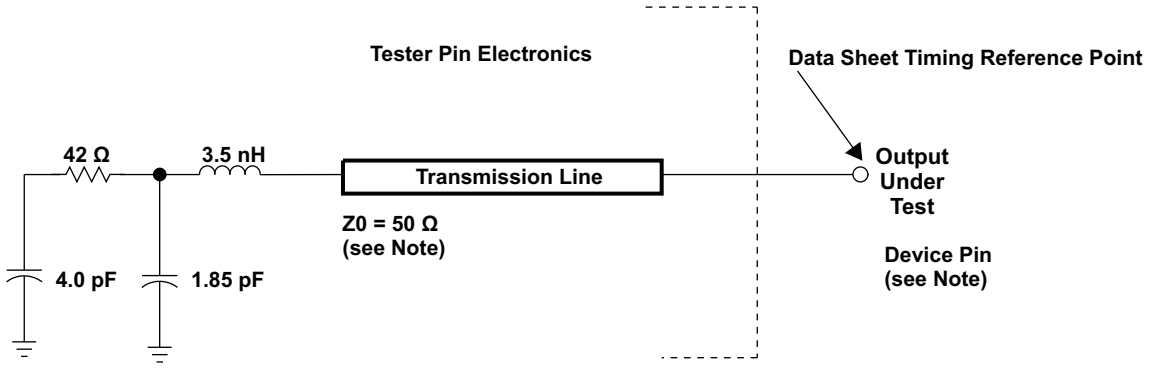
# 9 Peripheral Information and Timings

## 9.1 Parameter Information




NOTE: The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns) from the data sheet timings.

Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.

**Figure 9-1. Test Load Circuit for AC Timing Measurements**

The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

### *9.1.1 3.3-V Signal Transition Levels*

All input and output timing parameters are referenced to $V_{ref}$ for both "0" and "1" logic levels. For 3.3-V I/O, $V_{ref}$ = 1.5 V.

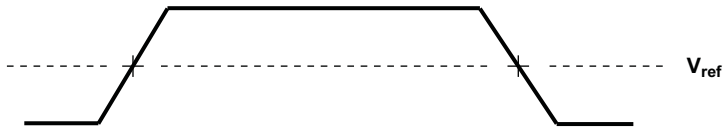



**Figure 9-2. Input and Output Voltage Reference Levels for AC Timing Measurements**

All rise and fall transition timing parameters are referenced to $V_{IL}$ MAX and $V_{IH}$ MIN for input clocks, $V_{OL}$ MAX and $V_{OH}$ MIN for output clocks.

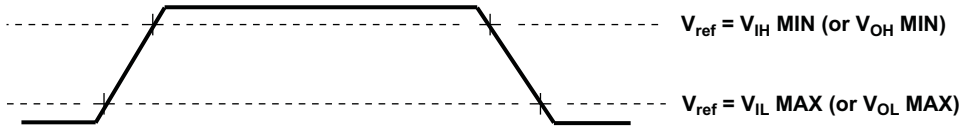



**Figure 9-3. Rise and Fall Transition Time Voltage Reference Levels**

### *9.1.2 3.3-V Signal Transition Rates*

All timings are tested with an input edge rate of 4 volts per nanosecond (4 V/ns).

### 9.1.3 Timing Parameters and Board Routing Analysis

The timing parameter values specified in this data manual do *not* include delays by board routings. As a good board design practice, such delays must *always* be taken into account. Timing values may be adjusted by increasing/decreasing such delays. TI recommends utilizing the available I/O buffer information specification (IBIS) models to analyze the timing characteristics correctly. To properly use IBIS models to attain accurate timing analysis for a given system, see the *Using IBIS Models for Timing Analysis* application report (Literature Number: SPRA839). If needed, external logic hardware such as buffers may be used to compensate any timing differences.

For the DDR2 memory controller interface, it is *not* necessary to use the IBIS models to analyze timing characteristics. TI provides a PCB routing rules solution that describes the routing rules to ensure the DDR2 memory controller interface timings are met.

## 9.2 Recommended Clock and Control Signal Transition Behavior

All clocks and control signals ***must*** transition between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$) in a monotonic manner.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## 9.3 Controller Area Network Interface (DCAN)

The device provides two DCAN interfaces for supporting distributed realtime control with a high level of security. The DCAN interfaces implement the following features:

- Supports CAN protocol version 2.0 part A, B
- Bit rates up to 1 MBit/s
- 64 message objects
- Individual identifier mask for each message object
- Programmable FIFO mode for message objects
- Programmable loop-back modes for self-test operation
- Suspend mode for debug support
- Software module reset
- Automatic bus on after Bus-Off state by a programmable 32-bit timer
- Message RAM parity check mechanism
- Direct access to Message RAM during test mode
- CAN Rx/Tx pins are configurable as general-purpose IO pins
- Two interrupt lines (plus additional parity-error interrupts line)
- RAM initialization
- DMA support

For more detailed information on the DCAN peripheral, see the *DCAN Controller Area Network* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

### 9.3.1 DCAN Peripheral Register Descriptions

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### 9.3.2 DCAN Electrical Data/Timing

**Table 9-1. Timing Requirements for DCANx Receive(1) (see Figure 9-4)**

| NO. | | | OPP100/120/166 | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | |
| | f(baud) | Maximum programmable baud rate | | | 1 | Mbps |
| 1 | $t_{w(DCANRX)}$ | Pulse duration, receive data bit (DCANx_RX) | H - 2 | | H + 2 | ns |

(1) H = period of baud rate, 1/programmed baud rate.

**Table 9-2. Switching Characteristics Over Recommended Operating Conditions for DCANx Transmit (1)(see Figure 9-4)**

| NO. | PARAMETER | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| | f(baud) | Maximum programmable baud rate | | 1 | Mbps |
| 2 | $t_{w(DCANTX)}$ | Pulse duration, transmit data bit (DCANx_TX) | H - 2 | H + 2 | ns |

(1) H = period of baud rate, 1/programmed baud rate.

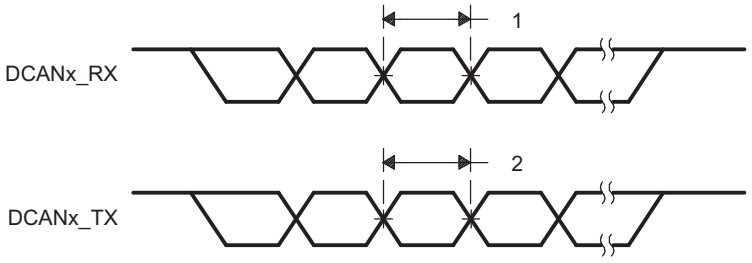


**Figure 9-4. DCANx Timings**


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## 9.4 EDMA

The EDMA controller handles all data transfers between memories and the device slave peripherals on the device. These data transfers include cache servicing, non-cacheable memory accesses, user-programmed data transfers, and host accesses.

### *9.4.1 EDMA Channel Synchronization Events*

The EDMA Channel controller supports up to 64 channels that service peripherals and memory. Each EDMA channel is mapped to a defaul EDMA synchronization event as shown in Table 9-3. By default, each event uses the parameter entry that matches its event number. However, because the device includes a channel mapping feature, each event may be mapped to any of 512 parameter table entries. For more detailed information, see the *Enhanced Direct Memory Access Controller* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

**Table 9-3. EDMA Default Synchronization Events**

| EVENT NUMBER | DEFAULT EVENT NAME | DEFAULT EVENT DESCRIPTION |
|---|---|---|
| 2 | SDTXEVT1 | SD1 Transmit |
| 3 | SDRXEVT1 | SD1 Receive |
| 8 | AXEVT0 | McASP0 Transmit |
| 9 | AREVT0 | McASP0 Receive |
| 10 | AXEVT1 | McASP1 Transmit |
| 11 | AREVT1 | McASP1 Receive |
| 12 | AXEVT2 | McASP2 Transmit |
| 13 | AREVT2 | McASP2 Receive |
| 14 | BXEVT | McBSP Transmit |
| 15 | BREVT | McBSP Receive |
| 16 | SPI0XEVT0 | SPI0 Transmit 0 |
| 17 | SPI0REVT0 | SPI0 Receive 0 |
| 18 | SPI0XEVT1 | SPI0 Transmit 1 |
| 19 | SPI0REVT1 | SPI0 Receive 1 |
| 20 | SPI0XEVT2 | SPI0 Transmit 2 |
| 21 | SPI0REVT2 | SPI0 Receive 2 |
| 22 | SPI0XEVT3 | SPI0 Transmit 3 |
| 23 | SPI0REVT3 | SPI0 Receive 3 |
| 24 | SDTXEVT0 | SD0 Transmit |
| 25 | SDRXEVT0 | SD0 Receive |
| 26 | UTXEVT0 | UART0 Transmit |
| 27 | URXEVT0 | UART0 Receive |
| 28 | UTXEVT1 | UART1 Transmit |
| 29 | URXEVT1 | UART1 Receive |
| 30 | UTXEVT2 | UART2 Transmit |
| 31 | URXEVT2 | UART2 Receive |
| 36 | ISS_DMA_REQ1 | ISS Event 1 |
| 37 | ISS_DMA_REQ2 | ISS Event 2 |
| 38 | ISS_DMA_REQ3 | ISS Event 3 |
| 39 | ISS_DMA_REQ4 | ISS Event 4 |
| 40 | CAN_IF1DMA | DCAN0 IF1 |
| 41 | CAN_IF2DMA | DCAN0 IF2 |
| 42 | SPI1XEVT0 | SPI1 Transmit 0 |

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**Table 9-3. EDMA Default Synchronization Events (continued)**

| EVENT NUMBER | DEFAULT EVENT NAME | DEFAULT EVENT DESCRIPTION |
|---|---|---|
| 43 | SPI1REVT0 | SPI1 Receive 0 |
| 44 | SPI1XEVT1 | SPI1 Transmit 1 |
| 45 | SPI1REVT1 | SPI1 Receive 1 |
| 47 | CAN_IF3DMA | DCAN0 IF3 |
| 48 | TINT4 | TIMER4 |
| 49 | TINT5 | TIMER5 |
| 50 | TINT6 | TIMER6 |
| 51 | TINT7 | TIMER7 |
| 52 | GPMCEVT | GPMC |
| 53 | HDMIEVT | HDMI |
| 54 | – | Reserved |
| 55 | – | Reserved |
| 56 | AXEVT3 | McASP3 Transmit |
| 57 | AREVT3 | McASP3 Receive |
| 58 | I2CTXEVT0 | I2C0 Transmit |
| 59 | I2CRXEVT0 | I2C0 Receive |
| 60 | I2CTXEVT1 | I2C1 Transmit |
| 61 | I2CRXEVT1 | I2C1 Receive |
| 62 | AXEVT4 | McASP4 Transmit |
| 63 | AREVT4 | McASP4 Receive |

**Table 9-4. EDMA Multiplexed Synchronization Events**

| EVT_MUX_x VALUE | MULTIPLEXED EVENT NAME | MULTIPLEXED EVENT DESCRIPTION |
|---|---|---|
| 0 | - | Default Event |
| 1 | SDTXEVT2 | SD2 Transmit |
| 2 | SDRXEVT2 | SD2 Receive |
| 3 | I2CTXEVT2 | I2C2 Transmit |
| 4 | I2CRXEVT2 | I2C2 Receive |
| 5 | I2CTXEVT3 | I2C3 Transmit |
| 6 | I2CRXEVT3 | I2C3 Receive |
| 7 | UTXEVT3 | UART3 Transmit |
| 8 | URXEVT3 | UART3 Receive |
| 9 | UTXEVT4 | UART4 Transmit |
| 10 | URXEVT4 | UART4 Receive |
| 11 | UTXEVT5 | UART5 Transmit |
| 12 | URXEVT5 | UART5 Receive |
| 13 | CAN_IF1DMA | DCAN1 IF1 |
| 14 | CAN_IF2DMA | DCAN1 IF2 |
| 15 | CAN_IF3DMA | DCAN1 IF3 |
| 16 | SPI2XEVT0 | SPI2 Transmit 0 |
| 17 | SPI2REVT0 | SPI2 Receive 0 |
| 18 | SPI2XEVT1 | SPI2 Transmit 1 |
| 19 | SPI2REVT1 | SPI2 Receive 1 |
| 20 | SPI3XEVT0 | SPI3 Transmit 0 |
| 21 | SPI3REVT0 | SPI3 Receive 0 |
| 22 | | |


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**Table 9-4. EDMA Multiplexed Synchronization Events (continued)**

| EVT_MUX_x VALUE | MULTIPLEXED EVENT NAME | MULTIPLEXED EVENT DESCRIPTION |
|---|---|---|
| 23 | TINT1 | TIMER1 |
| 24 | TINT2 | TIMER2 |
| 25 | TINT3 | TIMER3 |
| 26 | AXEVT5 | McASP5 Transmit |
| 27 | AREVT5 | McASP5 Receive |
| 28 | EDMAEVT0 | EDMA_EVT0 Pin |
| 29 | EDMAEVT1 | EDMA_EVT1 Pin |
| 30 | EDMAEVT2 | EDMA_EVT2 Pin |
| 31 | EDMAEVT3 | EDMA_EVT3 Pin |

### *9.4.2 EDMA Peripheral Register Descriptions*

**Table 9-5. EDMA Channel Controller (EDMA TPCC) Control Registers**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4900 0000 | PID | Peripheral Identification |
| 0x4900 0004 | CCCFG | EDMA3CC Configuration |
| 0x4900 0100 - 0x4900 01FC | DCHMAP0-63 | DMA Channel 0-63 Mappings |
| 0x4900 0200 | QCHMAP0 | QDMA Channel 0 Mapping |
| 0x4900 0204 | QCHMAP1 | QDMA Channel 1 Mapping |
| 0x4900 0208 | QCHMAP2 | QDMA Channel 2 Mapping |
| 0x4900 020C | QCHMAP3 | QDMA Channel 3 Mapping |
| 0x4900 0210 | QCHMAP4 | QDMA Channel 4 Mapping |
| 0x4900 0214 | QCHMAP5 | QDMA Channel 5 Mapping |
| 0x4900 0218 | QCHMAP6 | QDMA Channel 6 Mapping |
| 0x4900 021C | QCHMAP7 | QDMA Channel 7 Mapping |
| 0x4900 0240 | DMAQNUM0 | DMA Queue Number 0 |
| 0x4900 0244 | DMAQNUM1 | DMA Queue Number 1 |
| 0x4900 0248 | DMAQNUM2 | DMA Queue Number 2 |
| 0x4900 024C | DMAQNUM3 | DMA Queue Number 3 |
| 0x4900 0250 | DMAQNUM4 | DMA Queue Number 4 |
| 0x4900 0254 | DMAQNUM5 | DMA Queue Number 5 |
| 0x4900 0258 | DMAQNUM6 | DMA Queue Number 6 |
| 0x4900 025C | DMAQNUM7 | DMA Queue Number 7 |
| 0x4900 0260 | QDMAQNUM | QDMA Queue Number |
| 0x4900 0284 | QUEPRI | Queue Priority |
| 0x4900 0300 | EMR | Event Missed |
| 0x4900 0304 | EMRH | Event Missed High |
| 0x4900 0308 | EMCR | Event Missed Clear |
| 0x4900 030C | EMCRH | Event Missed Clear High |
| 0x4900 0310 | QEMR | QDMA Event Missed |
| 0x4900 0314 | QEMCR | QDMA Event Missed Clear |
| 0x4900 0318 | CCERR | EDMA3CC Error |
| 0x4900 031C | CCERRCLR | EDMA3CC Error Clear |
| 0x4900 0320 | EEVAL | Error Evaluate |
| 0x4900 0340 | DRAE0 | DMA Region Access Enable for Region 0 |
| 0x4900 0344 | DRAEH0 | DMA Region Access Enable High for Region 0 |
| 0x4900 0348 | DRAE1 | DMA Region Access Enable for Region 1 |

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**Table 9-5. EDMA Channel Controller (EDMA TPCC) Control Registers (continued)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4900 034C | DRAEH1 | DMA Region Access Enable High for Region 1 |
| 0x4900 0350 | DRAE2 | DMA Region Access Enable for Region 2 |
| 0x4900 0354 | DRAEH2 | DMA Region Access Enable High for Region 2 |
| 0x4900 0358 | DRAE3 | DMA Region Access Enable for Region 3 |
| 0x4900 035C | DRAEH3 | DMA Region Access Enable High for Region 3 |
| 0x4900 0360 | DRAE4 | DMA Region Access Enable for Region 4 |
| 0x4900 0364 | DRAEH4 | DMA Region Access Enable High for Region 4 |
| 0x4900 0368 | DRAE5 | DMA Region Access Enable for Region 5 |
| 0x4900 036C | DRAEH5 | DMA Region Access Enable High for Region 5 |
| 0x4900 0370 | DRAE6 | DMA Region Access Enable for Region 6 |
| 0x4900 0374 | DRAEH6 | DMA Region Access Enable High for Region 6 |
| 0x4900 0378 | DRAE7 | DMA Region Access Enable for Region 7 |
| 0x4900 037C | DRAEH7 | DMA Region Access Enable High for Region 7 |
| 0x4900 0380 - 0x4900 039C | QRAE0-7 | QDMA Region Access Enable for Region 0-7 |
| 0x4900 0400 - 0x4900 04FC | Q0E0-Q3E15 | Event Queue Entry Q0E0-Q3E15 |
| 0x4900 0600 - 0x4900 060C | QSTAT0-3 | Queue Status 0-3 |
| 0x4900 0620 | QWMTHRA | Queue Watermark Threshold A |
| 0x4900 0640 | CCSTAT | EDMA3CC Status |
| 0x4900 0800 | MPFAR | Memory Protection Fault Address |
| 0x4900 0804 | MPFSR | Memory Protection Fault Status |
| 0x4900 0808 | MPFCR | Memory Protection Fault Command |
| 0x4900 080C | MPPAG | Memory Protection Page Attribute Global |
| 0x4900 0810 - 0x4900 082C | MPPA0-7 | Memory Protection Page Attribute 0-7 |
| 0x4900 1000 | ER | Event |
| 0x4900 1004 | ERH | Event High |
| 0x4900 1008 | ECR | Event Clear |
| 0x4900 100C | ECRH | Event Clear High |
| 0x4900 1010 | ESR | Event Set |
| 0x4900 1014 | ESRH | Event Set High |
| 0x4900 1018 | CER | Chained Event |
| 0x4900 101C | CERH | Chained Event High |
| 0x4900 1020 | EER | Event Enable |
| 0x4900 1024 | EERH | Event Enable High |
| 0x4900 1028 | EECR | Event Enable Clear |
| 0x4900 102C | EECRH | Event Enable Clear High |
| 0x4900 1030 | EESR | Event Enable Set |
| 0x4900 1034 | EESRH | Event Enable Set High |
| 0x4900 1038 | SER | Secondary Event |
| 0x4900 103C | SERH | Secondary Event High |
| 0x4900 1040 | SECR | Secondary Event Clear |
| 0x4900 1044 | SECRH | Secondary Event Clear High |
| 0x4900 1050 | IER | Interrupt Enable |
| 0x4900 1054 | IERH | Interrupt Enable High |
| 0x4900 1058 | IECR | Interrupt Enable Clear |
| 0x4900 105C | IECRH | Interrupt Enable Clear High |
| 0x4900 1060 | IESR | Interrupt Enable Set |
| 0x4900 1064 | IESRH | Interrupt Enable Set High |


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**Table 9-5. EDMA Channel Controller (EDMA TPCC) Control Registers (continued)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4900 1068 | IPR | Interrupt Pending |
| 0x4900 106C | IPRH | Interrupt Pending High |
| 0x4900 1070 | ICR | Interrupt Clear |
| 0x4900 1074 | ICRH | Interrupt Clear High |
| 0x4900 1078 | IEVAL | Interrupt Evaluate |
| 0x4900 1080 | QER | QDMA Event |
| 0x4900 1084 | QEER | QDMA Event Enable |
| 0x4900 1088 | QEECR | QDMA Event Enable Clear |
| 0x4900 108C | QEESR | QDMA Event Enable Set |
| 0x4900 1090 | QSER | QDMA Secondary Event |
| 0x4900 1094 | QSECR | QDMA Secondary Event Clear |
| **Shadow Region 0 Channel Registers** | | |
| 0x4900 2000 | ER | Event |
| 0x4900 2004 | ERH | Event High |
| 0x4900 2008 | ECR | Event Clear |
| 0x4900 200C | ECRH | Event Clear High |
| 0x4900 2010 | ESR | Event Set |
| 0x4900 2014 | ESRH | Event Set High |
| 0x4900 2018 | CER | Chained Event |
| 0x4900 201C | CERH | Chained Event High |
| 0x4900 2020 | EER | Event Enable |
| 0x4900 2024 | EERH | Event Enable High |
| 0x4900 2028 | EECR | Event Enable Clear |
| 0x4900 202C | EECRH | Event Enable Clear High |
| 0x4900 2030 | EESR | Event Enable Set |
| 0x4900 2034 | EESRH | Event Enable Set High |
| 0x4900 2038 | SER | Secondary Event |
| 0x4900 203C | SERH | Secondary Event High |
| 0x4900 2040 | SECR | Secondary Event Clear |
| 0x4900 2044 | SECRH | Secondary Event Clear High |
| 0x4900 2050 | IER | Interrupt Enable |
| 0x4900 2054 | IERH | Interrupt Enable High |
| 0x4900 2058 | IECR | Interrupt Enable Clear |
| 0x4900 205C | IECRH | Interrupt Enable Clear High |
| 0x4900 2060 | IESR | Interrupt Enable Set |
| 0x4900 2064 | IESRH | Interrupt Enable Set High |
| 0x4900 2068 | IPR | Interrupt Pending |
| 0x4900 206C | IPRH | Interrupt Pending High |
| 0x4900 2070 | ICR | Interrupt Clear |
| 0x4900 2074 | ICRH | Interrupt Clear High |
| 0x4900 2078 | IEVAL | Interrupt Evaluate |
| 0x4900 2080 | QER | QDMA Event |
| 0x4900 2084 | QEER | QDMA Event Enable |
| 0x4900 2088 | QEECR | QDMA Event Enable Clear |
| 0x4900 208C | QEESR | QDMA Event Enable Set |
| 0x4900 2090 | QSER | QDMA Secondary Event |
| 0x4900 2094 | QSECR | QDMA Secondary Event Clear |

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**Table 9-5. EDMA Channel Controller (EDMA TPCC) Control Registers (continued)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4900 2200 - 0x4900 2294 | - | Shadow Region 1 Channels |
| 0x4900 2400 - 0x4900 2494 | - | Shadow Region 2 Channels |
| ... | | ... |
| 0x4900 2E00 - 0x4900 2E94 | - | Shadow Channels for MP Space 7 |

**Table 9-6. EDMA Transfer Controller (EDMA TPTC) Control Registers**

| TPTC0 HEX ADDRESS | TPTC1 HEX ADDRESS | TPTC2 HEX ADDRESS | TPTC3 HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|---|---|---|
| 0x4980 0000 | 0x4990 0000 | 0x49A0 0000 | 0x49B0 0000 | PID | Peripheral Identification |
| 0x4980 0004 | 0x4990 0004 | 0x49A0 0004 | 0x49B0 0004 | TCCFG | EDMA3TC Configuration |
| 0x4980 0100 | 0x4990 0100 | 0x49A0 0100 | 0x49B0 0100 | TCSTAT | EDMA3TC Channel Status |
| 0x4980 0120 | 0x4990 0120 | 0x49A0 0120 | 0x49B0 0120 | ERRSTAT | Error Status |
| 0x4980 0124 | 0x4990 0124 | 0x49A0 0124 | 0x49B0 0124 | ERREN | Error Enable |
| 0x4980 0128 | 0x4990 0128 | 0x49A0 0128 | 0x49B0 0128 | ERRCLR | Error Clear |
| 0x4980 012C | 0x4990 012C | 0x49A0 012C | 0x49B0 012C | ERRDET | Error Details |
| 0x4980 0130 | 0x4990 0130 | 0x49A0 0130 | 0x49B0 0130 | ERRCMD | Error Interrupt Command |
| 0x4980 0140 | 0x4990 0140 | 0x49A0 0140 | 0x49B0 0140 | RDRATE | Read Rate Register |
| 0x4980 0240 | 0x4990 0240 | 0x49A0 0240 | 0x49B0 0240 | SAOPT | Source Active Options |
| 0x4980 0244 | 0x4990 0244 | 0x49A0 0244 | 0x49B0 0244 | SASRC | Source Active Source Address |
| 0x4980 0248 | 0x4990 0248 | 0x49A0 0248 | 0x49B0 0248 | SACNT | Source Active Count |
| 0x4980 024C | 0x4990 024C | 0x49A0 024C | 0x49B0 024C | SADST | Source Active Destination Address |
| 0x4980 0250 | 0x4990 0250 | 0x49A0 0250 | 0x49B0 0250 | SABIDX | Source Active Source B-Index |
| 0x4980 0254 | 0x4990 0254 | 0x49A0 0254 | 0x49B0 0254 | SAMPPRXY | Source Active Memory Protection Proxy |
| 0x4980 0258 | 0x4990 0258 | 0x49A0 0258 | 0x49B0 0258 | SACNTRLD | Source Active Count Reload |
| 0x4980 025C | 0x4990 025C | 0x49A0 025C | 0x49B0 025C | SASRCBREF | Source Active Source Address B-Reference |
| 0x4980 0260 | 0x4990 0260 | 0x49A0 0260 | 0x49B0 0260 | SADSTBREF | Source Active Destination Address B-Reference |
| 0x4980 0280 | 0x4990 0280 | 0x49A0 0280 | 0x49B0 0280 | DFCNTRLD | Destination FIFO Set Count Reload |
| 0x4980 0284 | 0x4990 0284 | 0x49A0 0284 | 0x49B0 0284 | DFSRCBREF | Destination FIFO Set Destination Address B Reference |
| 0x4980 0288 | 0x4990 0288 | 0x49A0 0288 | 0x49B0 0288 | DFDSTBREF | Destination FIFO Set Destination Address B Reference |
| 0x4980 0300 | 0x4990 0300 | 0x49A0 0300 | 0x49B0 0300 | DFOPT0 | Destination FIFO Options 0 |
| 0x4980 0304 | 0x4990 0304 | 0x49A0 0304 | 0x49B0 0304 | DFSRC0 | Destination FIFO Source Address 0 |
| 0x4980 0308 | 0x4990 0308 | 0x49A0 0308 | 0x49B0 0308 | DFCNT0 | Destination FIFO Count 0 |
| 0x4980 030C | 0x4990 030C | 0x49A0 030C | 0x49B0 030C | DFDST0 | Destination FIFO Destination Address 0 |
| 0x4980 0310 | 0x4990 0310 | 0x49A0 0310 | 0x49B0 0310 | DFBIDX0 | Destination FIFO BIDX 0 |
| 0x4980 0314 | 0x4990 0314 | 0x49A0 0314 | 0x49B0 0314 | DFMPPRXY0 | Destination FIFO Memory Protection Proxy 0 |
| 0x4980 0340 | 0x4990 0340 | 0x49A0 0340 | 0x49B0 0340 | DFOPT1 | Destination FIFO Options 1 |
| 0x4980 0344 | 0x4990 0344 | 0x49A0 0344 | 0x49B0 0344 | DFSRC1 | Destination FIFO Source Address 1 |
| 0x4980 0348 | 0x4990 0348 | 0x49A0 0348 | 0x49B0 0348 | DFCNT1 | Destination FIFO Count 1 |


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**Table 9-6. EDMA Transfer Controller (EDMA TPTC) Control Registers (continued)**

| TPTC0 HEX ADDRESS | TPTC1 HEX ADDRESS | TPTC2 HEX ADDRESS | TPTC3 HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|---|---|---|
| 0x4980 034C | 0x4990 034C | 0x49A0 034C | 0x49B0 034C | DFDST1 | Destination FIFO Destination Address 1 |
| 0x4980 0350 | 0x4990 0350 | 0x49A0 0350 | 0x49B0 0350 | DFBIDX1 | Destination FIFO BIDX 1 |
| 0x4980 0354 | 0x4990 0354 | 0x49A0 0354 | 0x49B0 0354 | DFMPPRXY1 | Destination FIFO Memory Protection Proxy 1 |
| 0x4980 0380 | 0x4990 0380 | 0x49A0 0380 | 0x49B0 0380 | DFOPT2 | Destination FIFO Options 2 |
| 0x4980 0384 | 0x4990 0384 | 0x49A0 0384 | 0x49B0 0384 | DFSRC2 | Destination FIFO Source Address 2 |
| 0x4980 0388 | 0x4990 0388 | 0x49A0 0388 | 0x49B0 0388 | DFCNT2 | Destination FIFO Count 2 |
| 0x4980 038C | 0x4990 038C | 0x49A0 038C | 0x49B0 038C | DFDST2 | Destination FIFO Destination Address 2 |
| 0x4980 0390 | 0x4990 0390 | 0x49A0 0390 | 0x49B0 0390 | DFBIDX2 | Destination FIFO BIDX 2 |
| 0x4980 0394 | 0x4990 0394 | 0x49A0 0394 | 0x49B0 0394 | DFMPPRXY2 | Destination FIFO Memory Protection Proxy 2 |
| 0x4980 03C0 | 0x4990 03C0 | 0x49A0 03C0 | 0x49B0 03C0 | DFOPT3 | Destination FIFO Options 3 |
| 0x4980 03C4 | 0x4990 03C4 | 0x49A0 03C4 | 0x49B0 03C4 | DFSRC3 | Destination FIFO Source Address 3 |
| 0x4980 03C8 | 0x4990 03C8 | 0x49A0 03C8 | 0x49B0 03C8 | DFCNT3 | Destination FIFO Count 3 |
| 0x4980 03CC | 0x4990 03CC | 0x49A0 03CC | 0x49B0 03CC | DFDST3 | Destination FIFO Destination Address 3 |
| 0x4980 03D0 | 0x4990 03D0 | 0x49A0 03D0 | 0x49B0 03D0 | DFBIDX3 | Destination FIFO BIDX 3 |
| 0x4980 03D4 | 0x4990 03D4 | 0x49A0 03D4 | 0x49B0 03D4 | DFMPPRXY3 | Destination FIFO Memory Protection Proxy 3 |

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## 9.5 Emulation Features and Capability

### 9.5.1 Advanced Event Triggering (AET)

The device supports Advanced Event Triggering (AET). This capability can be used to debug complex problems as well as understand performance characteristics of user applications. AET provides the following capabilities:

- **Hardware Program Breakpoints:** specify addresses or address ranges that can generate events such as halting the processor or triggering the trace capture.
- **Data Watchpoints:** specify data variable addresses, address ranges, or data values that can generate events such as halting the processor or triggering the trace capture.
- **Counters:** count the occurrence of an event or cycles for performance monitoring.
- **State Sequencing:** allows combinations of hardware program breakpoints and data watchpoints to precisely generate events for complex sequences.

For more information on AET, see the following documents:

- *Using Advanced Event Triggering to Find and Fix Intermittent Real-Time Bugs* application report (Literature Number: SPRA753)
- *Using Advanced Event Triggering to Debug Real-Time Problems in High Speed Embedded Microprocessor Systems* application report (Literature Number: SPRA387)

### 9.5.2 Trace

The device supports Trace at the Cortex™-A8 and System levels. Trace is a debug technology that provides a detailed, historical account of application code execution, timing, and data accesses. Trace collects, compresses, and exports debug information for analysis. The debug information can be exported to the Embedded Trace Buffer (ETB), or to the 5-pin Trace Interface (system trace only). Trace works in real-time and does not impact the execution of the system.

For more information on board design guidelines for Trace Advanced Emulation, see the *Emulation and Trace Headers Technical Reference Manual* (Literature Number: SPRU655).

### 9.5.3 IEEE 1149.1 JTAG

The JTAG (IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture) interface is used for BSDL testing and emulation of the device. The $\overline{\text{TRST}}$ pin only needs to be released when it is necessary to use a JTAG controller to debug the device or exercise the boundary scan functionality of the device. For maximum reliability, the device includes an internal pulldown (IPD) on the $\overline{\text{TRST}}$ pin to ensure that $\overline{\text{TRST}}$ is always asserted upon power up and the internal emulation logic of the device is always properly initialized. JTAG controllers from Texas Instruments actively drive $\overline{\text{TRST}}$ high. However, some third-party JTAG controllers may not drive $\overline{\text{TRST}}$ high but expect the use of a pullup resistor on $\overline{\text{TRST}}$. When using this type of JTAG controller, assert $\overline{\text{TRST}}$ to initialize the device after powerup and externally drive $\overline{\text{TRST}}$ high before attempting any emulation or boundary-scan operations.

The main JTAG features include:

- 32KB embedded trace buffer (ETB)
- 5-pin system trace interface for debug
- Supports Advanced Event Triggering (AET)
- All processors can be emulated via JTAG ports
- All functions on EMU pins of the device:
  - EMU[1:0] - cross-triggering, boot mode (WIR), STM trace
  - EMU[4:2] - STM trace only (single direction)


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### 9.5.3.1 JTAG ID (JTAGID) Register Description

**Table 9-7. JTAG ID Register(1)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4814 0600 | JTAGID | JTAG Identification Register(2) |

(1) IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.
(2) Read-only. Provides the device 32-bit JTAG ID.

The JTAG ID register is a read-only register that identifies to the customer the JTAG/device ID. For this device, the JTAG ID register resides at address location 0x4814 0600. The register hex value for the device is: 0x0B8F 202F. For the actual register bit names and their associated bit field descriptions, see Figure 9-5 and Table 9-8.

| 31 28 | 27 12 | 11 1 | 0 |
|---|---|---|---|
| VARIANT (4-bit) | PART NUMBER (16-bit) | MANUFACTURER (11-bit) | LSB |
| R-xxxx | R-1011 1000 1111 0010 | R-0000 0010 111 | R-1 |

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

**Figure 9-5. JTAG ID Register Description - Device Register Value: 0x0B8F 202F**

**Table 9-8. JTAG ID Register Selection Bit Descriptions**

| Bit | Field | Description |
|---|---|---|
| 31:28 | VARIANT | Variant (4-bit) value. Device value: xxxx. This value reflects the device silicon revision [For example, 0x0 (0000) for initial silicon revision (SR) 1.0].<br>• SR2.1, 0011, register value: 0x3B8F 202F<br>• SR3.0, 0100, register value: 0x4B8F 202F<br>For more detailed information on the current device silicon revision, see the *TMS320DM8127 DaVinci™ Digital Media Processors Silicon Errata (Silicon Revisions 3.0, 2.1)* (Literature Number: SPRZ385). |
| 27:12 | PART NUMBER | Part Number (16-bit) value. Device value: 0xB8F2 (1011 1000 1111 0010) |
| 11:1 | MANUFACTURER | Manufacturer (11-bit) value. Device value: 0x017 (0000 0010 111) |
| 0 | LSB | LSB. This bit is read as a ""1 for this device. |

### 9.5.3.2 JTAG Electrical Data/Timing

**Table 9-9. Timing Requirements for IEEE 1149.1 JTAG**

(see Figure 9-6)

| NO. | | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{c(TCK)}$ | Cycle time, TCK | 51.15 | | ns |
| 1a | $t_{w(TCKH)}$ | Pulse duration, TCK high (40% of $t_c$) | 20.46 | | ns |
| 1b | $t_{w(TCKL)}$ | Pulse duration, TCK low (40% of $t_c$) | 20.46 | | ns |
| 3 | $t_{su(TDI-TCK)}$ | Input setup time, TDI valid to TCK high (20% of ($t_c$ * 0.5)) | 5.115 | | ns |
| 3 | $t_{su(TMS-TCK)}$ | Input setup time, TMS valid to TCK high (20% of ($t_c$ * 0.5)) | 5.115 | | ns |
| 4 | $t_{h(TCK-TDI)}$ | Input hold time, TDI valid from TCK high | 10 | | ns |
| | $t_{h(TCK-TMS)}$ | Input hold time, TMS valid from TCK high | 10 | | ns |

**Table 9-10. Switching Characteristics Over Recommended Operating Conditions for IEEE 1149.1 JTAG**

(see Figure 9-6)

| NO. | PARAMETER | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 2 | $t_{d(TCKL-TDOV)}$ | Delay time, TCK low to TDO valid | 0 | 23.575(1) | ns |

(1) (0.5 * $t_c$) - 2

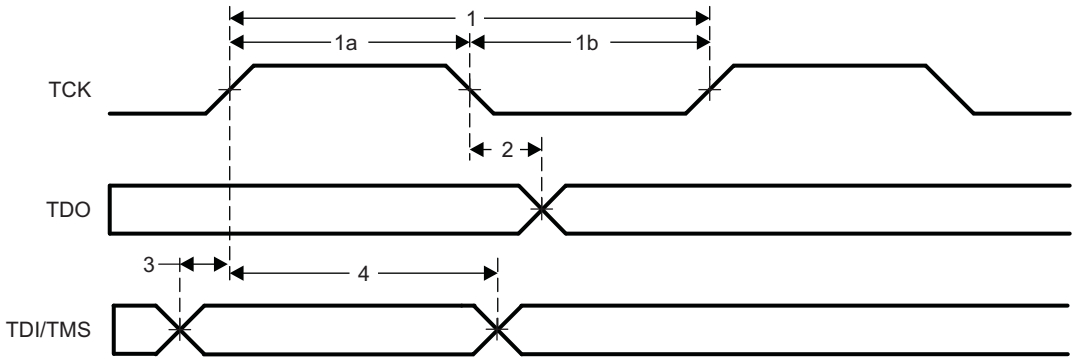


**Figure 9-6. JTAG Timing**

**Table 9-11. Timing Requirements for IEEE 1149.1 JTAG With RTCK**

(see Figure 9-6)

| NO. | | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{c(TCK)}$ | Cycle time, TCK | 51.15 | | ns |
| 1a | $t_{w(TCKH)}$ | Pulse duration, TCK high (40% of $t_c$) | 20.46 | | ns |
| 1b | $t_{w(TCKL)}$ | Pulse duration, TCK low (40% of $t_c$) | 20.46 | | ns |
| 3 | $t_{su(TDI-TCK)}$ | Input setup time, TDI valid to TCK high (20% of ($t_c$ * 0.5)) | 5.115 | | ns |
| 3 | $t_{su(TMS-TCK)}$ | Input setup time, TMS valid to TCK high (20% of ($t_c$ * 0.5)) | 5.115 | | ns |
| 4 | $t_{h(TCK-TDI)}$ | Input hold time, TDI valid from TCK high | 10 | | ns |
| | $t_{h(TCK-TMS)}$ | Input hold time, TMS valid from TCK high | 10 | | ns |

**Table 9-12. Switching Characteristics Over Recommended Operating Conditions for IEEE 1149.1 JTAG With RTCK**

(see Figure 9-7)

| NO. | PARAMETER | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 5 | $t_{d(TCK-RTCK)}$ | Delay time, TCK to RTCK with no selected subpaths (that is, ICEPick is the only tap selected - when the ARM is in the scan chain, the delay time is a function of the ARM functional clock.) | 0 | 21 | ns |
| 6 | $t_{c(RTCK)}$ | Cycle time, RTCK | 51.15 | | ns |
| 7 | $t_{w(RTCKH)}$ | Pulse duration, RTCK high (40% of $t_c$) | 20.46 | | ns |
| 8 | $t_{w(RTCKL)}$ | Pulse duration, RTCK low (40% of $t_c$) | 20.46 | | ns |

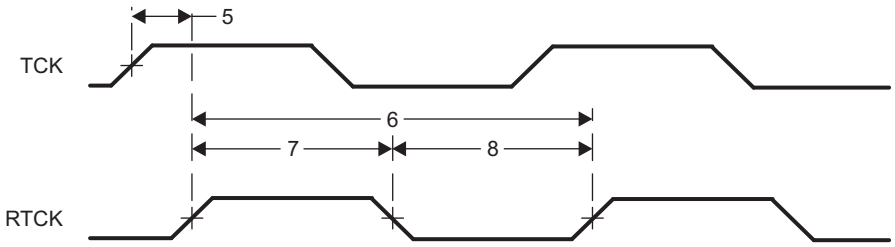


**Figure 9-7. JTAG With RTCK Timing**


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### Table 9-13. Switching Characteristics Over Recommended Operating Conditions for STM Trace

(see Figure 9-8)

| NO. | PARAMETER | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{w(EMUH50)}$ | Pulse duration, EMUx high detected at 50% $V_{OH}$ with 60/40 duty cycle | 4 (1) | | ns |
| | $t_{w(EMUH90)}$ | Pulse duration, EMUx high detected at 90% $V_{OH}$ | 3.5 | | ns |
| 2 | $t_{w(EMUL50)}$ | Pulse duration, EMUx low detected at 50% $V_{OH}$ with 60/40 duty cycle | 4 (1) | | ns |
| | $t_{w(EMUL10)}$ | Pulse duration, EMUx low detected at 10% $V_{OH}$ | 3.5 | | ns |
| 3 | $t_{sko(EMU)}$ | Output skew time, time delay difference between EMUx pins configured as trace. | -2 | 0.5 | ns |
| | $t_{skp(EMU)}$ | Pulse skew, magnitude of difference between high-to-low ($t_{PHL}$) and low-to-high ($t_{PLH}$) propagation delays | | 1 (1) | ns |
| | $t_{sldp_o(EMU)}$ | Output slew rate EMUx | 3.3 | | V/ns |

(1) This parameter applies to the maximum trace export frequency operating in a 40/60 duty cycle.

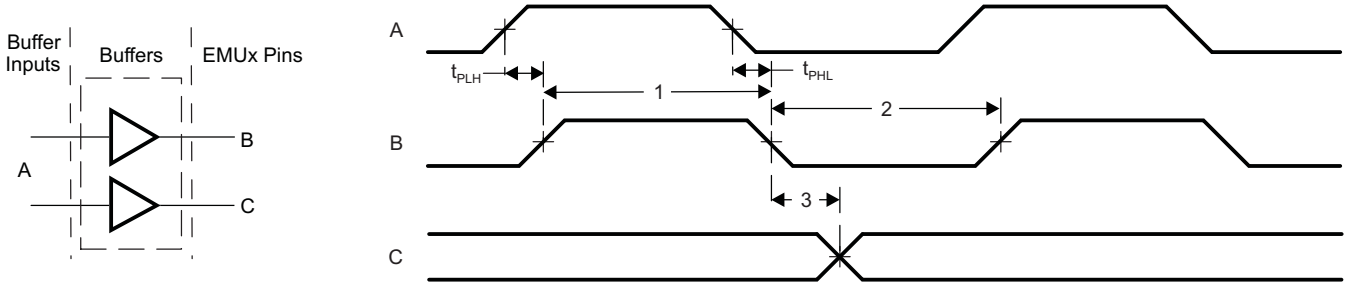


**Figure 9-8. STM Trace Timing**

## 9.6 Ethernet MAC Switch (EMAC SW)

The EMAC SW controls the flow of packet data between the device and two external Ethernet PHYs, with hardware flow control and quality-of-service (QOS) support. The EMAC SW contains a 3-port gigabit switch, where one port is internally connected and the other two ports are brought out externally. Each of the external EMAC ports supports 10Base-T (10 Mbits/second [Mbps]), and 100BaseTX (100 Mbps), in either half- or full-duplex mode, and 1000BaseT (1000 Mbps) in full-duplex mode.

The EMAC SW controls the flow of packet data from the device to the external PHYs. The EMAC0/1 ports on the device support four interface modes: Media Independent Interface (MII), Gigabit Media Independent Interface (GMII), Reduced Media Independent Interface (RMII) and Reduced Gigabit Media Independent Interface (RGMII). In addition, a single MDIO interface is pinned out to control the PHY configuration and status monitoring. Multiple external PHYs can be controlled by the MDIO interface.

The EMAC SW module conforms to the IEEE 802.3-2002 standard, describing the “Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer” specifications. The IEEE 802.3 standard has also been adopted by ISO/IEC and re-designated as ISO/IEC 8802-3:2000(E). Deviating from this standard, the EMAC SW module does not use the Transmit Coding Error signal MTXER. Instead of driving the error pin when an underflow condition occurs on a transmitted frame, the EMAC SW will intentionally generate an incorrect checksum by inverting the frame CRC, so that the transmitted frame will be detected as an error by the network. In addition, the EMAC SW I/Os operate at 3.3 V and are not compatible with 2.5-V I/O signaling. Therefore, only Ethernet PHYs with 3.3-V I/O interface should be used.

In networking systems, packet transmission and reception are critical tasks. The communications port programming interface (CPPI) protocol maximizes the efficiency of interaction between the host software and communications modules. The CPPI block contains 2048 words of 32-bit buffer descriptor memory that holds up to 512 buffer descriptors.

For more detailed information on the EMAC SW module, see the *3PSW Ethernet Subsystem* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

### *9.6.1 EMAC Peripheral Register Descriptions*

**Table 9-14. Ethernet MAC Switch Registers**

| ARM/L3 MASTERS EMAC HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4A10 0000 | CPSW_ID_VER | CPSW ID Version Register |
| 0x4A10 0004 | CPSW_CONTROL | CPSW Switch Control Register |
| 0x4A10 0008 | CPSW_SOFT_RESET | CPSW Soft Reset Register |
| 0x4A10 000C | CPSW_STAT_PORT_EN | CPSW Statistics Port Enable Register |
| 0x4A10 0010 | CPSW_PTYPE | CPSW Transmit Priority Type Register |
| 0x4A10 0014 | CPSW_SOFT_IDLE | CPSW Software Idle |
| 0x4A10 0018 | CPSW_THRU_RATE | CPSW Throughput Rate |
| 0x4A10 001C | CPSW_GAP_THRESH | CPSW CPGMAC_SL Short Gap Threshold |
| 0x4A10 0020 | CPSW_TX_START_WDS | CPSW Transmit Start Words |
| 0x4A10 0024 | CPSW_FLOW_CONTROL | CPSW Flow Control |
| 0x4A10 0028 | P0_MAX_BLKS | CPSW Port 0 Maximum FIFO Blocks Register |
| 0x4A10 002C | P0_BLK_CNT | CPSW Port 0 FIFO Block Usage Count Register (Read Only) |
| 0x4A10 0030 | P0_TX_IN_CTL | CPSW Port 0 Transmit FIFO Control |
| 0x4A10 0034 | P0_PORT_VLAN | CPSW Port 0 VLAN Register |
| 0x4A10 0038 | P0_TX_PRI_MAP | CPSW Port 0 Tx Header Priority to Switch Priority Mapping Register |


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**Table 9-14. Ethernet MAC Switch Registers (continued)**

| ARM/L3 MASTERS EMAC HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4A10 003C | CPDMA_TX_PRI_MAP | CPSW CPDMA TX (Port 0 Rx) Packet Priority to Header Priority Mapping Register |
| 0x4A10 0040 | CPDMA_RX_CH_Map | CPSW CPDMA RX (Port 0 Tx) Switch Priority to DMA Channel Mapping Register |
| 0x4A10 0050 | P1_MAX_BLKS | CPSW Port 1 Maximum FIFO Blocks Register |
| 0x4A10 0054 | P1_BLK_CNT | CPSW Port 1 FIFO Block Usage Count (Read Only) |
| 0x4A10 0058 | P1_TX_IN_CTL | CPSW Port 1 Transmit FIFO Control |
| 0x4A10 005C | P1_PORT_VLAN | CPSW Port 1 VLAN Register |
| 0x4A10 0060 | P1_TX_PRI_MAP | CPSW Port 1 Tx Header Priority to Switch Priority Mapping Register |
| 0x4A10 0064 | P1_TS_CTL | CPSW_3GF Port 1 Time Sync Control Register |
| 0x4A10 0068 | P1_TS_SEQ_LTYPE | CPSW_3GF Port 1 Time Sync LTYPE (and SEQ_ID_OFFSET) |
| 0x4A10 006C | P1_TS_VLAN | CPSW_3GF Port 1 Time Sync VLAN2 and VLAN2 Register |
| 0x4A10 0070 | SL1_SA_LO | CPSW CPGMAC_SL1 Source Address Low Register |
| 0x4A10 0074 | SL1_SA_HI | CPSW CPGMAC_SL1 Source Address High Register |
| 0x4A10 0078 | P1_SEND_PERCENT | CPSW Port 1 Transmit Queue Send Percentages |
| 0x4A10 007C – 0x4A10 008C | – | Reserved |
| 0x4A10 0090 | P2_MAX_BLKS | CPSW Port 2 Maximum FIFO Blocks Register |
| 0x4A10 0094 | P2_BLK_CNT | CPSW Port 2 FIFO Block Usage Count (Read Only) |
| 0x4A10 0098 | P2_TX_IN_CTL | CPSW Port 2 Transmit FIFO Control |
| 0x4A10 009C | P2_PORT_VLAN | CPSW Port 2 VLAN Register |
| 0x4A10 00A0 | P2_TX_PRI_MAP | CPSW Port 2 Tx Header Priority to Switch Priority Mapping Register |
| 0x4A10 00A4 | P2_TS_CTL | CPSW_3GF Port 2 Time Sync Control Register |
| 0x4A10 00A8 | P2_TS_SEQ_LTYPE | CPSW_3GF Port 2 Time Sync LTYPE (and SEQ_ID_OFFSET) |
| 0x4A10 00AC | P2_TS_VLAN | CPSW_3GF Port 2 Time Sync VLAN2 and VLAN2 Register |
| 0x4A10 00B0 | SL2_SA_LO | CPSW CPGMAC_SL2 Source Address Low Register |
| 0x4A10 00B4 | SL2_SA_HI | CPSW CPGMAC_SL2 Source Address High Register |
| 0x4A10 00B8 | P2_SEND_PERCENT | CPSW Port 2 Transmit Queue Send Percentages |
| 0x4A10 00BC – 0x4A10 00FC | – | Reserved |
| 0x4A10 0100 | TX_IDVER | CPDMA_REGS TX Identification and Version Register |
| 0x4A10 0104 | TX_CONTROL | CPDMA_REGS TX Control Register |
| 0x4A10 0108 | TX_TEARDOWN | CPDMA_REGS TX Teardown Register |
| 0x4A10 010C | – | Reserved |
| 0x4A10 0110 | RX_IDVER | CPDMA_REGS RX Identification and Version Register |
| 0x4A10 0114 | RX_CONTROL | CPDMA_REGS RX Control Register |
| 0x4A10 0118 | RX_TEARDOWN | CPDMA_REGS RX Teardown Register |
| 0x4A10 011C | SOFT_RESET | CPDMA_REGS Soft Reset Register |
| 0x4A10 0120 | DMACONTROL | CPDMA_REGS CPDMA Control Register |
| 0x4A10 0124 | DMASTATUS | CPDMA_REGS CPDMA Status Register |
| 0x4A10 0128 | RX_BUFFER_OFFSET | CPDMA_REGS Receive Buffer Offset |
| 0x4A10 012C | EMCONTROL | CPDMA_REGS Emulation Control |
| 0x4A10 0130 | TX_PRI0_RATE | CPDMA_REGS Transmit (Ingress) Priority 0 Rate |
| 0x4A10 0134 | TX_PRI1_RATE | CPDMA_REGS Transmit (Ingress) Priority 1 Rate |
| 0x4A10 0138 | TX_PRI2_RATE | CPDMA_REGS Transmit (Ingress) Priority 2 Rate |
| 0x4A10 013C | TX_PRI3_RATE | CPDMA_REGS Transmit (Ingress) Priority 3 Rate |
| 0x4A10 0140 | TX_PRI4_RATE | CPDMA_REGS Transmit (Ingress) Priority 4 Rate |
| 0x4A10 0144 | TX_PRI5_RATE | CPDMA_REGS Transmit (Ingress) Priority 5 Rate |

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**Table 9-14. Ethernet MAC Switch Registers (continued)**

| ARM/L3 MASTERS EMAC HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4A10 0148 | TX_PRI6_RATE | CPDMA_REGS Transmit (Ingress) Priority 6 Rate |
| 0x4A10 014C | TX_PRI7_RATE | CPDMA_REGS Transmit (Ingress) Priority 7 Rate |
| 0x4A10 0150 – 0x4A10 017C | – | Reserved |
| 0x4A10 0180 | TX_INTSTAT_RAW | CPDMA_INT TX Interrupt Status Register (Raw Value) |
| 0x4A10 0184 | TX_INTSTAT_MASKED | CPDMA_INT TX Interrupt Status Register (Masked Value) |
| 0x4A10 0188 | TX_INTMASK_SET | CPDMA_INT TX Interrupt Mask Set Register |
| 0x4A10 018C | TX_INTMASK_CLEAR | CPDMA_INT TX Interrupt Mask Clear Register |
| 0x4A10 0190 | CPDMA_IN_VECTOR | CPDMA_INT Input Vector (Read Only) |
| 0x4A10 0194 | CPDMA_EOI_VECTOR | CPDMA_INT End Of Interrupt Vector |
| 0x4A10 0198 – 0x4A10 019C | – | Reserved |
| 0x4A10 01A0 | RX_INTSTAT_RAW | CPDMA_INT RX Interrupt Status Register (Raw Value) |
| 0x4A10 01A4 | RX_INTSTAT_MASKED | CPDMA_INT RX Interrupt Status Register (Masked Value) |
| 0x4A10 01A8 | RX_INTMASK_SET | CPDMA_INT RX Interrupt Mask Set Register |
| 0x4A10 01AC | RX_INTMASK_CLEAR | CPDMA_INT RX Interrupt Mask Clear Register |
| 0x4A10 01B0 | DMA_INTSTAT_RAW | CPDMA_INT DMA Interrupt Status Register (Raw Value) |
| 0x4A10 01B4 | DMA_INTSTAT_MASKED | CPDMA_INT DMA Interrupt Status Register (Masked Value) |
| 0x4A10 01B8 | DMA_INTMASK_SET | CPDMA_INT DMA Interrupt Mask Set Register |
| 0x4A10 01BC | DMA_INTMASK_CLEAR | CPDMA_INT DMA Interrupt Mask Clear Register |
| 0x4A10 01C0 | RX0_PENDTHRESH | CPDMA_INT Receive Threshold Pending Register Channel 0 |
| 0x4A10 01C4 | RX1_PENDTHRESH | CPDMA_INT Receive Threshold Pending Register Channel 1 |
| 0x4A10 01C8 | RX2_PENDTHRESH | CPDMA_INT Receive Threshold Pending Register Channel 2 |
| 0x4A10 01CC | RX3_PENDTHRESH | CPDMA_INT Receive Threshold Pending Register Channel 3 |
| 0x4A10 01D0 | RX4_PENDTHRESH | CPDMA_INT Receive Threshold Pending Register Channel 4 |
| 0x4A10 01D4 | RX5_PENDTHRESH | CPDMA_INT Receive Threshold Pending Register Channel 5 |
| 0x4A10 01D8 | RX6_PENDTHRESH | CPDMA_INT Receive Threshold Pending Register Channel 6 |
| 0x4A10 01DC | RX7_PENDTHRESH | CPDMA_INT Receive Threshold Pending Register Channel 7 |
| 0x4A10 01E0 | RX0_FREEBUFFER | CPDMA_INT Receive Free Buffer Register Channel 0 |
| 0x4A10 01E4 | RX1_FREEBUFFER | CPDMA_INT Receive Free Buffer Register Channel 1 |
| 0x4A10 01E8 | RX2_FREEBUFFER | CPDMA_INT Receive Free Buffer Register Channel 2 |
| 0x4A10 01EC | RX3_FREEBUFFER | CPDMA_INT Receive Free Buffer Register Channel 3 |
| 0x4A10 01F0 | RX4_FREEBUFFER | CPDMA_INT Receive Free Buffer Register Channel 4 |
| 0x4A10 01F4 | RX5_FREEBUFFER | CPDMA_INT Receive Free Buffer Register Channel 5 |
| 0x4A10 01F8 | RX6_FREEBUFFER | CPDMA_INT Receive Free Buffer Register Channel 6 |
| 0x4A10 01FC | RX7_FREEBUFFER | CPDMA_INT Receive Free Buffer Register Channel 7 |
| 0x4A10 0200 | TX0_HDP | CPDMA_STATERAM TX Channel 0 Head Desc Pointer (1) |
| 0x4A10 0204 | TX1_HDP | CPDMA_STATERAM TX Channel 1 Head Desc Pointer (1) |
| 0x4A10 0208 | TX2_HDP | CPDMA_STATERAM TX Channel 2 Head Desc Pointer (1) |
| 0x4A10 020C | TX3_HDP | CPDMA_STATERAM TX Channel 3 Head Desc Pointer (1) |
| 0x4A10 0210 | TX4_HDP | CPDMA_STATERAM TX Channel 4 Head Desc Pointer (1) |
| 0x4A10 0214 | TX5_HDP | CPDMA_STATERAM TX Channel 5 Head Desc Pointer (1) |
| 0x4A10 0218 | TX6_HDP | CPDMA_STATERAM TX Channel 6 Head Desc Pointer (1) |
| 0x4A10 021C | TX7_HDP | CPDMA_STATERAM TX Channel 7 Head Desc Pointer (1) |
| 0x4A10 0220 | RX0_HDP | CPDMA_STATERAM RX 0 Channel 0 Head Desc Pointer (1) |
| 0x4A10 0224 | RX1_HDP | CPDMA_STATERAM RX 1 Channel 1 Head Desc Pointer (1) |
| 0x4A10 0228 | RX2_HDP | CPDMA_STATERAM RX 2 Channel 2 Head Desc Pointer (1) |

(1) Denotes CPPI 3.0 registers.


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**Table 9-14. Ethernet MAC Switch Registers (continued)**

| ARM/L3 MASTERS EMAC HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4A10 022C | RX3_HDP | CPDMA_STATERAM RX 3 Channel 3 Head Desc Pointer (1) |
| 0x4A10 0230 | RX4_HDP | CPDMA_STATERAM RX 4 Channel 4 Head Desc Pointer (1) |
| 0x4A10 0234 | RX5_HDP | CPDMA_STATERAM RX 5 Channel 5 Head Desc Pointer (1) |
| 0x4A10 0238 | RX6_HDP | CPDMA_STATERAM RX 6 Channel 6 Head Desc Pointer (1) |
| 0x4A10 023C | RX7_HDP | CPDMA_STATERAM RX 7 Channel 7 Head Desc Pointer (1) |
| 0x4A10 0240 | TX0_CP | CPDMA_STATERAM TX Channel 0 Completion Pointer Register(1) |
| 0x4A10 0244 | TX1_CP | CPDMA_STATERAM TX Channel 1 Completion Pointer Register (1) |
| 0x4A10 0248 | TX2_CP | CPDMA_STATERAM TX Channel 2 Completion Pointer Register (1) |
| 0x4A10 024C | TX3_CP | CPDMA_STATERAM TX Channel 3 Completion Pointer Register (1) |
| 0x4A10 0250 | TX4_CP | CPDMA_STATERAM TX Channel 4 Completion Pointer Register (1) |
| 0x4A10 0254 | TX5_CP | CPDMA_STATERAM TX Channel 5 Completion Pointer Register (1) |
| 0x4A10 0258 | TX6_CP | CPDMA_STATERAM TX Channel 6 Completion Pointer Register (1) |
| 0x4A10 025C | TX7_CP | CPDMA_STATERAM TX Channel 7 Completion Pointer Register (1) |
| 0x4A10 0260 | RX0_CP | CPDMA_STATERAM RX Channel 0 Completion Pointer Register (1) |
| 0x4A10 0264 | RX1_CP | CPDMA_STATERAM RX Channel 1 Completion Pointer Register (2) |
| 0x4A10 0268 | RX2_CP | CPDMA_STATERAM RX Channel 2 Completion Pointer Register (2) |
| 0x4A10 026C | RX3_CP | CPDMA_STATERAM RX Channel 3 Completion Pointer Register (2) |
| 0x4A10 0270 | RX4_CP | CPDMA_STATERAM RX Channel 4 Completion Pointer Register (2) |
| 0x4A10 0274 | RX5_CP | CPDMA_STATERAM RX Channel 5 Completion Pointer Register (2) |
| 0x4A10 0278 | Rx6_CP | CPDMA_STATERAM RX Channel 6 Completion Pointer Register (2) |
| 0x4A10 027C | Rx7_CP | CPDMA_STATERAM RX Channel 7 Completion Pointer Register (2) |
| 0x4A10 02C0 - 0x4A10 03FC | – | Reserved |
| 0x4A10 0400 | RXGOODFRAMES | CPSW_STATS Total Number of Good Frames Received |
| 0x4A10 0404 | RXBROADCASTFRAMES | CPSW_STATS Total Number of Good Broadcast Frames Received |
| 0x4A10 0408 | RXMULTICASTFRAMES | CPSW_STATS Total Number of Good Multicast Frames Received |
| 0x4A10 040C | RXPAUSEFRAMES | CPSW_STATS PauseRxFrames |
| 0x4A10 0410 | RXCRCERRORS | CPSW_STATS Total Number of CRC Errors Frames Received |
| 0x4A10 0414 | RXALIGNCODEERRORS | CPSW_STATS Total Number of Alignment/Code Errors Received |
| 0x4A10 0418 | RXOVERSIZEDFRAMES | CPSW_STATS Total Number of Oversized Frames Received |
| 0x4A10 041C | RXJABBERFRAMES | CPSW_STATS Total number of Jabber Frames Received |
| 0x4A10 0420 | RXUNDERSIZEDFRAMES | CPSW_STATS Total Number of Undersized Frames Received |
| 0x4A10 0424 | RXFRAGMENTS | CPSW_STATS RxFragments Received |
| 0x4A10 0428 - 0x4A10 042C | – | Reserved. Read as Zero |
| 0x4A10 0430 | RXOCTETS | CPSW_STATS Total Number of Received Bytes in Good Frames |
| 0x4A10 0434 | TXGOODFRAMES | CPSW_STATS GoodTxFrames |
| 0x4A10 0438 | TXBROADCASTFRAMES | CPSW_STATS BroadcastTxFrames |
| 0x4A10 043C | TXMULTICASTFRAMES | CPSW_STATS MulticastTxFrames |
| 0x4A10 0440 | TXPAUSEFRAMES | CPSW_STATS PauseTxFrames |
| 0x4A10 0444 | TXDEFERREDFRAMES | CPSW_STATS Deferred Frames |
| 0x4A10 0448 | TXCOLLISIONFRAMES | CPSW_STATS Collisions |
| 0x4A10 044C | TXSINGLECOLLFRAMES | CPSW_STATS SingleCollisionTxFrames |
| 0x4A10 0450 | TXMULTCOLLFRAMES | CPSW_STATS MultipleCollisionTxFrames |
| 0x4A10 0454 | TXEXCESSIVECOLLISIONS | CPSW_STATS ExcessiveCollisions |
| 0x4A10 0458 | TXLATECOLLISIONS | CPSW_STATS LateCollisions |

(2) Denotes CPPI 3.0 registers.

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**Table 9-14. Ethernet MAC Switch Registers (continued)**

| ARM/L3 MASTERS EMAC HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4A10 045C | TXUNDERRUN | CPSW_STATS Transmit Underrun Error |
| 0x4A10 0460 | TXCARRIERSENSEERRORS | CPSW_STATS CarrierSenseErrors |
| 0x4A10 0464 | TXOCTETS | CPSW_STATS TxOctets |
| 0x4A10 0468 | 64OCTETFRAMES | CPSW_STATS 64octetFrames |
| 0x4A10 046C | 65T127OCTETFRAMES | CPSW_STATS 65-127octetFrames |
| 0x4A10 0470 | 128T255OCTETFRAMES | CPSW_STATS 128-255octetFrames |
| 0x4A10 0474 | 256T511OCTETFRAMES | CPSW_STATS 256-511octetFrames |
| 0x4A10 0478 | 512T1023OCTETFRAMES | CPSW_STATS 512-1023octetFrames |
| 0x4A10 047C | 1024TUPOCTETFRAMES | CPSW_STATS 1023-1518octetFrames |
| 0x4A10 0480 | NETOCTETS | CPSW_STATS NetOctets |
| 0x4A10 0484 | RXSOFOVERRUNS | CPSW_STATS Receive FIFO or DMA Start of Frame Overruns |
| 0x4A10 0488 | RXMOFOVERRUNS | CPSW_STATS Receive FIFO or DMA Mid of Frame Overruns |
| 0x4A10 048C | RXDMAOVERRUNS | CPSW_STATS Receive DMA Start of Frame and Middle of Frame Overruns |
| 0x4A10 0490 - 0x4A10 04FC | – | Reserved |
| 0x4A10 0500 | CPTS_IDVER | Identification and Version Register |
| 0x4A10 0504 | CPTS_CONTROL | Time Sync Control Register |
| 0x4A10 0508 | CPTS_RFTCLK_SEL | Reference Clock Select Register |
| 0x4A10 050C | CPTS_TS_PUSH | Time Stamp Event Push Register |
| 0x4A10 0510 | CPTS_TS_LOAD_VAL | Time Stamp Load Value Register |
| 0x4A10 0514 | CPTSTS_LOAD_EN | Time Stamp Load Enable Register |
| 0x4A10 0518 - 0x4A10 051C | – | Reserved |
| 0x4A10 0520 | CPTS_INTSTAT_RAW | Time Sync Interrupt Status Raw Register |
| 0x4A10 0524 | CPTS_INTSTAT_MASKED | Time Sync Interrupt Status Masked Register |
| 0x4A10 0528 | CPTS_INT_ENABLE | Time Sync Interrupt Enable Register |
| 0x4A10 052C | – | Reserved |
| 0x4A10 0530 | CPTS_EVENT_POP | Event Interrupt Pop Register |
| 0x4A10 0534 | CPTS_EVENT_LOW | Lower 32-Bits of the Event Value |
| 0x4A10 0538 | CPTS_EVENT_HIGH | Upper 32-Bits of the Event Value |
| 0x4A10 053C - 0x4A10 05FC | – | Reserved |
| 0x4A10 0600 | ALE_IDVER | Address Lookup Engine ID/Version Register |
| 0x4A10 0604 | – | Reserved |
| 0x4A10 0608 | ALE_CONTROL | Address Lookup Engine Control Register |
| 0x4A10 060C | – | Reserved |
| 0x4A10 0610 | ALE_PRESCALE | Address Lookup Engine Prescale Register |
| 0x4A10 0614 | – | Reserved |
| 0x4A10 0618 | ALE_UNKNOWN_VLAN | Address Lookup Engine Unknown VLAN Register |
| 0x4A10 061C | – | Reserved |
| 0x4A10 0620 | ALE_TBLCTL | Address Lookup Engine Table Control |
| 0x4A10 0624 - 0x4A10 0630 | – | Reserved |
| 0x4A10 0634 | ALE_TBLW2 | Address Lookup Engine Table Word 2 Register |
| 0x4A10 0638 | ALE_TBLW1 | Address Lookup Engine Table Word 1 Register |
| 0x4A10 063C | ALE_TBLW0 | Address Lookup Engine Table Word 0 Register |
| 0x4A10 0640 | ALE_PORTCTL0 | Address Lookup Engine Port 0 Control Register |
| 0x4A10 0644 | ALE_PORTCTL1 | Address Lookup Engine Port 1 Control Register |


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**Table 9-14. Ethernet MAC Switch Registers (continued)**

| ARM/L3 MASTERS EMAC HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4A10 0648 | ALE_PORTCTL2 | Address Lookup Engine Port 2 Control Register |
| 0x4A10 064C | – | Reserved |
| 0x4A10 0650 | – | Reserved |
| 0x4A10 0654 | – | Reserved |
| 0x4A10 0658 - 0x4A10 06FF | – | Reserved |
| 0x4A10 0700 | SL1_IDVER | CPGMAC_SL1 ID/Version Register |
| 0x4A10 0704 | SL1_MACCONTROL | CPGMAC_SL1 Mac Control Register |
| 0x4A10 0708 | SL1_MACSTATUS | CPGMAC_SL1 Mac Status Register |
| 0x4A10 070C | SL1_SOFT_RESET | CPGMAC_SL1 Soft Reset Register |
| 0x4A10 0710 | SL1_RX_MAXLEN | CPGMAC_SL1 RX Maximum Length Register |
| 0x4A10 0714 | SL1_BOFFTEST | CPGMAC_SL1 Backoff Test Register |
| 0x4A10 0718 | SL1_RX_PAUSE | CPGMAC_SL1 Receive Pause Timer Register |
| 0x4A10 071C | SL1_TX_PAUSE | CPGMAC_SL1 Transmit Pause Timer Register |
| 0x4A10 0720 | SL1_EMCONTROL | CPGMAC_SL1 Emulation Control Register |
| 0x4A10 0724 | SL1_RX_PRI_MAP | CPGMAC_SL1 Rx Pkt Priority to Header Priority Mapping Register |
| 0x4A10 0728 - 0x4A10 073C | – | Reserved |
| 0x4A10 0740 | SL2_IDVER | CPGMAC_SL2 ID/Version Register |
| 0x4A10 0744 | SL2_MACCONTROL | CPGMAC_SL2 Mac Control Register |
| 0x4A10 0748 | SL2_MACSTATUS | CPGMAC_SL2 Mac Status Register |
| 0x4A10 074C | SL2_SOFT_RESET | CPGMAC_SL2 Soft Reset Register |
| 0x4A10 0750 | SL2_RX_MAXLEN | CPGMAC_SL2 RX Maximum Length Register |
| 0x4A10 0754 | SL2_BOFFTEST | CPGMAC_SL2 Backoff Test Register |
| 0x4A10 0758 | SL2_RX_PAUSE | CPGMAC_SL2 Receive Pause Timer Register |
| 0x4A10 075C | SL2_TX_PAUSE | CPGMAC_SL2 Transmit Pause Timer Register |
| 0x4A10 0760 | SL2_EMCONTROL | CPGMAC_SL2 Emulation Control |
| 0x4A10 0764 | SL2_RX_PRI_MAP | CPGMAC_SL2 Rx Pkt Priority to Header Priority Mapping Register |
| 0x4A10 0768 - 0x4A10 07FF | – | Reserved |
| 0x4A10 0800 - 0x4A10 08FF | see Table 9-27 | MDIO Registers |
| 0x4A10 0900 | IDVER | Subsystem ID Version Register |
| 0x4A10 0904 | SOFT_RESET | Subsystem Soft Reset Register |
| 0x4A10 0908 | CONTROL | Subsystem Control Register |
| 0x4A10 090C | INT_CONTROL | Subsystem Interrupt Control |
| 0x4A10 0910 | C0_RX_THRESH_EN | Subsystem Core 0 Receive Threshold Int Enable Register |
| 0x4A10 0914 | C0_RX_EN | Subsystem Core 0 Receive Interrupt Enable Register |
| 0x4A10 0918 | C0_TX_EN | Subsystem Core 0 Transmit Interrupt Enable Register |
| 0x4A10 091C | C0_MISC_EN | Subsystem Core 0 Misc Interrupt Enable Register |
| 0x4A10 0920 | C1_RX_THRESH_EN | Subsystem Core 1 Receive Threshold Int Enable Register |
| 0x4A10 0924 | C1_RX_EN | Subsystem Core 1 Receive Interrupt Enable Register |
| 0x4A10 0928 | C1_TX_EN | Subsystem Core 1 Transmit Interrupt Enable Register |
| 0x4A10 092C | C1_MISC_EN | Subsystem Core 1 Misc Interrupt Enable Register |
| 0x4A10 0930 | C2_RX_THRESH_EN | Subsystem Core 2 Receive Threshold Int Enable Register |
| 0x4A10 0934 | C2_RX_EN | Subsystem Core 2 Receive Interrupt Enable Register |
| 0x4A10 0938 | C2_TX_EN | Subsystem Core 2 Transmit Interrupt Enable Register |
| 0x4A10 093C | C2_MISC_EN | Subsystem Core 2 Misc Interrupt Enable Register |
| 0x4A10 0940 | C0_RX_THRESH_STAT | Subsystem Core 0 Rx Threshold Masked Int Status Register |
| 0x4A10 0944 | C0_RX_STAT | Subsystem Core 0 Rx Interrupt Masked Int Status Register |

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**Table 9-14. Ethernet MAC Switch Registers (continued)**

| ARM/L3 MASTERS EMAC HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4A10 0948 | C0_TX_STAT | Subsystem Core 0 Tx Interrupt Masked Int Status Register |
| 0x4A10 094C | C0_MISC_STAT | Subsystem Core 0 Misc Interrupt Masked Int Status Register |
| 0x4A10 0950 | C1_RX_THRESH_STAT | Subsystem Core 1 Rx Threshold Masked Int Status Register |
| 0x4A10 0954 | C1_RX_STAT | Subsystem Core 1 Receive Masked Interrupt Status Register |
| 0x4A10 0958 | C1_TX_STAT | Subsystem Core 1 Transmit Masked Interrupt Status Register |
| 0x4A10 095C | C1_MISC_STAT | Subsystem Core 1 Misc Masked Interrupt Status Register |
| 0x4A10 0960 | C2_RX_THRESH_STAT | Subsystem Core 2 Rx Threshold Masked Int Status Register |
| 0x4A10 0964 | C2_RX_STAT | Subsystem Core 2 Receive Masked Interrupt Status Register |
| 0x4A10 0968 | C2_TX_STAT | Subsystem Core 2 Transmit Masked Interrupt Status Register |
| 0x4A10 096C | C2_MISC_STAT | Subsystem Core 2 Misc Masked Interrupt Status Register |
| 0x4A10 0970 | C0_RX_IMAX | Subsystem Core 0 Receive Interrupts Per Millisecond |
| 0x4A10 0974 | C0_TX_IMAX | Subsystem Core 0 Transmit Interrupts Per Millisecond |
| 0x4A10 0978 | C1_RX_IMAX | Subsystem Core 1 Receive Interrupts Per Millisecond |
| 0x4A10 097C | C1_TX_IMAX | Subsystem Core 1 Transmit Interrupts Per Millisecond |
| 0x4A10 0980 | C2_RX_IMAX | Subsystem Core 2 Receive Interrupts Per Millisecond |
| 0x4A10 0984 | C2_TX_IMAX | Subsystem Core 2 Transmit Interrupts Per Millisecond |
| 0x4A10 2000 -0x4A10 3FFF | CPPI_RAM | CPPI RAM(3) |

(3) Denotes CPPI 3.0 registers.


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## 9.6.2 EMAC Electrical Data/Timing

### 9.6.2.1 EMAC MII and GMII Electrical Data/Timing

**Table 9-15. Timing Requirements for EMAC[x]_MRCLK - [G]MII Operation**

(see Figure 9-9)

| NO. | | | OPP100/120/166 | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | 1000 Mbps (1 Gbps) (GMII Only) | | 100 Mbps | | 10 Mbps | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(MRCLK)}$ | Cycle time, EMAC[x]_MRCLK | 8 | | 40 | | 400 | | ns |
| 2 | $t_{w(MRCLKH)}$ | Pulse duration, EMAC[x]_MRCLK high | 2.8 | | 14 | | 140 | | ns |
| 3 | $t_{w(MRCLKL)}$ | Pulse duration, EMAC[x]_MRCLK low | 2.8 | | 14 | | 140 | | ns |
| 4 | $t_{t(MRCLK)}$ | Transition time, EMAC[x]_MRCLK | | 1 | | 3 | | 3 | ns |

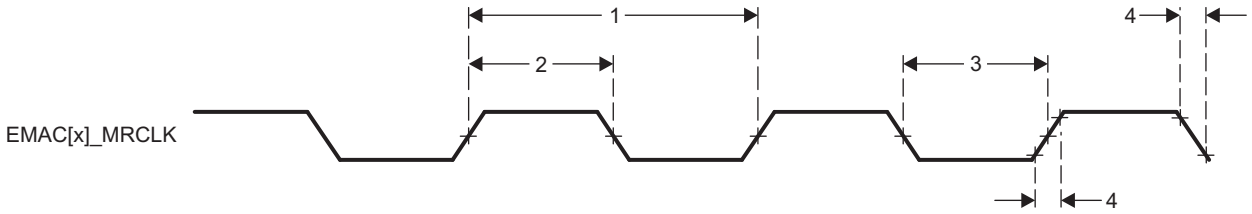


**Figure 9-9. EMAC[x]_MRCLK Timing (EMAC Receive) - [G]MII Operation**

**Table 9-16. Timing Requirements for EMAC[x]_MTCLK - [G]MII Operation**

(see Figure 9-14)

| NO. | | | OPP100/120/166 | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | 1000 Mbps (1 Gbps) (GMII Only) | | 100 Mbps | | 10 Mbps | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(MTCLK)}$ | Cycle time, EMAC[x]_MTCLK | 8 | | 40 | | 400 | | ns |
| 2 | $t_{w(MTCLKH)}$ | Pulse duration, EMAC[x]_MTCLK high | 2.8 | | 14 | | 140 | | ns |
| 3 | $t_{w(MTCLKL)}$ | Pulse duration, EMAC[x]_MTCLK low | 2.8 | | 14 | | 140 | | ns |
| 4 | $t_{t(MTCLK)}$ | Transition time, EMAC[x]_MTCLK | | 1 | | 3 | | 3 | ns |

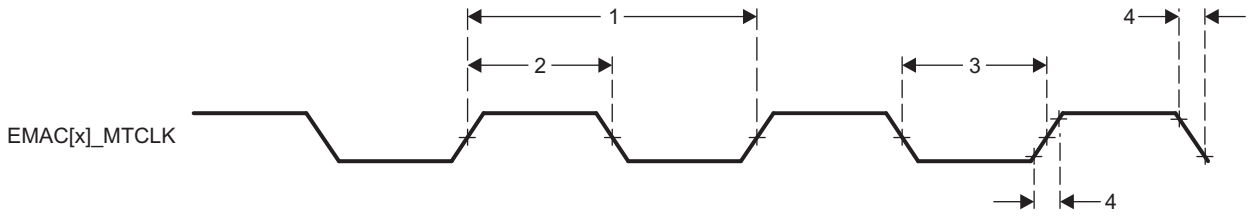


**Figure 9-10. EMAC[x]_MTCLK Timing (EMAC Transmit) - [G]MII Operation**

### Table 9-17. Timing Requirements for EMAC [G]MII Receive 10/100/1000 Mbit/s

(see Figure 9-11)

| NO. | | | OPP100/120/166 | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | 1000 Mbps (1 Gbps) | | 100/10 Mbps | | |
| | | | MIN | MAX | MIN | MAX | |
| 1 | $t_{su(MRXD-MRCLK)}$<br>$t_{su(MRXDV-MRCLK)}$<br>$t_{su(MRXER-MRCLK)}$ | Setup time, receive selected signals valid before EMAC[1:0]_MRCLK | 2 | | 8 | | ns |
| 2 | $t_{h(MRCLK-MRXD)}$<br>$t_{h(MRCLK-MRXDV)}$<br>$t_{h(MRCLK-MRXER)}$ | Hold time, receive selected signals valid after EMAC[1:0]_MRCLK | 0 | | 8 | | ns |

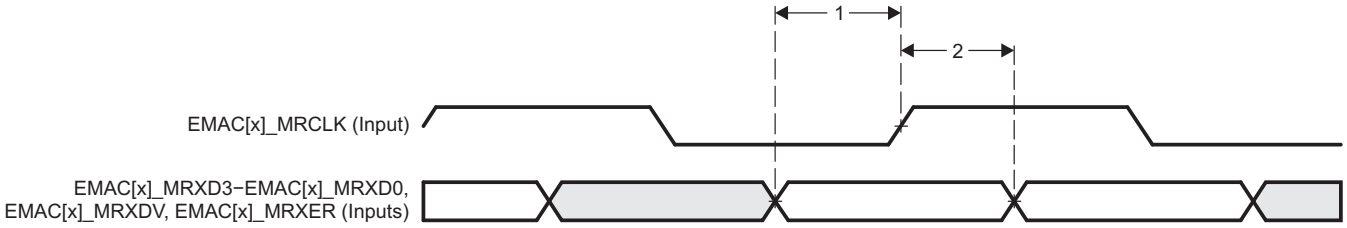


**Figure 9-11. EMAC Receive Interface Timing [G]MII Operation**

### Table 9-18. Switching Characteristics Over Recommended Operating Conditions for EMAC [G]MII Transmit 10/100 Mbits/s

(see Figure 9-12)

| NO. | PARAMETER | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|
| | | | 100/10 Mbps | | |
| | | | MIN | MAX | |
| 1 | $t_{d(MTXCLK-MTXD)}$<br>$t_{d(MTCLK-MTXEN)}$ | Delay time, EMAC[x]_MTCLK to transmit selected signals valid | 2.5 | 25 | ns |

### Table 9-19. Switching Characteristics Over Recommended Operating Conditions for EMAC [G]MII Transmit 1000 Mbits/s

(see Figure 9-12)

| NO. | PARAMETER | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|
| | | | 1000 Mbps (1 Gbps) | | |
| | | | MIN | MAX | |
| 1 | $t_{d(GMTCLK-MTXD)}$<br>$t_{d(GMTCLK-MTXEN)}$ | Delay time, EMAC[x]_GMTCLK to transmit selected signals valid | 0 | 5 | ns |

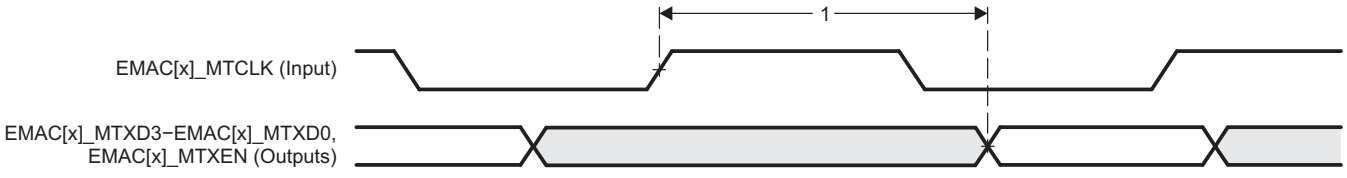


**Figure 9-12. EMAC Transmit Interface Timing [G]MII Operation**


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### 9.6.2.2 EMAC RMII Electrical Data/Timing

**Table 9-20. Timing Requirements for EMAC[x]_RMREFCLK - RMII Operation**

(see Figure 9-13)

| NO. | | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{c(RMREFCLK)}$ | Cycle time, EMAC[x]_RMREFCLK | 19.999 | 20.001 | ns |
| 2 | $t_{w(RMREFCLKH)}$ | Pulse duration, EMAC[x]_RMREFCLK high | 7 | 13 | ns |
| 3 | $t_{w(RMREFCLKL)}$ | Pulse duration, EMAC[x]_RMREFCLK low | 7 | 13 | ns |
| 4 | $t_{t(RMREFCLK)}$ | Transition time, EMAC[x]_RMREFCLK | | 3 | ns |

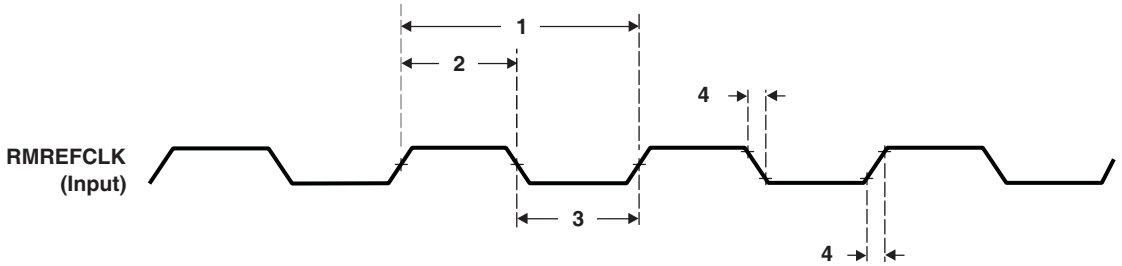


**Figure 9-13. RMREFCLK Timing RMII Operation**

**Table 9-21. Timing Requirements for EMAC RMII Receive**

(see Figure 9-13)

| NO. | | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{su(RMRXD-RMREFCLK)}$<br>$t_{su(RMCRSDV-RMREFCLK)}$<br>$t_{su(RMRXER-RMREFCLK)}$ | Setup time, receive selected signals valid before EMAC[x]_RMREFCLK | 4 | | ns |
| 2 | $t_{h(RMREFCLK-RMRXD)}$<br>$t_{h(RMREFCLK-RMCRSDV)}$<br>$t_{h(RMREFCLK-RMRXER)}$ | Hold time, receive selected signals valid after EMAC[x]_RMREFCLK | 2 | | ns |

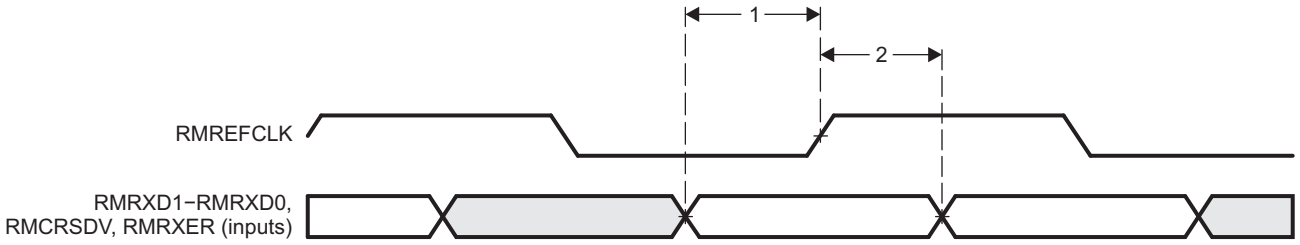


**Figure 9-14. EMAC Receive Interface Timing RMII Operation**

**Table 9-22. Switching Characteristics Over Recommended Operating Conditions for EMAC RMII Transmit 10/100 Mbits/s**

(see Figure 9-15)

| NO. | PARAMETER | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{d(RMREFCLK-RMTXD)}$ | Delay time, EMAC[x]_RMREFCLK high to EMAC[x]_RMTXD[x] valid | 2.5 | 13 | ns |
| 2 | $t_{dd(RMREFCLK-RMTXEN)}$ | Delay time, EMAC[x]_RMREFCLK high to EMAC[x]_RMTXEN valid | 2.5 | 13 | |

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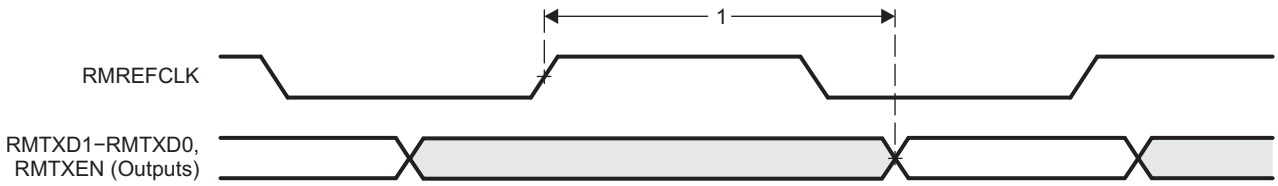


**Figure 9-15. EMAC Transmit Interface Timing RMII Operation**

### 9.6.2.3 EMAC RGMII Electrical Data/Timing

**Table 9-23. Timing Requirements for EMAC[x]_RGRXC - RGMII Operation**

(see Figure 9-16)

| NO. | | | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| 1 | $t_{c(RGRXC)}$ | Cycle time, EMAC[x]_RGRXC | 10 Mbps | 360 | 440 | ns |
| | | | 100 Mbps | 36 | 44 | |
| | | | 1000 Mbps | 7.2 | 8.8 | |
| 2 | $t_{w(RGRXCH)}$ | Pulse duration, EMAC[x]_RGRXC high | 10 Mbps | $0.40*t_{c(RGRXC)}$ | $0.60*t_{c(RGRXC)}$ | ns |
| | | | 100 Mbps | $0.40*t_{c(RGRXC)}$ | $0.60*t_{c(RGRXC)}$ | |
| | | | 1000 Mbps | $0.45*t_{c(RGRXC)}$ | $0.55*t_{c(RGRXC)}$ | |
| 3 | $t_{w(RGRXCL)}$ | Pulse duration, EMAC[x]_RGRXC low | 10 Mbps | $0.40*t_{c(RGRXC)}$ | $0.60*t_{c(RGRXC)}$ | ns |
| | | | 100 Mbps | $0.40*t_{c(RGRXC)}$ | $0.60*t_{c(RGRXC)}$ | |
| | | | 1000 Mbps | $0.45*t_{c(RGRXC)}$ | $0.55*t_{c(RGRXC)}$ | |
| 4 | $t_{t(RGRXC)}$ | Transition time, EMAC[x]_RGRXC | 10 Mbps | | 0.75 | ns |
| | | | 100 Mbps | | 0.75 | |
| | | | 1000 Mbps | | 0.75 | |


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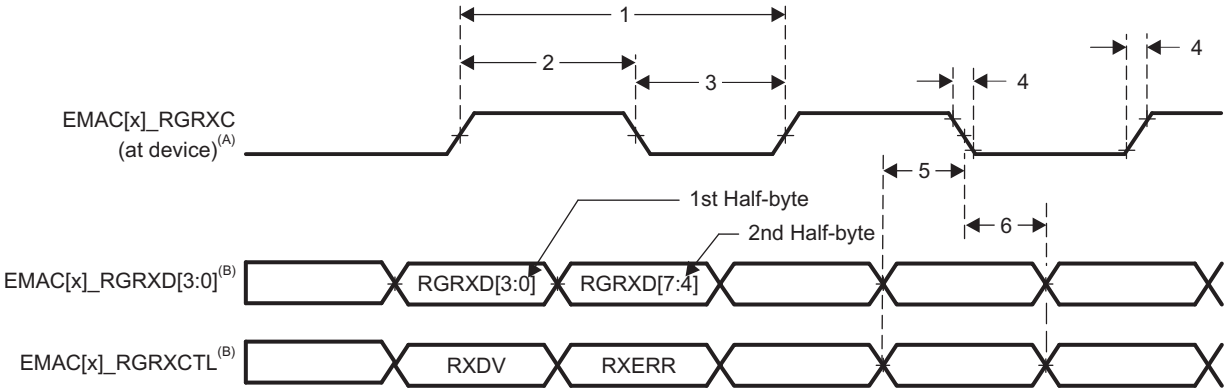
### Table 9-24. Timing Requirements for EMAC RGMII Input Receive for 10/100/1000 Mbps(1)

(see Figure 9-16)

| NO. | | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 5 | $t_{su(RGRXD-RGRXCH)}$ | Setup time, receive selected signals valid before EMAC[x]_RGRXC (at device) high/low | 1.0 | | ns |
| 6 | $t_{h(RGRXCH-RGRXD)}$ | Hold time, receive selected signals valid after EMAC[x]_RGRXC (at device) high/low | 1.0 | | ns |

(1) For RGMII, receive selected signals include: EMAC[x]_RGRXD[3:0] and EMAC[x]_RGRXCTL.




A. EMAC[x]_RGRXC must be externally delayed relative to the data and control pins. The internal delay can be enabled or disabled via the EMAC RGMIIx_ID_MODE register.

B. Data and control information is received using both edges of the clocks. EMAC[x]_RGRXD[3:0] carries data bits 3-0 on the rising edge of EMAC[x]_RGRXC and data bits 7-4 on the falling edge of EMAC[x]_RGRXC. Similarly, EMAC[x]_RGRXCTL carries RXDV on rising edge of EMAC[x]_RGRXC and RXERR on falling edge of EMAC[x]_RGRXC.

**Figure 9-16. EMAC Receive Interface Timing [RGMII Operation]**

### Table 9-25. Switching Characteristics Over Recommended Operating Conditions for RGTXC - RGMII Operation for 10/100/1000 Mbit/s

(see Figure 9-17)

| NO. | | | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| 1 | $t_{c(RGTXC)}$ | Cycle time, EMAC[x]_RGTXC | 10 Mbps | 360 | 440 | ns |
| | | | 100 Mbps | 36 | 44 | |
| | | | 1000 Mbps | 7.2 | 8.8 | |
| 2 | $t_{w(RGTXCH)}$ | Pulse duration, EMAC[x]_RGTXC high | 10 Mbps | $0.40*t_{c(RGTXC)}$ | $0.60*t_{c(RGTXC)}$ | ns |
| | | | 100 Mbps | $0.40*t_{c(RGTXC)}$ | $0.60*t_{c(RGTXC)}$ | |
| | | | 1000 Mbps | $0.45*t_{c(RGTXC)}$ | $0.55*t_{c(RGTXC)}$ | |
| 3 | $t_{w(RGTXCL)}$ | Pulse duration, EMAC[x]_RGTXC low | 10 Mbps | $0.40*t_{c(RGTXC)}$ | $0.60*t_{c(RGTXC)}$ | ns |
| | | | 100 Mbps | $0.40*t_{c(RGTXC)}$ | $0.60*t_{c(RGTXC)}$ | |
| | | | 1000 Mbps | $0.45*t_{c(RGTXC)}$ | $0.55*t_{c(RGTXC)}$ | |
| 4 | $t_{t(RGTXC)}$ | Transition time, EMAC[x]_RGTXC | 10 Mbps | | 0.75 | ns |
| | | | 100 Mbps | | 0.75 | |
| | | | 1000 Mbps | | 0.75 | |

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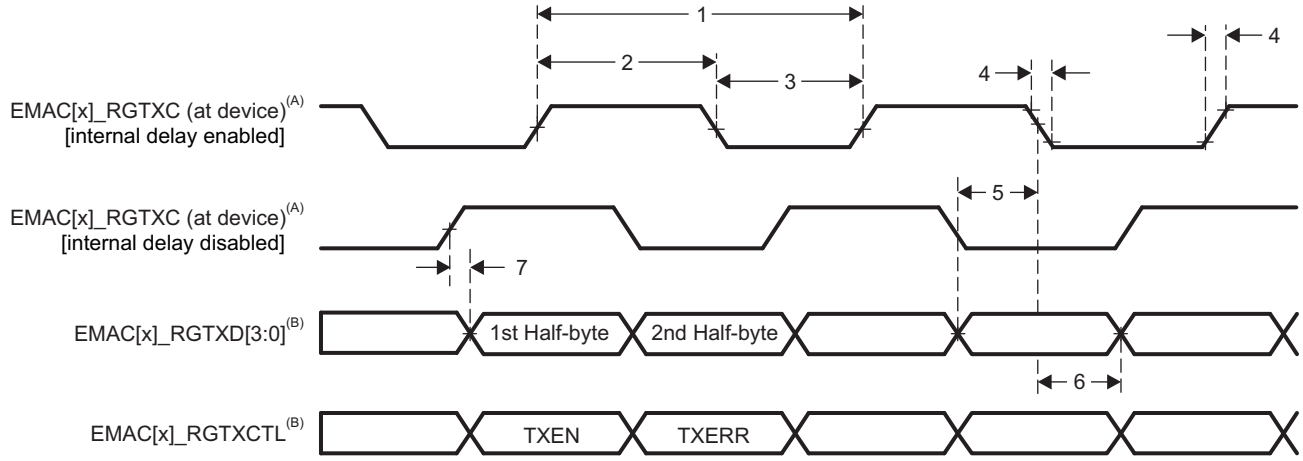
**Table 9-26. Switching Characteristics Over Recommended Operating Conditions for EMAC RGMII Transmit(1)**

(see Figure 9-17)

| NO. | PARAMETER | | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| 5 | $t_{su(RGTXD-RGTXCH)}$ | Setup time, transmit selected signals valid before EMAC[x]_RGTXC (at device) high/low | Internal delay enabled | 1.2 | | ns |
| 6 | $t_{h(RGTXCH-RGTXD)}$ | Hold time, transmit selected signals valid after EMAC[x]_RGTXC (at device) high/low | Internal delay enabled | 1.2 | | ns |
| 7 | $t_{sk(RGTXD-RGTXCH)}$ | Transmit selected signals to EMAC[x]_RGTXC (at device) output skew | Internal delay disabled | -0.5 | 0.5 | ns |

(1) For RGMII, transmit selected signals include: EMAC[x]_RGTXD[3:0] and EMAC[x]_RGTXCTL.




A. RGTXC is delayed internally before being driven to the EMAC[x]_RGTXC pin. The internal delay can be enabled or disabled via the EMAC RGMIIx_ID_MODE register.

B. Data and control information is transmitted using both edges of the clocks. EMAC[x]_RGTXD[3:0] carries data bits 3-0 on the rising edge of EMAC[x]_RGTXC and data bits 7-4 on the falling edge of EMAC[x]_RGTXC. Similarly, EMAC[x]_RGTXCTL carries TXEN on rising edge of EMAC[x]_RGTXC and TXERR of falling edge of EMAC[x]_RGTXC.

**Figure 9-17. EMAC Transmit Interface Timing [RGMII Operation]**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### 9.6.3 Management Data Input/Output (MDIO)

The Management Data Input/Output (MDIO) module continuously polls all 32 MDIO addresses in order to enumerate all PHY devices in the system.

The MDIO module implements the 802.3 serial management interface to interrogate and control Ethernet PHYs using a shared two-wire bus. Host software uses the MDIO module to configure the auto-negotiation parameters of each PHY attached to the EMAC SW, retrieve the negotiation results, and configure required parameters in the EMAC SW module for correct operation. The module is designed to allow almost transparent operation of the MDIO interface, with very little maintenance from the core processor. A single MDIO interface is pinned out to control the PHY configuration and status monitoring. Multiple external PHYs can be controlled by the MDIO interface.

For more detailed information on the MDIO peripheral, see the *3PSW Ethernet Subsystem* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

#### 9.6.3.1 MDIO Peripheral Register Descriptions

**Table 9-27. MDIO Registers**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4A10 0800 | VERSION | MDIO Version |
| 0x4A10 0804 | CONTROL | MDIO Control |
| 0x4A10 0808 | ALIVE | PHY Alive Status |
| 0x4A10 080C | LINK | PHY Link Status |
| 0x4A10 0810 | LINKINTRAW | MDIO Link Status Change Interrupt (Unmasked) |
| 0x4A10 0814 | LINKINTMASKED | MDIO Link Status Change Interrupt (Masked) |
| 0x4A10 0818 - 0x4A10 081C | - | Reserved |
| 0x4A10 0820 | USERINTRAW | MDIO User Command Complete Interrupt (Unmasked) |
| 0x4A10 0824 | USERINTMASKED | MDIO User Command Complete Interrupt (Masked) |
| 0x4A10 0828 | USERINTMASKSET | MDIO User Command Complete Interrupt Mask Set |
| 0x4A10 082C | USERINTMASKCLEAR | MDIO User Command Complete Interrupt Mask Clear |
| 0x4A10 0830 - 0x4A10 087C | - | Reserved |
| 0x4A10 0880 | USERACCESS0 | MDIO User Access 0 |
| 0x4A10 0884 | USERPHYSEL0 | MDIO User PHY Select 0 |
| 0x4A10 0888 | USERACCESS1 | MDIO User Access 1 |
| 0x4A10 088C | USERPHYSEL1 | MDIO User PHY Select 1 |
| 0x4A10 0990 - 0x4A10 08FF | - | Reserved |

#### 9.6.3.2 MDIO Electrical Data/Timing

**Table 9-28. Timing Requirements for MDIO Input**

(see Figure 9-18)

| NO. | | | OPP100/122/166 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{c(MDCLK)}$ | Cycle time, MDCLK | 400 | | ns |
| | $t_{w(MDCLK)}$ | Pulse duration, MDCLK high or low | 180 | | ns |
| 4 | $t_{su(MDIO-MDCLKH)}$ | Setup time, MDIO data input valid before MDCLK high | 20 | | ns |
| 5 | $t_{h(MDCLKH-MDIO)}$ | Hold time, MDIO data input valid after MDCLK high | 0 | | ns |

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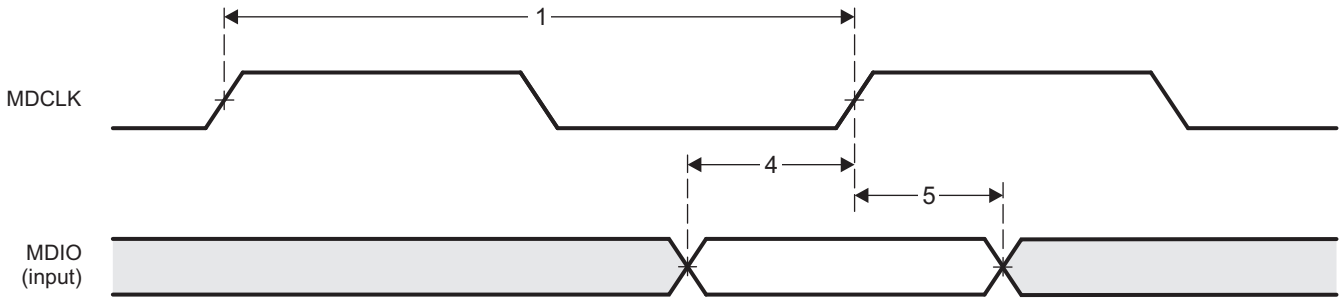


**Figure 9-18. MDIO Input Timing**

**Table 9-29. Switching Characteristics Over Recommended Operating Conditions for MDIO Output**

(see Figure 9-19)

| NO. | PARAMETER | | OPP100/122/1166 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 7 | $t_{d(MDCLKL-MDIO)}$ | Delay time, MDCLK low to MDIO data output valid | | 100 | ns |

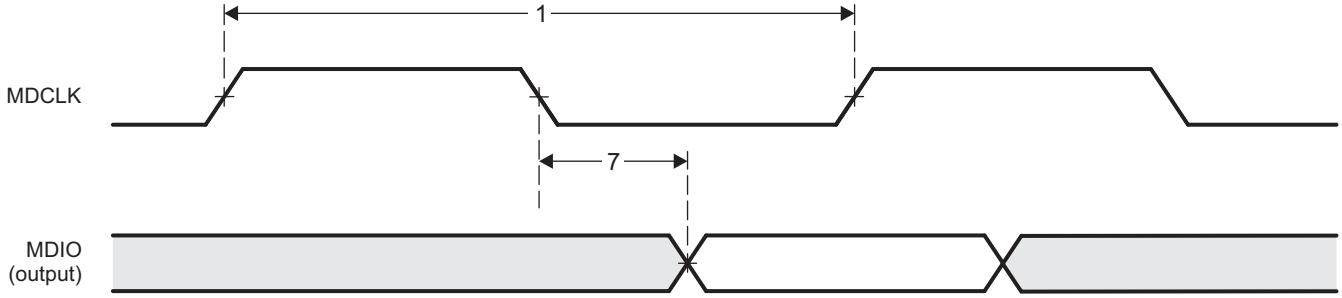


**Figure 9-19. MDIO Output Timing**


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## 9.7 General-Purpose Input/Output (GPIO)

The GPIO peripheral provides general-purpose pins that can be configured as either inputs or outputs. When configured as an output, a write to an internal register controls the state driven on the output pin. When configured as an input, the state of the input is detectable by reading the state of an internal register. In addition, the GPIO peripheral can produce CPU interrupts in different interrupt generation modes. The GPIO peripheral provides generic connections to external devices.

The device contains four GPIO modules and each GPIO module is made up of 32 identical channels.

The device GPIO peripheral supports the following:

- Up to 128 1.8-V/3.3-V GPIO pins, GP0[0:31], GP1[0:31], GP2[0:31], and GP3[0:31] (the exact number available varies as a function of the device configuration). Each channel can be configured to be used in the following applications:
  - Data input/output
  - Keyboard interface with a de-bouncing cell
  - Synchronous interrupt generation (in active mode) upon the detection of external events (signal transitions and/or signal levels).
- Synchronous interrupt requests from each channel are processed by four identical interrupt generation sub-modules to be used independently by the ARM or Media Controller. Interrupts can be triggered by rising and/or falling edge, specified for each interrupt-capable GPIO signal.
- Shared registers can be accessed through "Set and Clear" protocol. Software writes 1 to corresponding bit position or positions to set or to clear the GPIO signal. This allows multiple software processes to toggle GPIO output signals without critical section protection (disable interrupts, program GPIO, re-enable interrupts, to prevent context switching to another process during GPIO programming).
- Separate input/output registers.
- Output register in addition to set/clear so that, if preferred by software, some GPIO output signals can be toggled by direct write to the output register.
- Output register, when read, reflects output drive status. This, in addition to the input register reflecting pin status and open-drain I/O cell, allows wired logic to be implemented.

For more detailed information on GPIOs, see the *General-Purpose I/O (GPIO) Interface* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

### 9.7.1 GPIO Peripheral Register Descriptions

**Table 9-30. GPIO Registers**

| HEX ADDRESS | | | | | |
|---|---|---|---|---|---|
| GPIO0 | GPIO1 | GPIO2 | GPIO3 | ACRONYM | REGISTER NAME |
| 0x4803 2000 | 0x4804 C000 | 0x481A C000 | 0x481A E000 | GPIO_REVISION | GPIO Revision |
| 0x4803 2010 | 0x4804 C010 | 0x481A C010 | 0x481A E010 | GPIO_SYSCONFIG | System Configuration |
| 0x4803 2020 | 0x4804 C020 | 0x481A C020 | 0x481A E020 | GPIO_EOI | End of Interrupt |
| 0x4803 2024 | 0x4804 C024 | 0x481A C024 | 0x481A E024 | GPIO_IRQSTATUS_RAW_0 | Status Raw for Interrupt 1 |
| 0x4803 2028 | 0x4804 C028 | 0x481A C028 | 0x481A E028 | GPIO_IRQSTATUS_RAW_1 | Status Raw for Interrupt 2 |
| 0x4803 202C | 0x4804 C02C | 0x481A C02C | 0x481A E02C | GPIO_IRQSTATUS_0 | Status for Interrupt 1 |
| 0x4803 2030 | 0x4804 C030 | 0x481A C030 | 0x481A E030 | GPIO_IRQSTATUS_1 | Status for Interrupt 2 |
| 0x4803 2034 | 0x4804 C034 | 0x481A C034 | 0x481A E034 | GPIO_IRQSTATUS_SET_0 | Enable Set for Interrupt 1 |

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**Table 9-30. GPIO Registers (continued)**

| HEX ADDRESS | | | | | |
|---|---|---|---|---|---|
| GPIO0 | GPIO1 | GPIO2 | GPIO3 | ACRONYM | REGISTER NAME |
| 0x4803 2038 | 0x4804 C038 | 0x481A C038 | 0x481A E038 | GPIO_IRQSTATUS_SET_1 | Enable Set for Interrupt 2 |
| 0x4803 203C | 0x4804 C03C | 0x481A C03C | 0x481A E03C | GPIO_IRQSTATUS_CLR_0 | Enable Clear for Interrupt 1 |
| 0x4803 2040 | 0x4804 C040 | 0x481A C040 | 0x481A E040 | GPIO_IRQSTATUS_CLR_1 | Enable Clear for Interrupt 2 |
| 0x4803 2044 | 0x4804 C044 | 0x481A C044 | 0x481A E044 | GPIO_IRQWAKEN_0 | Wakeup Enable for Interrupt 1 |
| 0x4803 2048 | 0x4804 C048 | 0x481A C048 | 0x481A E048 | GPIO_IRQWAKEN_1 | Wakeup Enable for Interrupt 2 |
| 0x4803 2114 | 0x4804 C114 | 0x481A C114 | 0x481A E114 | GPIO_SYSSTATUS | System Status |
| 0x4803 2130 | 0x4804 C130 | 0x481A C130 | 0x481A E130 | GPIO_CTRL | Module Control |
| 0x4803 2134 | 0x4804 C134 | 0x481A C134 | 0x481A E134 | GPIO_OE | Output Enable |
| 0x4803 2138 | 0x4804 C138 | 0x481A C138 | 0x481A E138 | GPIO_DATAIN | Data Input |
| 0x4803 213C | 0x4804 C13C | 0x481A C13C | 0x481A E13C | GPIO_DATAOUT | Data Output |
| 0x4803 2140 | 0x4804 C140 | 0x481A C140 | 0x481A E140 | GPIO_LEVELDETECT0 | Detect Low Level |
| 0x4803 2144 | 0x4804 C144 | 0x481A C144 | 0x481A E144 | GPIO_LEVELDETECT1 | Detect High Level |
| 0x4803 2148 | 0x4804 C148 | 0x481A C148 | 0x481A E148 | GPIO_RISINGDETECT | Detect Rising Edge |
| 0x4803 214C | 0x4804 C14C | 0x481A C14C | 0x481A E14C | GPIO_FALLINGDETECT | Detect Falling Edge |
| 0x4803 2150 | 0x4804 C150 | 0x481A C150 | 0x481A E150 | GPIO_DEBOUNCENABLE | Debouncing Enable |
| 0x4803 2154 | 0x4804 C154 | 0x481A C154 | 0x481A E154 | GPIO_DEBOUNCINGTIME | Debouncing Value |
| 0x4803 2190 | 0x4804 C190 | 0x481A C190 | 0x481A E190 | GPIO_CLEARDATAOUT | Clear Data Output |
| 0x4803 2194 | 0x4804 C194 | 0x481A C194 | 0x481A E194 | GPIO_SETDATAOUT | Set Data Output |


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### 9.7.2 GPIO Electrical Data/Timing

**Table 9-31. Timing Requirements for GPIO Inputs**

(see Figure 9-20)

| NO. | | | OPP100/122/166 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{w(GPIH)}$ | Pulse duration, GPx[31:0] input high | 12P(1) | | ns |
| 2 | $t_{w(GPIL)}$ | Pulse duration, GPx[31:0] input low | 12P(1) | | ns |

(1) P = Module clock.

**Table 9-32. Switching Characteristics Over Recommended Operating Conditions for GPIO Outputs**

(see Figure 9-20)

| NO. | PARAMETER | | OPP100/122/166 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 3 | $t_{w(GPOH)}$ | Pulse duration, GPx[31:0] output high | 36P-8(1) | | ns |
| 4 | $t_{w(GPOL)}$ | Pulse duration, GPx[31:0] output low | 36P-8(1) | | ns |

(1) P = Module clock.

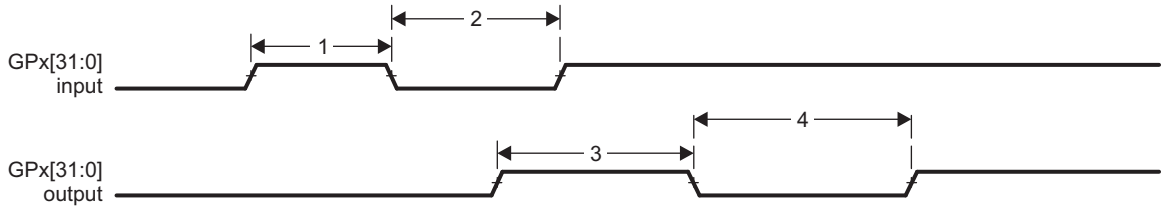


**Figure 9-20. GPIO Port Timing**

## 9.8 General-Purpose Memory Controller (GPMC) and Error Location Module (ELM)

The GPMC is a device memory controller used to provide a glueless interface to external memory devices such as NOR Flash, NAND Flash (with BCH and Hamming Error Code Detection for 8-bit or 16-bit NAND Flash), SRAM, and Pseudo-SRAM. The GPMC includes flexible asynchronous protocol control for interface to SRAM-like memories and custom logic (FPGA, CPLD, ASICs, etc.).

Other supported features include:

- 8-/16-bit wide multiplexed address/data bus
- 512 MBytes maximum addressing capability divided among up to eight chip selects
- Non-multiplexed address/data mode
- Pre-fetch and write posting engine associated with system DMA to get full performance from NAND device with minimum impact on NOR/SRAM concurrent access.

The device also contains an Error Locator Module (ELM) which is used to extract error addresses from syndrome polynomials generated using a BCH algorithm. Each of these polynomials gives a status of the read operations for a 512 bytes block from a NAND flash and its associated BCH parity bits, plus optionally spare area information. The ELM has the following features:

- 4-bit, 8-bit and 16-bit per 512byte block error location based on BCH algorithms
- Eight simultaneous processing contexts
- Page-based and continuous modes
- Interrupt generation on error location process completion
  - When the full page has been processed in page mode
  - For each syndrome polynomial in continuous mode


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### 9.8.1 GPMC and ELM Peripherals Register Descriptions

**Table 9-33. GPMC Registers**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x5000 0000 | GPMC_REVISION | GPMC Revision |
| 0x5000 0010 | GPMC_SYSCONFIG | System Configuration |
| 0x5000 0014 | GPMC_SYSSTATUS | System Status |
| 0x5000 0018 | GPMC_IRQSTATUS | Status for Interrupt |
| 0x5000 001C | GPMC_IRQENABLE | Interrupt Enable |
| 0x5000 0040 | GPMC_TIMEOUT_CONTROL | Timeout Counter Start Value |
| 0x5000 0044 | GPMC_ERR_ADDRESS | Error Address |
| 0x5000 0048 | GPMC_ERR_TYPE | Error Type |
| 0x5000 0050 | GPMC_CONFIG | GPMC Global Configuration |
| 0x5000 0054 | GPMC_STATUS | GPMC Global Status |
| 0x5000 0060 + (0x0000 0030 * i)(1) | GPMC_CONFIG1_0 - GPMC_CONFIG1_7 | Parameter Configuration 1_0-7 |
| 0x5000 0064 + (0x0000 0030 * i)(1) | GPMC_CONFIG2_0 - GPMC_CONFIG2_7 | Parameter Configuration 2_0-7 |
| 0x5000 0068 + (0x0000 0030 * i)(1) | GPMC_CONFIG3_0 - GPMC_CONFIG3_7 | Parameter Configuration 3_0-7 |
| 0x5000 006C + (0x0000 0030 * i)(1) | GPMC_CONFIG4_0 - GPMC_CONFIG4_7 | Parameter Configuration 4_0-7 |
| 0x5000 0070 + (0x0000 0030 * i)(1) | GPMC_CONFIG5_0 - GPMC_CONFIG5_7 | Parameter Configuration 5_0-7 |
| 0x5000 0074 + (0x0000 0030 * i)(1) | GPMC_CONFIG6_0 - GPMC_CONFIG6_7 | Parameter Configuration 6_0-7 |
| 0x5000 0078 + (0x0000 0030 * i)(1) | GPMC_CONFIG7_0 - GPMC_CONFIG7_7 | Parameter Configuration 7_0-7 |
| 0x5000 007C + (0x0000 0030 * i)(1) | GPMC_NAND_COMMAND_0 - GPMC_NAND_COMMAND_7 | NAND Command 0-7 |
| 0x5000 0080 + (0x0000 0030 * i)(1) | GPMC_NAND_ADDRESS_0 - GPMC_NAND_ADDRESS_7 | NAND Address 0-7 |
| 0x5000 0084 + (0x0000 0030 * i)(1) | GPMC_NAND_DATA_0 - GPMC_NAND_DATA_7 | NAND Data 0-7 |
| 0x5000 01E0 | GPMC_PREFETCH_CONFIG1 | Prefetch Configuration 1 |
| 0x5000 01E4 | GPMC_PREFETCH_CONFIG2 | Prefetch Configuration 2 |
| 0x5000 01EC | GPMC_PREFETCH_CONTROL | Prefetch Control |
| 0x5000 01F0 | GPMC_PREFETCH_STATUS | Prefetch Status |
| 0x5000 01F4 | GPMC_ECC_CONFIG | ECC Configuration |
| 0x5000 01F8 | GPMC_ECC_CONTROL | ECC Control |
| 0x5000 01FC | GPMC_ECC_SIZE_CONFIG | ECC Size Configuration |
| 0x5000 0200 + (0x0000 0004 * j)(2) | GPMC_ECC0_RESULT - GPMC_ECC8_RESULT | ECC0-8 Result |
| 0x5000 0240 + (0x0000 0010 * i)(1) | GPMC_BCH_RESULT0_0 - GPMC_BCH_RESULT0_7 | BCH Result 0_0-7 |
| 0x5000 0244 + (0x0000 0010 * i)(1) | GPMC_BCH_RESULT1_0 - GPMC_BCH_RESULT1_7 | BCH Result 1_0-7 |
| 0x5000 0248 + (0x0000 0010 * i)(1) | GPMC_BCH_RESULT2_0 - GPMC_BCH_RESULT2_7 | BCH Result 2_0-7 |
| 0x5000 024C + (0x0000 0010 * i)(1) | GPMC_BCH_RESULT3_0 - GPMC_BCH_RESULT3_7 | BCH Result 3_0-7 |
| 0x5000 0300 + (0x0000 0010 * i)(1) | GPMC_BCH_RESULT4_0 - GPMC_BCH_RESULT4_7 | BCH Result 4_0-7 |

(1) i = 0 to 7
(2) j = 0 to 8

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**Table 9-33. GPMC Registers (continued)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x5000 0304 + (0x0000 0010 * i)[1] | GPMC_BCH_RESULT5_0 - GPMC_BCH_RESULT5_7 | BCH Result 5_0-7 |
| 0x5000 0308 + (0x0000 0010 * i)[1] | GPMC_BCH_RESULT6_0 - GPMC_BCH_RESULT6_7 | BCH Result 6_0-7 |
| 0x5000 02D0 | GPMC_BCH_SWDATA | BCH Data |


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## 9.8.2 GPMC Electrical Data/Timing

### 9.8.2.1 GPMC/NOR Flash Interface Synchronous Mode Timing (Non-Multiplexed and Multiplexed Modes)

**Table 9-34. Timing Requirements for GPMC/NOR Flash Interface - Synchronous Mode**

(see Figure 9-21, Figure 9-22, Figure 9-23 for Non-Multiplexed Modes)
(see Figure 9-24, Figure 9-25, Figure 9-26 for Multiplexed Modes)

| NO. | | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 13 | $t_{su(DV-CLKH)}$ | Setup time, read GPMC_D[15:0] valid before GPMC_CLK high | 4 | | ns |
| 14 | $t_{h(CLKH-DV)}$ | Hold time, read GPMC_D[15:0] valid after GPMC_CLK high | 3 | | ns |
| 22 | $t_{su(WAITV-CLKH)}$ | Setup time, GPMC_WAIT[x] valid before GPMC_CLK high | 4 | | ns |
| 23 | $t_{h(CLKH-WAITV)}$ | Hold time, GPMC_WAIT[x] valid after GPMC_CLK high | 3 | | ns |

**Table 9-35. Switching Characteristics Over Recommended Operating Conditions for GPMC/NOR Flash Interface - Synchronous Mode**

(see Figure 9-21, Figure 9-22, Figure 9-23 for Non-Multiplexed Modes)
(see Figure 9-24, Figure 9-25, Figure 9-26 for Multiplexed Modes)

| NO. | PARAMETER | | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| 1 | $t_{c(CLK)}$ | Cycle time, output clock GPMC_CLK period | | 20[1] | | ns |
| 2 | $t_{w(CLKH)}$ | Pulse duration, output clock GPMC_CLK high | | 0.5P[2] | | ns |
| | $t_{w(CLKL)}$ | Pulse duration, output clock GPMC_CLK low | | 0.5P[2] | | |
| 3 | $t_{d(CLKH-nCSV)}$ | Delay time, GPMC_CLK rising edge to $\overline{\text{GPMC_CS[x]}}$ transition | | F - 3[3] | F + 6[3] | ns |
| 4 | $t_{d(CLKH-nCSIV)}$ | Delay time, GPMC_CLK rising edge to $\overline{\text{GPMC_CS[x]}}$ invalid | | E - 3[4] | E + 6[4] | ns |
| 5 | $t_{d(ADDV-CLK)}$ | Delay time, GPMC_A[27:0] address bus valid to GPMC_CLK first edge | MUX0 and Non-Multi Muxed pins | B - 6[5] | B + 6[5] | ns |
| | | | MUX1 for GPMC_A[15:0] | B - 10[5] | B + 6[5] | |
| | | | MUX1/2 for GPMC_A[27:20] | B - 10[5] | B + 6[5] | |
| | | | GPMC_AD[15:0] | B - 10[5] | B + 6[5] | |
| 6 | $t_{d(CLKH-ADDIV)}$ | Delay time, GPMC_CLK rising edge to GPMC_A[27:0] GPMC address bus invalid | MUX0 and Non-Multi Muxed pins | -3 | | ns |
| | | | MUX1 for GPMC_A[15:0] | -6 | | |
| | | | MUX1/2 for GPMC_A[27:20] | -6 | | |
| | | | GPMC_AD[15:0] | -6 | | |
| 7 | $t_{d(nBEV-CLK)}$ | Delay time, GPMC_$\overline{\text{BE0}}$_CLE, $\overline{\text{GPMC_BE1}}$ valid to GPMC_CLK first edge | | B - 3[5] | B + 3[5] | ns |

(1) Sync mode can operate at 50 MHz max.
(2) P = GPMC_CLK period.
(3) For nCS falling edge (CS activated):
- For GpmcFCLKDivider = 0:
  F = 0.5 * CSExtraDelay * GPMC_FCLK
- For GpmcFCLKDivider = 1:
  F = 0.5 * CSExtraDelay * GPMC_FCLK if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)
  F = (1 + 0.5 * CSExtraDelay) * GPMC_FCLK otherwise
- For GpmcFCLKDivider = 2:
  F = 0.5 * CSExtraDelay * GPMC_FCLK if ((CSOnTime – ClkActivationTime) is a multiple of 3)
  F = (1 + 0.5 * CSExtraDelay) * GPMC_FCLK if ((CSOnTime – ClkActivationTime – 1) is a multiple of 3)
  F = (2 + 0.5 * CSExtraDelay) * GPMC_FCLK if ((CSOnTime – ClkActivationTime – 2) is a multiple of 3)

(4) For single read: E = (CSRdOffTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: E = (CSRdOffTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst write: E = (CSWrOffTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
(5) B = ClkActivationTime * GPMC_FCLK

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**Table 9-35. Switching Characteristics Over Recommended Operating Conditions for GPMC/NOR Flash Interface - Synchronous Mode (continued)**

(see Figure 9-21, Figure 9-22, Figure 9-23 for Non-Multiplexed Modes)
(see Figure 9-24, Figure 9-25, Figure 9-26 for Multiplexed Modes)

| NO. | PARAMETER | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 8 | $t_{d(CLKH-nBEIV)}$ | Delay time, GPMC_CLK rising edge to GPMC_$\overline{BE0}$_CLE, $\overline{GPMC_BE1}$ invalid | D - 3(6) | D + 3(6) | ns |
| 9 | $t_{d(CLKH-nADV)}$ | Delay time, GPMC_CLK rising edge to GPMC_$\overline{ADV}$_ALE transition | G - 3(7) | G + 6(7) | ns |
| 10 | $t_{d(CLKH-nADVIV)}$ | Delay time, GPMC_CLK rising edge to GPMC_$\overline{ADV}$_ALE invalid | D - 3(6) | D + 6(6) | ns |
| 11 | $t_{d(CLKH-nOE)}$ | Delay time, GPMC_CLK rising edge to $\overline{GPMC_OE_RE}$ transition | H - 3(8) | H + 5(8) | ns |

(6) For single read: D = (RdCycleTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: D = (RdCycleTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst write: D = (WrCycleTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(7) For ADV falling edge (ADV activated):
- Case GpmcFCLKDivider = 0:
  G = 0.5 * ADVExtraDelay * GPMC_FCLK
- Case GpmcFCLKDivider = 1:
  G = 0.5 * ADVExtraDelay * GPMC_FCLK if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
  G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK otherwise
- Case GpmcFCLKDivider = 2:
  G = 0.5 * ADVExtraDelay * GPMC_FCLK if ((ADVOnTime – ClkActivationTime) is a multiple of 3)
  G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVOnTime – ClkActivationTime – 1) is a multiple of 3)
  G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVOnTime – ClkActivationTime – 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Reading mode:
- Case GpmcFCLKDivider = 0:
  G = 0.5 * ADVExtraDelay * GPMC_FCLK
- Case GpmcFCLKDivider = 1:
  G = 0.5 * ADVExtraDelay * GPMC_FCLK if (ClkActivationTime and ADVRdOffTime are odd) or (ClkActivationTime and ADVRdOffTime are even)
  G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK otherwise
- Case GpmcFCLKDivider = 2:
  G = 0.5 * ADVExtraDelay * GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime) is a multiple of 3)
  G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime – 1) is a multiple of 3)
  G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime – 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Writing mode:
- Case GpmcFCLKDivider = 0:
  G = 0.5 * ADVExtraDelay * GPMC_FCLK
- Case GpmcFCLKDivider = 1:
  G = 0.5 * ADVExtraDelay * GPMC_FCLK if (ClkActivationTime and ADVWrOffTime are odd) or (ClkActivationTime and ADVWrOffTime are even)
  G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK otherwise
- Case GpmcFCLKDivider = 2:
  G = 0.5 * ADVExtraDelay * GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime) is a multiple of 3)
  G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime – 1) is a multiple of 3)
  G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime – 2) is a multiple of 3)

(8) For OE falling edge (OE activated) / IO DIR rising edge (IN direction) :
- Case GpmcFCLKDivider = 0:
  H = 0.5 * OEExtraDelay * GPMC_FCLK
- Case GpmcFCLKDivider = 1:
  H = 0.5 * OEExtraDelay * GPMC_FCLK if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)
  H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK otherwise
- Case GpmcFCLKDivider = 2:
  H = 0.5 * OEExtraDelay * GPMC_FCLK if ((OEOnTime – ClkActivationTime) is a multiple of 3)
  H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOnTime – ClkActivationTime – 1) is a multiple of 3)
  H = (2 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOnTime – ClkActivationTime – 2) is a multiple of 3)

For OE rising edge (OE deactivated):
- Case GpmcFCLKDivider = 0:
  H = 0.5 * OEExtraDelay * GPMC_FCLK
- Case GpmcFCLKDivider = 1:
  H = 0.5 * OEExtraDelay * GPMC_FCLK if (ClkActivationTime and OEOffTime are odd) or (ClkActivationTime and OEOffTime are even)
  H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK otherwise
- Case GpmcFCLKDivider = 2:
  H = 0.5 * OEExtraDelay * GPMC_FCLK if ((OEOffTime – ClkActivationTime) is a multiple of 3)
  H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOffTime – ClkActivationTime – 1) is a multiple of 3)
  H = (2 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOffTime – ClkActivationTime – 2) is a multiple of 3)


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**Table 9-35. Switching Characteristics Over Recommended Operating Conditions for GPMC/NOR Flash Interface - Synchronous Mode (continued)**

(see Figure 9-21, Figure 9-22, Figure 9-23 for Non-Multiplexed Modes)
(see Figure 9-24, Figure 9-25, Figure 9-26 for Multiplexed Modes)

| NO. | PARAMETER | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 12 | $t_{d(CLKH-nOEIV)}$ | Delay time, GPMC_CLK rising edge to $\overline{GPMC_OE_RE}$ invalid | E - 3 (4) | E + 5 (4) | ns |
| 15 | $t_{d(CLKH-nWE)}$ | Delay time, GPMC_CLK rising edge to $\overline{GPMC_WE}$ transition | I - 3 (9) | I + 6 (9) | ns |
| 16 | $t_{d(CLKH-Data)}$ | Delay time, GPMC_CLK rising edge to GPMC_D[15:0] data bus transition | J - 3 (10) | J + 3 (10) | ns |
| 18 | $t_{d(CLKH-nBE)}$ | Delay time, GPMC_CLK rising edge to GPMC_$\overline{BE0}$_CLE, $\overline{GPMC_BE1}$ transition | J - 3 (10) | J + 3 (10) | ns |
| 19 | $t_{w(nCSV)}$ | Pulse duration, $\overline{GPMC_CS[x]}$ low | A (11) | | ns |
| 20 | $t_{w(nBEV)}$ | Pulse duration, GPMC_$\overline{BE0}$_CLE, $\overline{GPMC_BE1}$ low | C (12) | | ns |
| 21 | $t_{w(nADVV)}$ | Pulse duration, GPMC_$\overline{ADV}$_ALE low | K (13) | | ns |

(9) For WE falling edge (WE activated):
- Case GpmcFCLKDivider = 0:
  I = 0.5 * WEExtraDelay * GPMC_FCLK
- Case GpmcFCLKDivider = 1:
  I = 0.5 * WEExtraDelay * GPMC_FCLK if (ClkActivationTime and WEOnTime are odd) or (ClkActivationTime and WEOnTime are even)
  I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK otherwise
- Case GpmcFCLKDivider = 2:
  I = 0.5 * WEExtraDelay * GPMC_FCLK if ((WEOnTime – ClkActivationTime) is a multiple of 3)
  I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOnTime – ClkActivationTime – 1) is a multiple of 3)
  I = (2 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOnTime – ClkActivationTime – 2) is a multiple of 3)

For WE rising edge (WE deactivated):
- Case GpmcFCLKDivider = 0:
  I = 0.5 * WEExtraDelay * GPMC_FCLK
- Case GpmcFCLKDivider = 1:
  I = 0.5 * WEExtraDelay * GPMC_FCLK if (ClkActivationTime and WEOffTime are odd) or (ClkActivationTime and WEOffTime are even)
  I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK otherwise
- Case GpmcFCLKDivider = 2:
  I = 0.5 * WEExtraDelay * GPMC_FCLK if ((WEOffTime – ClkActivationTime) is a multiple of 3)
  I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOffTime – ClkActivationTime – 1) is a multiple of 3)
  I = (2 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOffTime – ClkActivationTime – 2) is a multiple of 3)

(10) J = GPMC_FCLK period.

(11) For single read: A = (CSRdOffTime - CSOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK period
For burst read: A = (CSRdOffTime - CSOnTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK period [n = page burst access number]
For burst write: A = (CSWrOffTime - CSOnTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK period [n = page burst access number]

(12) For single read: C = RdCycleTime * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: C = (RdCycleTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK [n = page burst access number]
For Burst write: C = (WrCycleTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK [n = page burst access number]

(13) For read: K = (ADVRdOffTime - ADVOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For write: K = (ADVWrOffTime - ADVOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK

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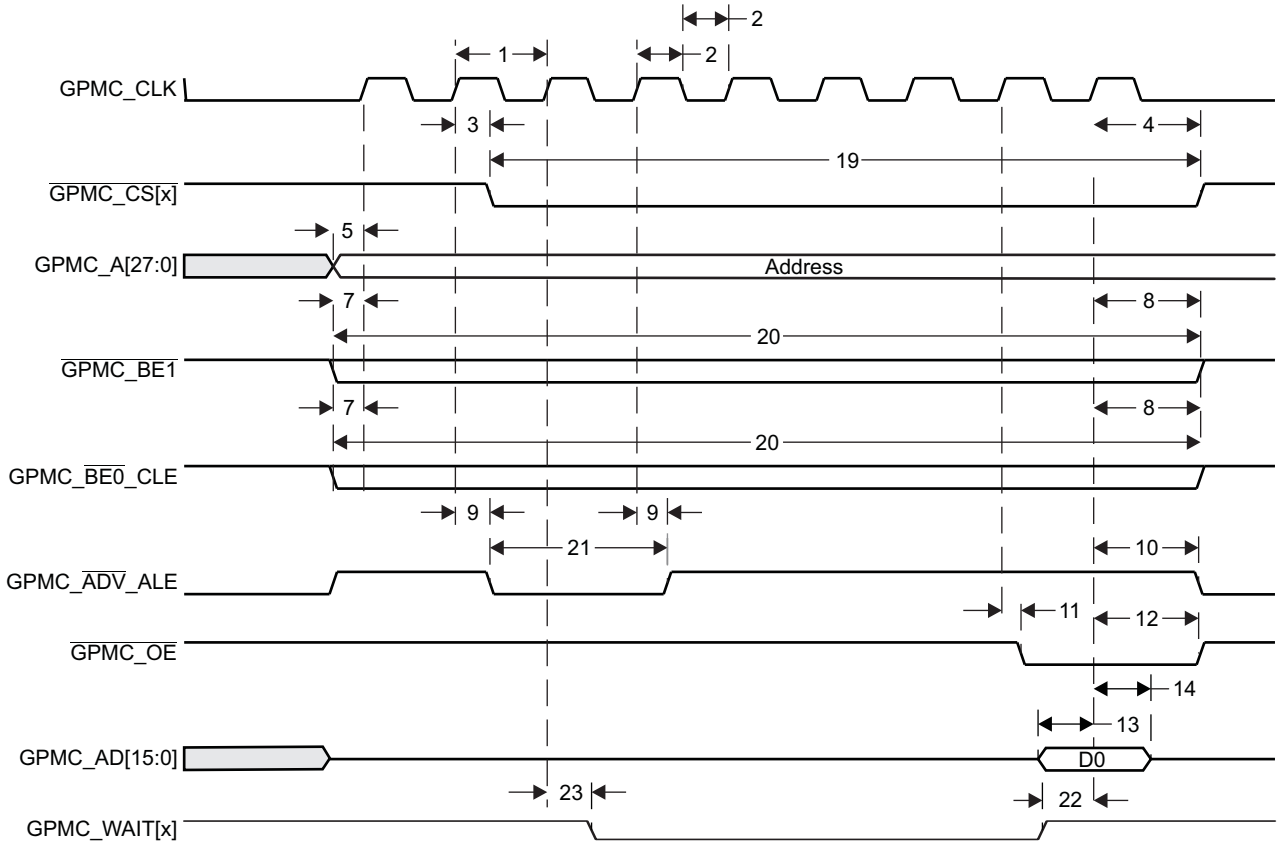


**Figure 9-21. GPMC Non-Multiplexed NOR Flash - Synchronous Single Read (GPMCFCLKDIVIDER = 0)**

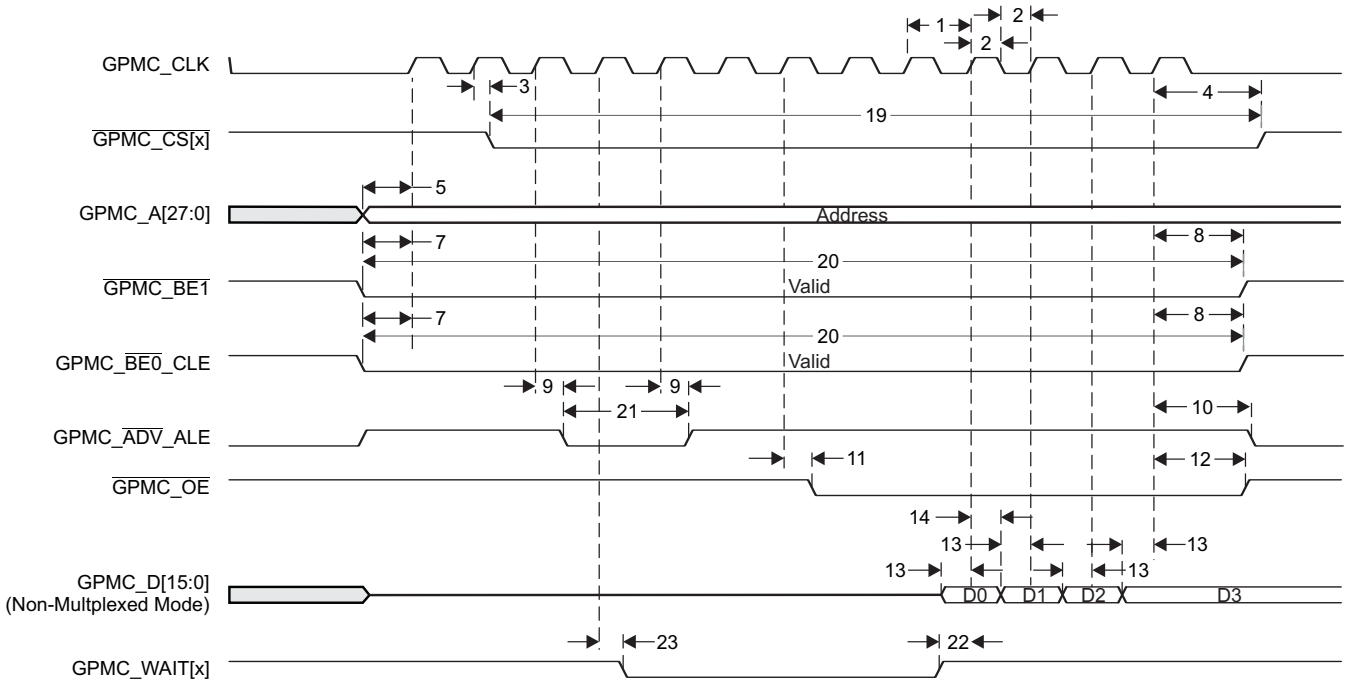


**Figure 9-22. GPMC Non-Multiplexed NOR Flash - 14x16-bit Synchronous Burst Read (GPMCFCLKDIVIDER = 0)**


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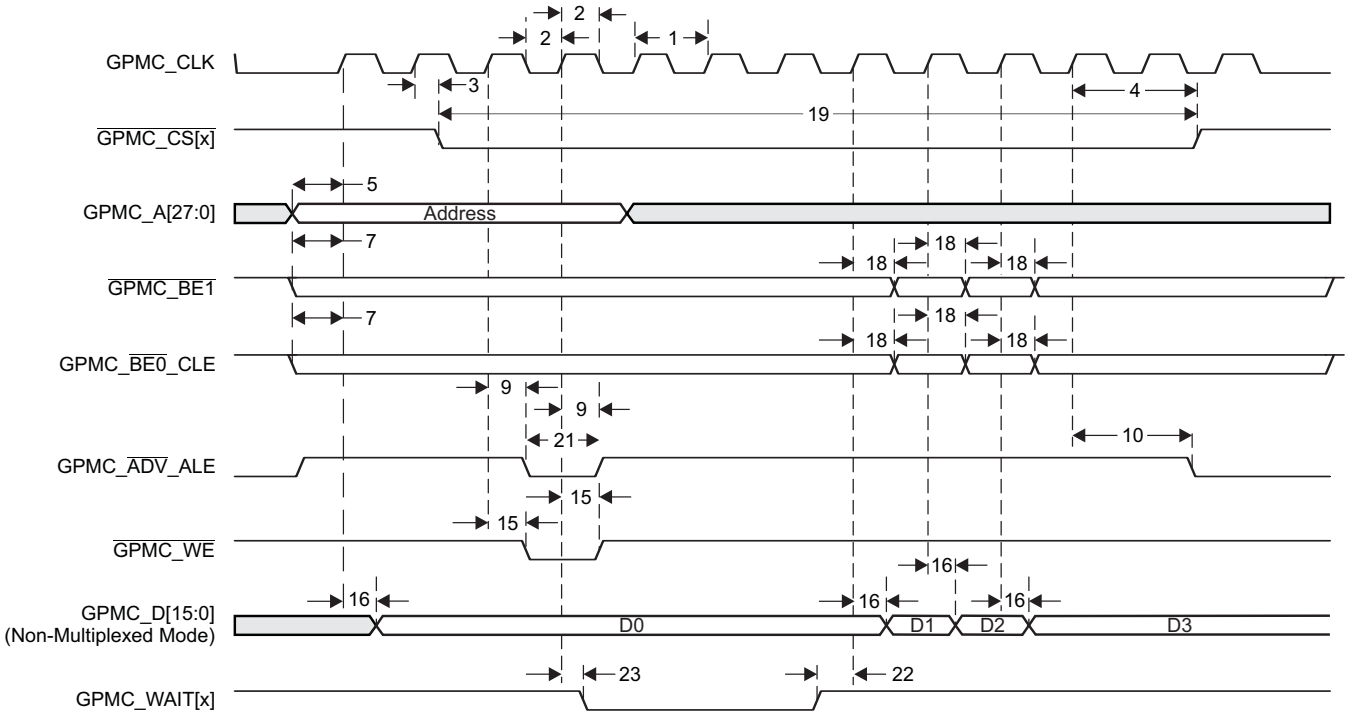


**Figure 9-23. GPMC Non-Multiplexed NOR Flash - Synchronous Burst Write (GPMCFCLKDIVIDER = 0)**

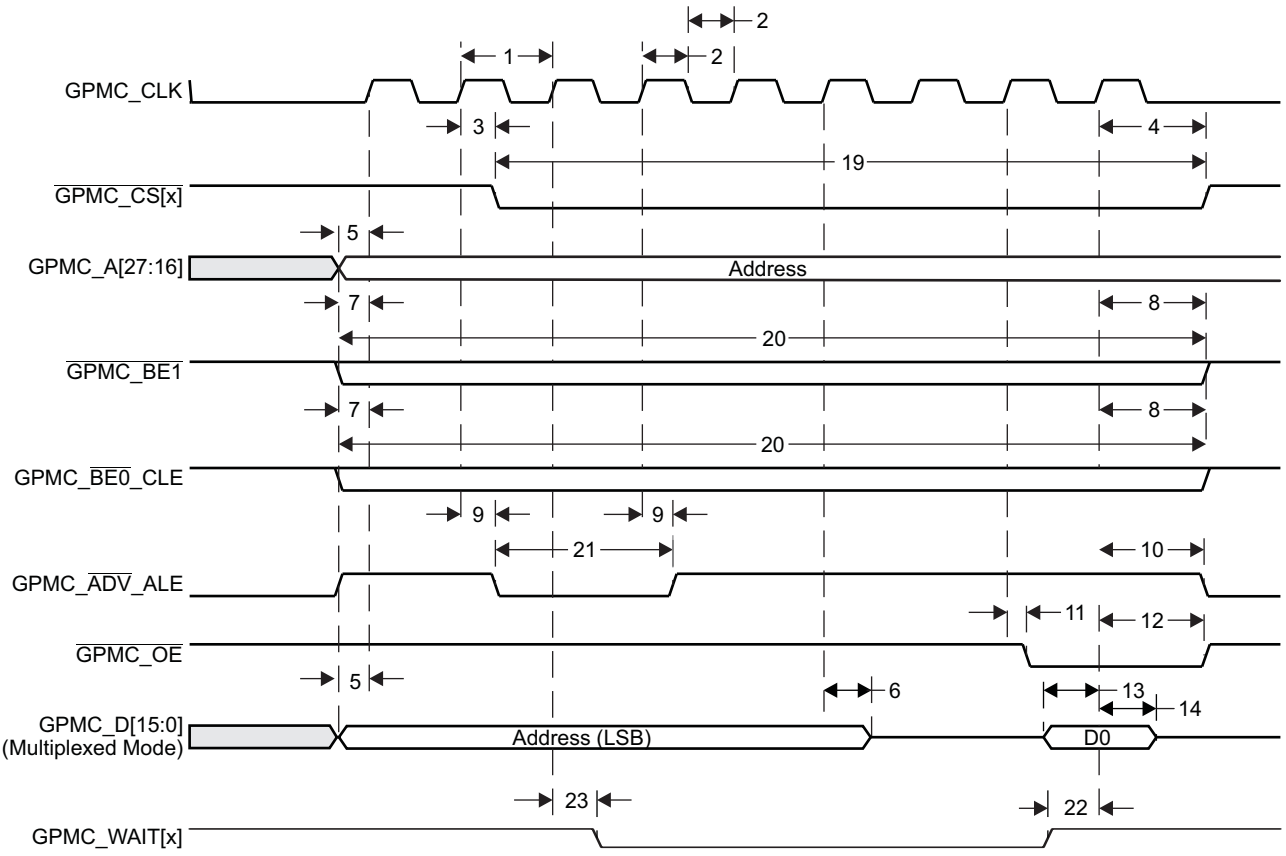


**Figure 9-24. GPMC Multiplexed NOR Flash - Synchronous Single Read (GPMCFCLKDIVIDER = 0)**

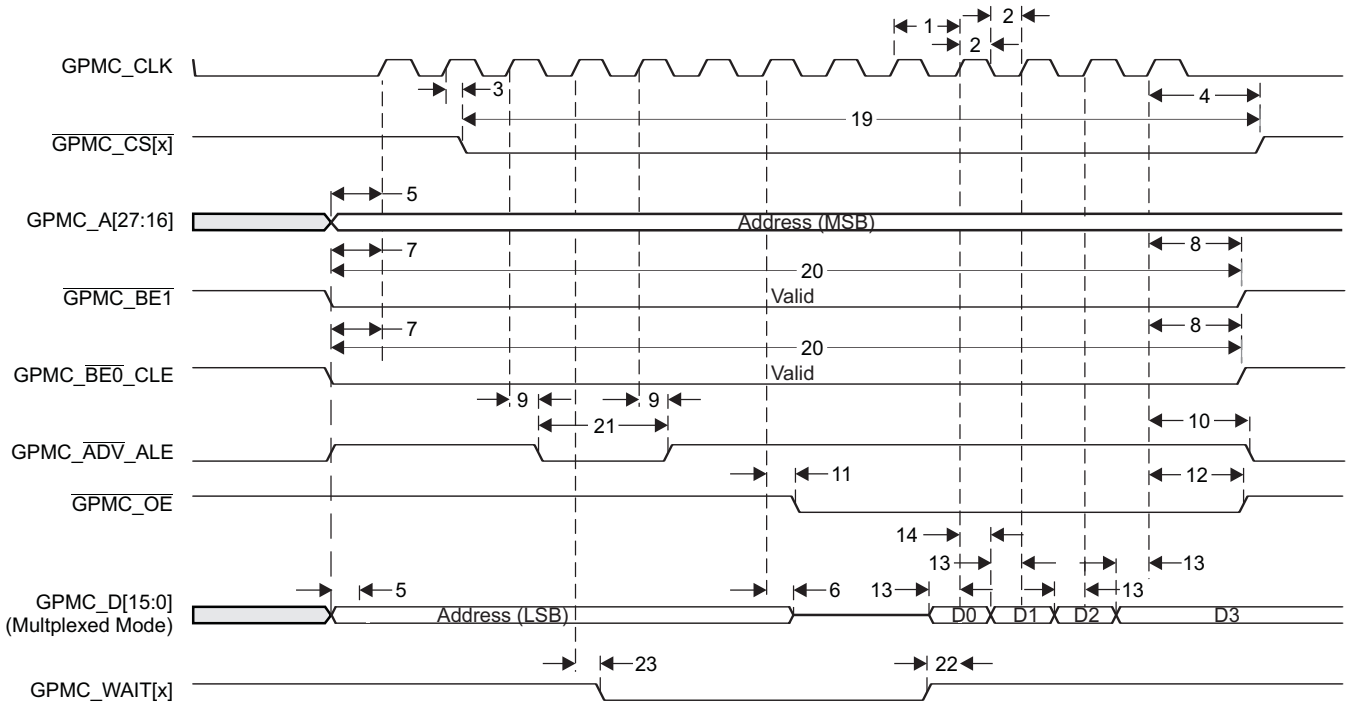


**Figure 9-25. GPMC Multiplexed NOR Flash - 14x16-bit Synchronous Burst Read (GPMCFCLKDIVIDER = 0)**

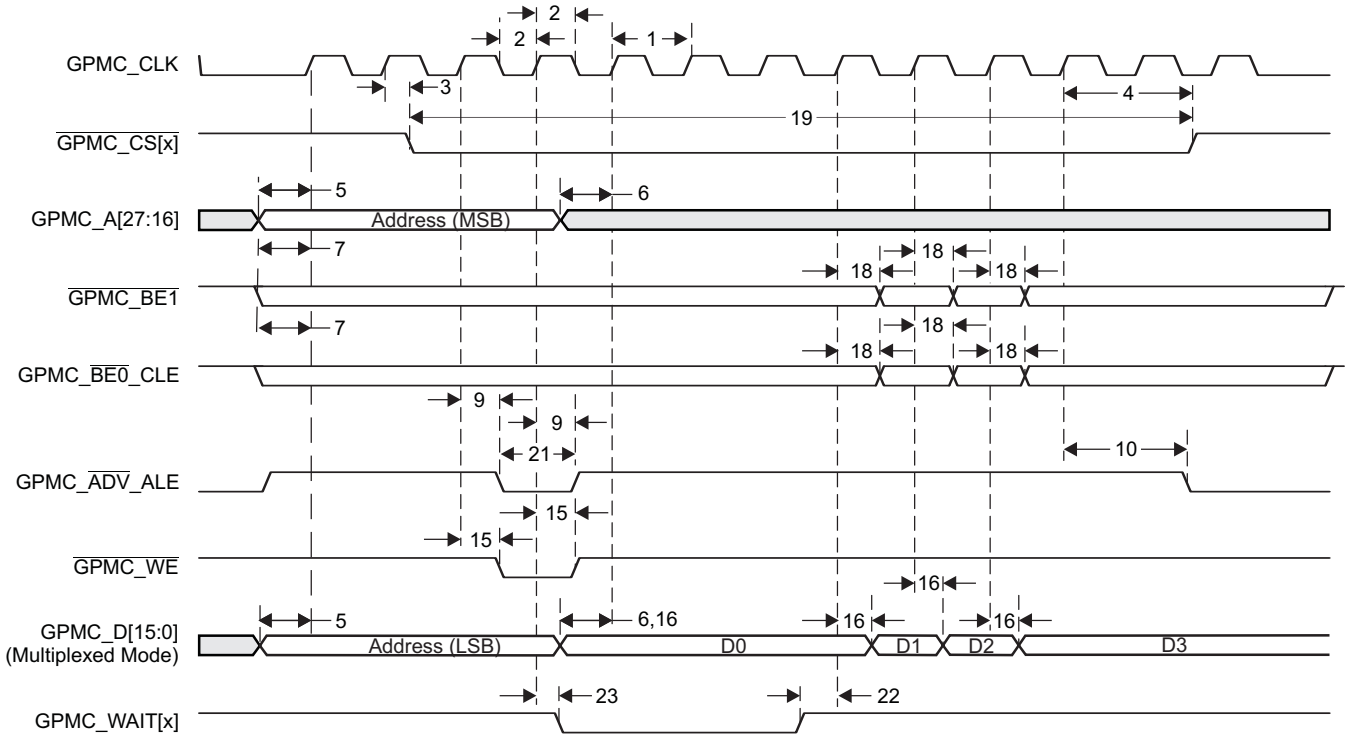


**Figure 9-26. GPMC Non-Multiplexed NOR Flash - Synchronous Burst Write (GPMCFCLKDIVIDER = 0)**

### 9.8.2.2 GPMC/NOR Flash Interface Asynchronous Mode Timing (Non-Multiplexed and Multiplexed Modes)


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### Table 9-36. Timing Requirements for GPMC/NOR Flash Interface - Asynchronous Mode[1]

(see Figure 9-27, Figure 9-28 for Non-Multiplexed Mode )
(see Figure 9-29, Figure 9-31 for Multiplexed Mode)

| NO. | | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 6 | $t_{acc(DAT)}$ | Data maximum access time (GPMC_FCLK cycles) | | H[2] | cycles |
| 21 | $t_{acc1\text{-}pgmode(DAT)}$ | Page mode successive data maximum access time (GPMC_FCLK cycles) | | P[3] | cycles |
| 22 | $t_{acc2\text{-}pgmode(DAT)}$ | Page mode first data maximum access time (GPMC_FCLK cycles) | | H[2] | cycles |

(1) The internal GPMC_FCLK is equal to SYSCLK6, and is nominally 100 MHz or 10 ns. For any additional constraints, see the *Clocking* section of this document.
(2) H = AccessTime * (TimeParaGranularity + 1)
(3) P = PageBurstAccessTime * (TimeParaGranularity + 1).

### Table 9-37. Switching Characteristics Over Recommended Operating Conditions for GPMC/NOR Flash Interface - Asynchronous Mode

(see Figure 9-27, Figure 9-28, Figure 9-29, Figure 9-30 for Non-Multiplexed Modes)
(see Figure 9-31, Figure 9-32 for Multiplexed Modes)

| NO. | PARAMETER | | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| 1 | $t_{w(nBEV)}$ | Pulse duration, GPMC_$\overline{BE0}$_CLE, $\overline{GPMC_BE1}$ valid time | | | N[1] | ns |
| 2 | $t_{w(nCSV)}$ | Pulse duration, $\overline{GPMC_CS[x]}$ low | | | A[2] | ns |
| 4 | $t_{d(nCSV\text{-}nADVIV)}$ | Delay time, $\overline{GPMC_CS[x]}$ valid to GPMC_NADV_ALE invalid | | B - 2[3] | B + 4[3] | ns |
| 5 | $t_{d(nCSV\text{-}nOEIV)}$ | Delay time, $\overline{GPMC_CS[x]}$ valid to $\overline{GPMC_OE_RE}$ invalid (single read) | | C - 2[4] | C + 4[4] | ns |
| 10 | $t_{d(AV\text{-}nCSV)}$ | Delay time, GPMC_A[27:0] address bus valid to $\overline{GPMC_CS[x]}$ valid | MUX0 and Non-Multi Muxed pins | J - 2[5] | J + 4[5] | ns |
| | | | MUX1 for GPMC_A[15:0] | J - 2[5] | J + 4[5] | ns |
| | | | MUX1/2 for GPMC_A[27:20] | J - 2[5] | J + 4[5] | ns |
| 11 | $t_{d(nBEV\text{-}nCSV)}$ | Delay time, GPMC_$\overline{BE0}$_CLE, $\overline{GPMC_BE1}$ valid to $\overline{GPMC_CS[x]}$ valid | | J - 2[5] | J + 4[5] | ns |
| 13 | $t_{d(nCSV\text{-}nADVV)}$ | Delay time, $\overline{GPMC_CS[x]}$ valid to GPMC_$\overline{ADV}$_ALE valid | | K - 2[6] | K + 4[6] | ns |
| 14 | $t_{d(nCSV\text{-}nOEV)}$ | Delay time, $\overline{GPMC_CS[x]}$ valid to $\overline{GPMC_OE_RE}$ valid | | L - 2[7] | L + 4[7] | ns |

(1) For single read: N = RdCycleTime * (TimeParaGranularity + 1) * GPMC_FCLK
For single write: N = WrCycleTime * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: N = (RdCycleTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst write: N = (WrCycleTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
(2) For single read: A = (CSRdOffTime - CSOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For single write: A = (CSWrOffTime - CSOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: A = (CSRdOffTime - CSOnTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst write: A = (CSWrOffTime - CSOnTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
(3) = B - nCS Max Delay + nADV Min Delay
For reading: B = ((ADVRdOffTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay - CSExtraDelay)) * GPMC_FCLK
For writing: B = ((ADVWrOffTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay - CSExtraDelay)) * GPMC_FCLK
(4) = C - nCS Max Delay + nOE Min Delay
C = ((OEOffTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay - CSExtraDelay)) * GPMC_FCLK
(5) = J - Address Max Delay + nCS Min Delay
J = (CSOnTime * (TimeParaGranularity + 1) + 0.5 * CSExtraDelay) * GPMC_FCLK
(6) = K - nCS Max Delay + nADV Min Delay
K = ((ADVOnTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay - CSExtraDelay)) * GPMC_FCLK
(7) = L - nCS Max Delay + nOE Min Delay
L = ((OEOnTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay - CSExtraDelay)) * GPMC_FCLK

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**Table 9-37. Switching Characteristics Over Recommended Operating Conditions for GPMC/NOR Flash Interface - Asynchronous Mode (continued)**

(see Figure 9-27, Figure 9-28, Figure 9-29, Figure 9-30 for Non-Multiplexed Modes)
(see Figure 9-31, Figure 9-32 for Multiplexed Modes)

| NO. | PARAMETER | | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| 17 | $t_{w(AIV)}$ | Pulse duration, GPMC_A[27:0] address bus invalid between 2 successive R/W accesses | MUX0 and Non-Multi Muxed pins | G (8) | | ns |
| | | | MUX1 for GPMC_A[15:0] | G (8) | | ns |
| | | | MUX1/2 for GPMC_A[27:20] | G (8) | | ns |
| | | | GPMC_D[15:0] | G (8) | | ns |
| 19 | $t_{d(nCSV-nOEIV)}$ | Delay time, $\overline{\text{GPMC_CS[x]}}$ valid to $\overline{\text{GPMC_OE_RE}}$ invalid (burst read) | | I - 2 (9) | I + 4 (9) | ns |
| 21 | $t_{w(AV)}$ | Pulse duration, GPMC_A[27:0] address bus valid: second, third and fourth accesses | MUX0 and Non-Multi Muxed pins | D (10) | | ns |
| | | | MUX1 for GPMC_A[15:0] | D (10) | | ns |
| | | | MUX1/2 for GPMC_A[27:20] | D (10) | | ns |
| | | | GPMC_D[15:0] | D (10) | | ns |
| 26 | $t_{d(nCSV-nWEV)}$ | Delay time, $\overline{\text{GPMC_CS[x]}}$ valid to $\overline{\text{GPMC_WE}}$ valid | | E - 2 (11) | E + 4 (11) | ns |
| 28 | $t_{d(nCSV-nWEIV)}$ | Delay time, $\overline{\text{GPMC_CS[x]}}$ valid to $\overline{\text{GPMC_WE}}$ invalid | | F - 2 (12) | F + 4 (12) | ns |
| 29 | $t_{d(nWEV-DV)}$ | Delay time, $\overline{\text{GPMC_WE}}$ valid to GPMC_D[15:0] data bus valid | | | 2.0 | ns |
| 30 | $t_{d(DV-nCSV)}$ | Delay time, GPMC_D[15:0] data bus valid to $\overline{\text{GPMC_CS[x]}}$ valid | | J - 2 (5) | J + 4 (5) | ns |
| 37 | $t_{d(ADVV-AIV)}$ | Delay time, GPMC_$\overline{\text{ADV}}$_ALE valid to GPMC_D[15:0] address invalid | MUX0 and Non-Multi Muxed pins | | 2.0 | ns |
| 38 | $t_{d(nOEV-AIV)}$ | Delay time, $\overline{\text{GPMC_OE_RE}}$ valid to GPMC_D[15:0] address/data busses phase end | MUX0 and Non-Multi Muxed pins | | 2.0 | ns |
| | | | MUX1 for GPMC_A[15:0] | | 2.0 | ns |
| | | | MUX1/2 for GPMC_A[27:20] | | 2.0 | ns |
| | | | GPMC_D[15:0] | | 2.0 | ns |
| 39 | $t_{d(AIV-ADVV)}$ | Delay time, GPMC_D[15:0] address valid to GPMC_$\overline{\text{ADV}}$_ALE invalid | MUX0 and Non-Multi Muxed pins | | 2.0 | ns |

(8) G = Cycle2CycleDelay * GPMC_FCLK
(9) = I - nCS Max Delay + nOE Min Delay
I = ((OEOffTime + (n - 1) * PageBurstAccessTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay - CSExtraDelay)) * GPMC_FCLK
(10) D = PageBurstAccessTime * (TimeParaGranularity + 1) * GPMC_FCLK
(11) = E - nCS Max Delay + nWE Min Delay
E = ((WEOnTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay - CSExtraDelay)) * GPMC_FCLK
(12) = F - nCS Max Delay + nWE Min Delay
F = ((WEOffTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay - CSExtraDelay)) * GPMC_FCLK


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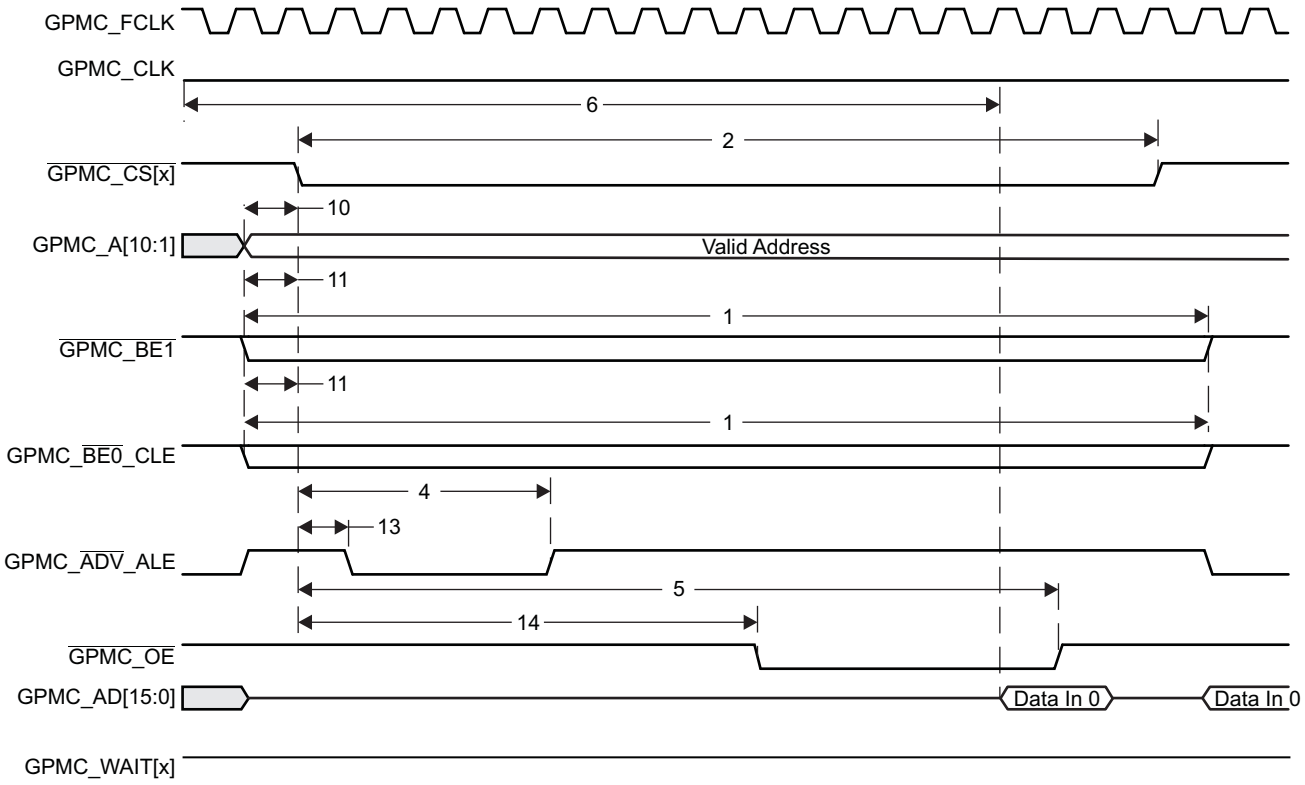


**Figure 9-27. GPMC/Non-Multiplexed NOR Flash - Asynchronous Read - Single Word Timing**

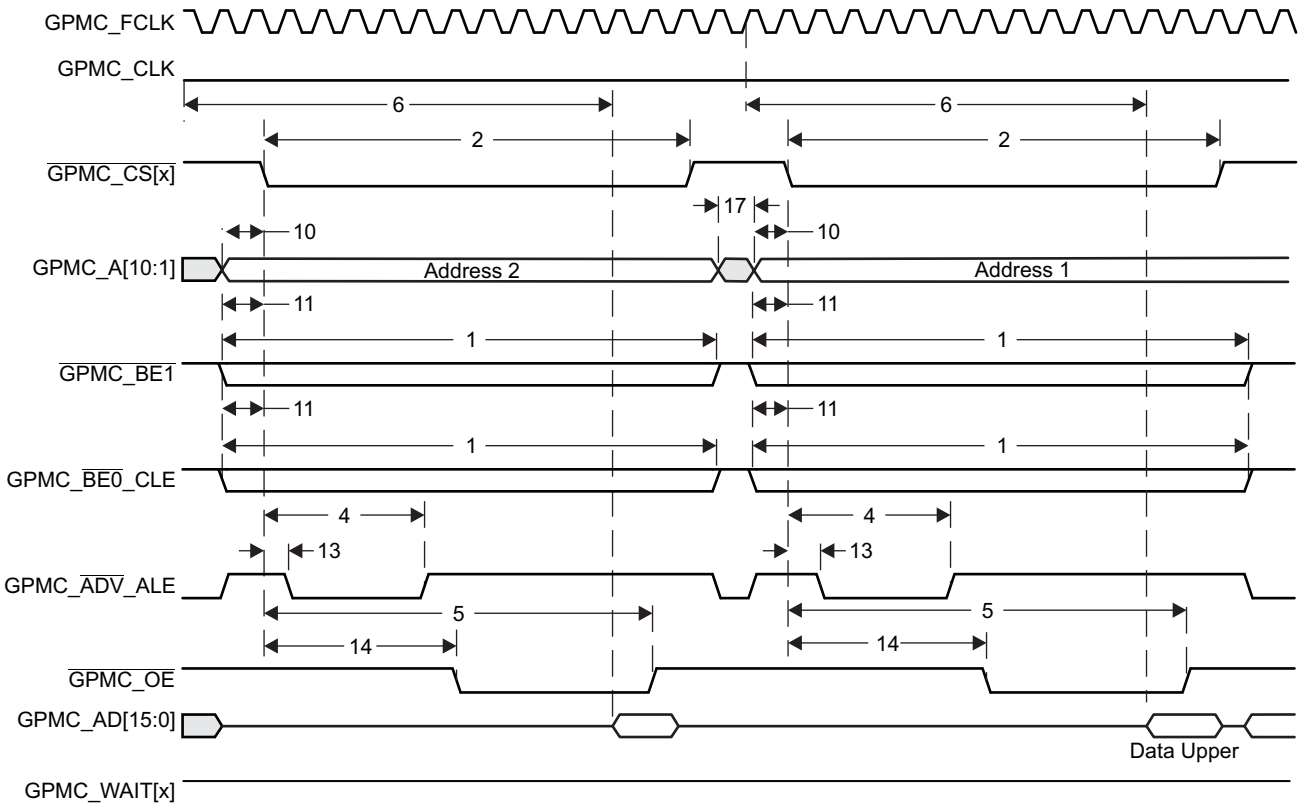


**Figure 9-28. GPMC/Non-Multiplexed NOR Flash - Asynchronous Read - 32-Bit Access Timing**

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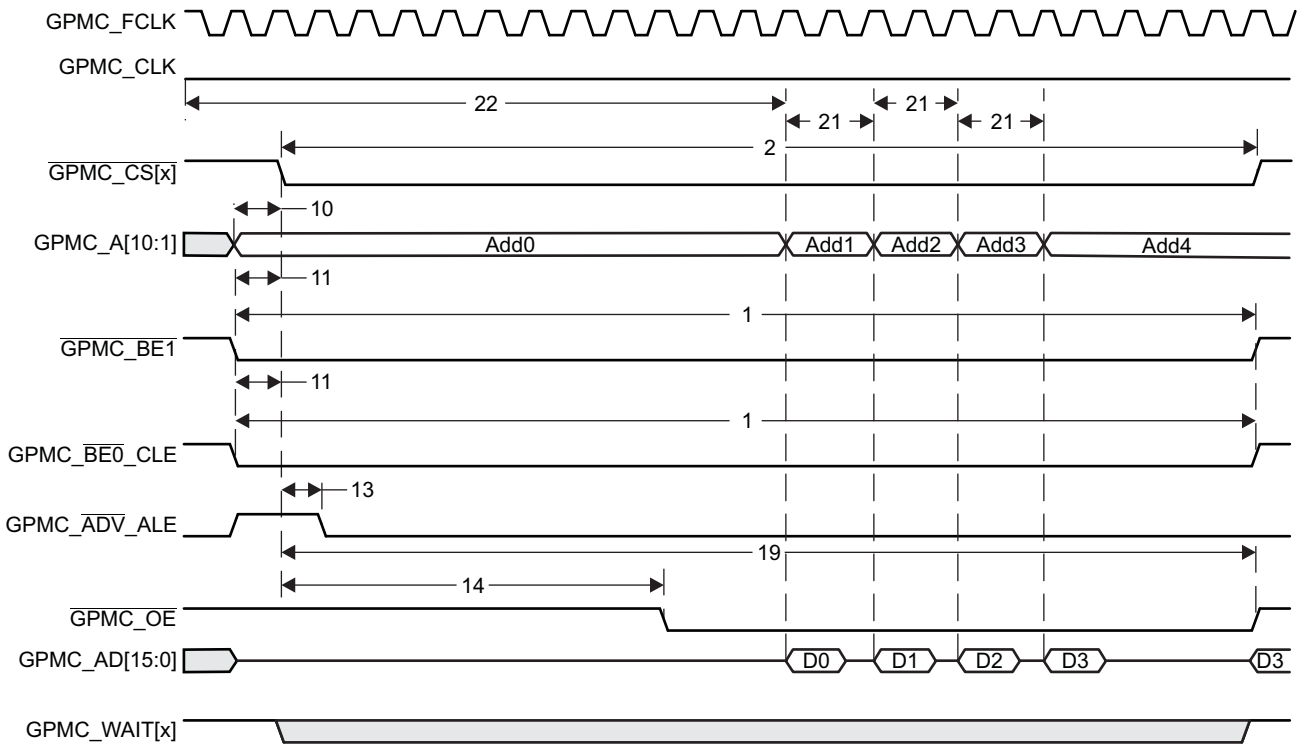


**Figure 9-29. GPMC/Non-Multiplexed *Only* NOR Flash - Asynchronous Read - Page Mode 4x16-Bit Timing**

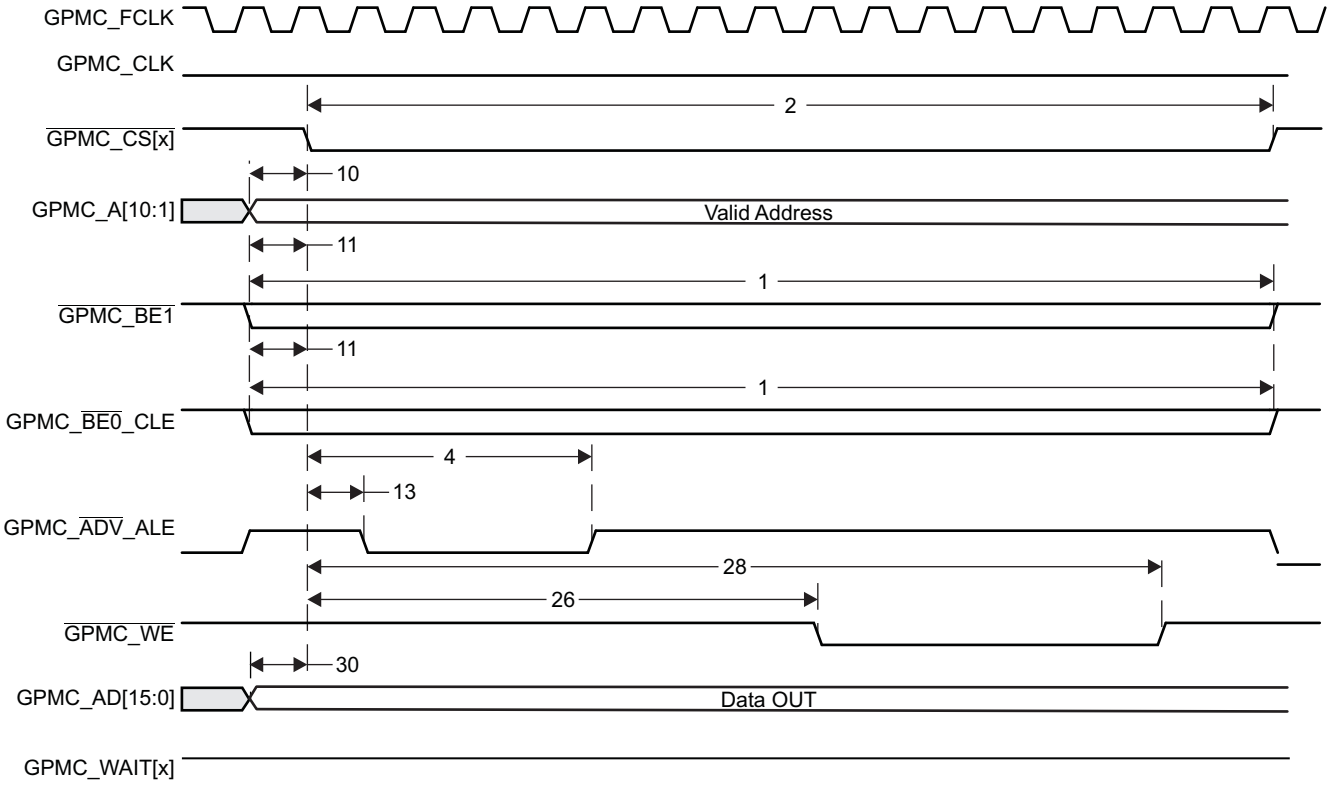


**Figure 9-30. GPMC/Non-Multiplexed NOR Flash - Asynchronous Write - Single Word Timing**


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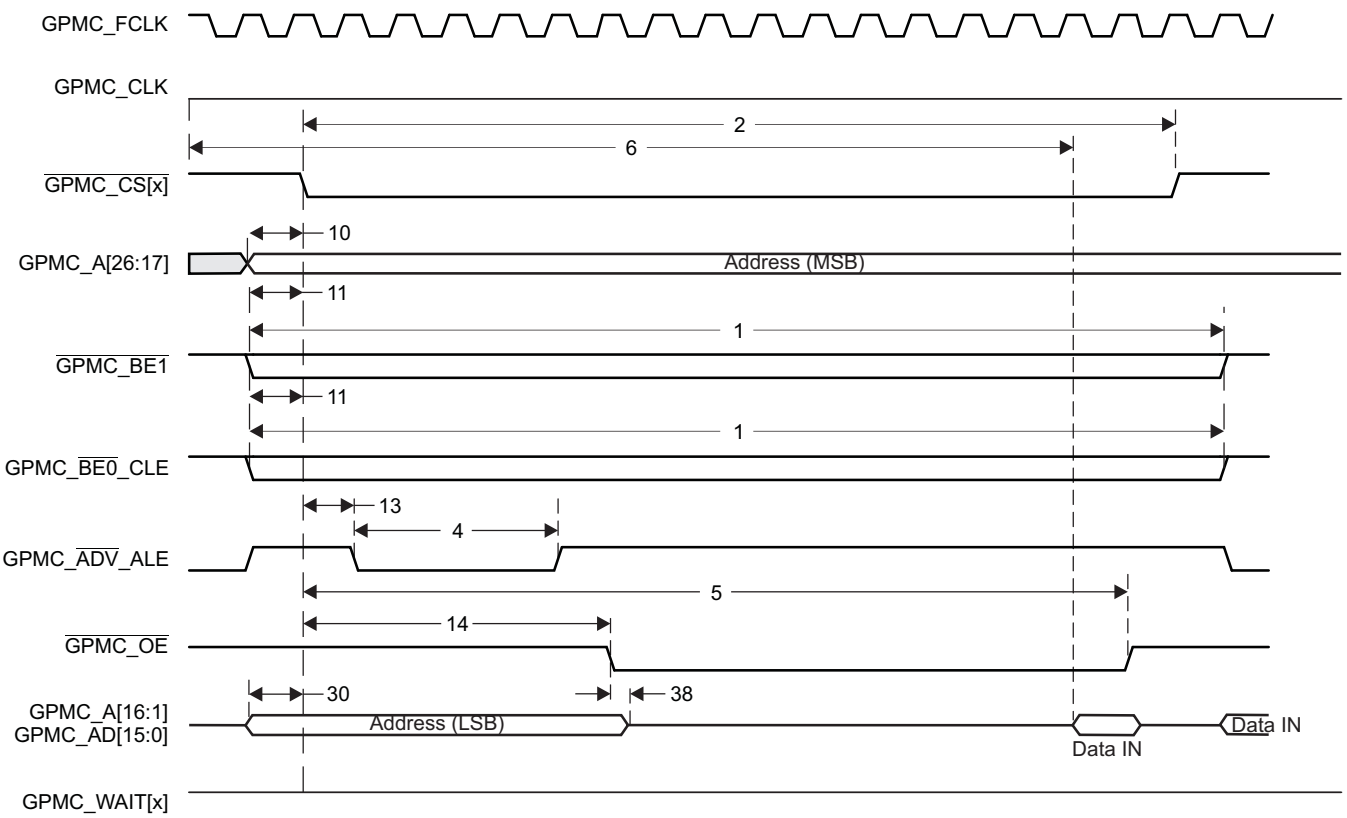


**Figure 9-31. GPMC/Multiplexed NOR Flash - Asynchronous Read - Single Word Timing**

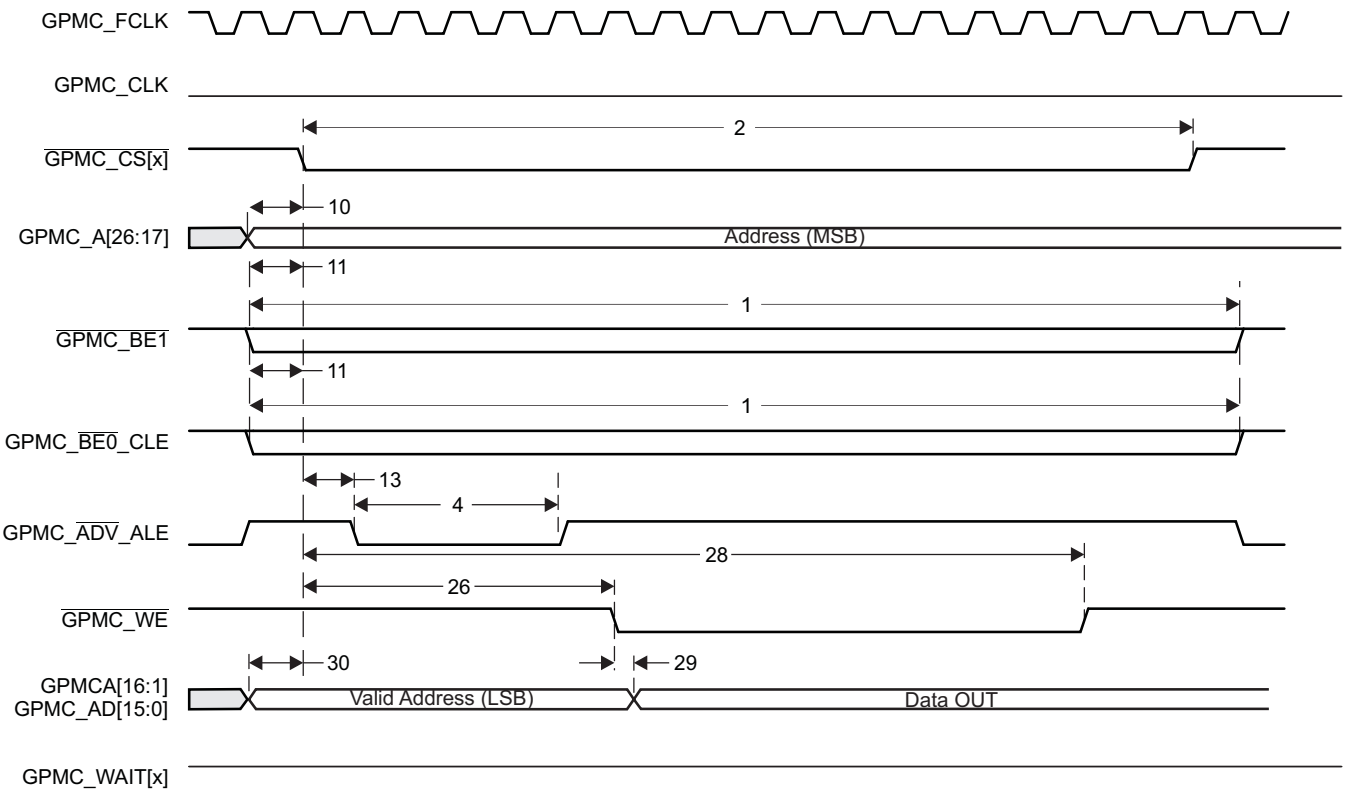


**Figure 9-32. GPMC/Multiplexed NOR Flash - Asynchronous Write - Single Word Timing**

### 9.8.2.3 GPMC/NAND Flash and ELM Interface Timing

**Table 9-38. Timing Requirements for GPMC/NAND Flash Interface**

(see Figure 9-35)

| NO. | | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 13 | $t_{acc(DAT)}$ | Data maximum access time (GPMC_FCLK cycles) | | J(1) | cycles |

(1) J = AccessTime * (TimeParaGranularity + 1)

**Table 9-39. Switching Characteristics Over Recommended Operating Conditions for GPMC/NAND Flash Interface**

(see Figure 9-33, Figure 9-34, Figure 9-35, Figure 9-36)

| NO. | PARAMETER | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{w(nWEV)}$ | Pulse duration, $\overline{GPMC_WE}$ valid time | | A(1) | ns |
| 2 | $t_{d(nCSV-nWEV)}$ | Delay time, $\overline{GPMC_CS[X]}$ valid to $\overline{GPMC_WE}$ valid | B - 2(2) | B + 4(2) | ns |
| 3 | $t_{d(CLEH-nWEV)}$ | Delay time, GPMC_$\overline{BE0}$_CLE high to $\overline{GPMC_WE}$ valid | C - 2(3) | C + 4(3) | ns |
| 4 | $t_{d(nWEV-DV)}$ | Delay time, GPMC_D[15:0] valid to $\overline{GPMC_WE}$ valid | D - 2(4) | D + 4(4) | ns |
| 5 | $t_{d(nWEIV-DIV)}$ | Delay time, $\overline{GPMC_WE}$ invalid to GPMC_AD[15:0] invalid | E - 2(5) | E + 4(5) | ns |
| 6 | $t_{d(nWEIV-CLEIV)}$ | Delay time, $\overline{GPMC_WE}$ invalid to GPMC_$\overline{BE0}$_CLE invalid | F - 2(6) | F + 4(6) | ns |
| 7 | $t_{d(nWEIV-nCSIV)}$ | Delay time, $\overline{GPMC_WE}$ invalid to $\overline{GPMC_CS[X]}$ invalid | G - 2(7) | G + 4(7) | ns |
| 8 | $t_{d(ALEH-nWEV)}$ | Delay time, GPMC_$\overline{ADV}$_ALE High to $\overline{GPMC_WE}$ valid | C - 2(3) | C + 4(3) | ns |
| 9 | $t_{d(nWEIV-ALEIV)}$ | Delay time, $\overline{GPMC_WE}$ invalid to GPMC_$\overline{ADV}$_ALE invalid | F - 2(6) | F + 4(6) | ns |
| 10 | $t_{c(nWE)}$ | Cycle time, write cycle time | | H(8) | ns |
| 11 | $t_{d(nCSV-nOEV)}$ | Delay time, $\overline{GPMC_CS[X]}$ valid to $\overline{GPMC_OE_RE}$ valid | I - 2(9) | I + 4(9) | ns |
| 12 | $t_{w(nOEV)}$ | Pulse duration, $\overline{GPMC_OE_RE}$ valid time | | K(10) | ns |
| 13 | $t_{c(nOE)}$ | Cycle time, read cycle time | | L(11) | ns |
| 14 | $t_{d(nOEIV-nCSIV)}$ | Delay time, $\overline{GPMC_OE_RE}$ invalid to $\overline{GPMC_CS[X]}$ invalid | M - 2(12) | M + 4(12) | ns |

(1) A = (WEOffTime - WEOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK
(2) = B + nWE Min Delay - nCS Max Delay
B = ((WEOnTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay - CSExtraDelay)) * GPMC_FCLK
(3) = C + nWE Min Delay - CLE Max Delay
C = ((WEOnTime - ADVOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay - ADVExtraDelay)) * GPMC_FCLK
(4) = D + nWE Min Delay - Data Max Delay
D = (WEOnTime * (TimeParaGranularity + 1) + 0.5 * WEExtraDelay ) * GPMC_FCLK
(5) =E + Data Min Delay - nWE Max Delay
E = ((WrCycleTime - WEOffTime) * (TimeParaGranularity + 1) - 0.5 * WEExtraDelay ) * GPMC_FCLK
(6) = F + CLE Min Delay - nWE Max Delay
F = ((ADVWrOffTime - WEOffTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay - WEExtraDelay )) * GPMC_FCLK
(7) =G + nCS Min Delay - nWE Max Delay
G = ((CSWrOffTime - WEOffTime) * (TimeParaGranularity + 1) + 0.5 * (CSExtraDelay - WEExtraDelay )) * GPMC_FCLK
(8) H = WrCycleTime * (1 + TimeParaGranularity) * GPMC_FCLK
(9) = I + nOE Min Delay - nCS Max Delay
I = ((OEOnTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay - CSExtraDelay)) * GPMC_FCLK
(10) K = (OEOffTime - OEOnTime) * (1 + TimeParaGranularity) * GPMC_FCLK
(11) L = RdCycleTime * (1 + TimeParaGranularity) * GPMC_FCLK
(12) =M + nCS Min Delay - nOE Max Delay
M = ((CSRdOffTime - OEOffTime) * (TimeParaGranularity + 1) + 0.5 * (CSExtraDelay - OEExtraDelay ))* GPMC_FCLK


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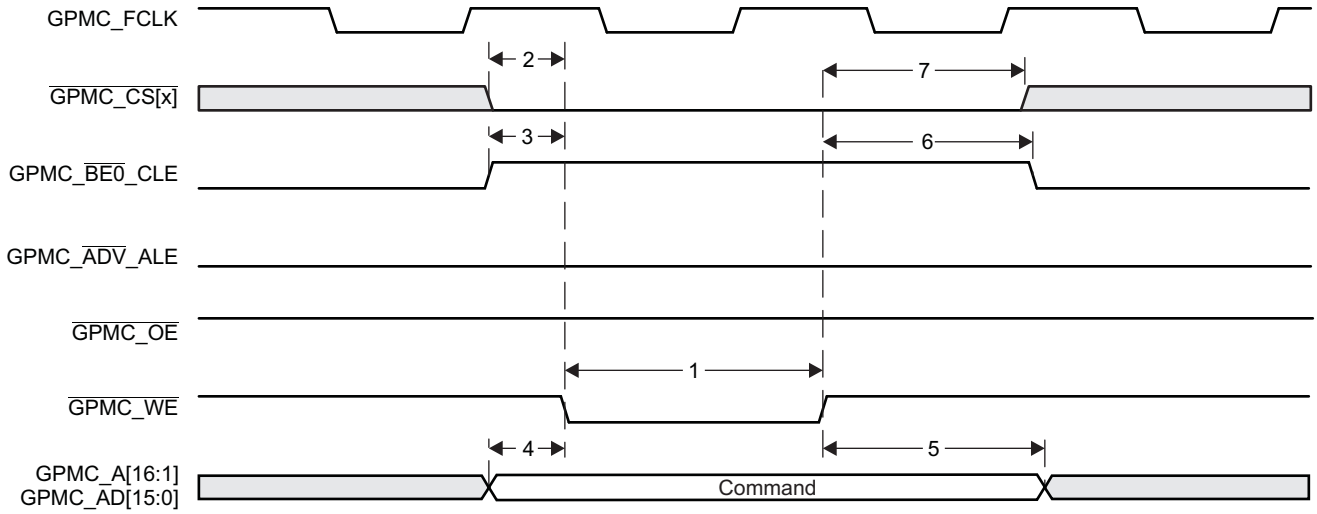


**Figure 9-33. GPMC/NAND Flash - Command Latch Cycle Timing**

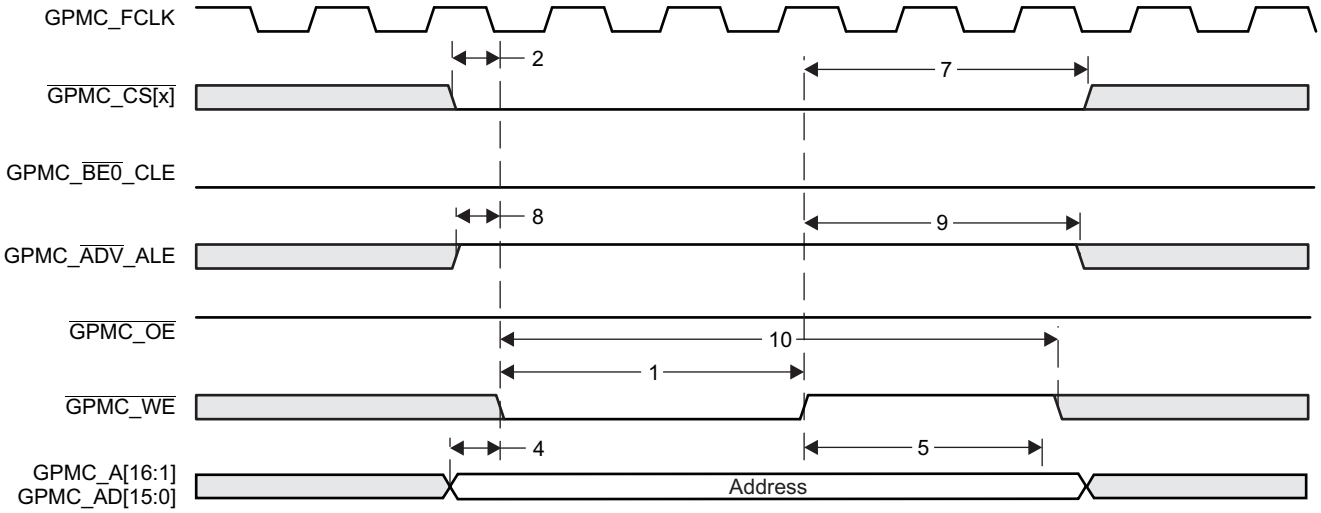


**Figure 9-34. GPMC/NAND Flash - Address Latch Cycle Timing**

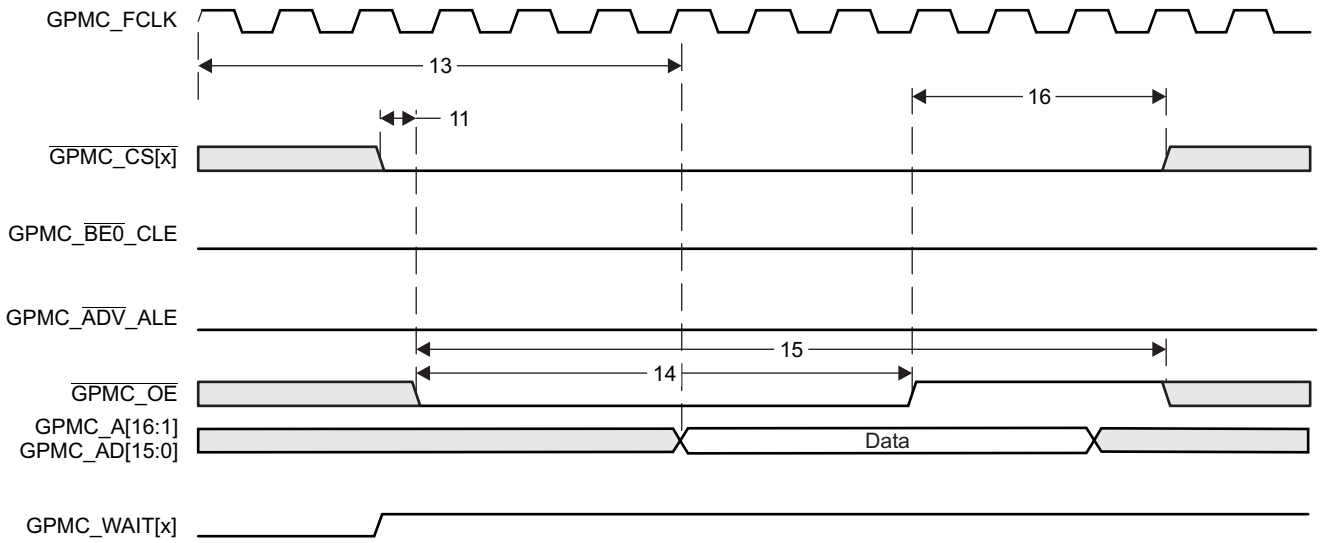


**Figure 9-35. GPMC/NAND Flash - Data Read Cycle Timing**

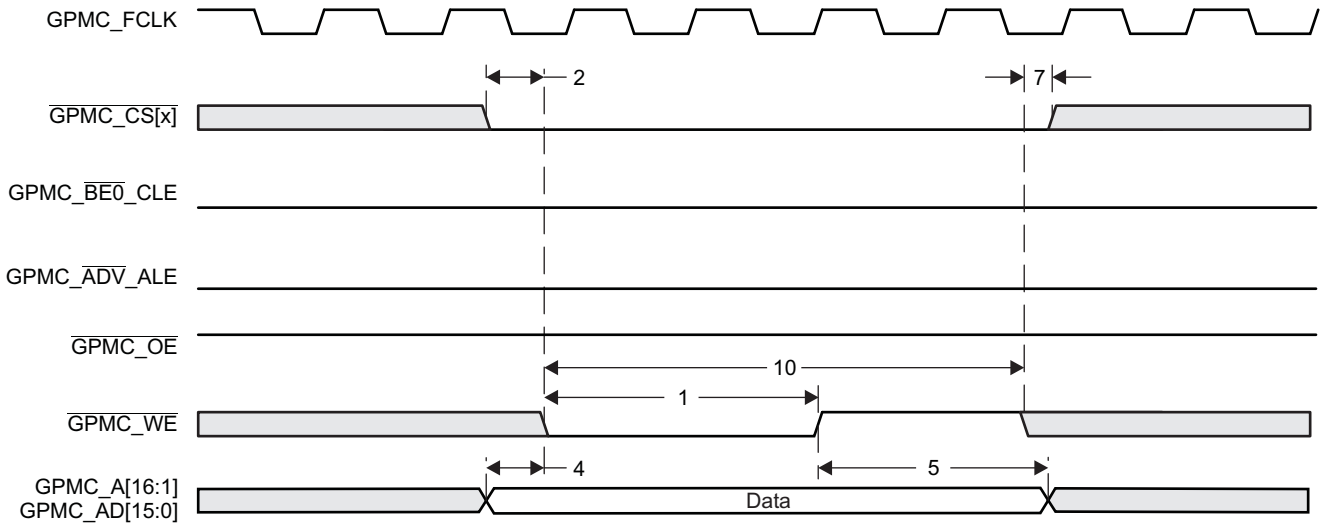


**Figure 9-36. GPMC/NAND Flash - Data Write Cycle Timing**


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## 9.9 High-Definition Multimedia Interface (HDMI)

The device includes an HDMI 1.3a-compliant transmitter for digital video and audio data to display devices. The HDMI interface consists of a digital HDMI transmitter core with TMDS encoder, a core wrapper with interface logic and control registers, and a transmit PHY, with the following features:

- Hot-plug detection
- Consumer electronics control (CEC) messages
- DVI 1.0 compliant (only RGB pixel format)
- CEA 861-D and VESA DMT formats
- Supports up to 165-MHz pixel clock
  - 1920 x 1080p @75 Hz with 8-bit/component color depth
  - 1600 x 1200 @60 Hz with 8-bit/component color depth
- Support for deep-color mode:
  - 10-bit/component color depth up to 1080p @60 Hz (Max pixel clock = 148.5 MHz)
  - 12-bit/component color depth up to 720p/1080i @60 Hz (Max pixel clock = 123.75 MHz)
- TMDS clock to the HDMI-PHY is up to 185.625 MHz
- Maximum supported pixel clock:
  - 165 MHz for 8-bit color depth
  - 148.5 MHz for 10-bit color depth
  - 123.75 MHz for 12-bit color depth
- Uncompressed multichannel (up to eight channels) audio (L-PCM) support
- Master I2C interface for display data channel (DDC) connection

For more details on the HDMI, see the *High-Definition Multimedia Interface (HDMI)* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

### *9.9.1 HDMI Design Guidelines*

This section provides PCB design and layout guidelines for the HDMI interface. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. Simulation and system design work has been done to ensure the HDMI interface requirements are met.

#### 9.9.1.1 HDMI Interface Schematic

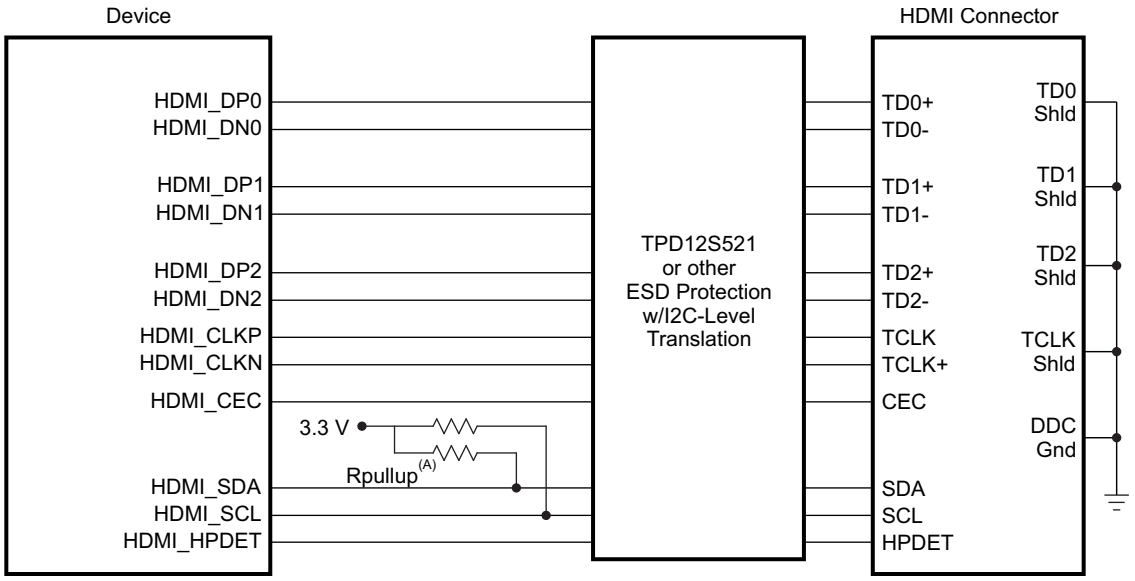
The HDMI bus is separated into three main sections:

1. Transition Minimized Differential Signaling (TMDS) high-speed digital video interface
2. Display Data Channel (I2C bus for configuration and status exchange between two devices)
3. Consumer Electronics Control (optional) for remote control of connected devices.

The DDC and CEC are low-speed interfaces, so nothing special is required for PCB layout of these signals. Their connection is shown in Figure 9-37, *HDMI Interface High-Level Schematic*.

The TMDS channels are high-speed differential pairs and, therefore, require the most care in layout. Specifications for TMDS layout are below.

Figure 9-37 shows the HDMI interface schematic. The specific pin numbers can be obtained from Table 4-16, *HDMI Terminal Functions*.




A. 5K-10K Ω pullup resistors are required if not integrated in the ESD protection chip.

**Figure 9-37. HDMI Interface High-Level Schematic**

### 9.9.1.2 TMDS Routing

The TMDS signals are high-speed differential pairs. Care must be taken in the PCB layout of these signals to ensure good signal integrity.

The TMDS differential signal traces must be routed to achieve 100 Ω (±10%) differential impedance and 60 Ω (±10%) single-ended impedance. Single-ended impedance control is required because differential signals are extremely difficult to closely couple on PCBs and, therefore, single-ended impedance becomes important.

These impedances are impacted by trace width, trace spacing, distance to reference planes, and dielectric material. Verify with a PCB design tool that the trace geometry for both data signal pairs results in as close to 60 Ω impedance traces as possible. For best accuracy, work with your PCB fabricator to ensure this impedance is met.

In general, closely coupled differential signal traces are not an advantage on PCBs. When differential signals are closely coupled, tight spacing and width control is necessary. Very small width and spacing variations affect impedance dramatically, so tight impedance control can be more problematic to maintain in production.

Loosely coupled PCB differential signals make impedance control much easier. Wider traces and spacing make obstacle avoidance easier, and trace width variations do not affect impedance as much; therefore, it is easier to maintain an accurate impedance over the length of the signal. The wider traces also show reduced skin effect and, therefore, often result in better signal integrity.

Table 9-40 shows the routing specifications for the TMDS signals.

**Table 9-40. TMDS Routing Specifications**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| -to-HDMI header trace length | | | 7000 | Mils |
| Number of stubs allowed on TMDS traces | | | 0 | Stubs |
| TX/RX pair differential impedance | 90 | 100 | 110 | Ω |
| TX/RX single ended impedance | 54 | 60 | 66 | Ω |
| Number of vias on each TMDS trace | | | 2 | Vias(1) |

(1) Vias must be used in pairs with their distance minimized.


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**Table 9-40. TMDS Routing Specifications (continued)**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| TMDS differential pair to any other trace spacing | 2*DS(2) | | | |

(2) DS = differential spacing of the HDMI traces.

#### 9.9.1.3 DDC Signals

As shown in Figure 9-37, *HDMI Interface High-Level Schematic*, the DDC connects just like a standard I2C bus. As such, resistor pullups must be used to pull up the open drain buffer signals unless they are integrated into the ESD protection chip used. If used, these pullup resistors should be connected to a 3.3-V supply.

#### 9.9.1.4 HDMI ESD Protection Device (Required)

Interfaces that connect to a cable such as HDMI generally require more ESD protection than can be built into the outputs of the processor. Therefore, this HDMI interface requires the use of an ESD protection chip to provide adequate ESD protection and to translate I2C voltage levels from the 3.3 V supplied by the device to the 5 volts required by the HDMI specification.

When selecting an ESD protection chip, choose the lowest capacitance ESD protection available to minimize signal degradation. In no case should the ESD protection circuit capacitance be more than 5 pF.

TI manufactures devices that provide ESD protection for HDMI signals such as the TPD12S521. For more information see the www.ti.com website.

#### 9.9.1.5 PCB Stackup Specifications

Table 9-41 shows the stackup and feature sizes required for HDMI.

**Table 9-41. HDMI PCB Stackup Specifications**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| PCB routing/plane layers | 4 | 6 | - | Layers |
| Signal routing layers | 2 | 3 | - | Layers |
| Number of ground plane cuts allowed within HDMI routing region | - | - | 0 | Cuts |
| Number of layers between HDMI routing region and reference ground plane | - | - | 0 | Layers |
| PCB trace width | - | 4 | - | Mils |
| PCB BGA escape via pad size | - | 20 | - | Mils |
| PCB BGA escape via hole size | - | 10 | | Mils |
| device BGA pad size(1)(2) | | 0.4 | | mm |

(1) Non-solder mask defined pad.
(2) Per IPC-7351A BGA pad size guideline.

#### 9.9.1.6 Grounding

Each TMDS channel has its own shield pin which should be grounded to provide a return current path for the TMDS signal.

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## 9.10 High-Definition Video Processing Subsystem (HDVPSS)

The device High-Definition Video Processing Subsystem (HDVPSS) provides a video input interface for external imaging peripherals (that is, image sensors, video decoders, and so on) and a video output interface for display devices, such as analog SDTV displays, digital HDTV displays, digital LCD panels, and so on. The HDVPSS includes HD and SD video encoders and an HDMI transmitter interface.

The device HDVPSS features include:

- Two display processing pipelines with de-interlacing, scaling, alpha blending, chroma keying, color space conversion, flicker filtering, and pixel format conversion.
- HD/SD compositor features for PIP support.
- Format conversions (up to 1080p 60 Hz) include scan format conversion, scan rate conversion, aspect-ratio conversion, and frame size conversion.
- Supports additional video processing capabilities by using the memory-to-memory feature of the subsystem.
- Two parallel video processing pipelines support HD (up to 1080p60) and SD (NTSC/PAL) simultaneous outputs.
  - SD analog output with OSD with embedded timing codes (BT.656)
    - S-video or Composite output
    - 2-channel SD-DAC with 10-bit resolution
    - Options available to support MacroVision and CGMS-A (contact local TI Sales rep for information).
  - Digital HDMI 1.3a-compliant transmitter (for details, see Section 9.9, *High-Definition Multimedia Interface (HDMI)*).
  - One digital video output supporting up to 30-bits @ 165 MHz
  - One digital video output supporting up to 24-bits @ 165 MHz
- One independently configurable external video input capture port (up to 165 MHz).
  - 16/24-bit HD digital video input or dual clock independent 8-bit SD inputs.
  - 8/16/24-bit digital video input
  - Embedded sync and external sync modes are supported for all input configurations.
  - De-multiplexing of both pixel-to-pixel and line-to-line multiplexed streams, effectively supporting up to 8 simultaneous SD inputs with a glueless interface to an external multiplexer such as the TVP5158.
  - Additional features include: programmable color space conversion, scaler and chroma downsampler, ancillary VANC/VBI data capture (decoded by software).
- Graphics features:
  - Three independently-generated graphics layers.
  - Each supports full-screen resolution graphics in HD, SD or both.
  - Up/down scaler optimized for graphics.
  - Global and pixel-level alpha blending supported.

For more detailed information on specific features and registers, see the *High Definition Video Processing Subsystem* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).


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### 9.10.1 HDVPSS Electrical Data/Timing

**Table 9-42. Timing Requirements for HDVPSS Input**

(see Figure 9-38 and Figure 9-39)

| NO. | | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| **VIN[X]A_CLK** | | | | | |
| 1 | $t_{c(CLK)}$ | Cycle time, VIN[x]A_CLK | 6.06(1) | | ns |
| 2 | $t_{w(CLKH)}$ | Pulse duration, VIN[x]A_CLK high (45% of $t_c$) | 2.73 | | ns |
| 3 | $t_{w(CLKH)}$ | Pulse duration, VIN[x]A_CLK low (45% of $t_c$) | 2.73 | | ns |
| 4 | $t_{su(DE-CLK)}$ | Input setup time, control valid to VIN[x]A_CLK high/low | 3 | | ns |
| | $t_{su(VSYNC-CLK)}$ | | | | |
| | $t_{su(FLD-CLK)}$ | | | | |
| | $t_{su(HSYNC-CLK)}$ | | | | |
| | $t_{su(D-CLK)}$ | Input setup time, data valid to VIN[x]A_CLK high/low | 3 | | |
| 5 | $t_{h(CLK-DE)}$ | Input hold time, control valid from VIN[x]A_CLK high/low | 0.1 | | ns |
| | $t_{h(CLK-VSYNC)}$ | | | | |
| | $t_{h(CLK-FLD)}$ | | | | |
| | $t_{h(CLK-HSYNC)}$ | | | | |
| | $t_{h(CLK-D)}$ | Input hold time, data valid from VIN[x]A_CLK high/low | 0.1 | | |
| **VIN[x]B_CLK** | | | | | |
| 1 | $t_{c(CLK)}$ | Cycle time, VIN[x]B_CLK | 6.06(1) | | ns |
| 2 | $t_{w(CLKH)}$ | Pulse duration, VIN[x]B_CLK high (45% of $t_c$) | 2.73 | | ns |
| 3 | $t_{w(CLKH)}$ | Pulse duration, VIN[x]B_CLK low (45% of $t_c$) | 2.73 | | ns |
| 4 | $t_{su(DE-CLK)}$ | Input setup time, control valid to VIN[x]B_CLK high/low | 3 | | ns |
| | $t_{su(VSYNC-CLK)}$ | | | | |
| | $t_{su(FLD-CLK)}$ | | | | |
| | $t_{su(HSYNC-CLK)}$ | | | | |
| | $t_{su(D-CLK)}$ | Input setup time, data valid to VIN[x]B_CLK high/low | 3 | | |
| 5 | $t_{h(CLK-DE)}$ | Input hold time, control valid from VIN[x]B_CLK high/low | 0.1 | | ns |
| | $t_{h(CLK-VSYNC)}$ | | | | |
| | $t_{h(CLK-FLD)}$ | | | | |
| | $t_{h(CLK-HSYNC)}$ | | | | |
| | $t_{h(CLK-D)}$ | Input hold time, data valid from VIN[x]B_CLK high/low | 0.1 | | |

(1) For maximum frequency of 165 MHz.

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### Table 9-43. Switching Characteristics Over Recommended Operating Conditions for HDVPSS Output

(see Figure 9-38 and Figure 9-40)

| NO. | PARAMETER | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{c(CLK)}$ | Cycle time, VOUT[x]_CLK | 6.06(1) | | ns |
| 2 | $t_{w(CLKH)}$ | Pulse duration, VOUT[x]_CLK high (45% of $t_c$) | 2.73 | | ns |
| 3 | $t_{w(CLKL)}$ | Pulse duration, VOUT[x]_CLK low (45% of $t_c$) | 2.73 | | ns |
| 7 | $t_{t(CLK)}$ | Transition time, VOUT[x]_CLK (10%-90%) | | 2.64 | ns |
| 6 | $t_{d(CLK-AVID)}$ | Delay time, VOUT[x]_CLK low (falling) to control valid | -1.2 | 2 | ns |
| | $t_{d(CLK-FLD)}$ | | | | |
| | $t_{d(CLK-VSYNC)}$ | | | | |
| | $t_{d(CLK-HSYNC)}$ | | | | |
| | $t_{d(CLK-RCR)}$ | Delay time, VOUT[0]_CLK low (falling) to data valid | -1.2 | 2 | ns |
| | $t_{d(CLK-GYYC)}$ | | | | |
| | $t_{d(CLK-BCBC)}$ | | | | |
| | $t_{d(CLK-YYC)}$ | Delay time, VOUT[1]_CLK low (falling) to data valid | | | |
| | $t_{d(CLK-C)}$ | | | | |

(1) For maximum frequency of 165 MHz.

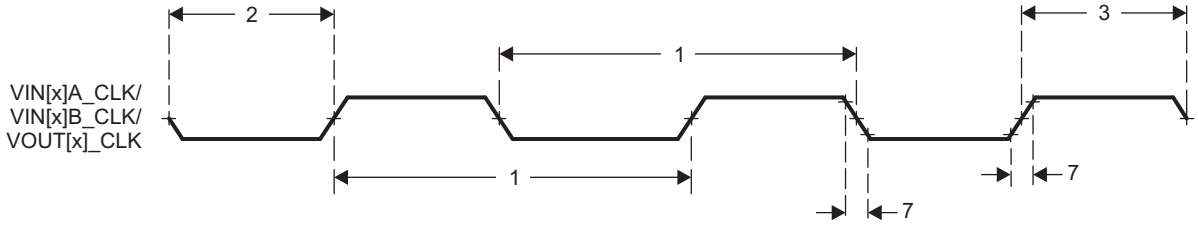


**Figure 9-38. HDVPSS Clock Timing**


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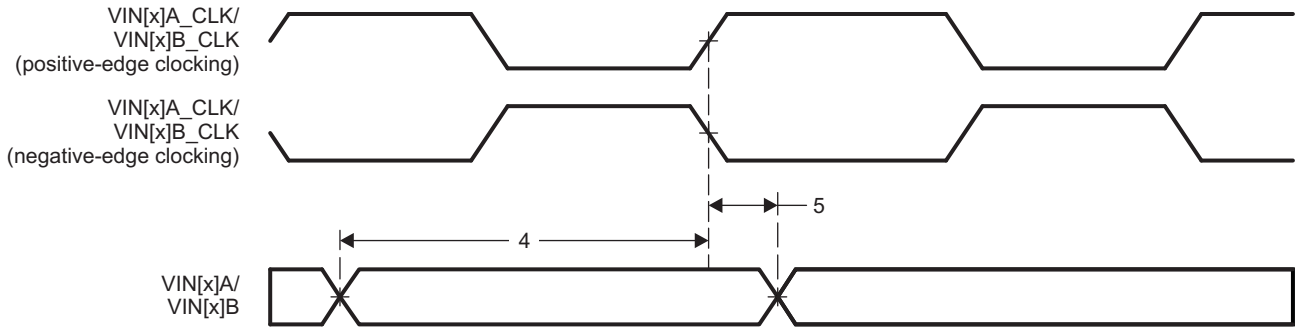



**Figure 9-39. HDVPSS Input Timing**

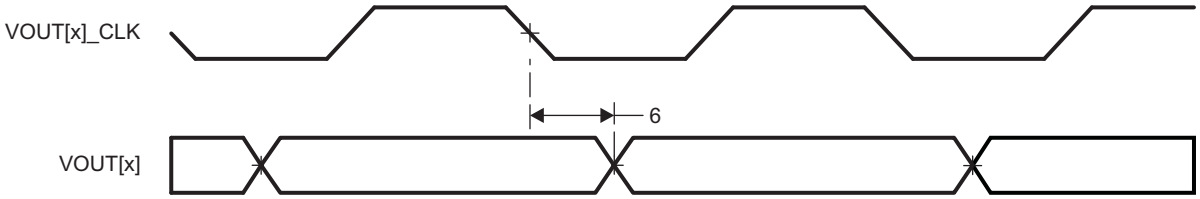
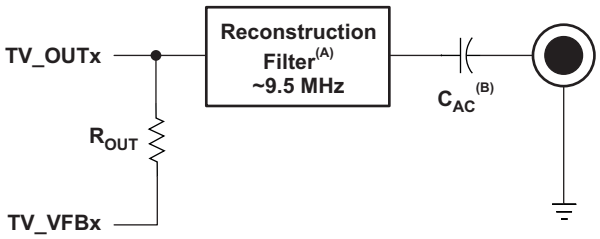



**Figure 9-40. HDVPSS Output Timing**

### 9.10.2 Video DAC Guidelines and Electrical Data/Timing

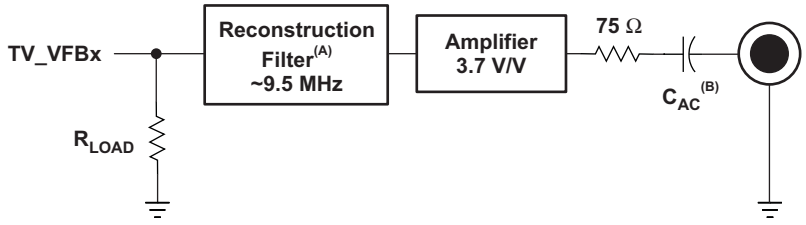
The analog video DAC outputs of the device can be operated in one of two modes: Normal mode and TVOUT Bypass mode. In Normal mode, the device's internal video amplifier is used. In TVOUT Bypass mode, the internal video amplifier is bypassed and an external amplifier is required.

Figure 9-41 shows a typical circuit that permits connecting the analog video output from the device to standard 75-Ω impedance video systems in Normal mode. Figure 9-42 shows a typical circuit that permits connecting the analog video output from the device to standard 75-Ω impedance video systems in TVOUT Bypass mode.




A. Reconstruction Filter (optional)
B. AC coupling capacitor (optional)

**Figure 9-41. TV Output (Normal Mode)**




A. Reconstruction Filter (optional). Note: An amplifier with an integrated reconstruction filter can alternatively be used instead of a discrete reconstruction filter.
B. AC coupling capacitor (optional)

**Figure 9-42. TV Output (TVOUT Bypass Mode)**

During board design, the onboard traces and parasitics must be matched for the channel. The video DAC output pins (TV_OUTx/TV_VFBx) are very high-frequency analog signals and must be routed with extreme care. As a result, the paths of these signals must be as short as possible, and as isolated as possible from other interfering signals. In TVOUT Bypass mode, the load resistor and amplifier/buffer should be placed as close as possible to the TV_VFBx pins. Other layout guidelines include:

- Take special care to bypass the VDDA_VDAC_1P8 power supply pin with a capacitor. For more information, see Section 8.2.9, *Power-Supply Decoupling*.
- In **TVOUT Bypass mode**, place the $R_{LOAD}$ resistor as close as possible to the Reconstruction Filter and Amplifier. In addition, place the 75-Ω resistor as close as possible (< 0.5 ") to the Amplifier/buffer output pin. To maintain a high-quality video signal, the onboard traces after the 75-Ω resistor should have a characteristic impedance of 75 Ω (± 20%).
- In **Normal mode**, TV_VFBx is the most sensitive pin in the TV out system. The $R_{OUT}$ resistor should be placed as close as possible to the device pins. To maintain a high-quality video signal, the onboard traces leading to the TV_OUTx pin should have a characteristic impedance of 75 Ω (± 20%) starting from the closest possible place to the device pin output.
- Minimize input trace lengths to the device to reduce parasitic capacitance.
- Include solid ground return paths.
- Match trace lengths as close as possible within a video format group (that is, Y and C for S-Video output should match each other).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For additional Video DAC Design guidelines, see the *High Definition Video Processing Subsystem* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

**Table 9-44. Static and Dynamic DAC Specifications**

| VDAC STATIC SPECIFICATIONS | | | | | |
|---|---|---|---|---|---|
| **PARAMETER** | **TEST CONDITIONS** | **MIN** | **TYP** | **MAX** | **UNIT** |
| Reference Current Setting Resistor ($R_{SET}$) | Normal Mode | 4653 | 4700 | 4747 | Ω |
| | TVOUT Bypass Mode | 9900 | 10000 | 10100 | Ω |
| Output resistor between TV_OUTx and TV_VFBx pins ($R_{OUT}$) | Normal Mode | 2673 | 2700 | 2727 | Ω |
| | TVOUT Bypass Mode | N/A | | | |
| Load Resistor ($R_{LOAD}$) | Normal Mode | 75-Ω Inside the Display | | | |
| | TVOUT Bypass Mode | 1485 | 1500 | 1515 | Ω |
| AC-Coupling Capacitor (Optional) [$C_{AC}$] | Normal Mode | 220 | | | uF |
| | TVOUT Bypass Mode | See External Amplifier Specification | | | |
| Total Capacitance from TV_OUTx to VSSA_VDAC_1P8 | Normal Mode | | | 300 | pF |
| | TVOUT Bypass Mode | N/A | | | |
| Resolution | | | 10 | | Bits |
| Integral Non-Linearity (INL), Best Fit | Normal Mode | -4 | | 4 | LSB |
| | TVOUT Bypass Mode | -1 | | 1 | LSB |
| Differential Non-Linearity (DNL) | Normal Mode | -2.5 | | 2.5 | LSB |
| | TVOUT Bypass Mode | -1 | | 1 | LSB |
| Full-Scale Output Voltage | Normal Mode ($R_{LOAD}$ = 75 Ω) | | 1.3 | | V |
| | TVOUT Bypass Mode ($R_{LOAD}$ = 1.5 kΩ) | | 0.7 | | V |
| Full-Scale Output Current | Normal Mode | N/A | | | |
| | TVOUT Bypass Mode | | 470 | | uA |
| Gain Error | Normal Mode (Composite) and TVOUT Bypass Mode | -10 | | 10 | %FS |
| | Normal Mode (S-Video) | -20 | | 20 | %FS |
| Gain Mismatch (Luma-to-Chroma) | Normal Mode (Composite) | N/A | | | |
| | Normal Mode (S-Video) | -10 | | 10 | % |
| Output Impedance | Looking into TV_OUTx nodes | | 75 | | Ω |
| **VDAC DYNAMIC SPECIFICATIONS** | | | | | |
| **PARAMETER** | **TEST CONDITIONS** | **MIN** | **TYP** | **MAX** | **UNIT** |
| Output Update Rate ($F_{CLK}$) | | | 54 | 60 | MHz |
| Signal Bandwidth | 3 dB | | 6 | | MHz |
| Spurious-Free Dynamic Range (SFDR) within bandwidth | $F_{CLK}$ = 54 MHz, $F_{OUT}$ = 1 MHz | | 50 | | dBc |
| Signal-to-Noise Ration (SNR) | $F_{CLK}$ = 54 MHz, $F_{OUT}$ = 1 MHz | | 54 | | dB |
| Power Supply Rejection (PSR) | Normal Mode, 100 mVpp @ 6 MHz on VDDA_VDAC_1P8 | | 6 | | dB |
| | TVOUT Bypass Mode, 100 mVpp @ 6 MHz on VDDA_VDAC_1P8 | | 20 | | |

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## 9.11 Inter-Integrated Circuit (I2C)

The device includes four inter-integrated circuit (I2C) modules which provide an interface to other devices compliant with Philips Semiconductors Inter-IC bus (I2C-bus™) specification version 2.1. External components attached to this 2-wire serial bus can transmit/receive 8-bit data to/from the device through the I2C module. The I2C port *does not* support CBUS compatible devices.

The I2C port supports the following features:

- Compatible with Philips I2C Specification Revision 2.1 (January 2000)
- Standard and fast modes from 10 - 400 Kbps (no fail-safe I/O buffers)
- Noise filter to remove noise 50 ns or less
- Seven- and ten-bit device addressing modes
- Multimaster transmitter/slave receiver mode
- Multimaster receiver/slave transmitter mode
- Combined master transmit/receive and receive/transmit modes
- Two DMA channels, one interrupt line
- Built-in FIFO (32 byte) for buffered read or write.

For more detailed information on the I2C peripheral, see the *Inter-Integrated Circuit (I2C) Controller Module* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

### 9.11.1 I2C Peripheral Register Descriptions

**Table 9-45. I2C Registers**

| HEX ADDRESS | | | | | |
|---|---|---|---|---|---|
| I2C0 | I2C1 | I2C2 | I2C3 | ACRONYM | REGISTER NAME |
| 0x4802 8000 | 0x4802 A000 | 0x4819 C000 | 0x4819 E000 | I2C_REVNB_LO | Module Revision (LOW BYTES) |
| 0x4802 8004 | 0x4802 A004 | 0x4819 C004 | 0x4819 E004 | I2C_REVNB_HI | Module Revision (HIGH BYTES) |
| 0x4802 8010 | 0x4802 A010 | 0x4819 C010 | 0x4819 E010 | I2C_SYSC | System configuration |
| 0x4802 8020 | 0x4802 A020 | 0x4819 C020 | 0x4819 E020 | I2C_EOI | I2C End of Interrupt |
| 0x4802 8024 | 0x4802 A024 | 0x4819 C024 | 0x4819 E024 | I2C_IRQSTATUS_RAW | I2C Status Raw |
| 0x4802 8028 | 0x4802 A028 | 0x4819 C028 | 0x4819 E028 | I2C_IRQSTATUS | I2C Status |
| 0x4802 802C | 0x4802 A02C | 0x4819 C02C | 0x4819 E02C | I2C_IRQENABLE_SET | I2C Interrupt Enable Set |
| 0x4802 8030 | 0x4802 A030 | 0x4819 C030 | 0x4819 E030 | I2C_IRQENABLE_CLR | I2C Interrupt Enable Clear |
| 0x4802 8034 | 0x4802 A034 | 0x4819 C034 | 0x4819 E034 | I2C_WE | I2C Wakeup Enable |
| 0x4802 8038 | 0x4802 A038 | 0x4819 C038 | 0x4819 E038 | I2C_DMARXENABLE_SET | Receive DMA Enable Set |
| 0x4802 803C | 0x4802 A03C | 0x4819 C03C | 0x4819 E03C | I2C_DMATXENABLE_SET | Transmit DMA Enable Set |
| 0x4802 8040 | 0x4802 A040 | 0x4819 C040 | 0x4819 E040 | I2C_DMARXENABLE_CLR | Receive DMA Enable Clear |
| 0x4802 8044 | 0x4802 A044 | 0x4819 C044 | 0x4819 E044 | I2C_DMATXENABLE_CLR | Transmit DMA Enable Clear |
| 0x4802 8048 | 0x4802 A048 | 0x4819 C048 | 0x4819 E048 | I2C_DMARXWAKE_EN | Receive DMA Wakeup |
| 0x4802 804C | 0x4802 A04C | 0x4819 C04C | 0x4819 E04C | I2C_DMATXWAKE_EN | Transmit DMA Wakeup |
| 0x4802 8090 | 0x4802 A090 | 0x4819 C090 | 0x4819 E090 | I2C_SYSS | System Status |
| 0x4802 8094 | 0x4802 A094 | 0x4819 C094 | 0x4819 E094 | I2C_BUF | Buffer Configuration |
| 0x4802 8098 | 0x4802 A098 | 0x4819 C098 | 0x4819 E098 | I2C_CNT | Data Counter |
| 0x4802 809C | 0x4802 A09C | 0x4819 C09C | 0x4819 E09C | I2C_DATA | Data Access |
| 0x4802 80A4 | 0x4802 A0A4 | 0x4819 C0A4 | 0x4819 E0A4 | I2C_CON | I2C Configuration |
| 0x4802 80A8 | 0x4802 A0A8 | 0x4819 C0A8 | 0x4819 E0A8 | I2C_OA | I2C Own Address |


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**Table 9-45. I2C Registers (continued)**

| HEX ADDRESS | | | | | |
|---|---|---|---|---|---|
| **I2C0** | **I2C1** | **I2C2** | **I2C3** | **ACRONYM** | **REGISTER NAME** |
| 0x4802 80AC | 0x4802 A0AC | 0x4819 C0AC | 0x4819 E0AC | I2C_SA | I2C Slave Address |
| 0x4802 80B0 | 0x4802 A0B0 | 0x4819 C0B0 | 0x4819 E0B0 | I2C_PSC | I2C Clock Prescaler |
| 0x4802 80B4 | 0x4802 A0B4 | 0x4819 C0B4 | 0x4819 E0B4 | I2C_SCLL | I2C SCL Low Time |
| 0x4802 80B8 | 0x4802 A0B8 | 0x4819 C0B8 | 0x4819 E0B8 | I2C_SCLH | I2C SCL High Time |
| 0x4802 80BC | 0x4802 A0BC | 0x4819 C0BC | 0x4819 E0BC | I2C_SYSTEST | System Test |
| 0x4802 80C0 | 0x4802 A0C0 | 0x4819 C0C0 | 0x4819 E0C0 | I2C_BUFSTAT | I2C Buffer Status |
| 0x4802 80C4 | 0x4802 A0C4 | 0x4819 C0C4 | 0x4819 E0C4 | I2C_OA1 | I2C Own Address 1 |
| 0x4802 80C8 | 0x4802 A0C8 | 0x4819 C0C8 | 0x4819 E0C8 | I2C_OA2 | I2C Own Address 2 |
| 0x4802 80CC | 0x4802 A0CC | 0x4819 C0CC | 0x4819 E0CC | I2C_OA3 | I2C Own Address 3 |
| 0x4802 80D0 | 0x4802 A0D0 | 0x4819 C0D0 | 0x4819 E0D0 | I2C_ACTOA | Active Own Address |
| 0x4802 80D4 | 0x4802 A0D4 | 0x4819 C0D4 | 0x4819 E0D4 | I2C_SBLOCK | I2C Clock Blocking Enable |

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### 9.11.2 I2C Electrical Data/Timing

**Table 9-46. Timing Requirements for I2C Input Timings(1)**

(see Figure 9-43)

| NO. | | | OPP100/120/166 | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | STANDARD MODE | | FAST MODE | | |
| | | | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(SCL)}$ | Cycle time, SCL | 10 | | 2.5 | | µs |
| 2 | $t_{su(SCLH-SDAL)}$ | Setup time, SCL high before SDA low (for a repeated START condition) | 4.7 | | 0.6 | | µs |
| 3 | $t_{h(SDAL-SCLL)}$ | Hold time, SCL low after SDA low (for a START and a repeated START condition) | 4 | | 0.6 | | µs |
| 4 | $t_{w(SCLL)}$ | Pulse duration, SCL low | 4.7 | | 1.3 | | µs |
| 5 | $t_{w(SCLH)}$ | Pulse duration, SCL high | 4 | | 0.6 | | µs |
| 6 | $t_{su(SDAV-SCLH)}$ | Setup time, SDA valid before SCL high | 250 | | 100(2) | | ns |
| 7 | $t_{h(SCLL-SDAV)}$ | Hold time, SDA valid after SCL low | 0(3) | 3.45(4) | 0(3) | 0.9(4) | µs |
| 8 | $t_{w(SDAH)}$ | Pulse duration, SDA high between STOP and START conditions | 4.7 | | 1.3 | | µs |
| 9 | $t_{r(SDA)}$ | Rise time, SDA | | 1000 | 20 + 0.1$C_b$ (5) | 300 | ns |
| 10 | $t_{r(SCL)}$ | Rise time, SCL | | 1000 | 20 + 0.1$C_b$ (5) | 300 | ns |
| 11 | $t_{f(SDA)}$ | Fall time, SDA | | 300 | 20 + 0.1$C_b$ (5) | 300 | ns |
| 12 | $t_{f(SCL)}$ | Fall time, SCL | | 300 | 20 + 0.1$C_b$ (5) | 300 | ns |
| 13 | $t_{su(SCLH-SDAH)}$ | Setup time, SCL high before SDA high (for STOP condition) | 4 | | 0.6 | | µs |
| 14 | $t_{w(SP)}$ | Pulse duration, spike (must be suppressed) | | | 0 | 50 | ns |
| 15 | $C_b$ (5) | Capacitive load for each bus line | | 400 | | 400 | pF |

(1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
(2) A Fast-mode I²C-bus™ device can be used in a Standard-mode I²C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq$ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_r$ max + $t_{su(SDA-SCLH)}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-Bus Specification) before the SCL line is released.
(3) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IHmin}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
(4) The maximum $t_{h(SDA-SCLL)}$ has only to be met if the device does not stretch the low period [$t_{w(SCLL)}$] of the SCL signal.
(5) $C_b$ = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

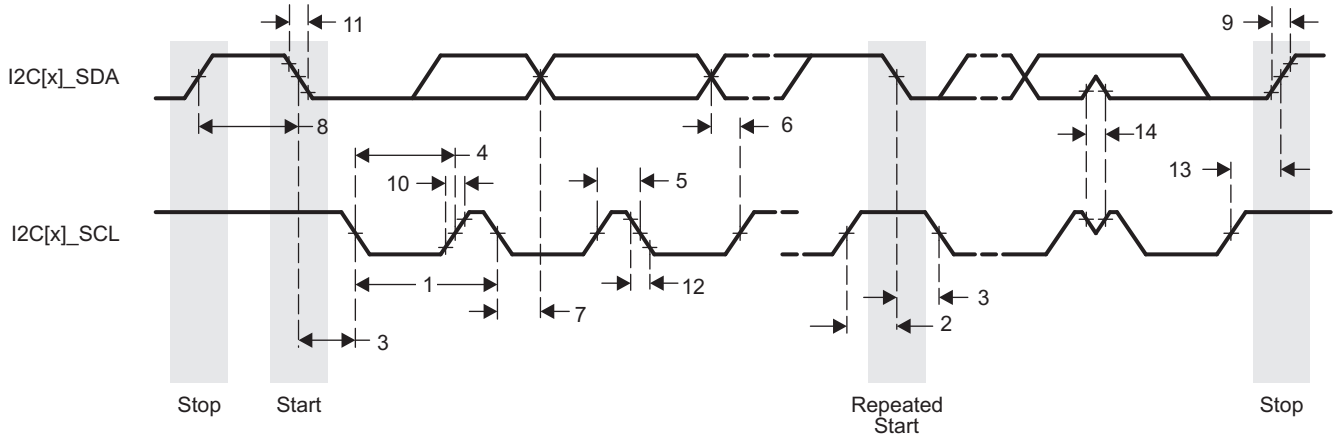


**Figure 9-43. I2C Receive Timing**


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### Table 9-47. Switching Characteristics Over Recommended Operating Conditions for I2C Output Timings

(see Figure 9-44)

| NO. | PARAMETER | | OPP100/120/166 | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | STANDARD MODE | | FAST MODE | | |
| | | | MIN | MAX | MIN | MAX | |
| 16 | $t_{c(SCL)}$ | Cycle time, SCL | 10 | | 2.5 | | µs |
| 17 | $t_{su(SCLH-SDAL)}$ | Setup time, SCL high before SDA low (for a repeated START condition) | 4.7 | | 0.6 | | µs |
| 18 | $t_{h(SDAL-SCLL)}$ | Hold time, SCL low after SDA low (for a START and a repeated START condition) | 4 | | 0.6 | | µs |
| 19 | $t_{w(SCLL)}$ | Pulse duration, SCL low | 4.7 | | 1.3 | | µs |
| 20 | $t_{w(SCLH)}$ | Pulse duration, SCL high | 4 | | 0.6 | | µs |
| 21 | $t_{su(SDAV-SCLH)}$ | Setup time, SDA valid before SCL high | 250 | | 100 | | ns |
| 22 | $t_{h(SCLL-SDAV)}$ | Hold time, SDA valid after SCL low (for I2C bus devices) | 0 | 3.45 | 0 | 0.9 | µs |
| 23 | $t_{w(SDAH)}$ | Pulse duration, SDA high between STOP and START conditions | 4.7 | | 1.3 | | µs |
| 24 | $t_{r(SDA)}$ | Rise time, SDA | | 1000 | $20 + 0.1C_b$ (1) | 300 | ns |
| 25 | $t_{r(SCL)}$ | Rise time, SCL | | 1000 | $20 + 0.1C_b$ (1) | 300 | ns |
| 26 | $t_{f(SDA)}$ | Fall time, SDA | | 300 | $20 + 0.1C_b$ (1) | 300 | ns |
| 27 | $t_{f(SCL)}$ | Fall time, SCL | | 300 | $20 + 0.1C_b$ (1) | 300 | ns |
| 28 | $t_{su(SCLH-SDAH)}$ | Setup time, SCL high before SDA high (for STOP condition) | 4 | | 0.6 | | µs |
| 29 | $C_p$ | Capacitance for each I2C pin | | 10 | | 10 | pF |

(1) $C_b$ = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

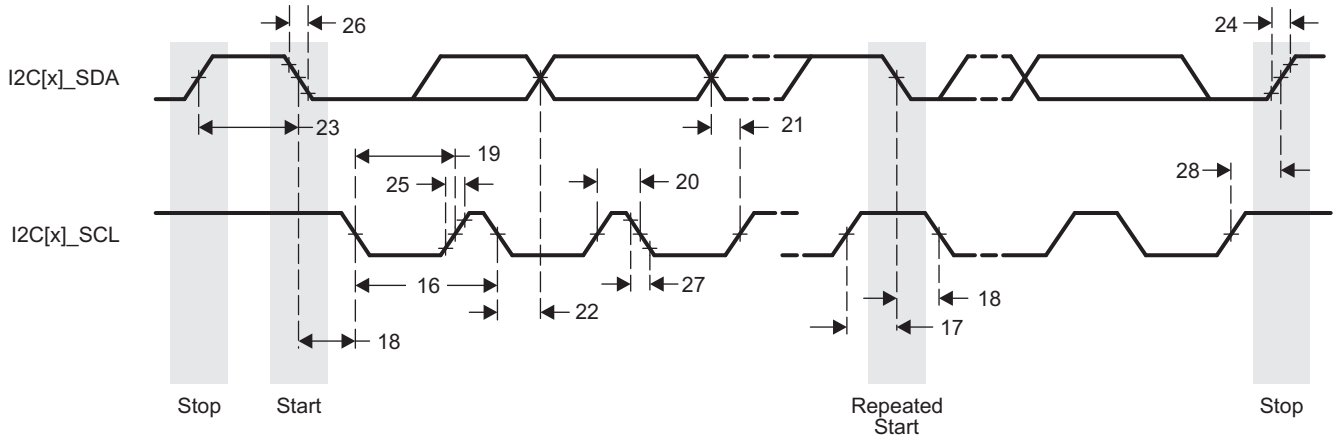


**Figure 9-44. I2C Transmit Timing**

## 9.12 Imaging Subsystem (ISS)

The device Imaging Subsystem captures and processes pixel data from external image and video inputs. The inputs can be connected to the Image Processing block through the Parallel Camera Interface (CAM) or the Serial Camera Interface (CSI2). The captured pixel data is processed by the Image Signal Processor (ISP). In addition, a Timing control module provides flash strobe and mechanical shutter interfaces. The features of each component of the ISS are described below.

- Parallel Camera (CAM) interface features:
  - Input format
    - Bayer pattern Raw (up to 16bit) or YCbCr 422 (8bit or 16bit) data.
    - ITU-R BT.656/1120 standard format
  - Generates HD/VD timing signals and field ID to an external timing generator, or can synchronize to the external timing generator.
  - Support for progressive and interlaced sensors (hardware support for up to 2 fields and firmware supports for higher number of fields, typically 3-, 4-, and 5-field sensors.
- Serial Camera Interface (CSI2) features:
  - Support for 1, 2, 3 or 4 Data-lanes at 1Gb/s per lane for up to 3 Data-lane, and 800 Mbps per lane for 4 Data-lane
  - Transfer pixels to the system memory or to the ISP
  - Error detection and correction by the protocol engine
  - DMA engine integrated with dedicated FIFO
  - 1-D and 2-D addressing mode
  - Up to 8 contexts to support 8 dedicated configurations
  - Ping-Pong mechanism for double buffering
  - All primary and secondary MIPI-defined formats are supported (RGB, RAW, YUV,…)
  - On-the-fly DPCM decompression
  - On-the-fly image cropping and A-Law/DPCM compression
- Image Sensor Interface (ISIF) features:
  - Support for up to 32K pixels (image size) in both the horizontal and vertical direction
  - Color space conversion for non-Bayer pattern Raw data
  - Digital black clamping with Horizontal/Vertical offset drift compensation
  - Vertical Line defect correction based on a lookup table
  - Color-dependent gain control and black level offset control
  - Ability to control output to the DDR2/DDR3 via an external write enable signal
  - Down sampling via programmable culling patterns
  - A-law/DPCM compression
  - Generating 16-, 12- or 8-bit output to memory


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- Image Signal Processor (ISP) features:
  - On-the-fly or memory to memory processing
  - Raw Data processing (IPIPE Front End)
    - On-the-fly or memory to memory processing
    - Supports up to 5376 pixels per line in single processing
    - Sensor data linearization for dynamic range extension
    - Programmable 2D Lens Shading Compensation (LSC) correction
    - Black level compensation
    - Defect pixel correction (LUT_DPC) with look-up table
    - Defect pixel correction (OTF_DPC) with on-the-fly detection and correction
    - Two spatial noise filtering
    - Digital gains and offset
    - A-law and DPCM compression/decompression for saving memory space
  - RGB and YUV DATA processing (IPIPE Back End)
    - Fine color correction through color correction matrices and 3D look-up table
    - Programmable Gamma Correction
    - RGB -> YUV4:2:2 : color space conversion
    - Edge Enhancement (EE)
    - False Color Suppression (FCS)
  - Two independent Resizers
    - Providing two different sizes of outputs simultaneously on one input
    - Maximum line width is 5376 and 2336, respectively
    - YUV422 to YUV420 conversion
    - Data output format: RGB565, ARGB888, YUV422 co sited and YUV4:2:0 planar
    - Resizer Ratio: x1/256 ~ x16
    - Input from IPIPE output or memory
  - Statistic data collection
    - On-the-fly or memory to memory operation
    - Data collection for 3A (Auto Exposure, White Balance, Focus)
    - Box car (sub-sampled Raw Data)
    - Histogram (Raw or Y up to 4 regions)
    - Boundary signal calculation
- Timing control module features:
  - STROBE signal for flash pre-strobe and flash strobe
  - SHUTTER signal for mechanical shutter control
  - Global reset control

For more detailed information on the ISS, see the ISS Overview section, the ISS Interfaces section, and the ISS ISP section of the *Watchdog Timer* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

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### 9.12.1 ISSCAM Electrical Data/Timing

**Table 9-48. Timing Requirements for ISSCAM (see Figure 9-45)**

| NO. | | | OPP100/120/166 | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | |
| 1 | $t_{c(PCLK)}$ | Cycle time, PCLK | 6.06 | | | ns |
| 2 | $t_{w(PCLKH)}$ | Pulse duration, PCLK high | 2.73 | | | ns |
| 3 | $t_{w(PCLKL)}$ | Pulse duration, PCLK low | 2.73 | | | ns |
| 4 | $t_{t(PCLK)}$ | Transition time, PCLK | | | 2.64 | ns |
| 5 | $t_{su(DATA-PCLK)}$ | Input setup time, Data/Control valid before PCLK high/low | 3.11 | | | ns |
| | $t_{su(DE-PCLK)}$ | | 3.11 | | | ns |
| | $t_{su(VS-PCLK)}$ | | 3.11 | | | ns |
| | $t_{su(HS-PCLK)}$ | | 3.11 | | | ns |
| | $t_{su(FLD-PCLK)}$ | | 3.11 | | | ns |
| 6 | $t_{h(PCLK-DATA)}$ | Input hold time, Data/Control valid after PCLK high/low | -0.15 | | | ns |
| | $t_{h(PCLK-DE)}$ | | -0.15 | | | ns |
| | $t_{h(PCLK-VS)}$ | | -0.15 | | | ns |
| | $t_{h(PCLK-HS)}$ | | -0.15 | | | ns |
| | $t_{h(PCLK-FLD)}$ | | -0.15 | | | ns |


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**Table 9-49. Switching Characteristics Over Recommended Operating Conditions for ISSCAM (see Figure 9-45)**

| NO. | PARAMETER | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 15 | $t_{d(PCLK-FLD)}$ | Delay time, PCLK rising/falling clock edge to Control valid | 3 | 11.5 | ns |
| 16 | $t_{d(PCLK-VS)}$ | Delay time, PCLK rising/falling clock edge to Control valid | 3 | 11.5 | ns |
| 17 | $t_{d(PCLK-HS)}$ | Delay time, PCLK rising/falling clock edge to Control valid | 3 | 11.5 | ns |
| 18 | $t_{d(PCLK-STROBE)}$ | Delay time, PCLK rising/falling clock edge to Control valid | 3 | 11.5 | ns |
| 19 | $t_{d(PCLK-SHUTTER)}$ | Delay time, PCLK rising/falling clock edge to Control valid | 3 | 11.5 | ns |

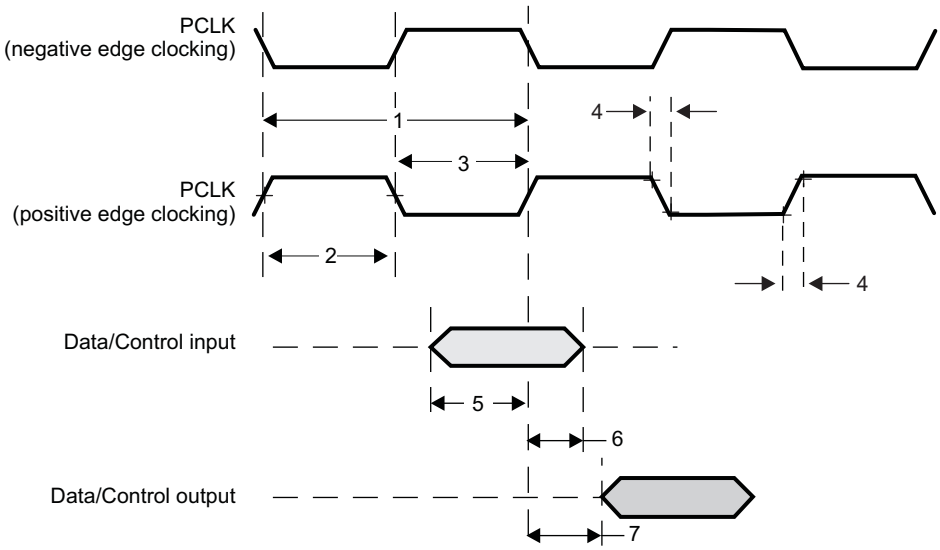


**Figure 9-45. ISSCAM Timings**

## 9.13 DDR2/DDR3 Memory Controller

The device has a dedicated interface to DDR3 and DDR2 SDRAM. The device dedicated interface also supports JEDEC standard compliant DDR2 and DDR3 SDRAM devices with the following features:

- 16-bit or 32-bit data path to external SDRAM memory
- Memory device capacity: 64Mb, 128Mb, 256Mb, 512Mb, 1Gb, 2Gb, and 4Gb devices
- Support for two independent chip selects, with their corresponding register sets, and independent page tracking
- Two interfaces with associated DDR2/DDR3 PHYs
- Dynamic memory manager allows for interleaving of data between the two DDR interfaces.

For details on the DDR2/DDR3 Memory Controller, see the *DDR2/DDR3 Memory Controller* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).


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### 9.13.1 DDR2/3 Memory Controller Register Descriptions

**Table 9-50. DDR2/3 Memory Controller Registers**

| DDR0 HEX ADDRESS | DDR1 HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|---|
| 0x4C00 0004 | 0x4D00 0004 | SDRSTAT | SDRAM Status Register |
| 0x4C00 0008 | 0x4D00 0008 | SDRCR | SDRAM Configuration Register |
| 0x4C00 000C | 0x4D00 000C | SDRCR2 | SDRAM Configuration Register 2 |
| 0x4C00 0010 | 0x4D00 0010 | SDRRCR | SDRAM Refresh Control Register |
| 0x4C00 0014 | 0x4D00 0014 | SDRRCSR | SDRAM Refresh Control Shadow Register |
| 0x4C00 0018 | 0x4D00 0018 | SDRTIM1 | SDRAM Timing 1 Register |
| 0x4C00 001C | 0x4D00 001C | SDRTIM1SR | SDRAM Timing 1 Shadow Register |
| 0x4C00 0020 | 0x4D00 0020 | SDRTIM2 | SDRAM Timing 2 Register |
| 0x4C00 0024 | 0x4D00 0024 | SDRTIM2SR | SDRAM Timing 2 Shadow Register |
| 0x4C00 0028 | 0x4D00 0028 | SDRTIM3 | SDRAM Timing 3 Register |
| 0x4C00 002C | 0x4D00 002C | SDRTIM3SR | SDRAM Timing 3 Shadow Register |
| 0x4C00 0038 | 0x4D00 0038 | PMCR | Power Management Control Register |
| 0x4C00 003C | 0x4D00 003C | PMCSR | Power Management Control Shadow Register |
| 0x4C00 0054 | 0x4D00 0054 | PBBPR | Peripheral Bus Burst Priority Register |
| 0x4C00 00A0 | 0x4D00 00A0 | EOI | End of Interrupt Register |
| 0x4C00 00A4 | 0x4D00 00A4 | SOIRSR | System OCP Interrupt Raw Status Register |
| 0x4C00 00AC | 0x4D00 00AC | SOISR | System OCP Interrupt Status Register |
| 0x4C00 00B4 | 0x4D00 00B4 | SOIESR | System OCP Interrupt Enable Set Register |
| 0x4C00 00BC | 0x4D00 00BC | SOIECR | System OCP Interrupt Enable Clear Register |
| 0x4C00 00C8 | 0x4D00 00C8 | ZQCR | SDRAM Output Impedance Calibration Configuration Register |
| 0x4C00 00D4 | 0x4D00 00D4 | RDWR_LVL_RMP_WIN | Read-Write Leveling Ramp Window Register |
| 0x4C00 00D8 | 0x4D00 00D8 | RDWR_LVL_RMP_CTRL | Read-Write Leveling Ramp Control Register |
| 0x4C00 00DC | 0x4D00 00DC | RWLCR | Read-Write Leveling Control Register |
| 0x4C00 00E4 | 0x4D00 00E4 | DDRPHYCR | DDR PHY Control Register |
| 0x4C00 00E8 | 0x4D00 00E8 | DDRPHYCSR | DDR PHY Control Shadow Register |
| 0x4C00 0100 | 0x4D00 0100 | PRI_COS_MAP | Priority to Class of Service Mapping Register |
| 0x4C00 0104 | 0x4D00 0104 | CONNID_COS_1_MAP | Connection ID to Class of Service 1 Mapping Register |
| 0x4C00 0108 | 0x4D00 0108 | CONNID_COS_2_MAP | Connection ID to Class of Service 2 Mapping Register |
| 0x4C00 0120 | 0x4D00 0120 | RD_WR_EXEC_THRSH | Read Write Execution Threshold Register |

### 9.13.2 DDR2/DDR3 PHY Register Descriptions

**Table 9-51. DDR2/DDR3 PHY Registers**

| DDR0 HEX ADDRESS | DDR1 HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|---|
| 0x47C0_C41C | 0x47C0_C81C | CMD0_REG_PHY_CTRL_SLAVE_RATIO_0 | DDR PHY Command 0 Address/Command Slave Ratio Register |
| 0x47C0_C428 | 0x47C0_C828 | CMD0_REG_PHY_DLL_LOCK_DIFF_0 | DDR PHY Command 0 Address/Command DLL Lock Difference Register |
| 0x47C0_C42C | 0x47C0_C82C | CMD0_REG_PHY_INVERT_CLKOUT_0 | DDR PHY Command 0 Invert Clockout Selection Register |
| 0x47C0_C450 | 0x47C0_C850 | CMD1_REG_PHY_CTRL_SLAVE_RATIO_0 | DDR PHY Command 1 Address/Command Slave Ratio Register |
| 0x47C0_C45C | 0x47C0_C85C | CMD1_REG_PHY_DLL_LOCK_DIFF_0 | DDR PHY Command 1 Address/Command DLL Lock Difference Register |

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**Table 9-51. DDR2/DDR3 PHY Registers (continued)**

| DDR0 HEX ADDRESS | DDR1 HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|---|
| 0x47C0_C460 | 0x47C0_C860 | CMD1_REG_PHY_INVERT_CLKOUT_0 | DDR PHY Command 1 Invert Clockout Selection Register |
| 0x47C0_C484 | 0x47C0_C884 | CMD2_REG_PHY_CTRL_SLAVE_RATIO_0 | DDR PHY Command 2 Address/Command Slave Ratio Register |
| 0x47C0_C490 | 0x47C0_C890 | CMD2_REG_PHY_DLL_LOCK_DIFF_0 | DDR PHY Command 2 Address/Command DLL Lock Difference Register |
| 0x47C0_C494 | 0x47C0_C894 | CMD2_REG_PHY_INVERT_CLKOUT_0 | DDR PHY Command 2 Invert Clockout Selection Register |
| 0x47C0_C4C8 | 0x47C0_C8C8 | DATA0_REG_PHY_RD_DQS_SLAVE_RATIO _0 | DDR PHY Data Macro 0 Read DQS Slave Ratio Register |
| 0x47C0_C4DC | 0x47C0_C8DC | DATA0_REG_PHY_WR_DQS_SLAVE_RATI O_0 | DDR PHY Data Macro 0 Write DQS Slave Ratio Register |
| 0x47C0_C4F0 | 0x47C0_C8F0 | DATA0_REG_PHY_WRLVL_INIT_RATIO_0 | DDR PHY Data Macro 0 Write Leveling Init Ratio Register |
| 0x47C0_C4F8 | 0x47C0_C8F8 | DATA0_REG_PHY_WRLVL_INIT_MODE_0 | DDR PHY Data Macro 0 Write Leveling Init Mode Ratio Selection Register |
| 0x47C0_C4FC | 0x47C0_C8FC | DATA0_REG_PHY_GATELVL_INIT_RATIO_0 | DDR PHY Data Macro 0 DQS Gate Training Init Ratio Register |
| 0x47C0_C504 | 0x47C0_C904 | DATA0_REG_PHY_GATELVL_INIT_MODE_0 | DDR PHY Data Macro 0 DQS Gate Training Init Mode Ratio Selection Register |
| 0x47C0_C508 | 0x47C0_C908 | DATA0_REG_PHY_FIFO_WE_SLAVE_RATI O_0 | DDR PHY Data Macro 0 DQS Gate Slave Ratio Register |
| 0x47C0_C51C | 0x47C0_C91C | DATA0_REG_PHY_DQ_OFFSET_0 | Offset Value From DQS to DQ for Data Macro 0 |
| 0x47C0_C520 | 0x47C0_C920 | DATA0_REG_PHY_WR_DATA_SLAVE_RATI O_0 | DDR PHY Data Macro 0 Write Data Slave Ratio Register |
| 0x47C0_C534 | 0x47C0_C934 | DATA0_REG_PHY_USE_RANK0_DELAYS | DDR PHY Data Macro 0 Delay Selection Register |
| 0x47C0_C538 | 0x47C0_C938 | DATA0_REG_PHY_DLL_LOCK_DIFF_0 | DDR PHY Data Macro 0 DLL Lock Difference Register |
| 0x47C0_C56C | 0x47C0_C96C | DATA1_REG_PHY_RD_DQS_SLAVE_RATIO _0 | DDR PHY Data Macro 1 Read DQS Slave Ratio Register |
| 0x47C0_C580 | 0x47C0_C980 | DATA1_REG_PHY_WR_DQS_SLAVE_RATI O_0 | DDR PHY Data Macro 1 Write DQS Slave Ratio Register |
| 0x47C0_C594 | 0x47C0_C994 | DATA1_REG_PHY_WRLVL_INIT_RATIO_0 | DDR PHY Data Macro 1 Write Leveling Init Ratio Register |
| 0x47C0_C59C | 0x47C0_C99C | DATA1_REG_PHY_WRLVL_INIT_MODE_0 | DDR PHY Data Macro 1 Write Leveling Init Mode Ratio Selection Register |
| 0x47C0_C5A0 | 0x47C0_C9A0 | DATA1_REG_PHY_GATELVL_INIT_RATIO_0 | DDR PHY Data Macro 1 DQS Gate Training Init Ratio Register |
| 0x47C0_C5A8 | 0x47C0_C9A8 | DATA1_REG_PHY_GATELVL_INIT_MODE_0 | DDR PHY Data Macro 1 DQS Gate Training Init Mode Ratio Selection Register |
| 0x47C0_C5AC | 0x47C0_C9AC | DATA1_REG_PHY_FIFO_WE_SLAVE_RATI O_0 | DDR PHY Data Macro 1 DQS Gate Slave Ratio Register |
| 0x47C0_C5C0 | 0x47C0_C9C0 | DATA1_REG_PHY_DQ_OFFSET_1 | Offset Value From DQS to DQ for Data Macro 1 |
| 0x47C0_C5C4 | 0x47C0_C9C4 | DATA1_REG_PHY_WR_DATA_SLAVE_RATI O_0 | DDR PHY Data Macro 1 Write Data Slave Ratio Register |
| 0x47C0_C5D8 | 0x47C0_C9D8 | DATA1_REG_PHY_USE_RANK0_DELAYS | DDR PHY Data Macro 1 Delay Selection Register |
| 0x47C0_C5DC | 0x47C0_C9DC | DATA1_REG_PHY_DLL_LOCK_DIFF_0 | DDR PHY Data Macro 1 DLL Lock Difference Register |


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**Table 9-51. DDR2/DDR3 PHY Registers (continued)**

| DDR0 HEX ADDRESS | DDR1 HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|---|
| 0x47C0_C610 | 0x47C0_CA10 | DATA2_REG_PHY_RD_DQS_SLAVE_RATIO _0 | DDR PHY Data Macro 2 Read DQS Slave Ratio Register |
| 0x47C0_C624 | 0x47C0_CA24 | DATA2_REG_PHY_WR_DQS_SLAVE_RATI O_0 | DDR PHY Data Macro 2 Write DQS Slave Ratio Register |
| 0x47C0_C638 | 0x47C0_CA38 | DATA2_REG_PHY_WRLVL_INIT_RATIO_0 | DDR PHY Data Macro 2 Write Leveling Init Ratio Register |
| 0x47C0_C640 | 0x47C0_CA40 | DATA2_REG_PHY_WRLVL_INIT_MODE_0 | DDR PHY Data Macro 2 Write Leveling Init Mode Ratio Selection Register |
| 0x47C0_C644 | 0x47C0_CA44 | DATA2_REG_PHY_GATELVL_INIT_RATIO_0 | DDR PHY Data Macro 2 DQS Gate Training Init Ratio Register |
| 0x47C0_C64C | 0x47C0_CA4C | DATA2_REG_PHY_GATELVL_INIT_MODE_0 | DDR PHY Data Macro 2 DQS Gate Training Init Mode Ratio Selection Register |
| 0x47C0_C650 | 0x47C0_CA50 | DATA2_REG_PHY_FIFO_WE_SLAVE_RATI O_0 | DDR PHY Data Macro 2 DQS Gate Slave Ratio Register |
| 0x47C0_C664 | 0x47C0_CA64 | DATA2_REG_PHY_DQ_OFFSET_2 | Offset value from DQS to DQ for Data Macro 2 |
| 0x47C0_C668 | 0x47C0_CA68 | DATA2_REG_PHY_WR_DATA_SLAVE_RATI O_0 | DDR PHY Data Macro 2 Write Data Slave Ratio Register |
| 0x47C0_C67C | 0x47C0_CA7C | DATA2_REG_PHY_USE_RANK0_DELAYS | DDR PHY Data Macro 2 Delay Selection Register |
| 0x47C0_C680 | 0x47C0_CA80 | DATA2_REG_PHY_DLL_LOCK_DIFF_0 | DDR PHY Data Macro 2 DLL Lock Difference Register |
| 0x47C0_C6B4 | 0x47C0_CAB4 | DATA3_REG_PHY_RD_DQS_SLAVE_RATIO _0 | DDR PHY Data Macro 3 Read DQS Slave Ratio Register |
| 0x47C0_C6C8 | 0x47C0_CAC8 | DATA3_REG_PHY_WR_DQS_SLAVE_RATI O_0 | DDR PHY Data Macro 3 Write DQS Slave Ratio Register |
| 0x47C0_C6DC | 0x47C0_CADC | DATA3_REG_PHY_WRLVL_INIT_RATIO_0 | DDR PHY Data Macro 3 Write Leveling Init Ratio Register |
| 0x47C0_C6E4 | 0x47C0_CAE4 | DATA3_REG_PHY_WRLVL_INIT_MODE_0 | DDR PHY Data Macro 3 Write Leveling Init Mode Ratio Selection Register |
| 0x47C0_C6E8 | 0x47C0_CAE8 | DATA3_REG_PHY_GATELVL_INIT_RATIO_0 | DDR PHY Data Macro 3 DQS Gate Training Init Ratio Register |
| 0x47C0_C6F0 | 0x47C0_CAF0 | DATA3_REG_PHY_GATELVL_INIT_MODE_0 | DDR PHY Data Macro 3 DQS Gate Training Init Mode Ratio Selection Register |
| 0x47C0_C6F4 | 0x47C0_CAF4 | DATA3_REG_PHY_FIFO_WE_SLAVE_RATI O_0 | DDR PHY Data Macro 3 DQS Gate Slave Ratio Register |
| 0x47C0_C708 | 0x47C0_CB08 | DATA3_REG_PHY_DQ_OFFSET_3 | Offset Value From DQS to DQ for Data Macro 3 |
| 0x47C0_C70C | 0x47C0_CB0C | DATA3_REG_PHY_WR_DATA_SLAVE_RATI O_0 | DDR PHY Data Macro 3 Write Data Slave Ratio Register |
| 0x47C0_C720 | 0x47C0_CB20 | DATA3_REG_PHY_USE_RANK0_DELAYS | DDR PHY Data Macro 3 Delay Selection Register |
| 0x47C0_C724 | 0x47C0_CB24 | DATA3_REG_PHY_DLL_LOCK_DIFF_0 | DDR PHY Data Macro 3 DLL Lock Difference Register |

### *9.13.3 DDR-Related Control Module Registers Description*

**Table 9-52. DDR-Related Control Module Registers**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4814 0694 | EMIF_CLK_GATE | EMIF0/1 PHY Clock Gate Control Register |
| 0x4814 0E04 | DDR0_IO_CTRL | DDR Memory Controller_0 IO Control Register |
| 0x4814 0E08 | DDR1_IO_CTRL | DDR Memory Controller_1 IO Control Register |

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**Table 9-52. DDR-Related Control Module Registers (continued)**

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4814 0E0C | DDR_VTP_CTRL_0 | DDR0 VTP Control Register |
| 0x4814 0E10 | DDR_VTP_CTRL_1 | DDR1 VTP Control Register |

### *9.13.4 DDR2/DDR3 Memory Controller Electrical Data/Timing*

TI only supports board designs that follow the DDR2 and DDR3 Routing Specifications outlined in this document. The switching characteristics and the timing diagram for the DDR2 memory controller are shown in Table 9-53 and Figure 9-46.

**Table 9-53. Switching Characteristics Over Recommended Operating Conditions for DDR2/DDR3 Memory Controller (1)**

| NO. | | | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| 1 | $t_{c(DDR_CLK)}$ | Cycle time, DDR[x]_CLK | DDR2 mode | 2.5 | | ns |
| | | | DDR3 mode | 1.876 | | |

(1) The PLL_DDR Controller *must* be programmed such that the resulting DDR[x]_CLK clock frequency is within the specified range.

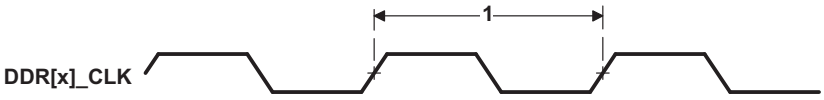


**Figure 9-46. DDR2/DDR3 Memory Controller Clock Timing**

#### 9.13.4.1 DDR2 Routing Specifications

##### *9.13.4.1.1 DDR2 Interface*

This section provides the timing specification for the DDR2 interface as a PCB design and manufacturing specification. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. These rules, when followed, result in a reliable DDR2 memory system without the need for a complex timing closure process. For more information regarding the guidelines for using this DDR2 specification, see the *Understanding TI's PCB Routing Rule-Based DDR Timing Specification* Application Report (Literature Number: SPRAAV0).

###### *9.13.4.1.1.1 DDR2 Interface Schematic*

Figure 9-47 shows the DDR2 interface schematic for a x32 DDR2 memory system. In Figure 9-48 the x16 DDR2 system schematic is identical except that the high-word DDR2 device is deleted.

When not using all or part of a DDR2 interface, the proper method of handling the unused pins is to tie off the DDR[x]_DQS[n] pins to the corresponding DVDD_DDR[x] supply via a 1k-Ω resistor and pulling the DDR[x]_DQS[n] pins to ground via a 1k-Ω resistor. This needs to be done for each byte not used. Also, include the 50-Ω pulldown for DDR[x]_VTP. The DVDD_DDR[x] and VREFSSTL_DDR[x] power supply pins need to be connected to their respective power supplies even if DDR[x] is not being used. All other DDR interface pins can be left unconnected. Note that the supported modes for use of the DDR EMIF are 32-bits wide, 16-bits wide, or not used.


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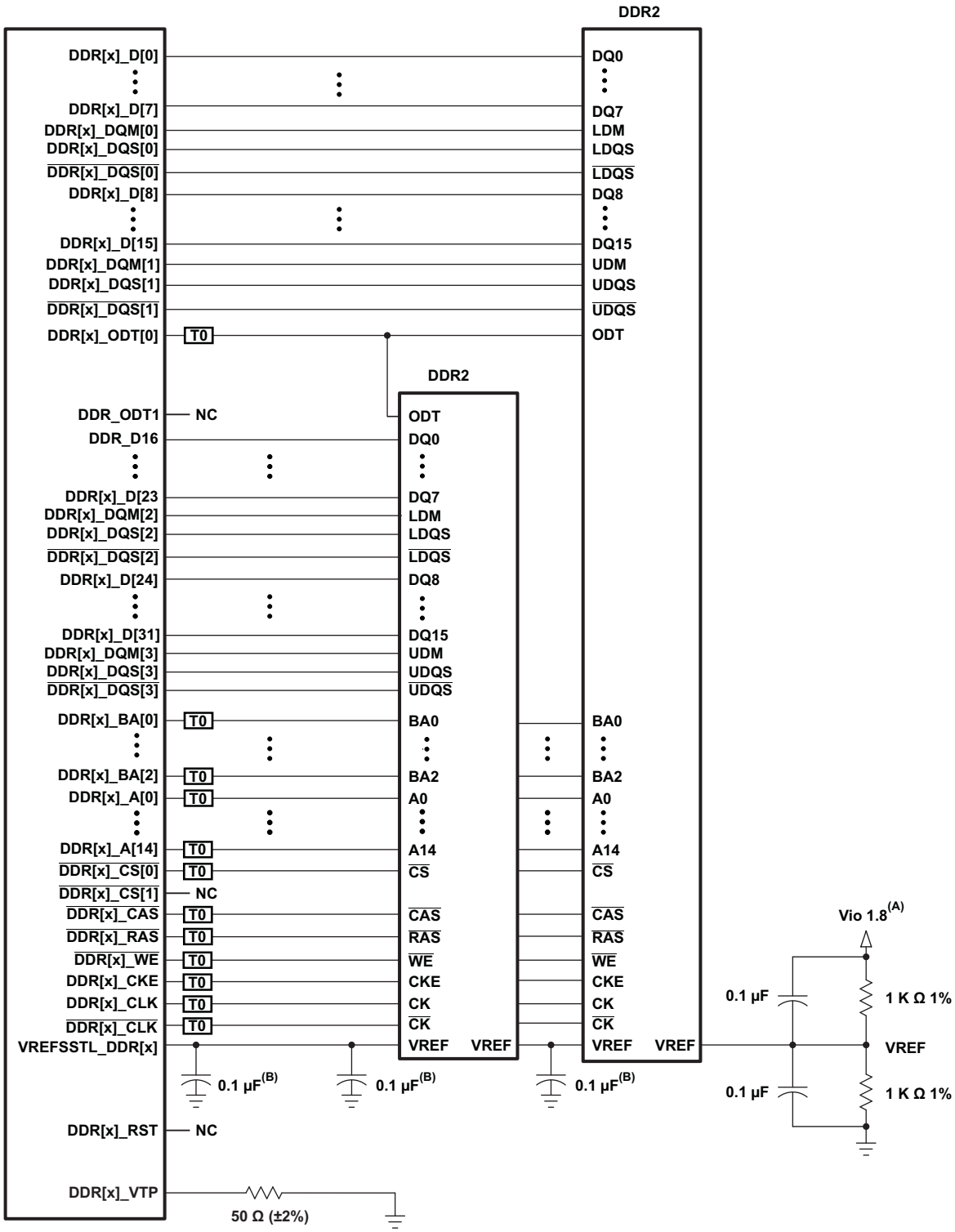
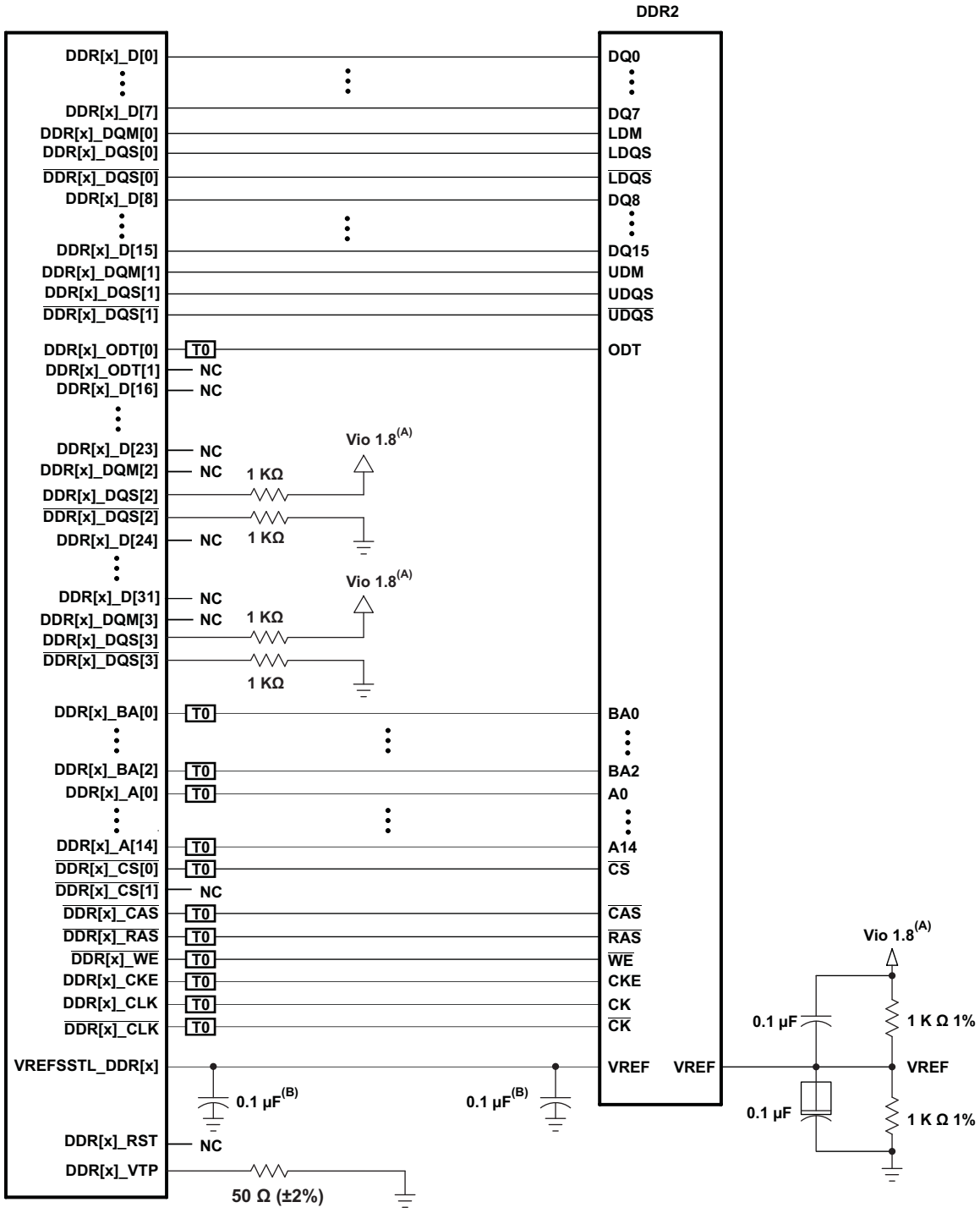



T0 Termination is required. See terminator comments.

A. Vio1.8 is the power supply for the DDR2 memories and the DM8127 DDR2 interface.

B. One of these capacitors can be eliminated if the divider and its capacitors are placed near a VREF pin.

**Figure 9-47. 32-Bit DDR2 High-Level Schematic**




T0 Termination is required. See terminator comments.

A. Vio1.8 is the power supply for the DDR2 memories and the DM8127 DDR2 interface.

B. One of these capacitors can be eliminated if the divider and its capacitors are placed near a VREF pin.

**Figure 9-48. 16-Bit DDR2 High-Level Schematic**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#### 9.13.4.1.1.2 Compatible JEDEC DDR2 Devices

Table 9-54 shows the parameters of the JEDEC DDR2 devices that are compatible with this interface. Generally, the DDR2 interface is compatible with x16 DDR2-800 speed grade DDR2 devices.

**Table 9-54. Compatible JEDEC DDR2 Devices (Per Interface)**

| NO. | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| 1 | JEDEC DDR2 device speed grade(1) | DDR2-800 | | |
| 2 | JEDEC DDR2 device bit width | x16 | x16 | Bits |
| 3 | JEDEC DDR2 device count(2) | 1 | 2 | Devices |
| 4 | JEDEC DDR2 device ball count(3) | 84 | 92 | Balls |

(1) Higher DDR2 speed grades are supported due to inherent JEDEC DDR2 backwards compatibility.
(2) One DDR2 device is used for a 16-bit DDR2 memory system. Two DDR2 devices are used for a 32-bit DDR2 memory system.
(3) The 92-ball devices are retained for legacy support. New designs will migrate to 84-ball DDR2 devices. Electrically, the 92- and 84-ball DDR2 devices are the same.

#### 9.13.4.1.1.3 PCB Stackup

The minimum stackup required for routing the DM8127 device is a six-layer stackup as shown in Table 9-55. Additional layers may be added to the PCB stackup to accommodate other circuitry or to reduce the size of the PCB footprint.

**Table 9-55. Minimum PCB Stackup**

| LAYER | TYPE | DESCRIPTION |
|---|---|---|
| 1 | Signal | Top routing mostly horizontal |
| 2 | Plane | Ground |
| 3 | Plane | Power |
| 4 | Signal | Internal routing |
| 5 | Plane | Ground |
| 6 | Signal | Bottom routing mostly vertical |

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Complete stackup specifications are provided in Table 9-56.

**Table 9-56. PCB Stackup Specifications**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | PCB routing/plane layers | 6 | | | |
| 2 | Signal routing layers | 3 | | | |
| 3 | Full ground layers under DDR2 routing region | 2 | | | |
| 4 | Number of ground plane cuts allowed within DDR routing region | | | 0 | |
| 5 | Number of ground reference planes required for each DDR2 routing layer | 1 | | | |
| 6 | Number of layers between DDR2 routing layer and reference ground plane | | | 0 | |
| 7 | PCB routing feature size | | 4 | | Mils |
| 8 | PCB trace width, w | | 4 | | Mils |
| 9 | PCB BGA escape via pad size(1) | | 18 | 20 | Mils |
| 10 | PCB BGA escape via hole size(1) | | 10 | | Mils |
| 11 | Processor BGA pad size | | 0.4 | | mm |
| 13 | Single-ended impedance, Zo | 50 | | 75 | Ω |
| 14 | Impedance control(2) | Z-5 | Z | Z+5 | Ω |

(1) A 20/10 via may be used if enough power routing resources are available. An 18/10 via allows for more flexible power routing to the processor.
(2) Z is the nominal singled-ended impedance selected for the PCB specified by item 13.


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#### 9.13.4.1.1.4 Placement

Figure 9-49 shows the required placement for the processor as well as the DDR2 devices. The dimensions for this figure are defined in Table 9-57. The placement does not restrict the side of the PCB on which the devices are mounted. The ultimate purpose of the placement is to limit the maximum trace lengths and allow for proper routing space. For a 16-bit DDR memory system, the high-word DDR2 device is omitted from the placement.

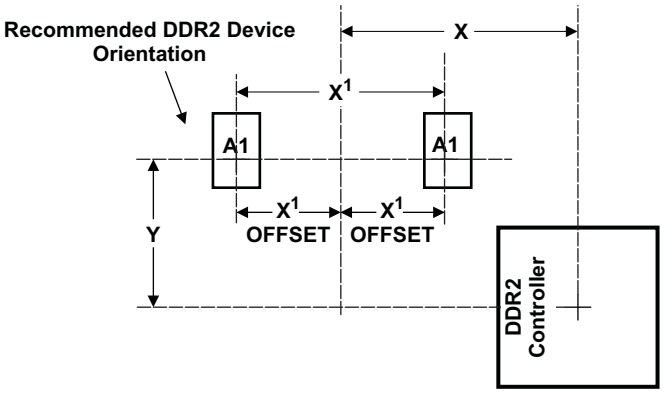


**Figure 9-49. DM8127 Device and DDR2 Device Placement**

**Table 9-57. Placement Specifications**

| NO. | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| 1 | X + Y (1) (2) | | 1660 | Mils |
| 2 | X' (1) (2) | | 1280 | Mils |
| 3 | X' Offset (1) (2) (3) | | 650 | Mils |
| 4 | DDR2 keepout region (4) | | | |
| 5 | Clearance from non-DDR2 signal to DDR2 keepout region (5) | 4 | | w |

(1) For dimension definitions, see Figure 9-47.
(2) Measurements from center of processor to center of DDR2 device.
(3) For 16-bit memory systems, it is recommended that X' offset be as small as possible.
(4) DDR2 keepout region to encompass entire DDR2 routing area.
(5) Non-DDR2 signals allowed within DDR2 keepout region provided they are separated from DDR2 routing layers by a ground plane.

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#### 9.13.4.1.1.5 DDR2 Keepout Region

The region of the PCB used for the DDR2 circuitry must be isolated from other signals. The DDR2 keepout region is defined for this purpose and is shown in Figure 9-50. The size of this region varies with the placement and DDR routing. Additional clearances required for the keepout region are shown in Table 9-57.

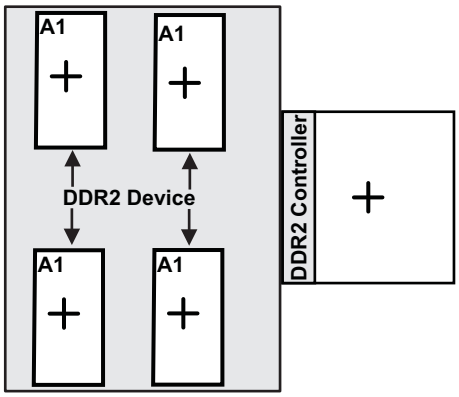


**Figure 9-50. DDR2 Keepout Region**

**NOTE**

The region shown in should encompass all the DDR2 circuitry and varies depending on placement. Non-DDR2 signals should not be routed on the DDR signal layers within the DDR2 keepout region. Non-DDR2 signals may be routed in the region, provided t hey are routed on layers separated from DDR2 signal layers by a ground layer. No breaks should be allowed in the reference ground layers in this region. In addition, the 1.8-V power plane should cover the entire keepout region. Routes for the two DDR interfaces must be separated by at least 4x; the more separation, the better.

#### 9.13.4.1.1.6 Bulk Bypass Capacitors

Bulk bypass capacitors are required for moderate speed bypassing of the DDR2 and other circuitry. Table 9-58 contains the minimum numbers and capacitance required for the bulk bypass capacitors. Note that this table only covers the bypass needs of the DDR2 interfaces and DDR2 device. Additional bulk bypass capacitance may be needed for other circuitry.

**Table 9-58. Bulk Bypass Capacitors**

| No. | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| 1 | DVDD18 bulk bypass capacitor count(1) | 6 | | Devices |
| 2 | DVDD18 bulk bypass total capacitance | 60 | | µF |
| 3 | DDR#1 bulk bypass capacitor count(1) | 1 | | Devices |
| 4 | DDR#1 bulk bypass total capacitance(1) | 10 | | µF |
| 5 | DDR#2 bulk bypass capacitor count(2) | 1 | | Devices |
| 6 | DDR#2 bulk bypass total capacitance(1)(2) | 10 | | µF |

(1) These devices should be placed near the device they are bypassing, but preference should be given to the placement of the high-speed (HS) bypass capacitors. Use half of these capacitors for DDR[0] and half for DDR[1].
(2) Only used on 32-bit wide DDR2 memory systems.


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#### 9.13.4.1.1.7 High-Speed Bypass Capacitors

High-speed (HS) bypass capacitors are critical for proper DDR2 interface operation. It is particularly important to minimize the parasitic series inductance of the HS bypass capacitors, processor/DDR power, and processor/DDR ground connections. Table 9-59 contains the specification for the HS bypass capacitors as well as for the power connections on the PCB.

**Table 9-59. High-Speed Bypass Capacitors**

| NO. | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| 1 | HS bypass capacitor package size(1) | | 0402 | 10 Mils |
| 2 | Distance from HS bypass capacitor to device being bypassed | | 250 | Mils |
| 3 | Number of connection vias for each HS bypass capacitor(2) | 2 | | Vias |
| 4 | Trace length from bypass capacitor contact to connection via | 1 | 30 | Mils |
| 5 | Number of connection vias for each processor power/ground ball | 1 | | Vias |
| 6 | Trace length from processor power/ground ball to connection via | | 35 | Mils |
| 7 | Number of connection vias for each DDR2 device power/ground ball | 1 | | Vias |
| 8 | Trace length from DDR2 device power/ground ball to connection via | | 35 | Mils |
| 9 | DVDD18 HS bypass capacitor count(3)(4) | 40 | | Devices |
| 10 | DVDD18 HS bypass capacitor total capacitance(5) | 2.4 | | µF |
| 11 | DDR device HS bypass capacitor count(6)(7) | 8 | | Devices |
| 12 | DDR device HS bypass capacitor total capacitance(7) | 0.4 | | µF |

(1) LxW, 10-mil units, that is, a 0402 is a 40x20-mil surface-mount capacitor.
(2) An additional HS bypass capacitor can share the connection vias only if it is mounted on the opposite side of the board.
(3) These devices should be placed as close as possible to the device being bypassed.
(4) Use half of these capacitors for DDR[0] and half for DDR[1].
(5) Use half of these capacitors for DDR[0] and half for DDR[1].
(6) These devices should be placed as close as possible to the device being bypassed.
(7) Per DDR device.

#### 9.13.4.1.1.8 Net Classes

Table 9-60 lists the clock net classes for the DDR2 interface. Table 9-61 lists the signal net classes, and associated clock net classes, for the signals in the DDR2 interface. These net classes are used for the termination and routing rules that follow.

**Table 9-60. Clock Net Class Definitions**

| CLOCK NET CLASS | PROCESSOR PIN NAMES |
|---|---|
| CK | DDR[x]_CLK/$\overline{\text{DDR[x]_CLK}}$ |
| DQS0 | DDR[x]_DQS[0]/$\overline{\text{DDR[x]_DQS[0]}}$ |
| DQS1 | DDR[x]_DQS[1]/$\overline{\text{DDR[x]_DQS[1]}}$ |
| DQS2(1) | DDR[x]_DQS[2]/$\overline{\text{DDR[x]_DQS[2]}}$ |
| DQS3(1) | DDR[x]_DQS[3]/$\overline{\text{DDR[x]_DQS[3]}}$ |

(1) Only used on 32-bit wide DDR2 memory systems.

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**Table 9-61. Signal Net Class Definitions**

| CLOCK NET CLASS | ASSOCIATED CLOCK NET CLASS | PROCESSOR PIN NAMES |
|---|---|---|
| ADDR_CTRL | CK | DDR[x]_BA[2:0], DDR[x]_A[14:0], DDR[x]_CS[x], DDR[x]_CAS, DDR[x]_RAS, DDR[x]_WE, DDR[x]_CKE, DDR[x]_ODT[x] |
| DQ0 | DQS0 | DDR[x]_D[7:0], DDR[x]_DQM[0] |
| DQ1 | DQS1 | DDR[x]_D[15:8], DDR[x]_DQM[1] |
| DQ2(1) | DQS2 | DDR[x]_D[23:16], DDR[x]_DQM[2] |
| DQ3(1) | DQS3 | DDR[x]_D[31:24], DDR[x]_DQM[3] |

(1) Only used on 32-bit wide DDR2 memory systems.

#### *9.13.4.1.1.9 DDR2 Signal Termination*

Signal terminators are required in CK and ADDR_CTRL net classes. Serial terminators may be used on data lines to reduce EMI risk; however, serial terminations are the only type permitted. ODTs are integrated on the data byte net classes. They should be enabled to ensure signal integrity.Table 9-62 shows the specifications for the series terminators.

**Table 9-62. DDR2 Signal Terminations**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | CK net class(1)(2) | 0 | | 10 | Ω |
| 2 | ADDR_CTRL net class(1) (2)(3)(4) | 0 | 22 | Zo | Ω |
| 3 | Data byte net classes (DQS0-DQS3, DQ0-DQ3)(5) | 0 | | Zo | Ω |

(1) Only series termination is permitted, parallel or SST specifically disallowed on board.
(2) Only required for EMI reduction.
(3) Terminator values larger than typical only recommended to address EMI issues.
(4) Termination value should be uniform across net class.
(5) No external terminations allowed for data byte net classes. ODT is to be used.

#### *9.13.4.1.1.10 VREFSSTL_DDR Routing*

VREFSSTL_DDR is used as a reference by the input buffers of the DDR2 memories as well as the processor. VREF is intended to be half the DDR2 power supply voltage and should be created using a resistive divider as shown in Figure 9-48. Other methods of creating VREF are not recommended. Figure 9-51 shows the layout guidelines for VREF.

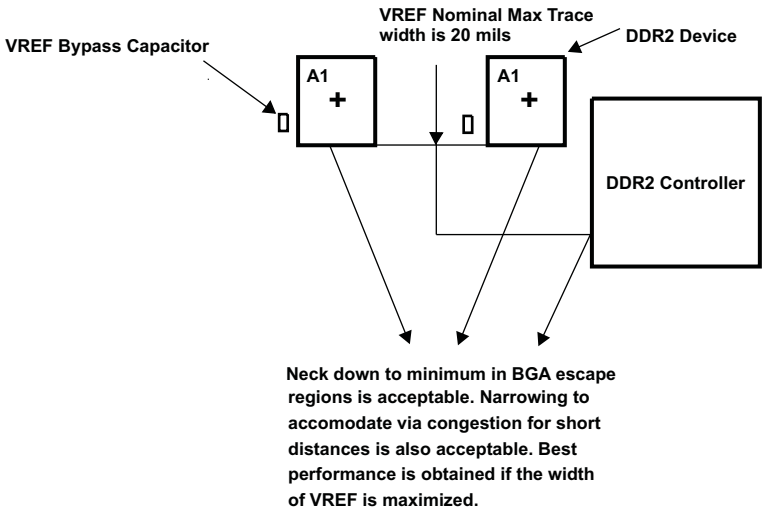


**Figure 9-51. VREF Routing and Topology**


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#### 9.13.4.1.2 DDR2 CK and ADDR_CTRL Routing

Figure 9-52 shows the topology of the routing for the CK and ADDR_CTRL net classes. The route is a balanced *T* as it is intended that the length of segments B and C be equal. In addition, the length of A (A'+A") should be maximized.

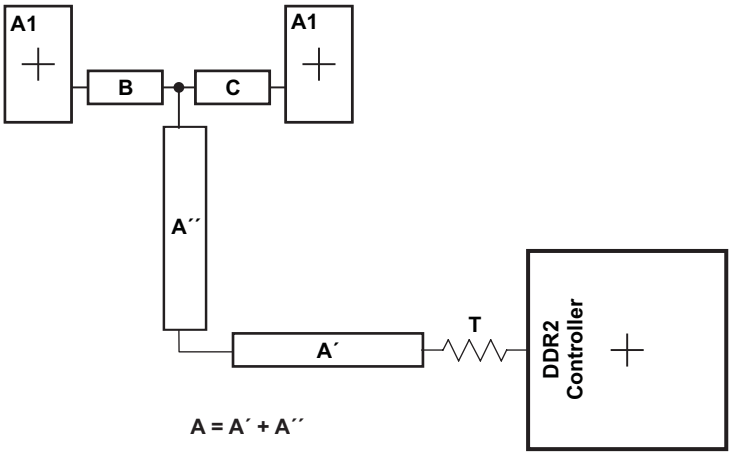


**Figure 9-52. CK and ADDR_CTRL Routing and Topology**

**Table 9-63. CK and ADDR_CTRL Routing Specification (1)**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | Center-to-center CK-$\overline{CK}$ spacing | | | 2w | |
| 2 | CK/$\overline{CK}$ skew(1) | | | 25 | Mils |
| 3 | CK A-to-B/A-to-C skew length mismatch(2) | | | 25 | Mils |
| 4 | CK B-to-C skew length mismatch | | | 25 | Mils |
| 5 | Center-to-center CK to other DDR2 trace spacing(3) | 4w | | | |
| 6 | CK/ADDR_CTRL nominal trace length(4) | CACLM-50 | CACLM | CACLM+50 | Mils |
| 7 | ADDR_CTRL-to-CK skew length mismatch | | | 100 | Mils |
| 8 | ADDR_CTRL-to-ADDR_CTRL skew length mismatch | | | 100 | Mils |
| 9 | Center-to-center ADDR_CTRL to other DDR2 trace spacing(3) | 4w | | | |
| 10 | Center-to-center ADDR_CTRL to other ADDR_CTRL trace spacing(3) | 3w | | | |
| 11 | ADDR_CTRL A-to-B/A-to-C skew length mismatch(2) | | | 100 | Mils |
| 12 | ADDR_CTRL B-to-C skew length mismatch | | | 100 | Mils |

(1) The length of segment A = A' + A″ as shown in Figure 9-52.
(2) Series terminator, if used, should be located closest to the processor.
(3) Center-to-center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.
(4) CACLM is the longest Manhattan distance of the CK and ADDR_CTRL net classes.

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Figure 9-53 shows the topology and routing for the DQS and DQ net classes; the routes are point to point. Skew matching across bytes is not needed nor recommended.

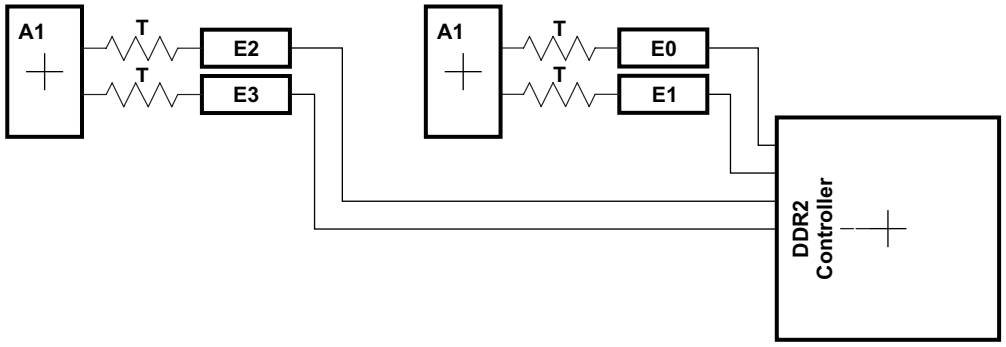


**Figure 9-53. DQS and DQ Routing and Topology**


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**Table 9-64. DQS and DQ Routing Specification**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | Center-to-center DQS-DQSn spacing in E0\|E1\|E2\|E3 | | | 2w | |
| 2 | DQS-DQSn skew in E0\|E1\|E2\|E3 | | | 25 | Mils |
| 3 | Center-to-center DQS to other DDR2 trace spacing(1) | 4w | | | |
| 4 | DQS/DQ nominal trace length (2)(3)(4) | DQLM-50 | DQLM | DQLM+50 | Mils |
| 5 | DQ-to-DQS skew length mismatch(2)(3)(4) | | | 100 | Mils |
| 6 | DQ-to-DQ skew length mismatch(2)(3)(4) | | | 100 | Mils |
| 7 | DQ-to-DQ/DQS via count mismatch(2)(3)(4) | | | 1 | Vias |
| 8 | Center-to-center DQ to other DDR2 trace spacing(1)(5) | 4w | | | |
| 9 | Center-to-center DQ to other DQ trace spacing(1)(6)(7) | 3w | | | |
| 10 | DQ/DQS E skew length mismatch(2)(3)(4) | | | 100 | Mils |

(1) Center-to-center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.
(2) A 16-bit DDR memory system has two sets of data net classes; one for data byte 0, and one for data byte 1, each with an associated DQS (2 DQSs) per DDR EMIF used.
(3) A 32-bit DDR memory system has four sets of data net classes; one each for data bytes 0 through 3, and each associated with a DQS (4 DQSs) per DDR EMIF used.
(4) There is no need, and it is not recommended, to skew match across data bytes; that is, from DQS0 and data byte 0 to DQS1 and data byte 1.
(5) DQs from other DQS domains are considered *other DDR2 trace*.
(6) DQs from other data bytes are considered *other DDR2 trace*.
(7) DQLM is the longest Manhattan distance of each of the DQS and DQ net classes.

### 9.13.4.2 DDR3 Routing Specifications

#### *9.13.4.2.1 DDR3 versus DDR2*

This specification only covers PCB designs that utilize DDR3 memory. PCB designs using other types of DDR memory should follow the specification appropriate for that type of memory. It is currently not possible to design a single PCB that supports multiple types of DDR memory.

#### *9.13.4.2.2 DDR3 EMIFs*

A processor may contain more than one EMIF. This specification covers only one EMIF and needs to be implemented for each additional EMIF. Requirements are identical between the EMIFs, however, the PCB layouts will most likely be different.

#### *9.13.4.2.3 DDR3 Device Combinations*

Since there are several possible combinations of device counts and single- or dual-side mounting, Table 9-65 summarizes the supported device configurations.

**Table 9-65. Supported DDR3 Device Combinations(1)**

| NUMBER OF DDR3 DEVICES | DDR3 DEVICE WIDTH (BITS) | MIRRORED? | DDR3 EMIF WIDTH (BITS) |
|---|---|---|---|
| 1 | 16 | N | 16 |
| 2 | 8 | Y(2) | 16 |
| 2 | 16 | N | 32 |
| 2 | 16 | Y(2) | 32 |
| 4 | 8 | N | 32 |
| 4 | 8 | Y(3) | 32 |

(1) This table is per EMIF.
(2) Two DDR3 devices are mirrored when one device is placed on the top of the board and the second device is placed on the bottom of the board.
(3) This is two mirrored pairs of DDR3 devices.

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#### 9.13.4.2.4 DDR3 Interface Schematic

The DDR3 interface schematic varies, depending upon the width of the DDR3 devices used and the width of the bus used (16 or 32 bits). General connectivity is straightforward and very similar. 16-bit DDR devices look like two 8-bit devices. Figure 9-54 and Figure 9-55 show the schematic connections for 32-bit interfaces using x16 and x8 devices.

Note that a 16-bit wide interface schematic is practically identical to the 32-bit interface; only the high-word DDR memories are removed.

When not using all or part of a DDR3 interface, the proper method of handling the unused pins is to tie off the DDR[x]_DQS[n] pins to the corresponding DVDD_DDR[x] supply via a 1-kΩ resistor and pulling the $\overline{\text{DDR[x]_DQS[n]}}$ pins to ground via a 1k-Ω resistor. This needs to be done for each byte not used. Although these signals have internal pullups and pulldowns, external pullups and pulldowns provide additional protection against external electrical noise causing activity on the signals.Also, include the 50-Ω pulldown for DDR[x]_VTP. The DVDD_DDR[x] and VREFSSTL_DDR[x] power supply pins need to be connected to their respective power supplies even if DDR[x] is not being used. All other DDR interface pins can be left unconnected. Note that the supported modes for use of the DDR EMIF are 32 bits wide, 16 bits wide, or not used.


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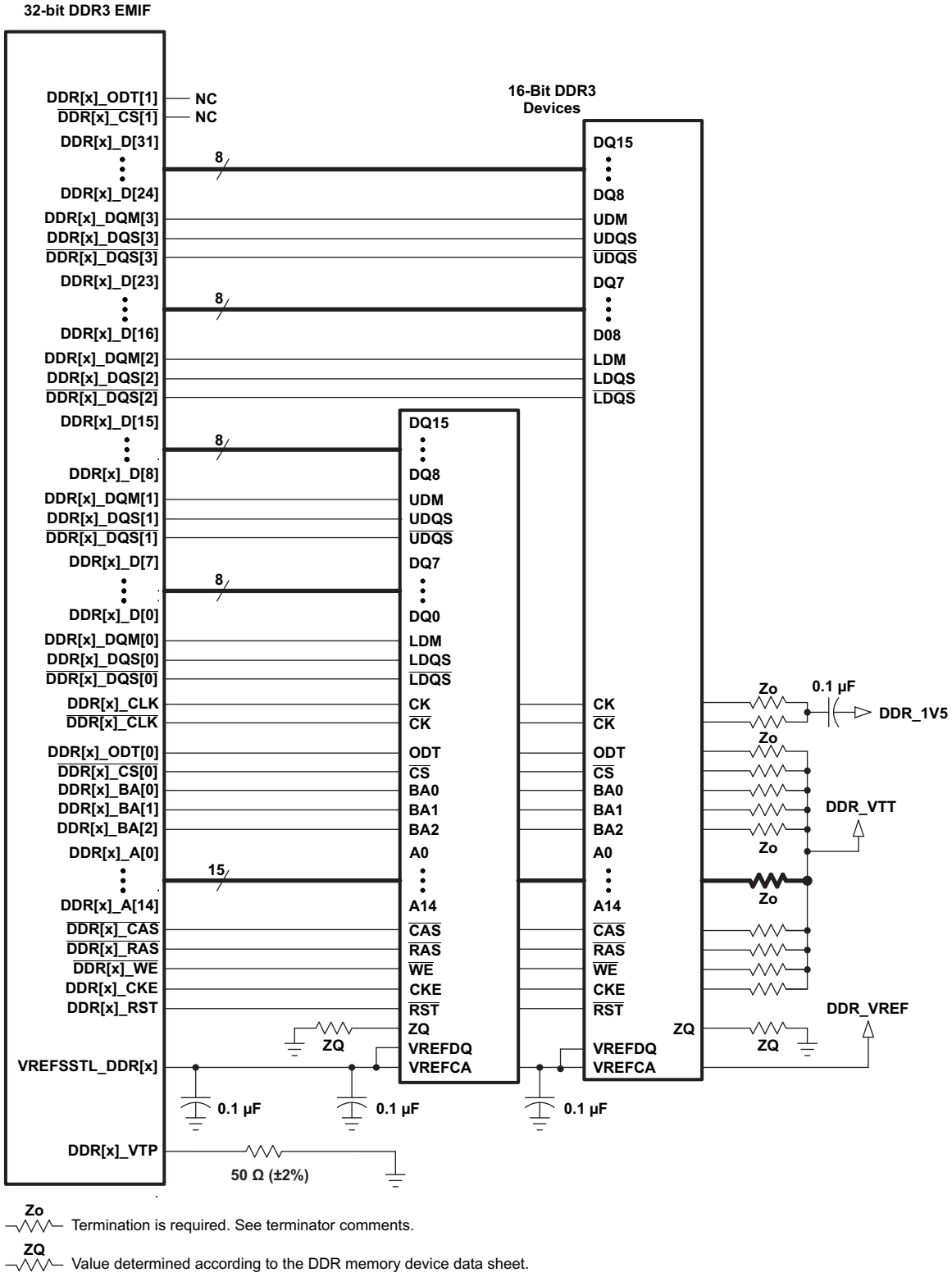
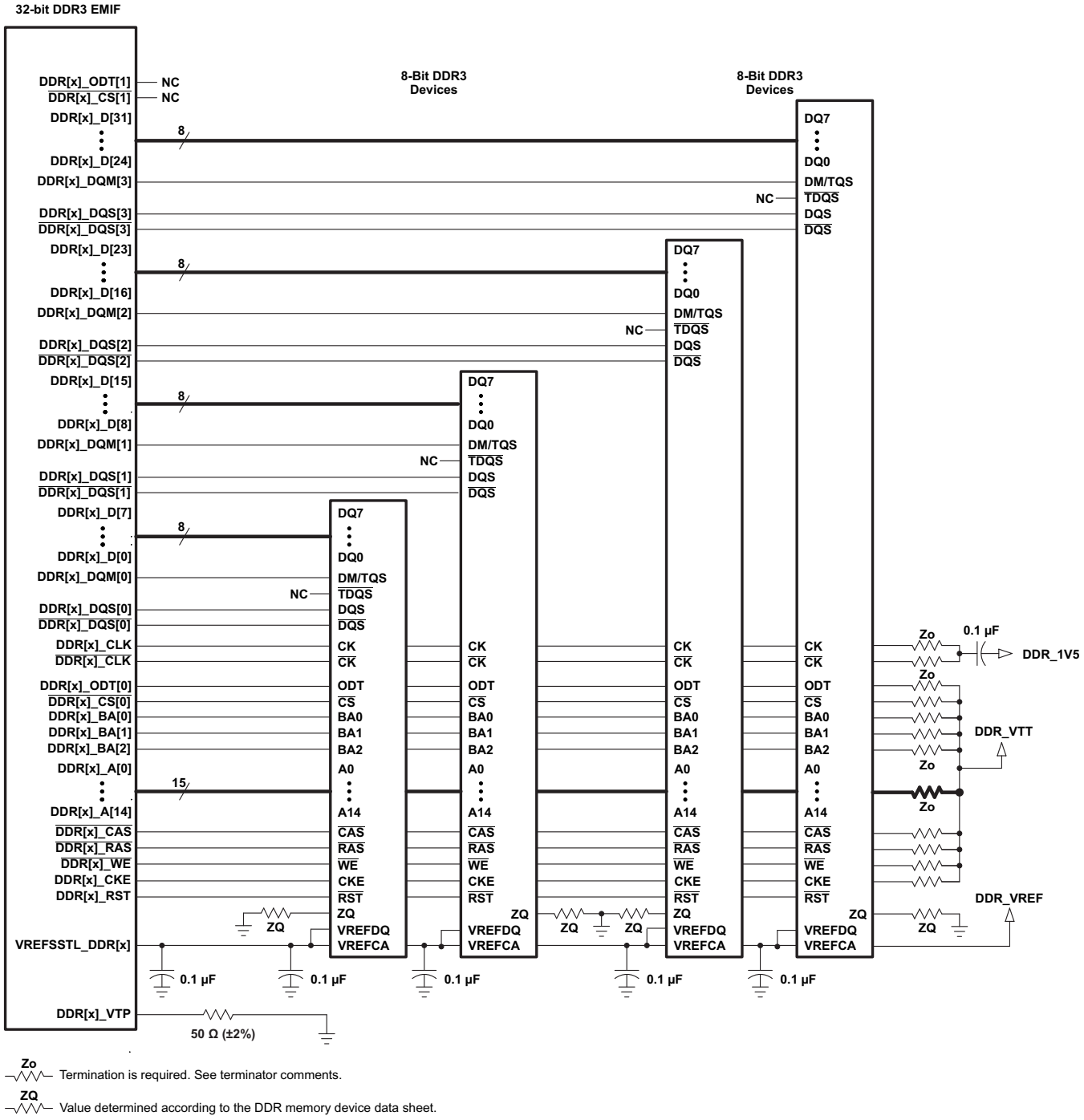



**Figure 9-54. 32-Bit, One-Bank DDR3 Interface Schematic Using Two 16-Bit DDR3 Devices**




Zo — Termination is required. See terminator comments.

ZQ — Value determined according to the DDR memory device data sheet.

**Figure 9-55. 32-Bit, One-Bank DDR3 Interface Schematic Using Four 8-Bit DDR3 Devices**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#### 9.13.4.2.4.1 Compatible JEDEC DDR3 Devices

Table 9-66 shows the parameters of the JEDEC DDR3 devices that are compatible with this interface. Generally, the DDR3 interface is compatible with DDR3-1600 devices in the x8 or x16 widths.

**Table 9-66. Compatible JEDEC DDR3 Devices (Per Interface)**

| NO. | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| 1 | JEDEC DDR3 device speed grade(1) | DDR3-800 | DDR3-1600(2) | |
| 2 | JEDEC DDR3 device bit width | x8 | x16 | Bits |
| 3 | JEDEC DDR3 device count(3) | 2 | 8 | Devices |

(1) DDR3 speed grade depends on desired clock rate. Data rate is 2x the clock rate. For DDR3-800, the clock rate is 400 MHz.
(2) DDR3 devices with speed grades up to DDR3-1600 are supported; however, max clock rate will still be limited to 533 MHz as stated in *Switching Characteristics Over Recommended Operating Conditions for DDR3 Memory Controller*.
(3) For valid DDR3 device configurations and device counts, see Section 9.13.4.2.4, Figure 9-54, and Figure 9-55.

#### 9.13.4.2.4.2 PCB Stackup

The minimum stackup for routing the DDR3 interface is a four-layer stack up as shown in Table 9-67. Additional layers may be added to the PCB stackup to accommodate other circuitry, enhance SI/EMI performance, or to reduce the size of the PCB footprint. A six-layer stackup is shown in Table 9-68. Complete stackup specifications are provided in Table 9-69.

**Table 9-67. Minimum PCB Stackup**

| LAYER | TYPE | DESCRIPTION |
|---|---|---|
| 1 | Signal | Top routing mostly vertical |
| 2 | Plane | Split power plane |
| 3 | Plane | Full ground plane |
| 4 | Signal | Bottom routing mostly horizontal |

**Table 9-68. Six-Layer PCB Stackup Suggestion**

| LAYER | TYPE | DESCRIPTION |
|---|---|---|
| 1 | Signal | Top routing mostly vertical |
| 2 | Plane | Ground |
| 3 | Plane | Split power plane |
| 4 | Plane | Split power plane or Internal routing |
| 5 | Plane | Ground |
| 6 | Signal | Bottom routing mostly horizontal |

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**Table 9-69. PCB Stackup Specifications**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | PCB routing/plane layers | 4 | 6 | | |
| 2 | Signal routing layers | 2 | | | |
| 3 | Full ground reference layers under DDR3 routing region(1) | 1 | | | |
| 4 | Full 1.5-V power reference layers under the DDR3 routing region(1) | 1 | | | |
| 5 | Number of reference plane cuts allowed within DDR routing region(2) | | | 0 | |
| 6 | Number of layers between DDR3 routing layer and reference plane(3) | | | 0 | |
| 7 | PCB routing feature size | | 4 | | Mils |
| 8 | PCB trace width, w | | 4 | | Mils |
| 13 | Single-ended impedance, Zo | 50 | | 75 | Ω |
| 14 | Impedance control(4) | Z-5 | Z | Z+5 | Ω |

(1) Ground reference layers are preferred over power reference layers. Be sure to include bypass caps to accommodate reference layer return current as the trace routes switch routing layers.
(2) No traces should cross reference plane cuts within the DDR routing region. High-speed signal traces crossing reference plane cuts create large return current paths which can lead to excessive crosstalk and EMI radiation.
(3) Reference planes are to be directly adjacent to the signal plane to minimize the size of the return current loop.
(4) Z is the nominal singled-ended impedance selected for the PCB specified by item 13.

#### *9.13.4.2.4.3 Placement*

Figure 9-56 shows the required placement for the processor as well as the DDR3 devices. The dimensions for this figure are defined in Table 9-70. The placement does not restrict the side of the PCB on which the devices are mounted. The ultimate purpose of the placement is to limit the maximum trace lengths and allow for proper routing space. For a 16-bit DDR memory system, the high-word DDR3 device(s) are omitted from the placement.

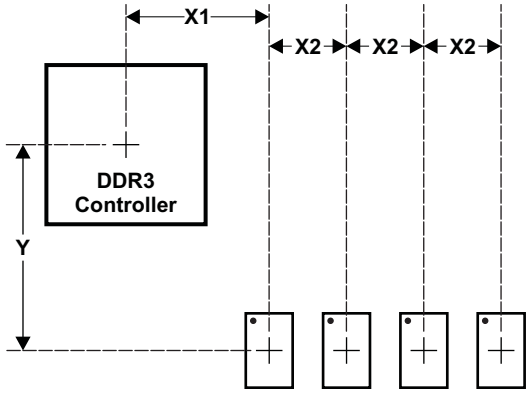


**Figure 9-56. Placement Specifications**

It is strongly recommended that high-speed bypass capacitors be placed and accommodated for during the placement and route planning phase. It is very difficult to add bypass capacitors once the board has been routed and significant rework may be required to meet the high-speed bypass capacitor requirements in Section 9.13.4.2.4.6, *High-Speed Bypass Capacitors* if the proper planning is not done. A particular challenge to placing bypass capacitors in congested areas is fitting the required vias. It is suggested that each pair of vias support two bypass capacitors by mounting one capacitor on the top of the board and other on the bottom. Do not share vias between capacitors mounted on the same side of the PCB. Another suggestion is to line up the vias for the bypass capacitors for the processor in rows forming channels to allow the signals to escape.


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**Table 9-70. Placement Specifications**

| NO. | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| 1 | X1 (1)(2)(3) | | 1000 | Mils |
| 2 | X2 (1)(2) | | 600 | Mils |
| 3 | Y Offset (1)(2)(3) | | 1500 | Mils |
| 4 | DDR3 keepout region | | | |
| 5 | Clearance from non-DDR3 signal to DDR3 keepout region (4)(5)(6) | 4 | | w |

(1) For dimension definitions, see Figure 9-56.
(2) Measurements from center of processor to center of DDR3 device.
(3) Minimizing X1 and Y improves timing margins.
(4) w is defined as the signal trace width.
(5) Non-DDR3 signals allowed within DDR3 keepout region provided they are separated from DDR3 routing layers by a ground plane.
(6) If a device has more than one DDR controller, the signals from the other controller(s) are considered non-DDR3 and should be separated by this specification.

#### *9.13.4.2.4.4 DDR3 Keepout Region*

The region of the PCB used for DDR3 circuitry must be isolated from other signals. The DDR3 keepout region is defined for this purpose and is shown in Figure 9-57. The size of this region varies with the placement and DDR routing. Additional clearances required for the keepout region are shown in Table 9-70. Non-DDR3 signals should not be routed on the DDR signal layers within the DDR3 keepout region. Non-DDR3 signals may be routed in the region, provided they are routed on layers separated from the DDR signal layers by a ground layer. No breaks should be allowed in the reference ground layers in this region. In addition, the 1.5-V DDR3 power plane should cover the entire keepout region. Also note that if there is more than one DDR controller, the signals from each controller need to be separated from each other by the specification in Table 9-70, item 5. Each DDR controller should have its own DDR keepout region.

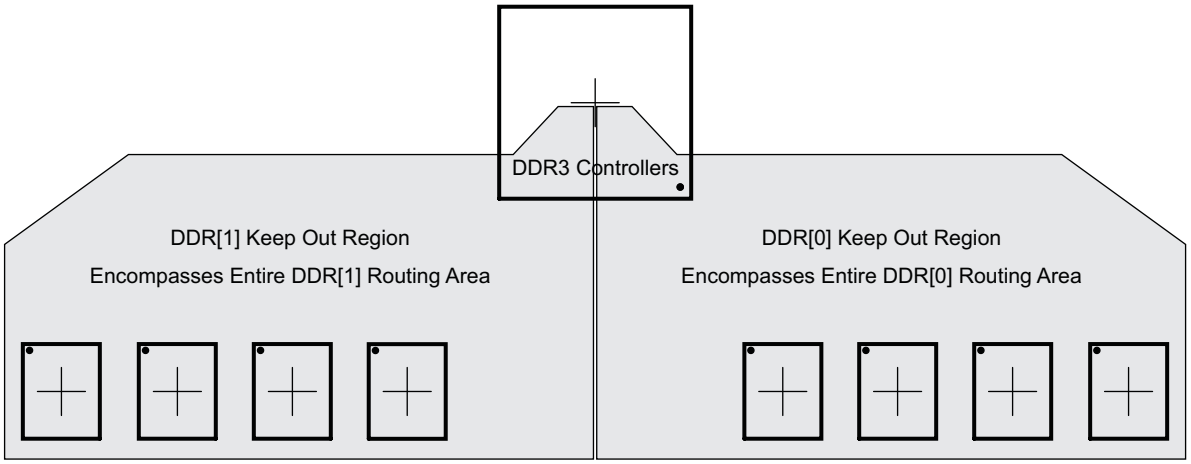


**Figure 9-57. DDR3 Keepout Region**

Figure 9-57 is an example of a processor with two DDR controllers. Processors with a single DDR controler will have only one DDR keepout region. Each DDR controller should have its own keepout region.

#### *9.13.4.2.4.5 Bulk Bypass Capacitors*

Bulk bypass capacitors are required for moderate speed bypassing of the DDR3 and other circuitry. Table 9-71 contains the minimum numbers and capacitance required for the bulk bypass capacitors. Note that this table only covers the bypass needs of the DDR3 controllers and DDR3 device(s). Additional bulk bypass capacitance may be needed for other circuitry.

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**Table 9-71. Bulk Bypass Capacitors Per DDR3 EMIF**

| NO. | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| 1 | DDR_1V5 bulk bypass capacitor count(1) | 3 | | Devices |
| 2 | DDR_1V5 bulk bypass total capacitance | 70 | | µF |

(1) These devices should be placed near the devices they are bypassing, but preference should be given to the placement of the high-speed (HS) bypass capacitors and DDR3 signal routing.

#### *9.13.4.2.4.6 High-Speed Bypass Capacitors*

High-speed (HS) bypass capacitors are critical for proper DDR3 interface operation. It is particularly important to minimize the parasitic series inductance of the HS bypass capacitors, processor/DDR power, and processor/DDR ground connections. Table 9-72 contains the specification for the HS bypass capacitors as well as for the power connections on the PCB. Generally speaking, it is good to:

1. Fit as many HS bypass capacitors as possible.
2. Minimize the distance from the bypass cap to the pins/balls being bypassed.
3. Use the smallest physical sized capacitors possible with the highest capacitance readily available.
4. Connect the bypass capacitor pads to their vias using the widest traces possible and using the largest hole size via possible.
5. Minimize via sharing. Note the limits on via sharing shown in Table 9-72.

**Table 9-72. High-Speed Bypass Capacitors**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | HS bypass capacitor package size(1) | | 201 | 402 | 10 Mils |
| 2 | Distance, HS bypass capacitor to processor being bypassed(2)(3)(4) | | | 400 | Mils |
| 3 | Processor DDR_1V5 HS bypass capacitor count(5) | 35 | | | Per DDR3 EMIF |
| 4 | Processor DDR_1V5 HS bypass capacitor total capacitance | 5 | | | µF |
| 5 | Number of connection vias for each device power/ground ball(6) | | | | Vias |
| 6 | Trace length from device power/ground ball to connection via(2) | | 35 | 70 | Mils |
| 7 | Distance, HS bypass capacitor to DDR device being bypassed(7) | | | 150 | Mils |
| 8 | DDR3 device HS bypass capacitor count(8) | 12 | | | Devices |
| 9 | DDR3 device HS bypass capacitor total capacitance(8) | 0.85 | | | µF |
| 10 | Number of connection vias for each HS capacitor(9)(10) | 2 | | | Vias |
| 11 | Trace length from bypass capacitor connect to connection via(2)(10) | | 35 | 100 | Mils |
| 12 | Number of connection vias for each DDR3 device power/ground ball(11) | 1 | | | Vias |
| 13 | Trace length from DDR3 device power/ground ball to connection via(2)(9) | | 35 | 60 | Mils |

(1) LxW, 10-mil units, i.e., a 0402 is a 40x20-mil surface-mount capacitor.
(2) Closer/shorter is better.
(3) Measured from the nearest processor power/ground ball to the center of the capacitor package.
(4) Three of these capacitors should be located underneath the processor, between the cluster of DDR_1V5 balls and ground balls, between the DDR interfaces on the package.
(5) Per DDR3 EMIF. For example, a processor with two DDR3 EMIFs would require 70 capacitors. The capacitors should be evenly distributed near the Processor's DDR_1V5 pins.
(6) See the Via Channel™ escape for the processor package.
(7) Measured from the DDR3 device power/ground ball to the center of the capacitor package.
(8) Per DDR3 EMIF.
(9) An additional HS bypass capacitor can share the connection vias only if it is mounted on the opposite side of the board. No sharing of vias is permitted on the same side of the board.
(10) An HS bypass capacitor may share a via with a DDR device mounted on the same side of the PCB. A wide trace should be used for the connection and the length from the capacitor pad to the DDR device pad should be less than 150 mils.
(11) Up to a total of two pairs of DDR power/ground balls may share a via.


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#### 9.13.4.2.4.6.1 Return Current Bypass Capacitors and Vias

If a power plane is used as a reference plane then additional bypass capacitors may be required to accommodate the signal return currents. Care should be taken to minimize the layer transitions during routing. If a layer transition is necessary, it is better to transition to a layer using the same reference plane. If this cannot be accommodated, ensure there is a nearby path to allow the return currents to transition between reference planes. Transitions from power reference planes to ground reference planes must go through a bypass capacitor. Transition between different ground references or DVDD_DDR planes can go through a connecting via. As many of these return current bypass capacitors or vias should be used as possible. The goal is to minimize the size of the return current loops. Generally, this type of situation happens where signals must transition from horizontal to vertical routing and vice-versa.

#### 9.13.4.2.4.7 Net Classes

Table 9-73 lists the clock net classes for the DDR3 interface. Table 9-74 lists the signal net classes, and associated clock net classes, for signals in the DDR3 interface. These net classes are used for the termination and routing rules that follow.

**Table 9-73. Clock Net Class Definitions**

| CLOCK NET CLASS | PROCESSOR PIN NAMES |
|---|---|
| CK | DDR[x]_CLK/$\overline{\text{DDR[x]_CLK}}$ |
| DQS0 | DDR[x]_DQS[0]/$\overline{\text{DDR[x]_DQS[0]}}$ |
| DQS1 | DDR[x]_DQS[1]/$\overline{\text{DDR[x]_DQS[1]}}$ |
| DQS2(1) | DDR[x]_DQS[2]/$\overline{\text{DDR[x]_DQS[2]}}$ |
| DQS3(1) | DDR[x]_DQS[3]/$\overline{\text{DDR[x]_DQS[3]}}$ |

(1) Only used on 32-bit wide DDR3 memory systems.

**Table 9-74. Signal Net Class Definitions**

| CLOCK NET CLASS | ASSOCIATED CLOCK NET CLASS | PROCESSOR PIN NAMES |
|---|---|---|
| ADDR_CTRL | CK | $\overline{\text{DDR[x]_BA}}$[2:0], DDR[x]_A[14:0], $\overline{\text{DDR[x]_CS[x]}}$, $\overline{\text{DDR[x]_CAS}}$, $\overline{\text{DDR[x]_RAS}}$, $\overline{\text{DDR[x]_WE}}$, DDR[x]_CKE, DDR[x]_ODT[x] |
| DQ0 | DQS0 | DDR[x]_D[7:0], DDR[x]_DQM[0] |
| DQ1 | DQS1 | DDR[x]_D[15:8], DDR[x]_DQM[1] |
| DQ2(1) | DQS2 | DDR[x]_D[23:16], DDR[x]_DQM[2] |
| DQ3(1) | DQS3 | DDR[x]_D[31:24], DDR[x]_DQM[3] |

(1) Only used on 32-bit wide DDR3 memory systems.

#### 9.13.4.2.4.8 DDR3 Signal Termination

Signal terminators are required for the CK and ADDR_CTRL net classes. The data lines are terminated by ODT and, thus, the PCB traces should be unterminated. Detailed termination specifications are covered in the routing rules in the following sections.

#### 9.13.4.2.4.9 VREFSSTL_DDR Routing

VREFSSTL_DDR (VREF) is used as a reference by the input buffers of the DDR3 memories as well as the processor. VREF is intended to be half the DDR3 power supply voltage and is typically generated with the DDR3 1.5-V and VTT power supply. It should be routed as a nominal 20-mil wide trace with 0.1 µF bypass capacitors near each device connection. Narrowing of VREF is allowed to accommodate routing congestion.

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#### 9.13.4.2.4.10 VTT

Like VREF, the nominal value of the VTT supply is half the DDR3 supply voltage. Unlike VREF, VTT is expected to source and sink current, specifically the termination current for the ADDR_CTRL net class Thevinen terminators. VTT is needed at the end of the address bus and it should be routed as a power sub-plane. VTT should be bypassed near the terminator resistors.

#### 9.13.4.2.4.11 CK and ADDR_CTRL Topologies and Routing Definition

The CK and ADDR_CTRL net classes are routed similarly and are length matched to minimize skew between them. CK is a bit more complicated because it runs at a higher transition rate and is differential. The following subsections show the topology and routing for various DDR3 configurations for CK and ADDR_CTRL. Only the components shown in the topologies are allowed. Items such as test points and additional terminations are specifically disallowed. The figures in the following subsections define the terms for the routing specification detailed in Table 9-75.

Care should be taken to minimize layer transitions during routing. If a layer transition is necessary, it is better to transition to a layer using the same reference plane. If this cannot be accommodated, ensure there are nearby ground vias to allow the return currents to transition between reference planes if both reference planes are ground or DVDD_DDR. Ensure there are nearby bypass capacitors to allow the return currents to transition between reference planes if one of the reference planes is ground. The goal is to minimize the size of the return current loops.

##### 9.13.4.2.4.11.1 Four DDR3 Devices

Four DDR3 devices are supported on the DDR EMIF consisting of four x8 DDR3 devices arranged as one bank (CS). These four devices may be mounted on a single side of the PCB, or may be mirrored in two pairs to save board space at a cost of increased routing complexity and parts on the backside of the PCB.

##### 9.13.4.2.4.11.2 CK and ADDR_CTRL Topologies, Four DDR3 Devices

Figure 9-58 shows the topology of the CK net classes and Figure 9-59 shows the topology for the corresponding ADDR_CTRL net classes.

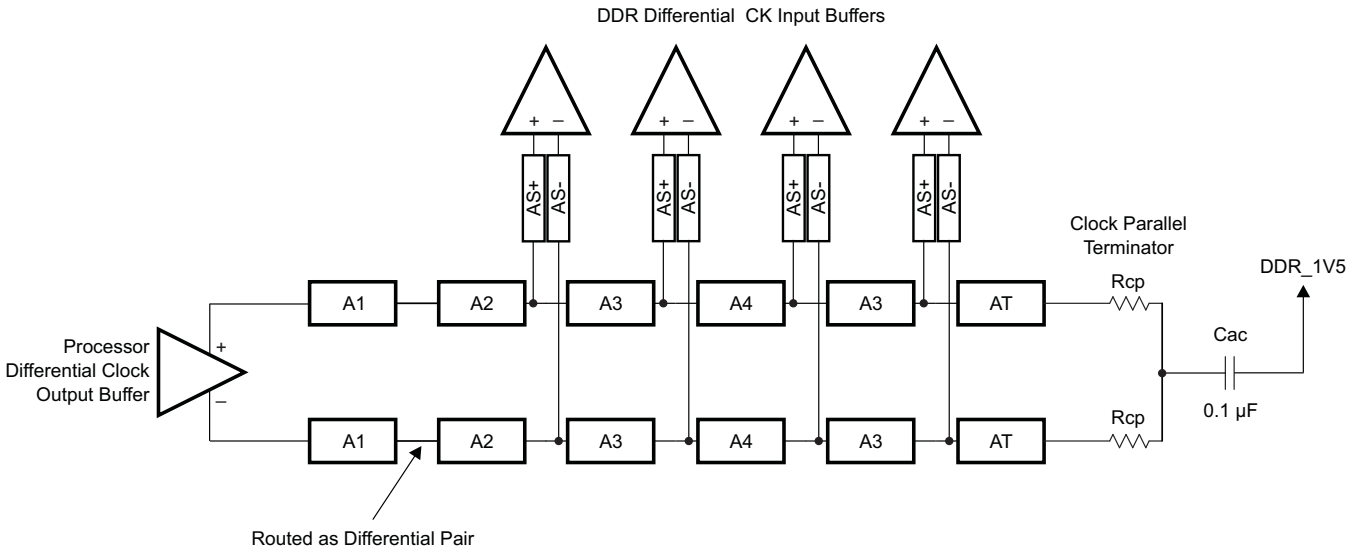


**Figure 9-58. CK Topology for Four x8 DDR3 Devices**


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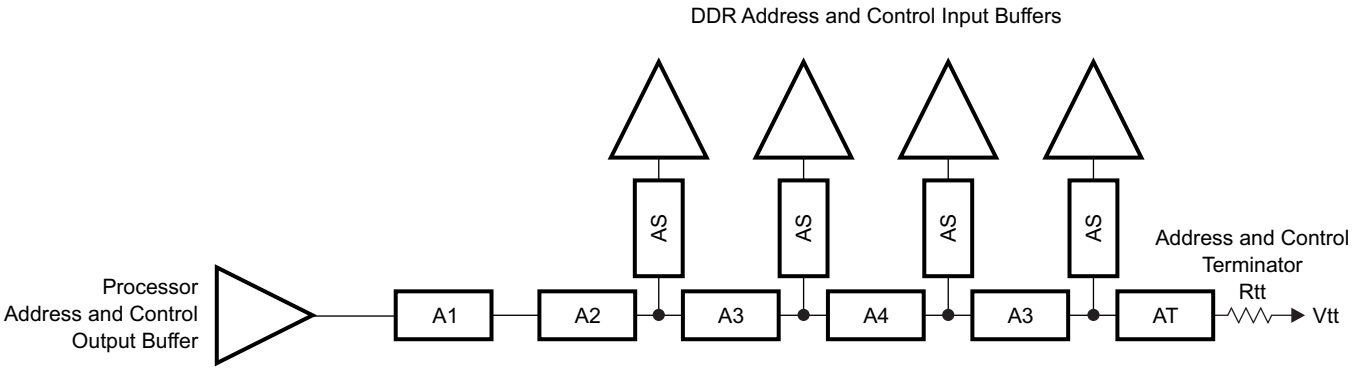


**Figure 9-59. ADDR_CTRL Topology for Four x8 DDR3 Devices**

### *9.13.4.2.4.11.3 CK and ADDR_CTRL Routing, Four DDR3 Devices*

Figure 9-60 shows the CK routing for four DDR3 devices placed on the same side of the PCB. Figure 9-61 shows the corresponding ADDR_CTRL routing.

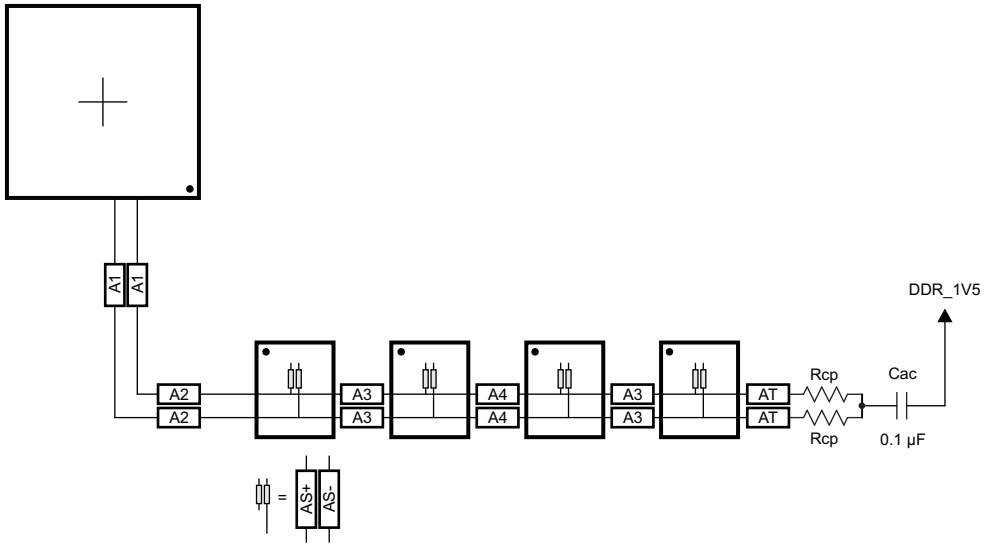


**Figure 9-60. CK Routing for Four Single-Side DDR3 Devices**

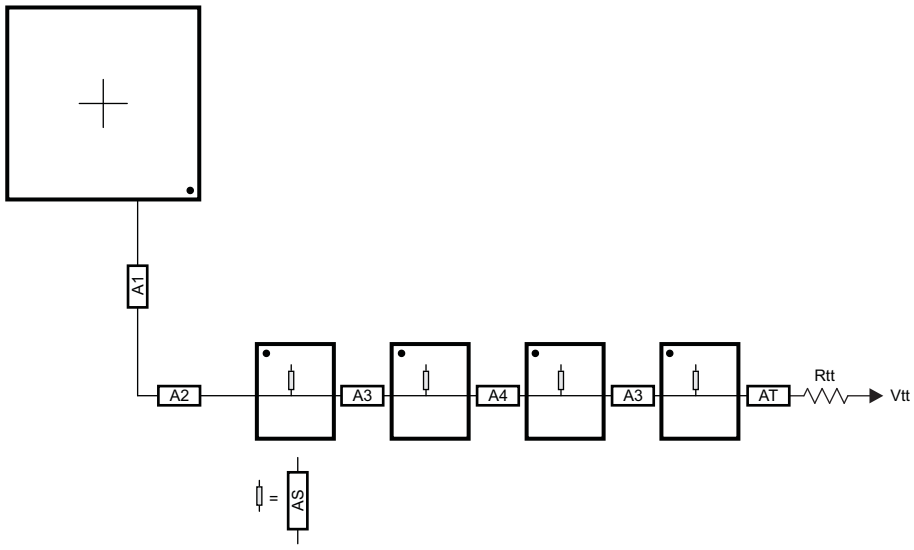


**Figure 9-61. ADDR_CTRL Routing for Four Single-Side DDR3 Devices**

To save PCB space, the four DDR3 memories may be mounted as two mirrored pairs at a cost of increased routing and assembly complexity. Figure 9-62 and Figure 9-63 show the routing for CK and ADDR_CTRL, respectively, for four DDR3 devices mirrored in a two-pair configuration.

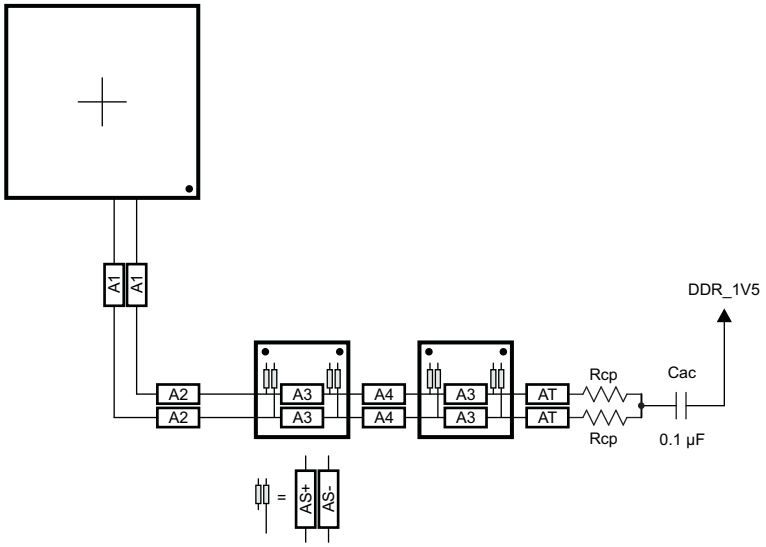


**Figure 9-62. CK Routing for Four Mirrored DDR3 Devices**


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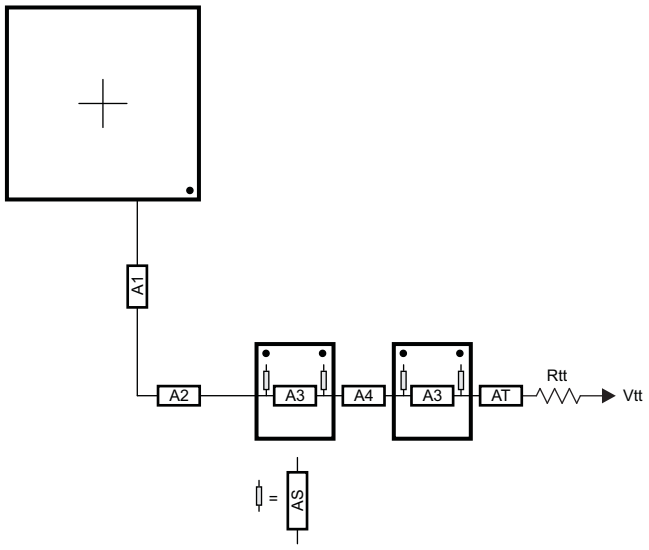


**Figure 9-63. ADDR_CTRL Routing for Four Mirrored DDR3 Devices**

#### *9.13.4.2.4.11.4 Two DDR3 Devices*

Two DDR3 devices are supported on the DDR EMIF consisting of two x8 DDR3 devices arranged as one bank (CS), 16-bits wide, or two x16 DDR3 devices arranged as one bank (CS), 32-bits wide. These two devices may be mounted on a single side of the PCB, or may be mirrored in a pair to save board space at a cost of increased routing complexity and parts on the backside of the PCB.

#### *9.13.4.2.4.11.5 CK and ADDR_CTRL Topologies, Two DDR3 Devices*

Figure 9-64 shows the topology of the CK net classes and Figure 9-65 shows the topology for the corresponding ADDR_CTRL net classes.

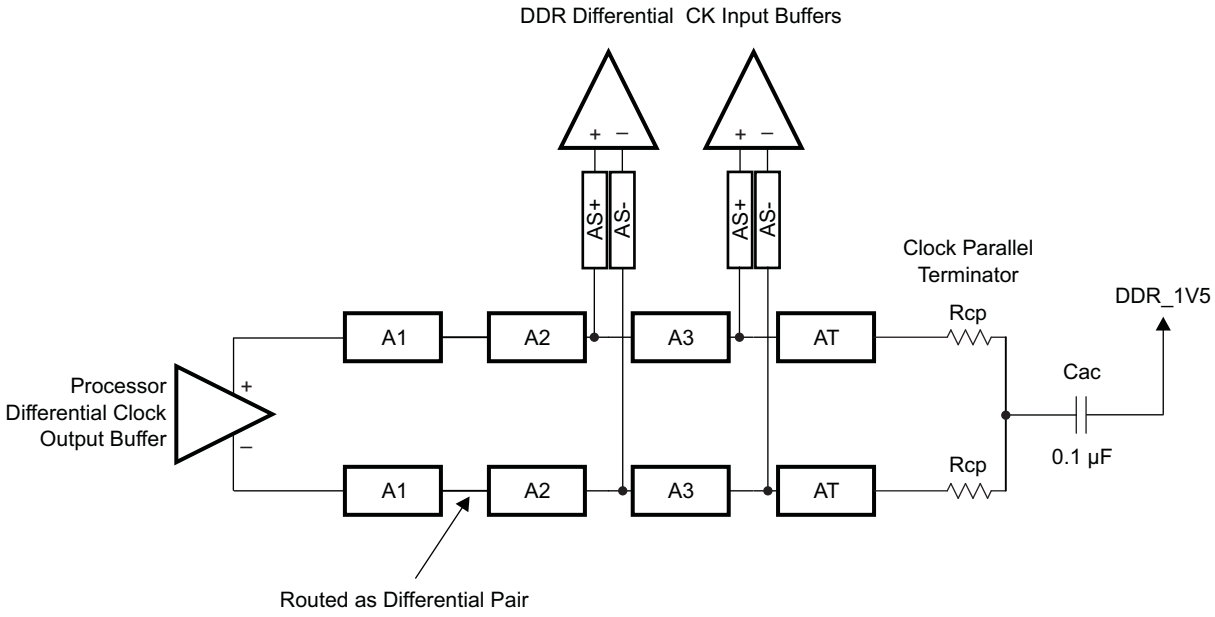


**Figure 9-64. CK Topology for Two DDR3 Devices**

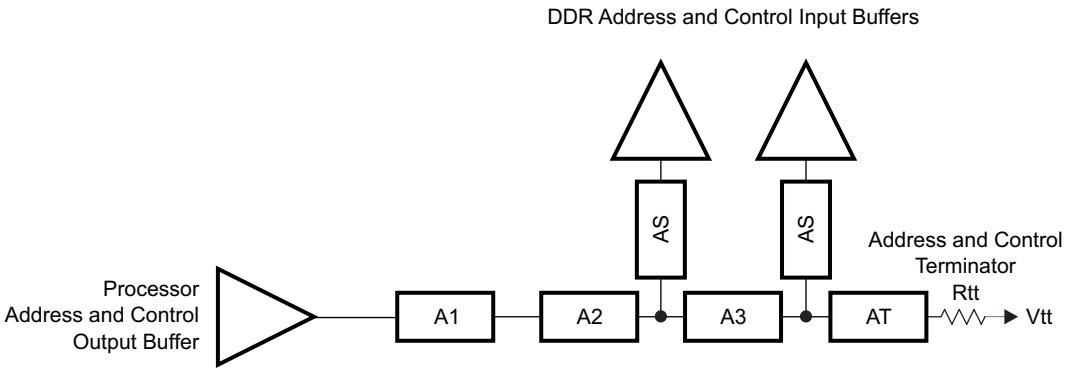


**Figure 9-65. ADDR_CTRL Topology for Two DDR3 Devices**

### *9.13.4.2.4.11.6 CK and ADDR_CTRL Routing, Two DDR3 Devices*

Figure 9-66 shows the CK routing for two DDR3 devices placed on the same side of the PCB. Figure 9-67 shows the corresponding ADDR_CTRL routing.

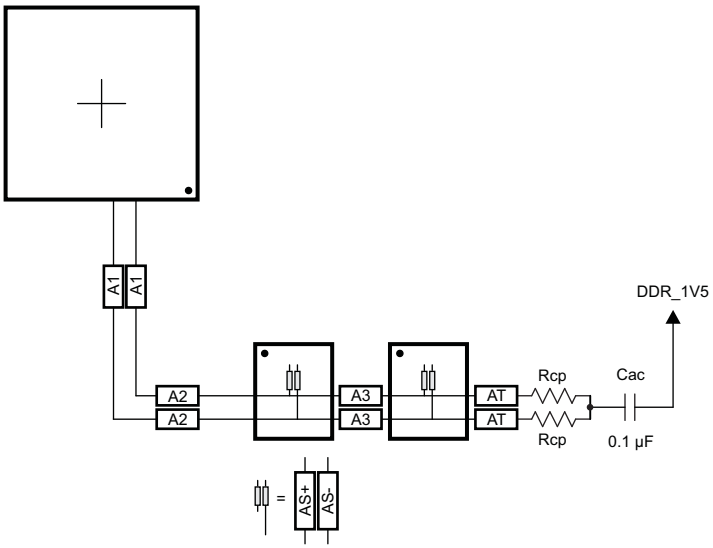


**Figure 9-66. CK Routing for Two Single-Side DDR3 Devices**


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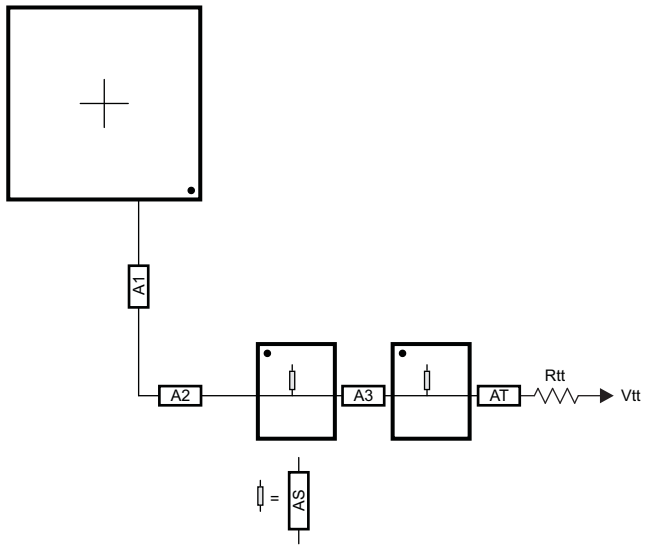


**Figure 9-67. ADDR_CTRL Routing for Two Single-Side DDR3 Devices**

To save PCB space, the two DDR3 memories may be mounted as a mirrored pair at a cost of increased routing and assembly complexity. Figure 9-68 and Figure 9-69 show the routing for CK and ADDR_CTRL, respectively, for two DDR3 devices mirrored in a single-pair configuration.

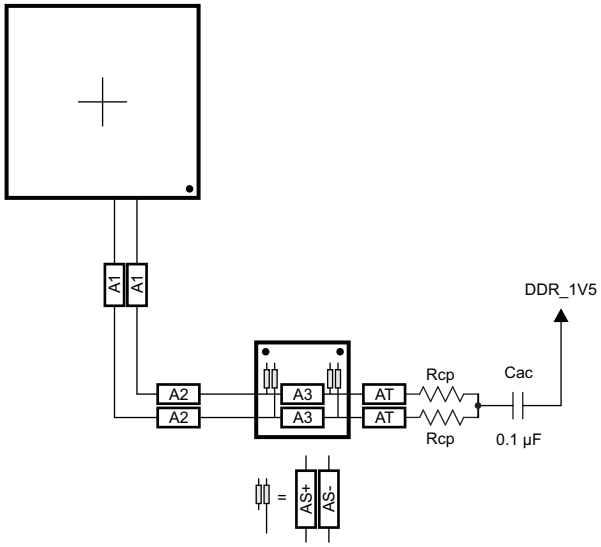


**Figure 9-68. CK Routing for Two Mirrored DDR3 Devices**

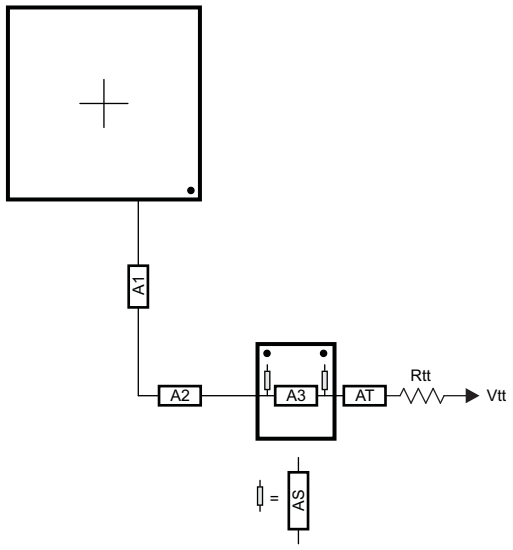


**Figure 9-69. ADDR_CTRL Routing for Two Mirrored DDR3 Devices**

#### *9.13.4.2.4.11.7 One DDR3 Device*

A single DDR3 device is supported on the DDR EMIF consisting of one x16 DDR3 device arranged as one bank (CS), 16-bits wide.

#### *9.13.4.2.4.11.8 CK and ADDR_CTRL Topologies, One DDR3 Device*

Figure 9-70 shows the topology of the CK net classes and Figure 9-71 shows the topology for the corresponding ADDR_CTRL net classes.

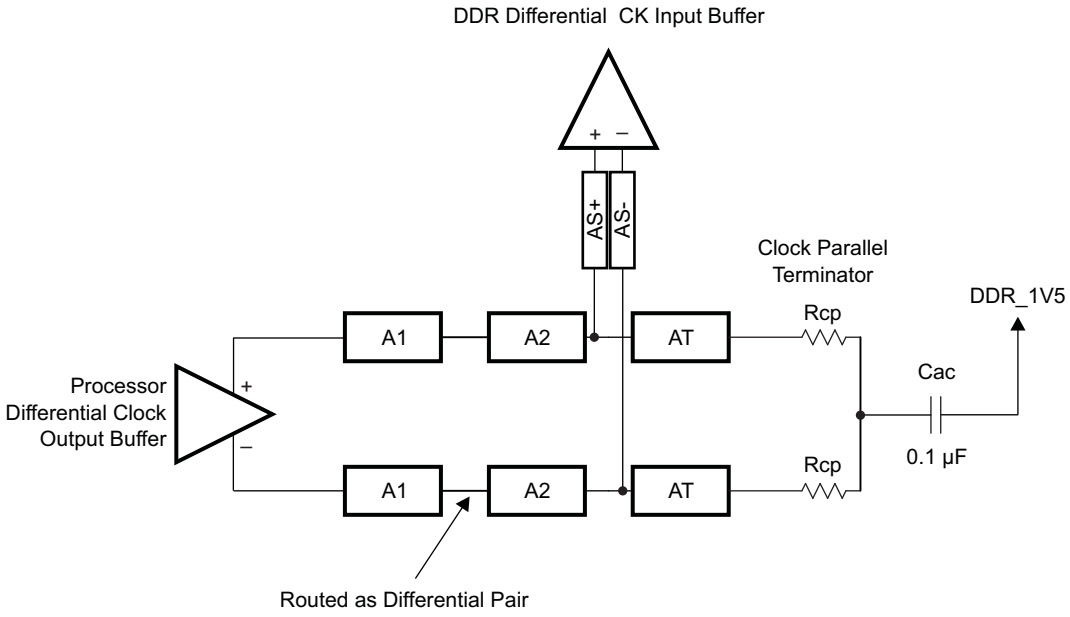


**Figure 9-70. CK Topology for One DDR3 Device**


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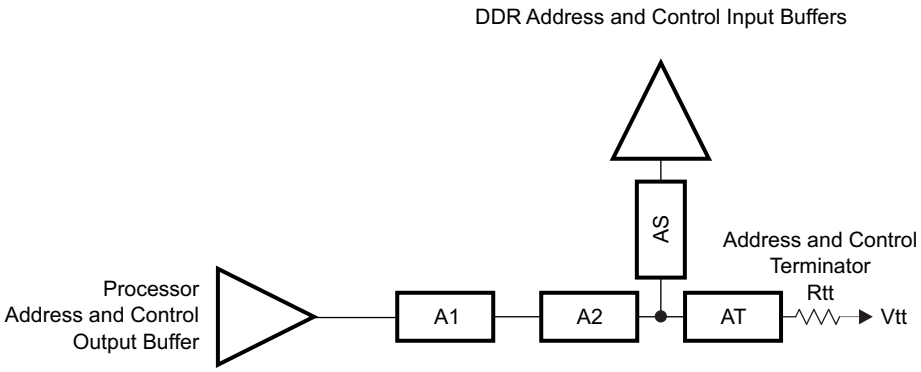


**Figure 9-71. ADDR_CTRL Topology for One DDR3 Device**

### *9.13.4.2.4.11.9 CK and ADDR/CTRL Routing, One DDR3 Device*

Figure 9-72 shows the CK routing for one DDR3 device placed on the same side of the PCB. Figure 9-73 shows the corresponding ADDR_CTRL routing.

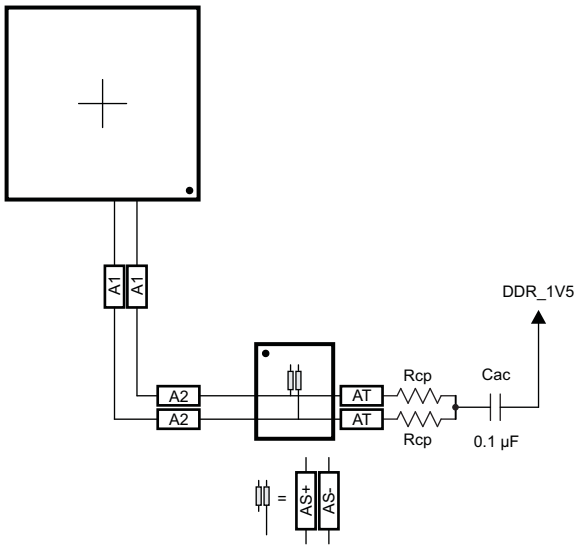


**Figure 9-72. CK Routing for One DDR3 Device**

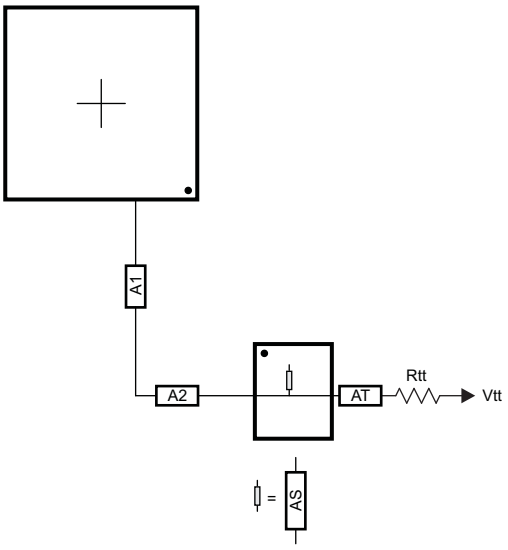


**Figure 9-73. ADDR_CTRL Routing for One DDR3 Device**

#### *9.13.4.2.4.12 Data Topologies and Routing Definition*

No matter the number of DDR3 devices used, the data line topology is always point-to-point, so its definition is simple.

Care should be taken to minimize layer transitions during routing. If a layer transition is necessary, it is better to transition to a layer using the same reference plane. If this cannot be accommodated, ensure there are nearby ground vias to allow the return currents to transition between reference planes if both reference planes are ground or DVDD_DDR. Ensure there are nearby bypass capacitors to allow the return currents to transition between reference planes if one of the reference planes is ground. The goal is to minimize the size of the return current loops.

#### *9.13.4.2.4.12.1 DQS and DQ/DM Topologies, Any Number of Allowed DDR3 Devices*

DQS lines are point-to-point differential, and DQ/DM lines are point-to-point singled ended. Figure 9-74 and Figure 9-75 show these topologies.

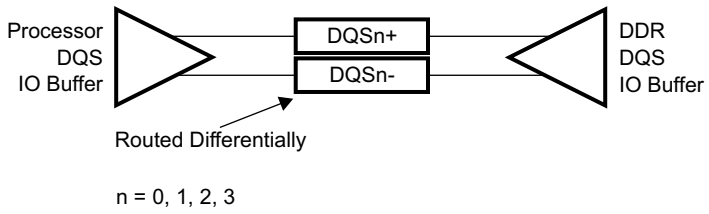


**Figure 9-74. DQS Topology**

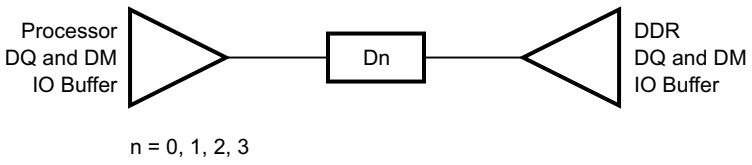


**Figure 9-75. DQ/DM Topology**

#### *9.13.4.2.4.12.2 DQS and DQ/DM Routing, Any Number of Allowed DDR3 Devices*

Figure 9-76 and Figure 9-77 show the DQS and DQ/DM routing.


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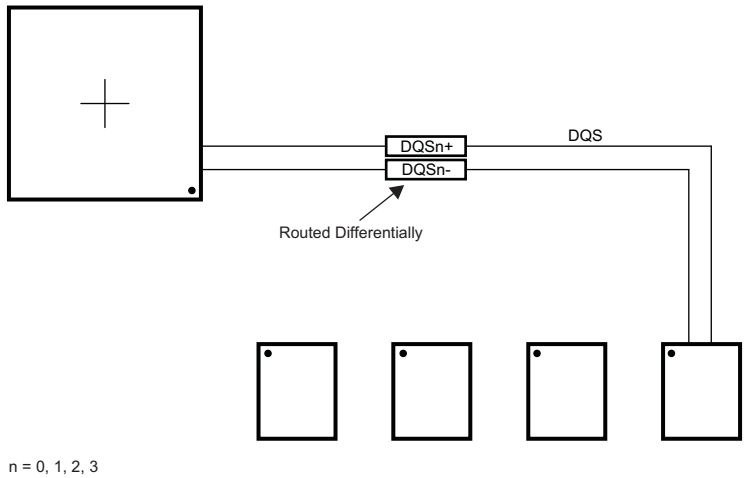



**Figure 9-76. DQS Routing With Any Number of Allowed DDR3 Devices**

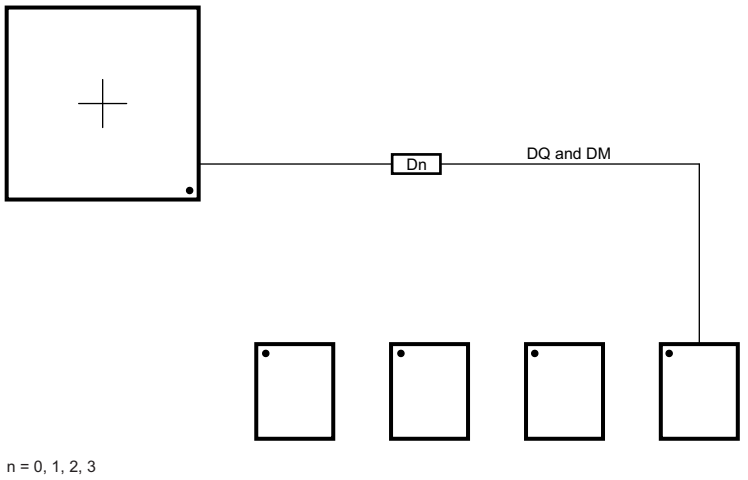


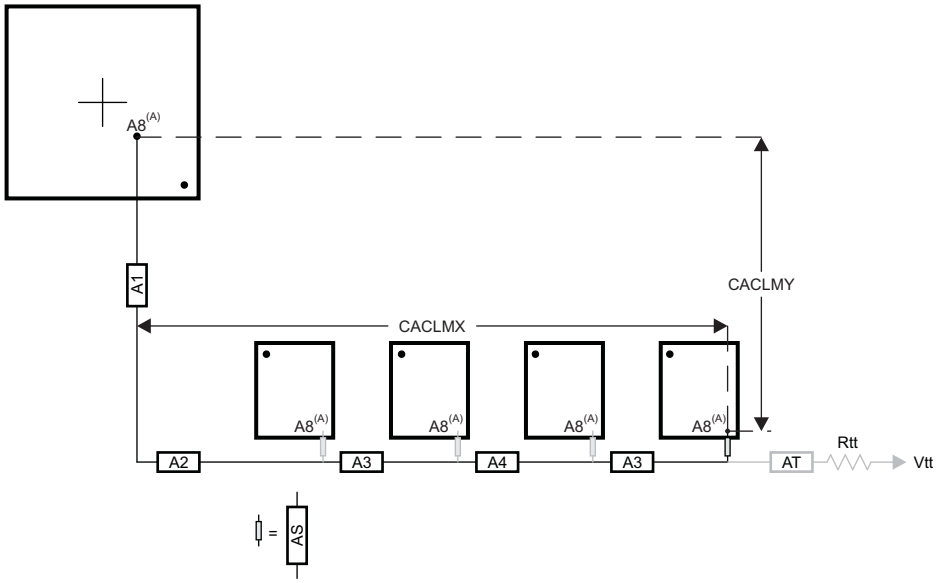

**Figure 9-77. DQ/DM Routing With Any Number of Allowed DDR3 Devices**

#### *9.13.4.2.4.13 Routing Specification*

##### *9.13.4.2.4.13.1 CK and ADDR_CTRL Routing Specification*

Skew within the CK and ADDR_CTRL net classes directly reduces setup and hold margin and, thus, this skew must be controlled. The only way to practically match lengths on a PCB is to lengthen the shorter traces up to the length of the longest net in the net class and its associated clock. A metric to establish this maximum length is Manhattan distance. The Manhattan distance between two points on a PCB is the length between the points when connecting them only with horizontal or vertical segments. A reasonable trace route length is to within a percentage of its Manhattan distance. CACLM is defined as Clock Address Control Longest Manhattan distance.

Given the clock and address pin locations on the processor and the DDR3 memories, the maximum possible Manhattan distance can be determined given the placement. Figure 9-78 and Figure 9-79 show this distance for four loads and two loads, respectively. It is from this distance that the specifications on the lengths of the transmission lines for the address bus are determined. CACLM is determined similarly for other address bus configurations; i.e., it is based on the longest net of the CK/ADDR_CTRL net class. For CK and ADDR_CTRL routing, these specifications are contained in Table 9-75.

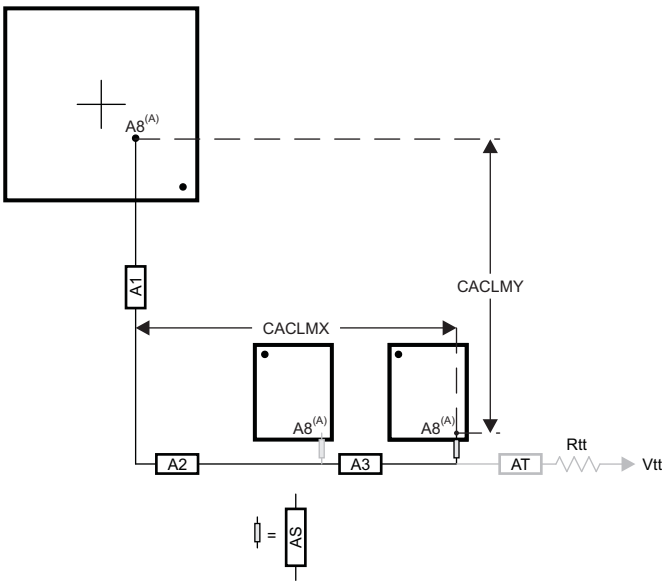



A. It is very likely that the longest CK/ADDR_CTRL Manhattan distance will be for Address Input 8 (A8) on the DDR3 memories. CACLM is based on the longest Manhattan distance due to the device placement. Verify the net class that satisfies this criteria and use as the baseline for CK/ADDR_CTRL skew matching and length control.

The length of shorter CK/ADDR_CTRL stubs as well as the length of the terminator stub are not included in this length calculation. Non-included lengths are grayed out in the figure.

Assuming A8 is the longest, CALM = CACLMY + CACLMX + 300 mils.
The extra 300 mils allows for routing down lower than the DDR3 memories and returning up to reach A8.

**Figure 9-78. CACLM for Four Address Loads on One Side of PCB**




A. It is very likely that the longest CK/ADDR_CTRL Manhattan distance will be for Address Input 8 (A8) on the DDR3 memories. CACLM is based on the longest Manhattan distance due to the device placement. Verify the net class that satisfies this criteria and use as the baseline for CK/ADDR_CTRL skew matching and length control.

The length of shorter CK/ADDR_CTRL stubs as well as the length of the terminator stub are not included in this length calculation. Non-included lengths are grayed out in the figure.

Assuming A8 is the longest, CALM = CACLMY + CACLMX + 300 mils.
The extra 300 mils allows for routing down lower than the DDR3 memories and returning up to reach A8.

**Figure 9-79. CACLM for Two Address Loads on One Side of PCB**


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**Table 9-75. CK and ADDR_CTRL Routing Specification(1)(2)**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | A1+A2 length | | | 2500 | mils |
| 2 | A1+A2 skew | | | 25 | mils |
| 3 | A3 length | | | 660 | mils |
| 4 | A3 skew(3) | | | 25 | mils |
| 5 | A3 skew(4) | | | 125 | mils |
| 6 | A4 length | | | 660 | mils |
| 7 | A4 skew | | | 25 | mils |
| 8 | AS length | | | 100 | mils |
| 9 | AS skew | | | 100 | mils |
| 10 | AS+/AS- length | | | 70 | mils |
| 11 | AS+/AS- skew | | | 5 | mils |
| 12 | AT length(5) | | 500 | | mils |
| 13 | AT skew(6) | | 100 | | mils |
| 14 | AT skew(7) | | | 5 | mils |
| 15 | CK/ADDR_CTRL nominal trace length(8) | CACLM-50 | CACLM | CACLM+50 | mils |
| 16 | Center-to-center CK to other DDR3 trace spacing(9) | 4w | | | |
| 17 | Center-to-center ADDR_CTRL to other DDR3 trace spacing(9)(10) | 4w | | | |
| 18 | Center-to-center ADDR_CTRL to other ADDR_CTRL trace spacing(9) | 3w | | | |
| 19 | CK center-to-center spacing(11) | | (12) | | |
| 20 | CK spacing to other net(9) | 4w | | | |
| 21 | Rcp(13) | Zo-1 | Zo | Zo+ | Ω |
| 22 | Rtt(13)(14) | Zo-5 | Zo | Zo+5 | Ω |

(1) The use of vias should be minimized.
(2) Additional bypass capacitors are required when using the DDR_1V5 plane as the reference plane to allow the return current to jump between the DDR_1V5 plane and the ground plane when the net class switches layers at a via.
(3) Non-mirrored configuration (all DDR3 memories on same side of PCB).
(4) Mirrored configuration (one DDR3 device on top of the board and one DDR3 device on the bottom).
(5) While this length can be increased for convenience, its length should be minimized.
(6) ADDR_CTRL net class only (not CK net class). Minimizing this skew is recommended, but not required.
(7) CK net class only.
(8) CACLM is the longest Manhattan distance of the CK and ADDR_CTRL net classes + 300 mils. For definition, see Section 9.13.4.2.4.13.1, Figure 9-78, and Figure 9-79.
(9) Center-to-center spacing is allowed to fall to minimum (w) for up to 1250 mils of routed length.
(10) The ADDR_CTRL net class of the other DDR EMIF is considered *other DDR3 trace spacing*.
(11) CK spacing set to ensure proper differential impedance.
(12) The most important thing to do is control the impedance so inadvertent impedance mismatches are not created. Generally speaking, center-to-center spacing should be either 2w or slightly larger than 2w to achieve a differential impedance equal to twice the single-ended impedance, Zo.
(13) Source termination (series resistor at driver) is specifically not allowed.
(14) Termination values should be uniform across the net class.

### *9.13.4.2.4.13.2 DQS and DQ Routing Specification*

Skew within the DQS and DQ/DM net classes directly reduces setup and hold margin and thus this skew must be controlled. The only way to practically match lengths on a PCB is to lengthen the shorter traces up to the length of the longest net in the net class and its associated clock. As with CK and ADDR_CTRL, a reasonable trace route length is to within a percentage of its Manhattan distance. DQLMn is defined as DQ Longest Manhattan distance n, where n is the byte number. For a 32-bit interface, there are four DQLMs, DQLM0–DQLM3. Likewise, for a 16-bit interface, there are two DQLMs, DQLM0–DQLM1.

**NOTE**

It is not required, nor is it recommended, to match the lengths across all bytes. Length matching is only required within each byte.

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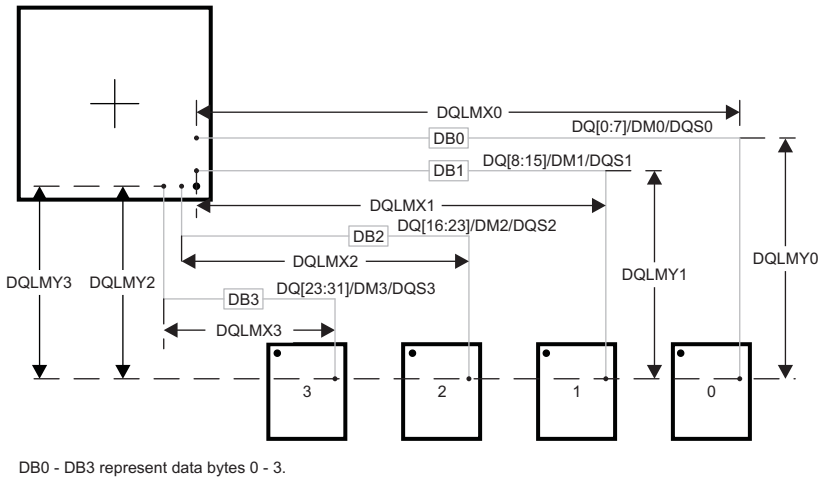
Given the DQS and DQ/DM pin locations on the processor and the DDR3 memories, the maximum possible Manhattan distance can be determined given the placement. Figure 9-80 shows this distance for four loads. It is from this distance that the specifications on the lengths of the transmission lines for the data bus are determined. For DQS and DQ/DM routing, these specifications are contained in Table 9-76.




DB0 - DB3 represent data bytes 0 - 3.

There are four DQLMs, one for each byte (32-bit interface). Each DQLM is the longest Manhattan distance of the byte; therefore:
DQLM0 = DQLMX0 + DQLMY0
DQLM1 = DQLMX1 + DQLMY1
DQLM2 = DQLMX2 + DQLMY2
DQLM3 = DQLMX3 + DQLMY3

**Figure 9-80. DQLM for Any Number of Allowed DDR3 Devices**

**Table 9-76. Data Routing Specification(1)**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | DB0 nominal length(2)(3) | | | DQLM0 | mils |
| 2 | DB1 nominal length(2)(4) | | | DQLM1 | mils |
| 3 | DB2 nominal length(2)(5) | | | DQLM2 | mils |
| 4 | DB3 nominal length(2)(6) | | | DQLM3 | mils |
| 5 | DBn skew(7) | | | 25 | mils |
| 6 | DQSn+ to DQSn- skew | | | 5 | mils |
| 7 | DQSn to DBn skew(7)(8) | | | 25 | mils |
| 8 | Center-to-center DBn to other DDR3 trace spacing(9)(10) | 4w | | | |
| 9 | Center-to-center DBn to other DBn trace spacing(9)(11) | 3w | | | |
| 10 | DQSn center-to-center spacing(12) | | (13) | | |
| 11 | DQSn center-to-center spacing to other net(9) | 4w | | | |

(1) External termination disallowed. Data termination should use built-in ODT functionality.
(2) DQLMn is the longest Manhattan distance of a byte. For definition, see Section 9.13.4.2.4.13.2 and Figure 9-80.
(3) DQLM0 is the longest Manhattan length for the net classes of Byte 0.
(4) DQLM1 is the longest Manhattan length for the net classes of Byte 1.
(5) DQLM2 is the longest Manhattan length for the net classes of Byte 2.
(6) DQLM3 is the longest Manhattan length for the net classes of Byte 3.
(7) Length matching is only done within a byte. Length matching across bytes is neither required nor recommended.
(8) Each DQS pair is length matched to its associated byte.
(9) Center-to-center spacing is allowed to fall to minimum (w) for up to 1250 mils of routed length.
(10) Other DDR3 trace spacing means other DDR3 net classes not within the byte.
(11) This applies to spacing within the net classes of a byte.
(12) DQS pair spacing is set to ensure proper differential impedance.
(13) The most important thing to do is control the impedance so inadvertent impedance mismatches are not created. Generally speaking, center-to-center spacing should be either 2w or slightly larger than 2w to achieve a differential impedance equal to twice the single-ended impedance, Zo.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## 9.14 Multichannel Audio Serial Port (McASP)

The multichannel audio serial port (McASP) functions as a general-purpose audio serial port optimized for the needs of multichannel audio applications. The McASP is useful for time-division multiplexed (TDM) stream, Inter-Integrated Sound (I2S) protocols, and inter-component digital audio interface transmission (DIT).

### *9.14.1 McASP Device-Specific Information*

The device includes six multichannel audio serial port (McASP) interface peripherals (McASP0, McASP1, McASP2, McASP3, McASP4, and McASP5). The McASP module consists of a transmit and receive section. On McASP0/1, these sections can operate completely independently with different data formats, separate master clocks, bit clocks, and frame syncs or, alternatively, the transmit and receive sections may be synchronized. On McASP2, McASP3, McASP4, and McASP5, the transmit and receive sections must always be synchronized. The McASP module also includes shift registers that may be configured to operate as either transmit data or receive data.

The transmit section of the McASP can transmit data in either a time-division-multiplexed (TDM) synchronous serial format or in a digital audio interface (DIT) format where the bit stream is encoded for S/PDIF, AES-3, IEC-60958, CP-430 transmission. The receive section of the McASP peripheral supports the TDM synchronous serial format.

The McASP module can support one transmit data format (either a TDM format or DIT format) and one receive format at a time. All transmit shift registers use the same format and all receive shift registers use the same format; however, the transmit and receive formats need not be the same. Both the transmit and receive sections of the McASP also support burst mode, which is useful for non-audio data (for example, passing control information between two devices).

The McASP peripheral has additional capability for flexible clock generation and error detection/handling, as well as error management.

The device McASP0 and McASP1 modules have up to 10 serial data pins, while McASP2, McASP3, McASP4, and McASP5 are limited to up to four serial data pins each. The McASP FIFO size is 256 bytes and two DMA and two interrupt requests are supported. Buffers are used transparently to better manage DMA, which can be leveraged to manage data flow more efficiently.

For more detailed information on and the functionality of the McASP peripheral, see the *Multichannel Audio Serial Port (McASP)* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

### *9.14.2 McASP0, McASP1, McASP2, McASP3, McASP4, and McASP5 Peripheral Registers Descriptions*

**Table 9-77. McASP0/1/2/3/4/5 Registers**

| HEX ADDRESS RANGE | | | | | | ACRONYM | REGISTER NAME |
|---|---|---|---|---|---|---|---|
| MCASP0 | MCASP1 | MCASP2 | MCASP3 | MCASP4 | MCASP5 | | |
| 0x4803 8000 | 0x4803 C000 | 0x4805 0000 | 0x4A1A 2000 | 0x4A1A 8000 | 0x4A1A E000 | PID | Peripheral ID |
| 0x4803 8010 | 0x4803 C010 | 0x4805 0010 | 0x4A1A 2010 | 0x4A1A 8010 | 0x4A1A E010 | PFUNC | Pin Function |
| 0x4803 8014 | 0x4803 C014 | 0x4805 0014 | 0x4A1A 2014 | 0x4A1A 8014 | 0x4A1A E014 | PDIR | Pin Direction |
| 0x4803 8018 | 0x4803 C018 | 0x4805 0018 | 0x4A1A 2018 | 0x4A1A 8018 | 0x4A1A E018 | PDOUT | Pin Data Out |
| 0x4803 801C | 0x4803 C01C | 0x4805 001C | 0x4A1A 201C | 0x4A1A 801C | 0x4A1A E01C | PDIN | Pin Data Input (Read)<br>Read returns pin data input |
| | | | | | | PDSET | Pin Data Set (Write)<br>Writes effect pin data set (Alternate Write Address PDOUT) |

**Table 9-77. McASP0/1/2/3/4/5 Registers (continued)**

| HEX ADDRESS RANGE | | | | | | ACRONYM | REGISTER NAME |
|---|---|---|---|---|---|---|---|
| MCASP0 | MCASP1 | MCASP2 | MCASP3 | MCASP4 | MCASP5 | | |
| 0x4803 8020 | 0x4803 C020 | 0x4805 0020 | 0x4A1A 2020 | 0x4A1A 8020 | 0x4A1A E020 | PDCLR | Pin Data Clear (Alternate Write Address PDOUT) |
| 0x4803 8044 | 0x4803 C044 | 0x4805 0044 | 0x4A1A 2044 | 0x4A1A 8044 | 0x4A1A E044 | GBLCTL | Global Control |
| 0x4803 8048 | 0x4803 C048 | 0x4805 0048 | 0x4A1A 2048 | 0x4A1A 8048 | 0x4A1A E048 | AMUTE | Mute Control |
| 0x4803 804C | 0x4803 C04C | 0x4805 004C | 0x4A1A 204C | 0x4A1A 804C | 0x4A1A E04C | LBCTL | Loop-Back Test Control |
| 0x4803 8050 | 0x4803 C050 | 0x4805 0050 | 0x4A1A 2050 | 0x4A1A 8050 | 0x4A1A E050 | TXDITCTL | Transmit DIT Mode Control |
| 0x4803 8060 | 0x4803 C060 | 0x4805 0060 | 0x4A1A 2060 | 0x4A1A 8060 | 0x4A1A E060 | GBLCTLR | Alias of GBLCTL containing only receiver reset bits; allows transmit to be reset independently from receive |
| 0x4803 8064 | 0x4803 C064 | 0x4805 0064 | 0x4A1A 2064 | 0x4A1A 8064 | 0x4A1A E064 | RXMASK | Receiver Bit Mask |
| 0x4803 8068 | 0x4803 C068 | 0x4805 0068 | 0x4A1A 2068 | 0x4A1A 8068 | 0x4A1A E068 | RXFMT | Receive Bitstream Format |
| 0x4803 806C | 0x4803 C06C | 0x4805 006C | 0x4A1A 206C | 0x4A1A 806C | 0x4A1A E06C | RXFMCTL | Receive Frame Sync Control |
| 0x4803 8070 | 0x4803 C070 | 0x4805 0070 | 0x4A1A 2070 | 0x4A1A 8070 | 0x4A1A E070 | ACLKRCTL | Receive Clock Control |
| 0x4803 8074 | 0x4803 C074 | 0x4805 0074 | 0x4A1A 2074 | 0x4A1A 8074 | 0x4A1A E074 | AHCLKRCTL | High Frequency Receive Clock Control |
| 0x4803 8078 | 0x4803 C078 | 0x4805 0078 | 0x4A1A 2078 | 0x4A1A 8078 | 0x4A1A E078 | RXTDM | Receive TDM Slot 0-31 |
| 0x4803 807C | 0x4803 C07C | 0x4805 007C | 0x4A1A 207C | 0x4A1A 807C | 0x4A1A E07C | EVTCTLR | Receiver Interrupt Control |
| 0x4803 8080 | 0x4803 C080 | 0x4805 0080 | 0x4A1A 2080 | 0x4A1A 8080 | 0x4A1A E080 | RXSTAT | Status Receiver |
| 0x4803 8084 | 0x4803 C084 | 0x4805 0084 | 0x4A1A 2084 | 0x4A1A 8084 | 0x4A1A E084 | RXTDMSLOT | Current Receive TDM Slot |
| 0x4803 8088 | 0x4803 C088 | 0x4805 0088 | 0x4A1A 2088 | 0x4A1A 8088 | 0x4A1A E088 | RXCLKCHK | Receiver Clock Check Control |
| 0x4803 808C | 0x4803 C08C | 0x4805 008C | 0x4A1A 208C | 0x4A1A 808C | 0x4A1A E08C | REVTCTL | Receiver DMA Event Control |
| 0x4803 80A0 | 0x4803 C0A0 | 0x4805 00A0 | 0x4A1A 20A0 | 0x4A1A 80A0 | 0x4A1A E0A0 | GBLCTLX | Alias of GBLCTL containing only transmit reset bits; allows transmit to be reset independently from receive |
| 0x4803 80A4 | 0x4803 C0A4 | 0x4805 00A4 | 0x4A1A 20A4 | 0x4A1A 80A4 | 0x4A1A E0A4 | TXMASK | Transmit Format Unit Bit Mask |
| 0x4803 80A8 | 0x4803 C0A8 | 0x4805 00A8 | 0x4A1A 20A8 | 0x4A1A 80A8 | 0x4A1A E0A8 | TXFMT | Transmit Bitstream Format |
| 0x4803 80AC | 0x4803 C0AC | 0x4805 00AC | 0x4A1A 20AC | 0x4A1A 80AC | 0x4A1A E0AC | TXFMCTL | Transmit Frame Sync Control |
| 0x4803 80B0 | 0x4803 C0B0 | 0x4805 00B0 | 0x4A1A 20B0 | 0x4A1A 80B0 | 0x4A1A E0B0 | ACLKXCTL | Transmit Clock Control |
| 0x4803 80B4 | 0x4803 C0B4 | 0x4805 00B4 | 0x4A1A 20B4 | 0x4A1A 80B4 | 0x4A1A E0B4 | AHCLKXCTL | High Frequency Transmit Clock Control |
| 0x4803 80B8 | 0x4803 C0B8 | 0x4805 00B8 | 0x4A1A 20B8 | 0x4A1A 80B8 | 0x4A1A E0B8 | TXTDM | Transmit TDM Slot 0-31 |
| 0x4803 80BC | 0x4803 C0BC | 0x4805 00BC | 0x4A1A 20BC | 0x4A1A 80BC | 0x4A1A E0BC | EVTCTLX | Transmitter Interrupt Control |
| 0x4803 80C0 | 0x4803 C0C0 | 0x4805 00C0 | 0x4A1A 20C0 | 0x4A1A 80C0 | 0x4A1A E0C0 | TXSTAT | Status Transmitter |
| 0x4803 80C4 | 0x4803 C0C4 | 0x4805 00C4 | 0x4A1A 20C4 | 0x4A1A 80C4 | 0x4A1A E0C4 | TXTDMSLOT | Current Transmit TDM Slot |
| 0x4803 80C8 | 0x4803 C0C8 | 0x4805 00C8 | 0x4A1A 20C8 | 0x4A1A 80C8 | 0x4A1A E0C8 | TXCLKCHK | Transmit Clock Check Control |
| 0x4803 80CC | 0x4803 C0CC | 0x4805 00CC | 0x4A1A 20CC | 0x4A1A 80CC | 0x4A1A E0CC | XEVTCTL | Transmitter DMA Control |
| 0x4803 80D0 | 0x4803 C0D0 | 0x4805 00D0 | 0x4A1A 20D0 | 0x4A1A 80D0 | 0x4A1A E0D0 | CLKADJEN | One-shot Clock Adjust Enable |


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**Table 9-77. McASP0/1/2/3/4/5 Registers (continued)**

| HEX ADDRESS RANGE | | | | | | ACRONYM | REGISTER NAME |
|---|---|---|---|---|---|---|---|
| MCASP0 | MCASP1 | MCASP2 | MCASP3 | MCASP4 | MCASP5 | | |
| 0x4803 8100 | 0x4803 C100 | 0x4805 0100 | 0x4A1A 2100 | 0x4A1A 8100 | 0x4A1A E100 | DITCSRA0 | Left (Even TDM Slot) Channel Status Register File |
| 0x4803 8104 | 0x4803 C104 | 0x4805 0104 | 0x4A1A 2104 | 0x4A1A 8104 | 0x4A1A E104 | DITCSRA1 | Left (Even TDM Slot) Channel Status Register File |
| 0x4803 8108 | 0x4803 C108 | 0x4805 0108 | 0x4A1A 2108 | 0x4A1A 8108 | 0x4A1A E108 | DITCSRA2 | Left (Even TDM Slot) Channel Status Register File |
| 0x4803 810C | 0x4803 C10C | 0x4805 010C | 0x4A1A 210C | 0x4A1A 810C | 0x4A1A E10C | DITCSRA3 | Left (Even TDM Slot) Channel Status Register File |
| 0x4803 8110 | 0x4803 C110 | 0x4805 0110 | 0x4A1A 2110 | 0x4A1A 8110 | 0x4A1A E110 | DITCSRA4 | Left (Even TDM Slot) Channel Status Register File |
| 0x4803 8114 | 0x4803 C114 | 0x4805 0114 | 0x4A1A 2114 | 0x4A1A 8114 | 0x4A1A E114 | DITCSRA5 | Left (Even TDM Slot) Channel Status Register File |
| 0x4803 8118 | 0x4803 C118 | 0x4805 0118 | 0x4A1A 2118 | 0x4A1A 8118 | 0x4A1A E118 | DITCSRB0 | Right (Odd TDM Slot) Channel Status Register File |
| 0x4803 811C | 0x4803 C11C | 0x4805 011C | 0x4A1A 211C | 0x4A1A 811C | 0x4A1A E11C | DITCSRB1 | Right (Odd TDM Slot) Channel Status Register File |
| 0x4803 8120 | 0x4803 C120 | 0x4805 0120 | 0x4A1A 2120 | 0x4A1A 8120 | 0x4A1A E120 | DITCSRB2 | Right (Odd TDM Slot) Channel Status Register File |
| 0x4803 8124 | 0x4803 C124 | 0x4805 0124 | 0x4A1A 2124 | 0x4A1A 8124 | 0x4A1A E124 | DITCSRB3 | Right (Odd TDM Slot) Channel Status Register File |
| 0x4803 8128 | 0x4803 C128 | 0x4805 0128 | 0x4A1A 2128 | 0x4A1A 8128 | 0x4A1A E128 | DITCSRB4 | Right (Odd TDM Slot) Channel Status Register File |
| 0x4803 812C | 0x4803 C12C | 0x4805 012C | 0x4A1A 212C | 0x4A1A 812C | 0x4A1A E12C | DITCSRB5 | Right (Odd TDM Slot) Channel Status Register File |
| 0x4803 8130 | 0x4803 C130 | 0x4805 0130 | 0x4A1A 2130 | 0x4A1A 8130 | 0x4A1A E130 | DITUDRA0 | Left (Even TDM Slot) User Data Register File |
| 0x4803 8134 | 0x4803 C134 | 0x4805 0134 | 0x4A1A 2134 | 0x4A1A 8134 | 0x4A1A E134 | DITUDRA1 | Left (Even TDM Slot) User Data Register File |
| 0x4803 8138 | 0x4803 C138 | 0x4805 0138 | 0x4A1A 2138 | 0x4A1A 8138 | 0x4A1A E138 | DITUDRA2 | Left (Even TDM Slot) User Data Register File |
| 0x4803 813C | 0x4803 C13C | 0x4805 013C | 0x4A1A 213C | 0x4A1A 813C | 0x4A1A E13C | DITUDRA3 | Left (Even TDM Slot) User Data Register File |
| 0x4803 8140 | 0x4803 C140 | 0x4805 0140 | 0x4A1A 2140 | 0x4A1A 8140 | 0x4A1A E140 | DITUDRA4 | Left (Even TDM Slot) User Data Register File |
| 0x4803 8144 | 0x4803 C144 | 0x4805 0144 | 0x4A1A 2144 | 0x4A1A 8144 | 0x4A1A E144 | DITUDRA5 | Left (Even TDM Slot) User Data Register File |
| 0x4803 8148 | 0x4803 C148 | 0x4805 0148 | 0x4A1A 2148 | 0x4A1A 8148 | 0x4A1A E148 | DITUDRB0 | Right (Odd TDM Slot) User Data Register File |
| 0x4803 814C | 0x4803 C14C | 0x4805 014C | 0x4A1A 214C | 0x4A1A 814C | 0x4A1A E14C | DITUDRB1 | Right (Odd TDM Slot) User Data Register File |
| 0x4803 8150 | 0x4803 C150 | 0x4805 0150 | 0x4A1A 2150 | 0x4A1A 8150 | 0x4A1A E150 | DITUDRB2 | Right (Odd TDM Slot) User Data Register File |
| 0x4803 8154 | 0x4803 C154 | 0x4805 0154 | 0x4A1A 2154 | 0x4A1A 8154 | 0x4A1A E154 | DITUDRB3 | Right (Odd TDM Slot) User Data Register File |
| 0x4803 8158 | 0x4803 C158 | 0x4805 0158 | 0x4A1A 2158 | 0x4A1A 8158 | 0x4A1A E158 | DITUDRB4 | Right (Odd TDM Slot) User Data Register File |
| 0x4803 815C | 0x4803 C15C | 0x4805 015C | 0x4A1A 215C | 0x4A1A 815C | 0x4A1A E15C | DITUDRB5 | Right (Odd TDM Slot) User Data Register File |
| 0x4803 8180 - 0x4803 81BC | 0x4803 C180 - 0x4803 C1BC | 0x4805 0180 - 0x4805 01BC | 0x4A1A 2180 - 0x4A1A 21BC | 0x4A1A 8180 - 0x4A1A 81BC | 0x4A1A E180 - 0x4A1A E1BC | XRSRCTL0 - XRSRCTL15 | Serializer 0 Control - Serializer 15 Control |
| 0x4803 8200 - 0x4803 8 23C | 0x4803 C200 - 0x4803 C23C | 0x4805 0200 - 0x4805 023C | 0x4A1A 2200 - 0x4A1A 223C | 0x4A1A 8200 - 0x4A1A 823C | 0x4A1A E200 - 0x4A1A E23C | TXBUF0 - TXBUF15 | Transmit Buffer for Serializer 0 - Transmit Buffer for Serializer 15 |

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**Table 9-77. McASP0/1/2/3/4/5 Registers (continued)**

| HEX ADDRESS RANGE | | | | | | ACRONYM | REGISTER NAME |
|---|---|---|---|---|---|---|---|
| MCASP0 | MCASP1 | MCASP2 | MCASP3 | MCASP4 | MCASP5 | | |
| 0x4803 8280 - 0x4803 82BC | 0x4803 C280 - 0x4803 C2BC | 0x4805 0280 - 0x4805 02BC | 0x4A1A 2280 - 0x4A1A 22BC | 0x4A1A 8280 - 0x4A1A 82BC | 0x4A1A E280 - 0x4A1A E2BC | RXBUF0 - RXBUF15 | Receive Buffer for Serializer 0 - Receive Buffer for Serializer 15 |
| 0x4803 9000 | 0x4803 D000 | 0x4805 1000 | 0x4A1A 3000 | 0x4A1A 9000 | 0x4A1A F000 | BUFFER_CFGRD_WFIFOCTL | Write FIFO Control |
| 0x4803 9004 | 0x4803 D004 | 0x4805 1004 | 0x4A1A 3004 | 0x4A1A 9004 | 0x4A1A F004 | BUFFER_CFGRD_WFIFOSTS | Write FIFO Status |
| 0x4803 9008 | 0x4803 D008 | 0x4805 1008 | 0x4A1A 3008 | 0x4A1A 9008 | 0x4A1A F008 | BUFFER_CFGRD_RFIFOCTL | Read FIFO Control |
| 0x4803 900C | 0x4803 D00C | 0x4805 100C | 0x0A1A 300C | 0x0A1A 900C | 0x0A1A F00C | BUFFER_CFGRD_RFIFOSTS | Read FIFO Status |
| 0x4803 9010 - 0x4803 9FFF | 0x4803 D010 - 0x4803 DFFF | 0x4805 1010 - 0x4805 1FFF | 0x4A1A 3010 - 0x4A1A 3FFF | 0x4A1A 9010 - 0x4A1A 9FFF | 0x4A1A F010 - 0x4A1A FFFF | – | Reserved |


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### 9.14.3 McASP (McASP[5:0]) Electrical Data/Timing

**Table 9-78. Timing Requirements for McASP(1)**

(see Figure 9-81)

| NO. | | | | OPP100/120/166 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | McASP[5:2,0] Only | | McASP1 Only | | |
| | | | | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(AHCLKRX)}$ | Cycle time, MCA[x]_AHCLKR/X | | 20 | | 20 | | ns |
| 2 | $t_{w(AHCLKRX)}$ | Pulse duration, MCA[x]_AHCLKR/X high or low | | 0.5P - 3(2) | | 0.5P - 3(2) | | ns |
| 3 | $t_{c(ACLKRX)}$ | Cycle time, MCA[x]_ACLKR/X | Any Other Conditions | 20 | | 20 | | ns |
| | | | ACLKx, AFSX and AXR are all inputs | – | | 12.5 | | ns |
| 4 | $t_{w(ACLKRX)}$ | Pulse duration, MCA[x]_ACLKR/X high or low | Any Other Conditions | 0.5R - 3(3) | | 0.5R - 3(3) | | ns |
| | | | ACLKx, AFSX and AXR are all inputs | – | | 0.5R - 1.5(3) | | ns |
| 5 | $t_{su(AFSRX-ACLKRX)}$ | Setup time, MCA[x]_AFSR/X input valid before MCA[X]_ACLKR/X | ACLKR/X int | 10.5 | | 10.5 | | ns |
| | | | ACLKR/X ext in | 4 | | 2 | | |
| | | | ACLKR/X ext out | 4 | | 2 | | |
| 6 | $t_{h(ACLKRX-AFSRX)}$ | Hold time, MCA[x]_AFSR/X input valid after MCA[X]_ACLKR/X | ACLKR/X int | -1 | | -1 | | ns |
| | | | ACLKR/X ext in | 1 | | 2 | | |
| | | | ACLKR/X ext out | 1 | | 2 | | |
| 7 | $t_{su(AXR-ACLKRX)}$ | Setup time, MCA[x]_AXR input valid before MCA[X]_ACLKR/X | ACLKR/X int | 10.5 | | 10.5 | | ns |
| | | | ACLKR/X ext in | 4 | | 2 | | |
| | | | ACLKR/X ext out | 4 | | 2 | | |
| 8 | $t_{h(ACLKRX-AXR)}$ | Hold time, MCA[x]_AXR input valid after MCA[X]_ACLKR/X | ACLKR/X int | -1 | | -1 | | ns |
| | | | ACLKR/X ext in | 1 | | 2 | | |
| | | | ACLKR/X ext out | 1 | | 2 | | |

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1
(2) P = MCA[x]_AHCLKR/X period in nano seconds (ns).
(3) R = MCA[x]_ACLKR/X period in ns.

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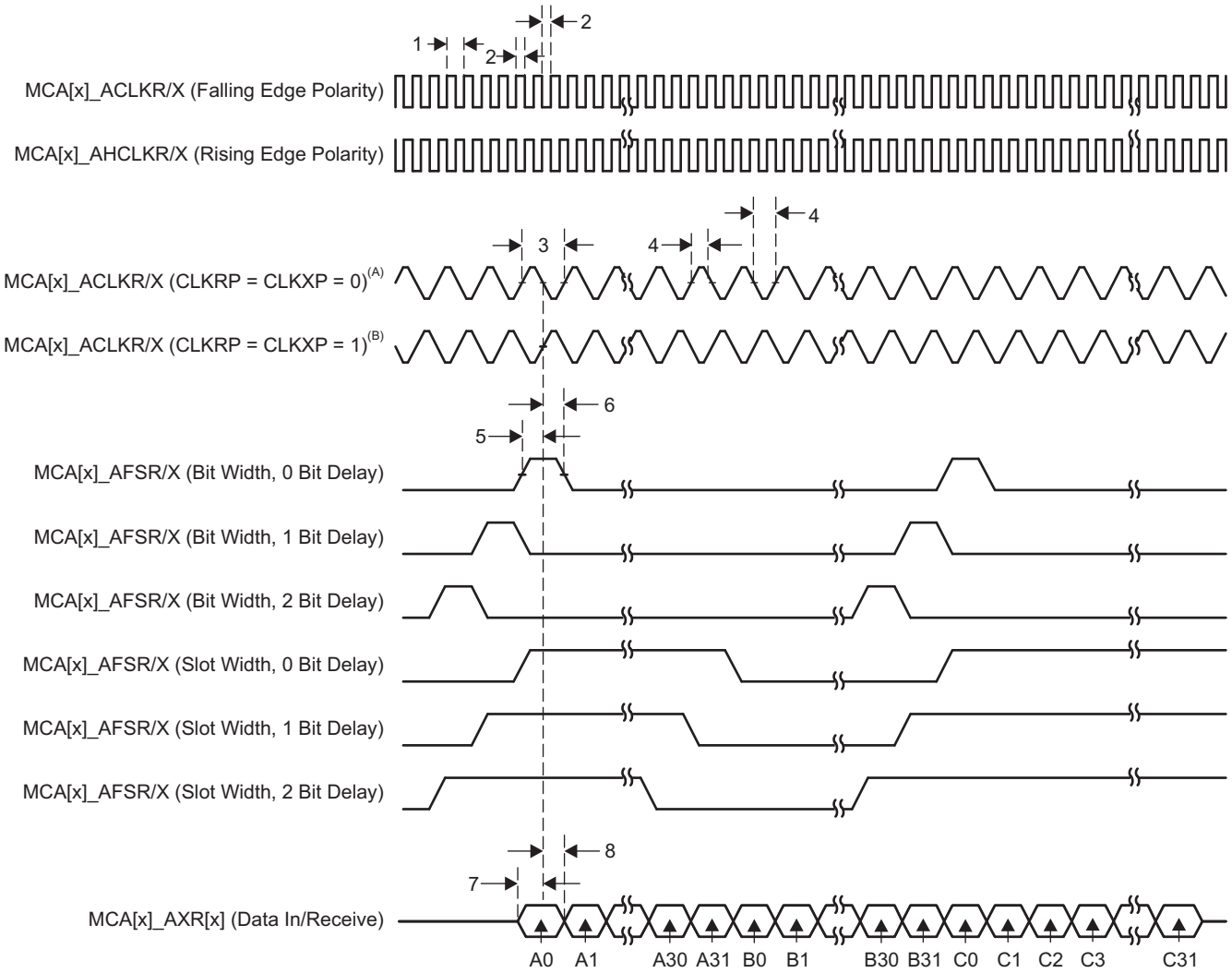


A. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

B. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).

**Figure 9-81. McASP Input Timing**


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### Table 9-79. Switching Characteristics Over Recommended Operating Conditions for McASP[1]

(see Figure 9-82)

| NO. | PARAMETER | | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| 9 | $t_{c(AHCLKRX)}$ | Cycle time, MCA[X]_AHCLKR/X | | 20[2] | | ns |
| 10 | $t_{w(AHCLKRX)}$ | Pulse duration, MCA[X]_AHCLKR/X high or low | | 0.5P - 2.5[3] | | ns |
| 11 | $t_{c(ACLKRX)}$ | Cycle time, MCA[X]_ACLKR/X | | 20 | | ns |
| 12 | $t_{w(ACLKRX)}$ | Pulse duration, MCA[X]_ACLKR/X high or low | | 0.5P - 2.5[3] | | ns |
| 13 | $t_{d(ACLKRX-AFSRX)}$ | Delay time, MCA[X]_ACLKR/X transmit edge to MCA[X]_AFSR/X output valid | ACLKR/X int | -2 | 5 | ns |
| | | | ACLKR/X ext in | 1 | 11.5 | |
| | | Delay time, MCA[X]_ACLKR/X transmit edge to MCA[X]_AFSR/X output valid with Pad Loopback | ACLKR/X ext out | 1 | 11.5 | |
| 14 | $t_{d(ACLKX-AXR)}$ | Delay time, MCA[X]_ACLKX transmit edge to MCA[X]_AXR output valid | ACLKX int | -2 | 5 | ns |
| | | | ACLKX ext in | 1 | 11.5 | |
| | | Delay time, MCA[X]_ACLKX transmit edge to MCA[X]_AXR output valid with Pad Loopback | ACLKX ext out | 1 | 11.5 | |
| 15 | $t_{dis(ACLKX-AXR)}$ | Disable time, MCA[X]_ACLKX transmit edge to MCA[X]_AXR output high impedance | ACLKX int | -2 | 5 | ns |
| | | | ACLKX ext in | 1 | 11.5 | |
| | | Disable time, MCA[X]_ACLKX transmit edge to MCA[X]_AXR output high impedance with Pad Loopback | ACLKX ext out | 1 | 11.5 | |

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1
(2) 50 MHz
(3) P = AHCLKR/X period.

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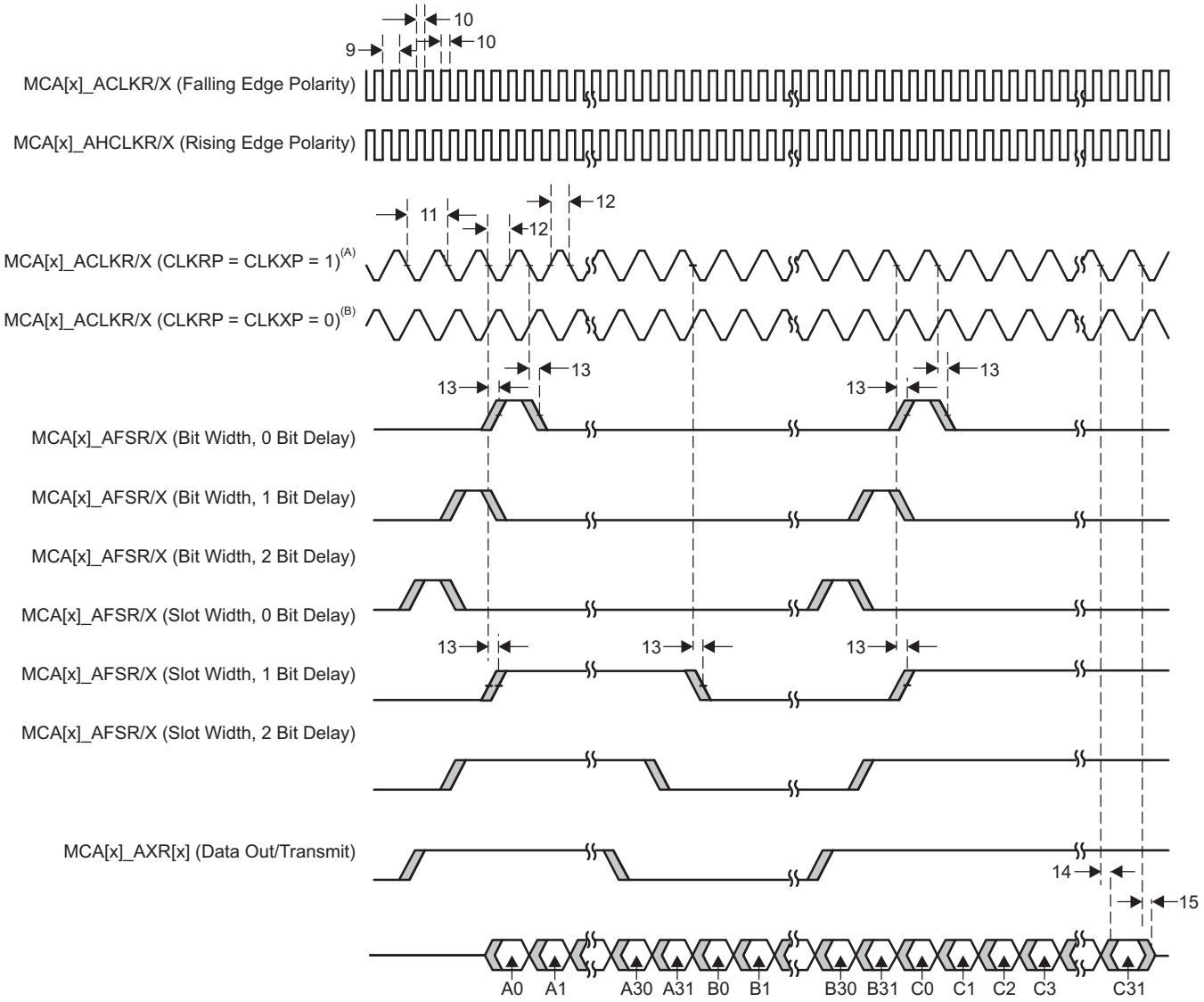


A. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).

B. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

**Figure 9-82. McASP Output Timing**


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## 9.15 Multichannel Buffered Serial Port (McBSP)

The McBSP provides these functions:

- Full-duplex communication
- Double-buffered data registers, which allow a continuous data stream
- Independent framing and clocking for receive and transmit
- Direct interface to industry-standard codecs, analog interface chips (AICs), and other serially connected analog-to-digital (A/D) and digital-to-analog (D/A) devices
- Supports TDM, I2S, and similar formats
- External shift clock or an internal, programmable frequency shift clock for data transfer
- 5KB Tx and Rx buffer
- Supports three interrupt and two DMA requests.

The McBSP module may support two types of data transfer at the system level:

- The full-cycle mode, for which one clock period is used to transfer the data, generated on one edge and captured on the same edge (one clock period later).
- The half-cycle mode, for which one half clock period is used to transfer the data, generated on one edge and captured on the opposite edge (one half clock period later). Note that a new data is generated only every clock period, which secures the required hold time. The interface clock (CLKX/CLKR) activation edge (data/frame sync capture and generation) has to be configured accordingly with the external peripheral (activation edge capability) and the type of data transfer required at the system level.

For more detailed information on the McBSP peripheral, see the *Multichannel Buffered Serial Port (McBSP)* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

The following sections describe the timing characteristics for applications in normal mode (that is, the McBSP connected to one peripheral) and TDM applications in multipoint mode.

### *9.15.1 McBSP Peripheral Register Descriptions*

**Table 9-80. McBSP Registers(1)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4700 0000 | REVNB | Revision Number Register |
| 0x4700 0010 | SYSCONFIG_REG | System Configuration Register |
| 0x4700 0020 | EOI | End of Interrupt Register |
| 0x4700 0024 | IRQSTATUS_RAW | Interrupt Status Raw Register |
| 0x4700 0028 | IRQSTATUS | Interrupt Status Register |
| 0x4700 002C | IRQENABLE_SET | Interrupt Enable Set Register |
| 0x4700 0030 | IRQENABLE_CLR | Interrupt Enable Clear Register |
| 0x4700 0034 | DMARXENABLE_SET | DMA Rx Enable Set Register |
| 0x4700 0038 | DMATXENABLE_SET | DMA Tx Enable Set Register |
| 0x4700 003C | DMARXENABLE_CLR | DMA Rx Enable Clear Register |
| 0x4700 0040 | DMATXENABLE_CLR | DMA Tx Enable Clear Register |
| 0x4700 0048 | DMARXWAKE_EN | DMA Rx Wake Enable Register |
| 0x4700 004C | DMATXWAKE_EN | DMA Tx Wake Enable Register |
| 0x4700 0100 | DRR_REG | McBSP data receive |
| 0x4700 0108 | DXR_REG | McBSP data transmit |
| 0x4700 0110 | SPCR2_REG | McBSP serial port control 2 |
| 0x4700 0114 | SPCR1_REG | McBSP serial port control 1 |

(1) Note that the McBSP registers are 32-bit aligned.

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**Table 9-80. McBSP Registers[1] (continued)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4700 0118 | RCR2_REG | McBSP receive control 2 |
| 0x4700 011C | RCR1_REG | McBSP receive control 1 |
| 0x4700 0120 | XCR2_REG | McBSP transmit control 2 |
| 0x4700 0124 | XCR1_REG | McBSP transmit control 1 |
| 0x4700 0128 | SRGR2_REG | McBSP sample rate generator 2 |
| 0x4700 012C | SRGR1_REG | McBSP sample rate generator 1 |
| 0x4700 0130 | MCR2_REG | McBSP multichannel 2 |
| 0x4700 0134 | MCR1_REG | McBSP multichannel 1 |
| 0x4700 0138 | RCERA_REG | McBSP receive channel enable partition A |
| 0x4700 013C | RCERB_REG | McBSP receive channel enable partition B |
| 0x4700 0140 | XCERA_REG | McBSP transmit channel enable partition A |
| 0x4700 0144 | XCERB_REG | McBSP transmit channel enable partition B |
| 0x4700 0148 | PCR_REG | McBSP pin control |
| 0x4700 014C | RCERC_REG | McBSP receive channel enable partition C |
| 0x4700 0150 | RCERD_REG | McBSP receive channel enable partition D |
| 0x4700 0154 | XCERC_REG | McBSP transmit channel enable partition C |
| 0x4700 0158 | XCERD_REG | McBSP transmit channel enable partition D |
| 0x4700 015C | RCERE_REG | McBSP receive channel enable partition E |
| 0x4700 0160 | RCERF_REG | McBSP receive channel enable partition F |
| 0x4700 0164 | XCERE_REG | McBSP transmit channel enable partition E |
| 0x4700 0168 | XCERF_REG | McBSP transmit channel enable partition F |
| 0x4700 016C | RCERG_REG | McBSP receive channel enable partition G |
| 0x4700 0170 | RCERH_REG | McBSP receive channel enable partition H |
| 0x4700 0174 | XCERG_REG | McBSP transmit channel enable partition G |
| 0x4700 0178 | XCERH_REG | McBSP transmit channel enable partition H |
| 0x4700 017C | REV_REG | McBSP revision number |
| 0x4700 0180 | RINTCLR_REG | McBSP receive interrupt clear |
| 0x4700 0184 | XINTCLR_REG | McBSP transmit interrupt clear |
| 0x4700 0188 | ROVFLCLR_REG | McBSP receive overflow interrupt clear |
| 0x4700 018C | SYSCONFIG_REG | McBSP system configuration |
| 0x4700 0190 | THRSH2_REG | McBSP transmit buffer threshold (DMA or IRQ trigger) |
| 0x4700 0194 | THRSH1_REG | McBSP receive buffer threshold (DMA or IRQ trigger) |
| 0x4700 01A0 | IRQSTATATUS | McBSP interrupt status (OCP compliant IRQ line) |
| 0x4700 01A4 | IRQENABLE | McBSP interrupt enable (OCP compliant IRQ line) |
| 0x4700 01A8 | WAKEUPEN | McBSP wakeup enable |
| 0x4700 01AC | XCCR_REG | McBSP transmit configuration control |
| 0x4700 01B0 | RCCR_REG | McBSP receive configuration control |
| 0x4700 01B4 | XBUFFSTAT_REG | McBSP transmit buffer status |
| 0x4700 01B8 | RBUFFSTAT_REG | McBSP receive buffer status |
| 0x4700 01C0 | STATUS_REG | McBSP status |


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### 9.15.2 McBSP Electrical Data/Timing

**Table 9-81. Timing Requirements for McBSP - Master Mode(1)**

(see Figure 9-83)

| NO. | | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 6 | $t_{su(DRV-CLKAE)}$ | Setup time, MCB_DR valid before MCB_CLK active edge(2) | 3.5 | | ns |
| 7 | $t_{h(CLKAE-DRV)}$ | Hold time, MCB_DR valid after MCB_CLK active edge(2) | 3.5 | | ns |

(1) The timings apply to all configurations regardless of MCB_CLK polarity and which clock edges are used to drive output data and capture input data.
(2) MCB_CLK corresponds to either MCB_CLKX or MCB_CLKR.

**Table 9-82. Switching Characteristics Over Recommended Operating Conditions for McBSP - Master Mode(1)**

(see Figure 9-83)

| NO. | PARAMETER | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{c(CLK)}$ | Cycle time, output MCB_CLK period(2) | 20.83 | | ns |
| 2 | $t_{w(CLKL)}$ | Pulse duration, output MCB_CLK low(2) | 0.5*P - 1(3) | | ns |
| 3 | $t_{w(CLKH)}$ | Pulse duration, output MCB_CLK high(2) | 0.5*P - 1(3) | | ns |
| 4 | $t_{d(CLKAE-FSV)}$ | Delay time, output MCB_CLK active edge to output MCB_FS valid(2)(4) | 0.3 | 9.4 | ns |
| 5 | $t_{d(CLKXAE-DXV)}$ | Delay time, output MCB_CLKX active edge to output MCB_DX valid | 0.3 | 9.4 | ns |

(1) The timings apply to all configurations regardless of MCB_CLK polarity and which clock edges are used to drive output data and capture input data.
(2) MCB_CLK corresponds to either MCB_CLKX or MCB_CLKR.
(3) P = MCB_CLKX/MCB_CLKR output CLK period, in ns; use whichever value is greater. This parameter applies to the maximum McBSP frequency. Operate serial clocks (CLKX/R) in the reasonable range of 40/60 duty cycle.
(4) MCB_FS corresponds to either MCB_FSX or MCB_FSR.

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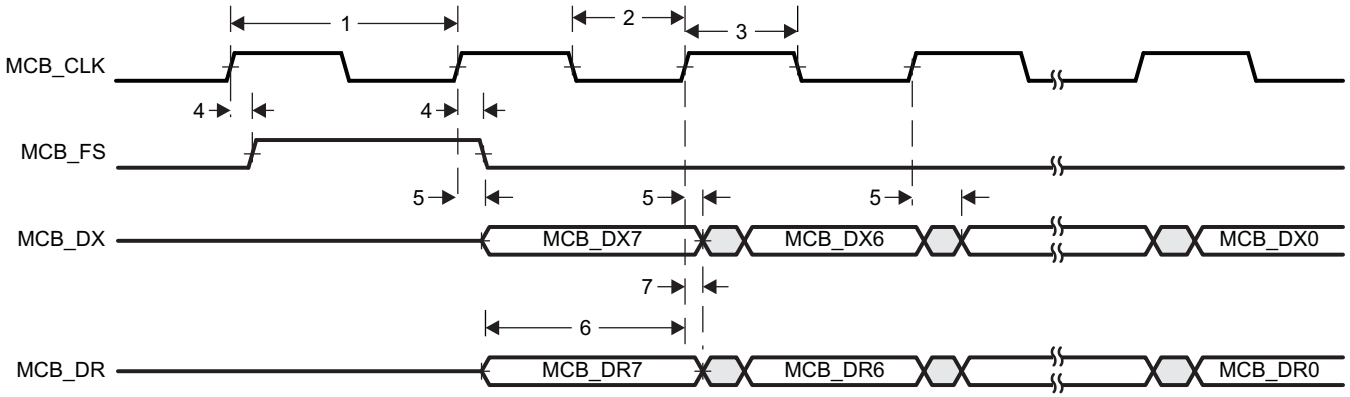


A. The timings apply to all configurations regardless of MCB_CLK polarity and which clock edges are used to drive output data and capture input data.

B. MCBSP_CLK corresponds to either MCBSP_CLKX or MCBSP_CLKR; MCBSP_FS corresponds to either MCBSP_FSX or MCBSP_FSR. McBSP in 6-pin mode: DX and DR as data pins; CLKX, CLKR, FSX and FSR as control pins. McBSP in 4-pin mode: DX and DR as data pins; CLKX and FSX pins as control pins. The CLKX and FSX pins are internally looped back via software configuration, respectively to the CLKR and FSR internal signals for data receive.

C. The polarity of McBSP frame synchronization is software configurable.

D. The active clock edge selection of MCBSP_CLK (rising or falling) on which MCBSP_DX data is latched and MCBSP_DR data is sampled is software configurable.

E. Timing diagrams are for data delay set to 1.

F. For further details about the registers used to configure McBSP, see the *Multichannel Buffered Serial Port (McBSP)* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

**Figure 9-83. McBSP Master Mode Timing**

**Table 9-83. Timing Requirements for McBSP - Slave Mode(1)**

(see Figure 9-84)

| NO. | | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{c(CLK)}$ | Cycle time, MCB_CLK period(2) | 20.83 | | ns |
| 2 | $t_{w(CLKL)}$ | Pulse duration, MCB_CLK low(2) | 0.5*P - 1(3) | | ns |
| 3 | $t_{w(CLKH)}$ | Pulse duration, MCB_CLK high(2) | 0.5*P - 1(3) | | ns |
| 4 | $t_{su(FSV-CLKAE)}$ | Setup time, MCB_FS valid before MCB_CLK active edge(2)(4) | 3.8 | | ns |
| 5 | $t_{h(CLKAE-FSV)}$ | Hold time, MCB_FS valid after MCB_CLK active edge(2)(4) | 0.5 | | ns |
| 7 | $t_{su(DRV-CLKAE)}$ | Setup time, MCB_DR valid before MCB_CLK active edge(2) | 3.8 | | ns |
| 8 | $t_{h(CLKAE-DRV)}$ | Hold time, MCB_DR valid after MCB_CLK active edge(2) | 0.5 | | ns |

(1) The timings apply to all configurations regardless of MCB_CLK polarity and which clock edges are used to drive output data and capture input data.
(2) MCB_CLK corresponds to either MCB_CLKX or MCB_CLKR.
(3) P = MCB_CLKX/MCB_CLKR output CLK period, in ns; use whichever value is greater. This parameter applies to the maximum McBSP frequency. Operate serial clocks (CLKX/R) in the reasonable range of 40/60 duty cycle.
(4) MCB_FS corresponds to either MCB_FSX or MCB_FSR.

**Table 9-84. Switching Characteristics Over Recommended Operating Conditions for McBSP - Slave Mode(1)**

(see Figure 9-84)

| NO. | PARAMETER | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 6 | $t_{d(CLKXAE-DXV)}$ | Delay time, input MCB_CLKx active edge to output MCB_DX valid | 0.5 | 12.5 | ns |

(1) The timings apply to all configurations regardless of MCB_CLK polarity and which clock edges are used to drive output data and capture input data.


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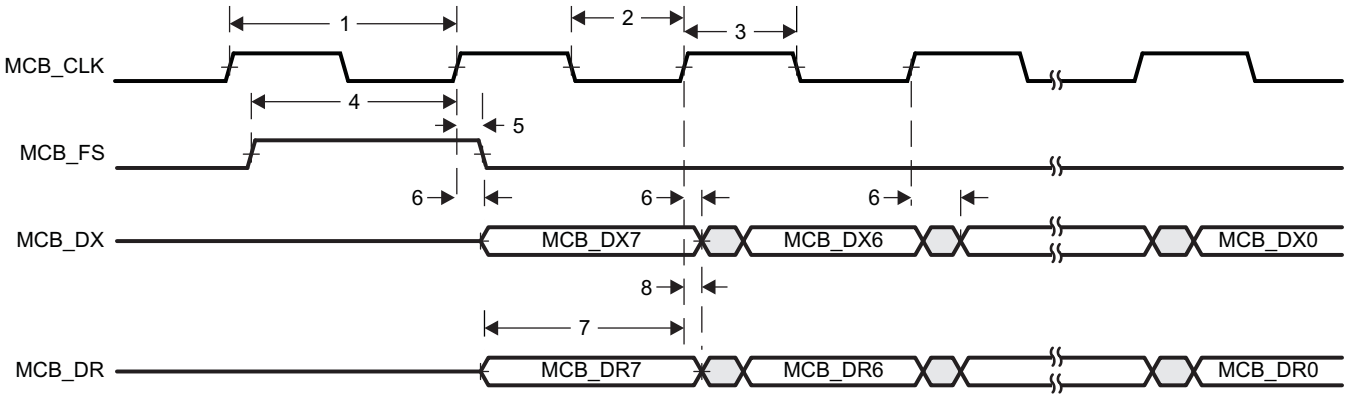


A. The timings apply to all configurations regardless of MCB_CLK polarity and which clock edges are used to drive output data and capture input data.

B. MCBSP_CLK corresponds to either MCBSP_CLKX or MCBSP_CLKR; MCBSP_FS corresponds to either MCBSP_FSX or MCBSP_FSR. McBSP in 6-pin mode: DX and DR as data pins; CLKX, CLKR, FSX and FSR as control pins. McBSP in 4-pin mode: DX and DR as data pins; CLKX and FSX pins as control pins. The CLKX and FSX pins are internally looped back via software configuration, respectively to the CLKR and FSR internal signals for data receive.

C. The polarity of McBSP frame synchronization is software configurable.

D. The active clock edge selection of MCBSP_CLK (rising or falling) on which MCBSP_DX data is latched and MCBSP_DR data is sampled is software configurable.

E. Timing diagrams are for data delay set to 1.

F. For further details about the registers used to configure McBSP, see the *Multichannel Buffered Serial Port (McBSP)* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

**Figure 9-84. McBSP Slave Mode Timing**

## 9.16 MultiMedia Card/Secure Digital/Secure Digital Input Output (MMC/SD/SDIO)

The device includes 3 MMC/SD/SDIO Controllers which are compliant with MMC V4.3, Secure Digital Part 1 Physical Layer Specification V2.00 and Secure Digital Input Output (SDIO) V2.00 specifications.

The device MMC/SD/SDIO Controller has the following features:

- MultiMedia card (MMC)
- Secure Digital (SD) memory card
- MMC/SD protocol support
- SDIO protocol support
- Programmable clock frequency
- 1024 byte read/write FIFO to lower system overhead
- Slave EDMA transfer capability
- SD High capacity support

### *9.16.1 MMC/SD/SDIO Peripheral Register Descriptions*

**Table 9-85. MMC/SD/SDIO Registers(1)**

| MMC/SD/SDIO0 HEX ADDRESS | MMC/SD/SDIO1 HEX ADDRESS | MMC/SD/SDIO2 HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|---|---|
| 0x4806 0000 | 0x481D 8000 | 0x4781 0000 | MMCHS_HL_REV | IP Revision Identifier |
| 0x4806 0004 | 0x481D 8004 | 0x4781 0004 | MMCHS_HL_HWINFO | Hardware Configuration |
| 0x4806 0010 | 0x481D 8010 | 0x4781 0010 | MMCHS_HL_SYSCONFIG | Clock Management Configuration |
| 0x4806 0110 | 0x481D 8110 | 0x4781 0110 | MMCHS_SYSCONFIG | System Configuration |
| 0x4806 0114 | 0x481D 8114 | 0x4781 0114 | MMCHS_SYSSTATUS | System Status |
| 0x4806 0124 | 0x481D 8124 | 0x4781 0124 | MMCHS_CSRE | Card status response error |
| 0x4806 0128 | 0x481D 8128 | 0x4781 0128 | MMCHS_SYSTEST | System Test |
| 0x4806 012C | 0x481D 812C | 0x4781 012C | MMCHS_CON | Configuration |
| 0x4806 0130 | 0x481D 8130 | 0x4781 0130 | MMCHS_PWCNT | Power counter |
| 0x4806 0200 | 0x481D 8200 | 0x4781 0200 | MMCHS_SDMASA | SDMA System address: |
| 0x4806 0204 | 0x481D 8204 | 0x4781 0204 | MMCHS_BLK | Transfer Length Configuration |
| 0x4806 0208 | 0x481D 8208 | 0x4781 0208 | MMCHS_ARG | Command argument |
| 0x4806 020C | 0x481D 820C | 0x4781 020C | MMCHS_CMD | Command and transfer mode |
| 0x4806 0210 | 0x481D 8210 | 0x4781 0210 | MMCHS_RSP10 | Command Response 0 and 1 |
| 0x4806 0214 | 0x481D 8214 | 0x4781 0214 | MMCHS_RSP32 | Command Response 2 and 3 |
| 0x4806 0218 | 0x481D 8218 | 0x4781 0218 | MMCHS_RSP54 | Command Response 4 and 5 |
| 0x4806 021C | 0x481D 821C | 0x4781 021C | MMCHS_RSP76 | Command Response 6 and 7 |
| 0x4806 0220 | 0x481D 8220 | 0x4781 0220 | MMCHS_DATA | Data |
| 0x4806 0224 | 0x481D 8224 | 0x4781 0224 | MMCHS_PSTATE | Present state |
| 0x4806 0228 | 0x481D 8228 | 0x4781 0228 | MMCHS_HCTL | Host Control |
| 0x4806 022C | 0x481D 822C | 0x4781 022C | MMCHS_SYSCTL | SD system control |
| 0x4806 0230 | 0x481D 8230 | 0x4781 0230 | MMCHS_STAT | Interrupt status |
| 0x4806 0234 | 0x481D 8234 | 0x4781 0234 | MMCHS_IE | Interrupt SD enable |
| 0x4806 0238 | 0x481D 8238 | 0x4781 0238 | MMCHS_ISE | Interrupt Signal Enable |
| 0x4806 023C | 0x481D 823C | 0x4781 023C | MMCHS_AC12 | Auto CMD12 Error Status |
| 0x4806 0240 | 0x481D 8240 | 0x4781 0240 | MMCHS_CAPA | Capabilities |
| 0x4806 0248 | 0x481D 8248 | 0x4781 0248 | MMCHS_CUR_CAPA | Maximum current capabilities |

(1) SD/SDIO registers are limited to 32-bit data accesses; 16-bit and 8-bit accesses are not allowed and can corrupt register content.


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**Table 9-85. MMC/SD/SDIO Registers[1] (continued)**

| MMC/SD/SDIO0 HEX ADDRESS | MMC/SD/SDIO1 HEX ADDRESS | MMC/SD/SDIO2 HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|---|---|
| 0x4806 0250 | 0x481D 8250 | 0x4781 0250 | MMCHS_FE | Force Event |
| 0x4806 0254 | 0x481D 8254 | 0x4781 0254 | MMCHS_ADMAES | ADMA Error Status |
| 0x4806 0258 | 0x481D 8258 | 0x4781 0258 | MMCHS_ADMASAL | ADMA System address Low bits |
| 0x4806 025C | 0x481D 825C | 0x4781 025C | MMCHS_ADMASAH | ADMA System address High bits |
| 0x4806 02FC | 0x481D 82FC | 0x4781 02FC | MMCHS_REV | Versions |

### 9.16.2 MMC/SD/SDIO Electrical Data/Timing

**Table 9-86. Timing Requirements for MMC/SD/SDIO**

(see Figure 9-86, Figure 9-88)

| NO. | | | | OPP100/120/166 ALL MODES MIN | OPP100/120/166 ALL MODES MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{su(CMDV-CLKH)}$ | Setup time, SD_CMD valid before SD_CLK rising clock edge | | 4.1 | | ns |
| 2 | $t_{h(CLKH-CMDV)}$ | Hold time, SD_CMD valid after SD_CLK rising clock edge | SD1 | 1.9 | | ns |
| | | | SD0, SD2 | 2.9 | | |
| 3 | $t_{su(DATV-CLKH)}$ | Setup time, SD_DATx valid before SD_CLK rising clock edge | | 4.1 | | ns |
| 4 | $t_{h(CLKH-DATV)}$ | Hold time, SD_DATx valid after SD_CLK rising clock edge | SD1 | 1.9 | | ns |
| | | | SD0, SD2 | 2.9 | | |

**Table 9-87. Switching Characteristics Over Recommended Operating Conditions for MMC/SD/SDIO**

(see Figure 9-85 through Figure 9-88)

| NO. | PARAMETER | | OPP100/120/166 MODES 3.3 V STD 1.8 V SDR12 MIN | 3.3 V STD 1.8 V SDR12 MAX | 3.3 V HS 1.8 V SDR25 MIN | 3.3 V HS 1.8 V SDR25 MAX | UNIT |
|---|---|---|---|---|---|---|---|
| 7 | $f_{op(CLK)}$ | Operating frequency, SD_CLK | | 24 | | 48 | MHz |
| | $t_{c(CLK)}$ | Operating period: SD_CLK | 41.7 | | 20.8 | | ns |
| 8 | $f_{op(CLKID)}$ | Identification mode frequency, SD_CLK | | 400 | | 400 | kHz |
| | $t_{c(CLKID)}$ | Identification mode period: SD_CLK | 2500.0 | | 2500.0 | | ns |
| 9 | $t_{w(CLKL)}$ | Pulse duration, SD_CLK low | 0.5*P[1] | | 0.5*P[1] | | ns |
| 10 | $t_{w(CLKH)}$ | Pulse duration, SD_CLK high | 0.5*P[1] | | 0.5*P[1] | | ns |
| 11 | $t_{r(CLK)}$ | Rise time, All Signals (10% to 90%) | | 2.2 | | 2.2 | ns |
| 12 | $t_{f(CLK)}$ | Fall time, All Signals (10% to 90%) | | 2.2 | | 2.2 | ns |
| 13 | $t_{d(CLKL-CMD)}$ | Delay time, SD_CLK rising clock edge to SD_CMD transition | 1.5 | 10 | 1.5 | 10 | ns |
| 14 | $t_{d(CLKL-DAT)}$ | Delay time, SD_CLK rising clock edge to SD_DATx transition | 1.5 | 10 | 1.5 | 10 | ns |

(1) P = SD_CLK period.

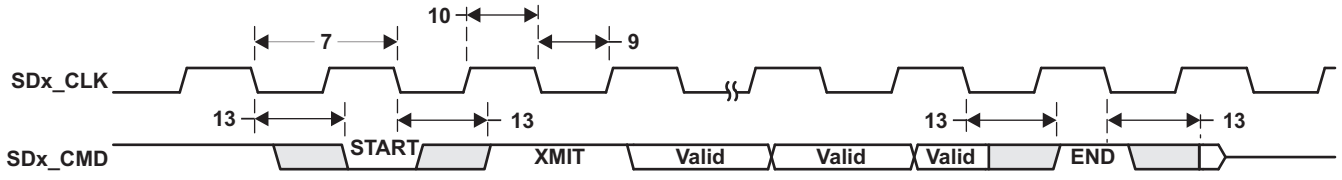


**Figure 9-85. MMC/SD/SDIO Host Command Timing**

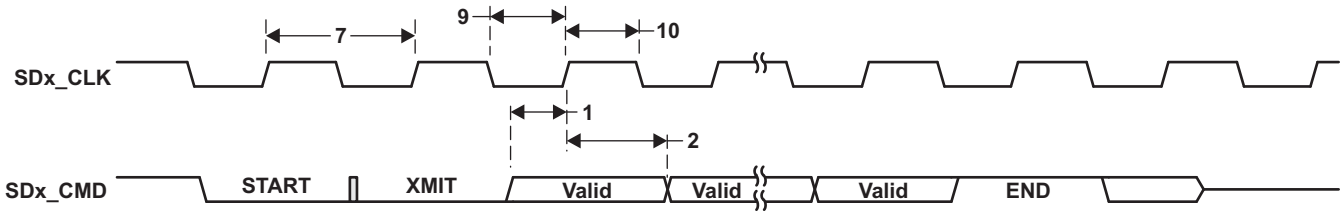


**Figure 9-86. MMC/SD/SDIO Card Response Timing**

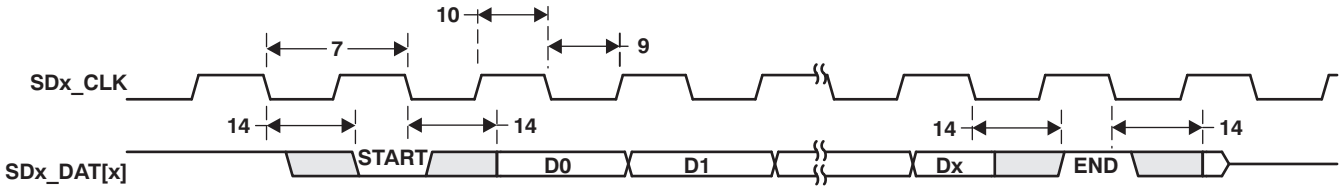


**Figure 9-87. MMC/SD/SDIO Host Write Timing**

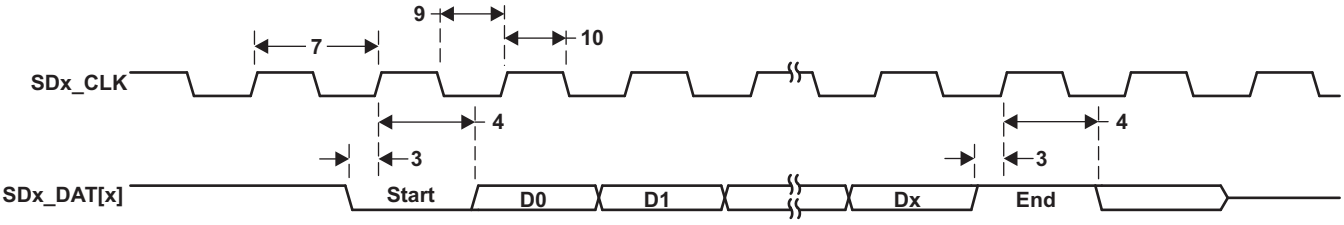


**Figure 9-88. MMC/SD/SDIO Host Read and Card CRC Status Timing**


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## 9.17 Peripheral Component Interconnect Express (PCIe)

The device supports connections to PCIe-compliant devices via the integrated PCIe master/slave bus interface. The PCIe module is comprised of a dual-mode PCIe core and a SerDes PHY. The device implements a single one-lane PCIe 2.0 (5.0 GT/s) Endpoint/Root Complex port.

The device PCIe supports the following features:

- Supports Gen1/Gen2 in x1 or x2 mode
- One port with one 5 GT/s lane
- Single virtual channel (VC), single traffic class (TC)
- Single function in end-point mode
- Automatic width and speed negotiation and lane reversal
- Max payload: 128 byte outbound, 256 byte inbound
- Automatic credit management
- ECRC generation and checking
- Configurable BAR filtering
- Supports PCIe messages
- Legacy interrupt reception (RC) and generation (EP)
- MSI generation and reception
- PCI device power management, except D3 cold with vaux
- Active state power management state L0 and L1.

For more detailed information on the PCIe port peripheral module, see the *PCI Express (PCIe) Module* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

The PCIe peripheral on the device conforms to the PCI Express Base 2.0 Specification.

### *9.17.1 PCIe Peripheral Register Descriptions*

**Table 9-88. PCIe Registers**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x5100 0000 | PID | Peripheral Version and ID |
| 0x5100 0004 | CMD_STATUS | Command Status |
| 0x5100 0008 | CFG_SETUP | Config Transaction Setup |
| 0x5100 000C | IOBASE | IO TLP Base |
| 0x5100 0010 | TLPCFG | TLP Attribute Configuration |
| 0x5100 0014 | RSTCMD | Reset Command and Status |
| 0x5100 0020 | PMCMD | Power Management Command |
| 0x5100 0024 | PMCFG | Power Management Configuration |
| 0x5100 0028 | ACT_STATUS | Activity Status |
| 0x5100 0030 | OB_SIZE | Outbound Size |
| 0x5100 0034 | DIAG_CTRL | Diagnostic Control |
| 0x5100 0038 | ENDIAN | Endian Mode |
| 0x5100 003C | PRIORITY | CBA Transaction Priority |
| 0x5100 0050 | IRQ_EOI | End of Interrupt |
| 0x5100 0054 | MSI_IRQ | MSI Interrupt IRQ |
| 0x5100 0064 | EP_IRQ_SET | Endpoint Interrupt Request Set |
| 0x5100 0068 | EP_IRQ_CLR | Endpoint Interrupt Request Clear |
| 0x5100 006C | EP_IRQ_STATUS | Endpoint Interrupt Status |
| 0x5100 0070 | GPRO | General Purpose 0 |

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**Table 9-88. PCIe Registers (continued)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x5100 0074 | GPR1 | General Purpose 1 |
| 0x5100 0078 | GPR2 | General Purpose 2 |
| 0x5100 007C | GPR3 | General Purpose 3 |
| 0x5100 0100 | MSI0_IRQ_STATUS_RAW | MSI 0 Interrupt Raw Status |
| 0x5100 0104 | MSI0_IRQ_STATUS | MSI 0 Interrupt Enabled Status |
| 0x5100 0108 | MSI0_IRQ_ENABLE_SET | MSI 0 Interrupt Enable Set |
| 0x5100 010C | MSI0_IRQ_ENABLE_CLR | MSI 0 Interrupt Enable Clear |
| 0x5100 0180 | IRQ_STATUS_RAW | Raw Interrupt Status |
| 0x5100 0184 | IRQ_STATUS | Interrupt Enabled Status |
| 0x5100 0188 | IRQ_ENABLE_SET | Interrupt Enable Set |
| 0x5100 018C | IRQ_ENABLE_CLR | Interrupt Enable Clear |
| 0x5100 01C0 | ERR_IRQ_STATUS_RAW | Raw ERR Interrupt Status |
| 0x5100 01C4 | ERR_IRQ_STATUS | ERR Interrupt Enabled Status |
| 0x5100 01C8 | ERR_IRQ_ENABLE_SET | ERR Interrupt Enable Set |
| 0x5100 01CC | ERR_IRQ_ENABLE_CLR | ERR Interrupt Enable Clear |
| 0x5100 01D0 | PMRST_IRQ_STATUS_RAW | Power Management and Reset Interrupt Status |
| 0x5100 01D4 | PMRST_IRQ_STATUS | Power Management and Reset Interrupt Enabled Status |
| 0x5100 01D8 | PMRST_ENABLE_SET | Power Management and Reset Interrupt Enable Set |
| 0x5100 01DC | PMRST_ENABLE_CLR | Power Management and Reset Interrupt Enable Clear |
| 0x5100 0200 | OB_OFFSET_INDEXn | Outbound Translation Region N Offset Low and Index |
| 0x5100 0204 | OB_OFFSETn_HI | Outbound Translation Region N Offset High |
| 0x5100 0300 | IB_BAR0 | Inbound Translation Bar Match 0 |
| 0x5100 0304 | IB_START0_LO | Inbound Translation 0 Start Address Low |
| 0x5100 0308 | IB_START0_HI | Inbound Translation 0 Start Address High |
| 0x5100 030C | IB_OFFSET0 | Inbound Translation 0 Address Offset |
| 0x5100 0310 | IB_BAR1 | Inbound Translation Bar Match 1 |
| 0x5100 0314 | IB_START1_LO | Inbound Translation 1 Start Address Low |
| 0x5100 0318 | IB_START1_HI | Inbound Translation 1 Start Address High |
| 0x5100 031C | IB_OFFSET1 | Inbound Translation 1 Address Offset |
| 0x5100 0320 | IB_BAR2 | Inbound Translation Bar Match 2 |
| 0x5100 0324 | IB_START2_LO | Inbound Translation 2 Start Address Low |
| 0x5100 0328 | IB_START2_HI | Inbound Translation 2 Start Address High |
| 0x5100 032C | IB_OFFSET2 | Inbound Translation 2 Address Offset |
| 0x5100 0330 | IB_BAR3 | Inbound Translation Bar Match 3 |
| 0x5100 0334 | IB_START3_LO | Inbound Translation 3 Start Address Low |
| 0x5100 0338 | IB_START3_HI | Inbound Translation 3 Start Address High |
| 0x5100 033C | IB_OFFSET3 | Inbound Translation 3 Address Offset |
| 0x5100 0380 | PCS_CFG0 | PCS Configuration 0 |
| 0x5100 0384 | PCS_CFG1 | PCS Configuration 1 |
| 0x5100 0388 | PCS_STATUS | PCS Status |
| 0x5100 038C | SERDES_STATUS | SerDes Status |
| 0x5100 0390 | SERDES_RXCFG0 | SerDes Receive Configuration 0 Register |
| 0x5100 0394 | SERDES_RXCFG1 | SerDes Receive Configuration 1 Register |
| 0x5100 0398 | SERDES_RXCFG2 | SerDes Receive Configuration 2 Register |
| 0x5100 039C | SERDES_RXCFG3 | SerDes Receive Configuration 3 Register |
| 0x5100 03A0 | SERDES_RXCFG4 | SerDes Receive Configuration 4 Register |
| 0x5100 03A4 | SERDES_TXCFG0 | SerDes Transmit Configuration 0 Register |


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**Table 9-88. PCIe Registers (continued)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x5100 03A8 | SERDES_TXCFG1 | SerDes Transmit Configuration 1 Register |
| 0x5100 03AC | SERDES_TXCFG2 | SerDes Transmit Configuration 2 Register |
| 0x5100 03B0 | SERDES_TXCFG3 | SerDes Transmit Configuration 3 Register |
| 0x5100 03B4 | SERDES_TXCFG4 | SerDes Transmit Configuration 4 Register |

**Table 9-89. Configuration Registers Type 0 Summary**

| HEX ADDRESS | ACRONYM | NAME |
|---|---|---|
| 5100_1000 | VENDOR_DEVICE_ID | Vendor Device ID Register |
| 5100_1004 | STATUS_COMMAND | Status and Command Register |
| 5100_1008 | CLASSCODE_REVID | Class Code and Revision Register |
| 5100_100C | BIST_HEADER | BIST, Header Type, Latency Time, and Cache Line Size register |
| 5100_1010 | BAR0 (64/-32-Bit Mode) | Base Address Register 0 |
| 5100_1014 | BAR1 (32-Bit Mode) | Base Address Register 1 |
| | BAR1 (64-Bit Mode) | Base Address Register 1 (64-bit BAR0) |
| 5100_1018 | BAR2 (64/-32-Bit Mode) | Base Address Register 2 |
| 5100_101C | BAR3 (32-Bit Mode) | Base Address Register 3 |
| | BAR3 (64-Bit Mode) | Base Address Register 3 (64-bit BAR2) |
| 5100_1020 | BAR4 (64/-32-Bit Mode) | Base Address Register 4 |
| 5100_1024 | BAR5 (32-Bit Mode) | Base Address Register 5 |
| | BAR5 (64-Bit Mode) | Base Address Register 5 (64-bit BAR4) |
| 5100_1028 | CARDBUS | CardBus CIS Pointer Register |
| 5100_102C | SUBSYS_VNDR_ID | Subsystem and Subsystem Vendor ID Register |
| 5100_1030 | EXPNSN_ROM | Expansion ROM Base Address Register |
| 5100_1034 | CAP_PTR | Capabilities Pointer Register |
| 5100_103C | INT_PIN | Interrupt Pin Register |

**Table 9-90. Configuration Registers Type 1 Summary**

| HEX ADDRESS | ACRONYM | NAME |
|---|---|---|
| 5100_1000 | VENDOR_DEVICE_ID | Vendor Device ID Register |
| 5100_1004 | STATUS_COMMAND | Status and Command Register |
| 5100_1008 | CLASSCODE_REVID | Class Code and Revision Register |
| 5100_100C | BIST_HEADER | BIST, Header Type, Latency Time, and Cache Line Size register |
| 5100_1010 | BAR0 (64/-32-Bit Mode) | Base Address Register 0 (64/32-bit mode) |

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**Table 9-90. Configuration Registers Type 1 Summary (continued)**

| HEX ADDRESS | ACRONYM | NAME |
|---|---|---|
| 5100_1014 | BAR1 (32-Bit Mode) | Base Address Register 1 (32-bit mode) |
| | BAR1 (64-Bit Mode) | Base Address Register 1 (64-bit BAR0) |
| 5100_1018 | BUSNUM | Latency Timer and Bus Number Register |
| 5100_101C | SECSTAT | Secondary Status and I/O Base/Limit Register |
| 5100_1020 | MEMSPACE | Memory Limit and Base Register |
| 5100_1024 | PREFETCH_MEM | Prefetchable Memory Limit and Base Register |
| 5100_1028 | PREFETCH_BASE | Prefetchable Memory Base Upper 32-bits Register |
| 5100_102C | PREFETCH_LIMIT | Prefetchable Limit Upper 32-bits Register |
| 5100_1030 | IOSPACE | I/O Base and Limit Upper 16-bits Register |
| 5100_1034 | CAP_PTR | Capabilities Pointer Register |
| 5100_1038 | EXPNSN_ROM | Expansion ROM Base Address Register |
| 5100_103C | BRIDGE_INT | Bridge Control Register |

**Table 9-91. Power Management Capability Register Summary**

| HEX ADDRESS | ACRONYM | NAME |
|---|---|---|
| 5100_1040 | PMCAP | Power Management Capability Register |
| 5100_1044 | PM_CTL_STAT | Power Management Control and Status Register |

**Table 9-92. Message Signaled Interrupts (MSI) Register Summary**

| HEX ADDRESS | ACRONYM | NAME |
|---|---|---|
| 5100_1050 | MSI_CAP | MSI Capabilities Register |
| 5100_1054 | MSI_LOW32 | MSI Lower 32 bits Register |
| 5100_1058 | MSI_UP32 | MSI Upper 32 bits Register |
| 5100_105C | MSI_DATA | MSI Data Register |

**Table 9-93. PCI Express Capabilities Register Summary**

| HEX ADDRESS | ACRONYM | NAME |
|---|---|---|
| 5100_1070 | PCIES_CAP | PCI Express Capabilities Register |
| 5100_1074 | DEVICE_CAP | Device Capabilities Register |
| 5100_1078 | DEV_STAT_CTRL | Device Status and Control Register |
| 5100_107C | LINK_CAP | Link Capabilities Register |
| 5100_1080 | LINK_STAT_CTRL | Link Status and Control Register |
| 5100_1084 | SLOT_CAP | Slot Capabilities Register (RC Mode Only) |
| 5100_1088 | SLOT_STAT_CTRL | Slot Status and Control Register (RC Mode Only) |
| 5100_108C | ROOT_CTRL_CAP | Root Control and Capabilities Register (RC Mode Only) |
| 5100_1090 | ROOT_STATUS | Root Status and Control Register (RC Mode Only) |
| 5100_1094 | DEV_CAP2 | Device Capabilities 2 Register |
| 5100_1098 | DEV_STAT_CTRL2 | Device Status and Control 2 Register |
| 5100_10A0 | LINK_CTRL2 | Link Control 2 Register |

**Table 9-94. PCI Express Extended Capabilities Register Summary**

| HEX ADDRESS | ACRONYM | NAME |
|---|---|---|
| 5100_1100 | PCIE_EXTCAP | PCI Express Extended Capabilities Header Register |
| 5100_1104 | PCIE_UNCERR | PCI Express Uncorrectable Error Status Register |
| 5100_1108 | PCIE_UNCERR_MASK | PCI Express Uncorrectable Error Mask Register |
| 5100_110C | PCIE_UNCERR_SVRTY | PCI Express Uncorrectable Error Severity Register |


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**Table 9-94. PCI Express Extended Capabilities Register Summary (continued)**

| HEX ADDRESS | ACRONYM | NAME |
|---|---|---|
| 5100_1110 | PCIE_CERR | PCI Express Correctable Error Status Register |
| 5100_1114 | PCIE_CERR_MASK | PCI Express Correctable Error Mask Register |
| 5100_1118 | PCIE_ACCR | PCI Express Advanced Capabilities and Control Register |
| 5100_111C | HDR_LOG0 | Header Log 0 Register |
| 5100_1120 | HDR_LOG1 | Header Log 1 Register |
| 5100_1124 | HDR_LOG2 | Header Log 2 Register |
| 5100_1128 | HDR_LOG3 | Header Log 3 Register |
| 5100_112C | RC_ERR_CMD | Root Error Command Register |
| 5100_1130 | RC_ERR_ST | Root Error Status Register |
| 5100_1134 | ERR_SRC_ID | Error Source Identification Register |

**Table 9-95. Port Logic Register Summary**

| HEX ADDRESS | ACRONYM | NAME |
|---|---|---|
| 5100_1700 | PL_ACKTIMER | Ack Latency Time and Replay Timer Register |
| 5100_1704 | PL_OMSG | Other Message Register |
| 5100_1708 | PL_FORCE_LINK | Port Force Link Register |
| 5100_170C | ACK_FREQ | Ack Frequency Register |
| 5100_1710 | PL_LINK_CTRL | Port Link Control Register |
| 5100_1714 | LANE_SKEW | Lane Skew Register |
| 5100_1718 | SYM_NUM | Symbol Number Register |
| 5100_171C | SYMTIMER_FLTMASK | Symbol Timer and Filter Mask Register |
| 5100_1720 | FLT_MASK2 | Filter Mask 2 Register |
| 5100_1728 | DEBUG0 | Debug 0 Register |
| 5100_172C | DEBUG1 | Debug 1 Register |
| 5100_180C | PL_GEN2 | Gen2 Register |

### *9.17.2 PCIe Electrical Data/Timing*

Texas Instruments (TI) has performed the simulation and system characterization to ensure that the PCIe peripheral meets all AC timing specifications as required by the PCI Express Base 2.0 Specification. Therefore, the AC timing specifications are not reproduced here. For more information on the AC timing specifications, see Sections 4.3.3.5 and 4.3.4.4 of the PCI Express Base 2.0 Specification.

### *9.17.3 PCIe Design and Layout Guidelines*

#### 9.17.3.1 Clock Source

A standard 100-MHz PCIe differential clock source must be used for PCIe operation (for more details, see Section 8.4.2, *SERDES CLKN/P Input Clock*).

#### 9.17.3.2 PCIe Connections and Interface Compliance

The PCIe interface on the device is compliant with the PCI Express Base 2.0 Specification. Refer to the PCIe specifications for all connections that are described in it. For coupling capacitor selection, see Section 9.17.3.2.1, *Coupling Capacitors*.

The use of PCIe-compatible bridges and switches is allowed for interfacing with more than one other processor or PCIe device.

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#### 9.17.3.2.1 Coupling Capacitors

AC coupling capacitors are required on the transmit data pair. Table 9-96 shows the requirements for these capacitors.

**Table 9-96. AC Coupling Capacitors Requirements**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| PCIe AC coupling capacitor value | 75 | | 200 | nF |
| PCIe AC coupling capacitor package size(1) | | 0402 | 0603 | EIA(2) |

(1) The physical size of the capacitor should be as small as practical. Use the same size on both lines in each pair, placed side by side.
(2) EIA LxW units; that is, a 0402 is a 40x20 mil (thousandths of an inch) surface-mount capacitor.

#### 9.17.3.2.2 Polarity Inversion

The PCIe specification requires polarity inversion support. This means, for layout purposes, polarity is unimportant since each signal can change its polarity on-die inside the chip. This means polarity within a lane is unimportant for layout.

### 9.17.3.3 Non-Standard PCIe Connections

The following sections contain suggestions for any PCIe connection that is ***not*** described in the official PCIe specification, such as an on-board device-to-device connection, or device-to-other PCIe-compliant processor connection.

#### 9.17.3.3.1 PCB Stackup Specifications

Table 9-97 shows the stackup and feature sizes required for these types of PCIe connections.

**Table 9-97. PCIe PCB Stackup Specifications**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| PCB Routing/Plane Layers | 4 | 6 | - | Layers |
| Signal Routing Layers | 2 | 3 | - | Layers |
| Number of ground plane cuts allowed within PCIe routing region | - | - | 0 | Cuts |
| Number of layers between PCIe routing area and reference plane(1) | - | - | 0 | Layers |
| PCB Routing clearance | - | 4 | - | Mils |
| PCB Trace width(2) | - | 4 | - | Mils |
| PCB BGA escape via pad size | - | 20 | - | Mils |
| PCB BGA escape via hole size | - | 10 | | Mils |
| BGA pad size(3)(4) | | 0.4 | | mm |

(1) A reference plane may be a ground plane or the power plane referencing the PCIe signals.
(2) In breakout area.
(3) Non-solder mask defined pad.
(4) Per IPC-7351A BGA pad size guideline.

#### 9.17.3.3.2 Routing Specifications

The PCIe data signal traces must be routed to achieve 100 Ω (±20%) differential impedance and 60 Ω (±15%) single-ended impedance. The single-ended impedance is required because differential signals are extremely difficult to closely couple on PCBs and, therefore, single-ended impedance becomes important. These requirements are the same as those recommended in the *PCIe Motherboard Checklist 1.0* document, available from PCI-SIG.

These impedances are impacted by trace width, trace spacing, distance between signals and referencing planes, and dielectric material. Verify with a PCB design tool that the trace geometry for both data signal pairs result in as close to 100 Ω differential impedance and 60 Ω single-ended impedance as possible. For best accuracy, work with your PCB fabricator to ensure this impedance is met.


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In general, closely coupled differential signal traces are not an advantage on PCBs. When differential signals are closely coupled, tight spacing and width control is necessary. Very small width and spacing variations affect impedance dramatically, so tight impedance control can be more problematic to maintain in production.

Loosely coupled PCB differential signals make impedance control much easier. Wider traces and spacing make obstacle avoidance easier, and trace width variations do not affect impedance as much; therefore, it is easier to maintain an accurate impedance over the length of the signal. The wider traces also show reduced skin effect and, therefore, often result in better signal integrity.

Table 9-98 shows the routing specifications for the PCIe data signals.

**Table 9-98. PCIe Routing Specifications**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| PCIe signal trace length | | | 10 (1) | Inches |
| Differential pair trace matching | | | 10 (2) | Mils |
| Number of stubs allowed on PCIe traces (3) | | | 0 | Stubs |
| TX/RX pair differential impedance | 80 | 100 | 120 | Ω |
| TX/RX single ended impedance | 51 | 60 | 69 | Ω |
| Pad size of vias on PCIe trace | | | 25 (4) | Mils |
| Hole size of vias on PCIe trace | | | 14 | Mils |
| Number of vias on each PCIe trace | | | 3 | Vias (5) |
| PCIe differential pair to any other trace spacing | 2*DS (6) | | | |

(1) Beyond this, signal integrity may suffer.
(2) For example, RXP0 within 10 Mils of RXN0.
(3) In-line pads may be used for probing.
(4) 35-Mil antipad max recommended.
(5) Vias must be used in pairs with their distance minimized.
(6) DS = differential spacing of the PCIe traces.

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## 9.18 Serial Peripheral Interface (SPI)

The SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (4 to 32 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communication between the device and external peripherals. Typical applications include an interface-to-external I/O or peripheral expansion via devices such as shift registers, display drivers, SPI EEPROMs, and Analog-to-Digital Converters (ADCs).

The SPI supports the following features:

- Master/Slave operation
- Four chip selects for interfacing/control to up to four SPI Slave devices and connection to a single external Master
- 32-bit shift register
- Buffered receive/transmit data register per channel (1 word deep), FIFO size is 64 bytes
- Programmable SPI configuration per channel (clock definition, enable polarity and word width)
- Supports one interrupt request and two DMA requests per channel.

For more detailed information on the SPI, see the *Multichannel Serial Port Interface (McSPI)* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

### 9.18.1 SPI Peripheral Register Descriptions

**Table 9-99. SPI Registers**

| HEX ADDRESS RANGE | | | | ACRONYM | REGISTER NAME |
|---|---|---|---|---|---|
| SPI0 | SPI1 | SPI2 | SPI3 | | |
| 0x4803 0000 | 0x481A 0000 | 0x481A 2000 | 0x481A 4000 | MCSPI_HL_REV | SPI REVISION |
| 0x4803 0004 | 0x481A 0004 | 0x481A 2004 | 0x481A 4004 | MCSPI_HL_HWINFO | SPI HARDWARE INFORMATION |
| 0x4803 0008 - 0x4803 000C | 0x481A 0008 - 0x481A 000C | 0x481A 2008 - 0x481A 200C | 0x481A 4008 - 0x481A 400C | - | RESERVED |
| 0x4803 0010 | 0x481A 0010 | 0x481A 2010 | 0x481A 4010 | MCSPI_HL_SYSCONFIG | SPI SYSTEM CONFIGURATION |
| 0x4803 0014 - 0x4803 00FF | 0x481A 0014 - 0x481A 00FF | 0x481A 2014 - 0x481A 20FF | 0x481A 4014 - 0x481A 40FF | - | RESERVED |
| 0x4803 0100 | 0x481A 0100 | 0x481A 2100 | 0x481A 4100 | MCSPI_REVISION | REVISION |
| 0x4803 0104 - 0x4803 010C | 0x481A 0104 - 0x481A 010C | 0x481A 2104 - 0x481A 210C | 0x481A 4104 - 0x481A 410C | - | RESERVED |
| 0x4803 0110 | 0x481A 0110 | 0x481A 2110 | 0x481A 4110 | MCSPI_SYSCONFIG | SYSTEM CONFIGURATION |
| 0x4803 0114 | 0x481A 0114 | 0x481A 2114 | 0x481A 4114 | MCSPI_SYSSTATUS | SYSTEM STATUS |
| 0x4803 0118 | 0x481A 0118 | 0x481A 2118 | 0x481A 4118 | MCSPI_IRQSTATUS | INTERRUPT STATUS |
| 0x4803 011C | 0x481A 011C | 0x481A 211C | 0x481A 411C | MCSPI_IRQENABLE | INTERRUPT ENABLE |
| 0x4803 0120 | 0x481A 0120 | 0x481A 2120 | 0x481A 4120 | MCSPI_WAKEUPENABLE | WAKEUP ENABLE |
| 0x4803 0124 | 0x481A 0124 | 0x481A 2124 | 0x481A 4124 | MCSPI_SYST | SYSTEM TEST |
| 0x4803 0128 | 0x481A 0128 | 0x481A 2128 | 0x481A 4128 | MCSPI_MODULCTRL | MODULE CONTROL |
| 0x4803 012C | 0x481A 012C | 0x481A 212C | 0x481A 412C | MCSPI_CH0CONF | CHANNEL 0 CONFIGURATION |
| 0x4803 0130 | 0x481A 0130 | 0x481A 2130 | 0x481A 4130 | MCSPI_CH0STAT | CHANNEL 0 STATUS |
| 0x4803 0134 | 0x481A 0134 | 0x481A 2134 | 0x481A 4134 | MCSPI_CH0CTRL | CHANNEL 0 CONTROL |
| 0x4803 0138 | 0x481A 0138 | 0x481A 2138 | 0x481A 4138 | MCSPI_TX0 | CHANNEL 0 TRANSMITTER |


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**Table 9-99. SPI Registers (continued)**

| HEX ADDRESS RANGE | | | | ACRONYM | REGISTER NAME |
|---|---|---|---|---|---|
| SPI0 | SPI1 | SPI2 | SPI3 | | |
| 0x4803 013C | 0x481A 013C | 0x481A 213C | 0x481A 413C | MCSPI_RX0 | CHANNEL 0 RECEIVER |
| 0x4803 0140 | 0x481A 0140 | 0x481A 2140 | 0x481A 4140 | MCSPI_CH1CONF | CHANNEL 1 CONFIGURATION |
| 0x4803 0144 | 0x481A 0144 | 0x481A 2144 | 0x481A 4144 | MCSPI_CH1STAT | CHANNEL 1 STATUS |
| 0x4803 0148 | 0x481A 0148 | 0x481A 2148 | 0x481A 4148 | MCSPI_CH1CTRL | CHANNEL 1 CONTROL |
| 0x4803 014C | 0x481A 014C | 0x481A 214C | 0x481A 414C | MCSPI_TX1 | CHANNEL 1 TRANSMITTER |
| 0x4803 0150 | 0x481A 0150 | 0x481A 2150 | 0x481A 4150 | MCSPI_RX1 | CHANNEL 1 RECEIVER |
| 0x4803 0154 | 0x481A 0154 | 0x481A 2154 | 0x481A 4154 | MCSPI_CH2CONF | CHANNEL 2 CONFIGURATION |
| 0x4803 0158 | 0x481A 0158 | 0x481A 2158 | 0x481A 4158 | MCSPI_CH2STAT | CHANNEL 2 STATUS |
| 0x4803 015C | 0x481A 015C | 0x481A 215C | 0x481A 415C | MCSPI_CH2CTRL | CHANNEL 2 CONTROL |
| 0x4803 0160 | 0x481A 0160 | 0x481A 2160 | 0x481A 4160 | MCSPI_TX2 | CHANNEL 2 TRANSMITTER |
| 0x4803 0164 | 0x481A 0164 | 0x481A 2164 | 0x481A 4164 | MCSPI_RX2 | CHANNEL 2 RECEIVER |
| 0x4803 0168 | 0x481A 0168 | 0x481A 2168 | 0x481A 4168 | MCSPI_CH3CONF | CHANNEL 3 CONFIGURATION |
| 0x4803 016C | 0x481A 016C | 0x481A 216C | 0x481A 416C | MCSPI_CH3STAT | CHANNEL 3 STATUS |
| 0x4803 0170 | 0x481A 0170 | 0x481A 2170 | 0x481A 4170 | MCSPI_CH3CTRL | CHANNEL 3 CONTROL |
| 0x4803 0174 | 0x481A 0174 | 0x481A 2174 | 0x481A 4174 | MCSPI_TX3 | CHANNEL 3 TRANSMITTER |
| 0x4803 0178 | 0x481A 0178 | 0x481A 2178 | 0x481A 4178 | MCSPI_RX3 | CHANNEL 3 RECEIVER |
| 0x4803 017C | 0x481A 017C | 0x481A 217C | 0x481A 417C | MCSPI_XFERLEVEL | TRANSFER LEVELS |
| 0x4803 0180 | 0x481A 0180 | 0x481A 2180 | 0x481A 4180 | MCSPI_DAFTX | DMA ADDRESS ALIGNED FIFO TRANSMITTER |
| 0x4803 0184 - 0x4803 019C | 0x481A 0184 - 0x481A 019C | 0x481A 2184 - 0x481A 219C | 0x481A 4184 - 0x481A 419C | - | RESERVED |
| 0x4803 01A0 | 0x481A 01A0 | 0x481A 21A0 | 0x481A 41A0 | MCSPI_DAFRX | DMA ADDRESS ALIGNED FIFO RECEIVER |
| 0x4803 01A4 - 0x4803 01FF | 0x481A 01A4 - 0x481A 01FF | 0x481A 21A4 - 0x481A 21FF | 0x481A 41A4 - 0x481A 41FF | - | RESERVED |

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### 9.18.2 SPI Electrical Data/Timing

**Table 9-100. Timing Requirements for SPI - Master Mode**

(see Figure 9-89 and Figure 9-90)

| NO. | | | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| **MASTER: SPI0, SPI1, SPI2 (M0) and SPI3 (M0)1 LOAD AT A MAXIMUM OF 5 pF** | | | | | | |
| 1 | $t_{c(SPICLK)}$ | Cycle time, SPI_CLK (1) (2) | | 20.8 (3) | | ns |
| 2 | $t_{w(SPICLKL)}$ | Pulse duration, SPI_CLK low (1) | | 0.5*P - 1 (4) | | ns |
| 3 | $t_{w(SPICLKH)}$ | Pulse duration, SPI_CLK high (1) | | 0.5*P - 1 (4) | | ns |
| 4 | $t_{su(MISO-SPICLK)}$ | Setup time, SPI_D[x] valid before SPI_CLK active edge (1) | SPI0, SPI1 | 2.29 | | ns |
| | | | SPI2, SPI3 | 4 | | |
| 5 | $t_{h(SPICLK-MISO)}$ | Hold time, SPI_D[x] valid after SPI_CLK active edge (1) | | 2.67 | | ns |
| 6 | $t_{d(SPICLK-MOSI)}$ | Delay time, SPI_CLK active edge to SPI_D[x] transition (1) | | -3.57 | 3.57 | ns |
| 7 | $t_{d(SCS-MOSI)}$ | Delay time, $\overline{\text{SPI_SCS[x]}}$ active edge to SPI_D[x] transition | | | 3.57 | ns |
| 8 | $t_{d(SCS-SPICLK)}$ | Delay time, $\overline{\text{SPI_SCS[x]}}$ active to SPI_CLK first edge (1) | MASTER_PHA0 (5) | B-4.2 (6) | | ns |
| | | | MASTER_PHA1 (5) | A-4.2 (7) | | ns |
| 9 | $t_{d(SPICLK-SCS)}$ | Delay time, SPI_CLK last edge to $\overline{\text{SPI_SCS[x]}}$ inactive (1) | MASTER_PHA0 (5) | A-4.2 (7) | | ns |
| | | | MASTER_PHA1 (5) | B-4.2 (6) | | ns |
| **MASTER: SPI0, SPI1, SPI2 (M0) and SPI3 (M0) LOAD AT MAX 25pF<br>MASTER: SPI2 (M1, M2, M3) and SPI3 (M1, M2, M3) 1 to 4 LOAD AT 5 to 25pF** | | | | | | |
| 1 | $t_{c(SPICLK)}$ | Cycle time, SPI_CLK (1) (2) | | 41.7 (8) | | ns |
| 2 | $t_{w(SPICLKL)}$ | Pulse duration, SPI_CLK low (1) | | 0.5*P - 2 (4) | | ns |
| 3 | $t_{w(SPICLKH)}$ | Pulse duration, SPI_CLK high (1) | | 0.5*P - 2 (4) | | ns |
| 4 | $t_{su(MISO-SPICLK)}$ | Setup time, SPI_D[x] valid before SPI_CLK active edge (1) | SPI0, SPI1 | 4 | | ns |
| | | | SPI2, SPI3 | 6 | | |
| 5 | $t_{h(SPICLK-MISO)}$ | Hold time, SPI_D[x] valid after SPI_CLK active edge (1) | | 3.8 | | ns |
| 6 | $t_{d(SPICLK-MOSI)}$ | Delay time, SPI_CLK active edge to SPI_D[x] transition (1) | | -5.5 | 5.5 | ns |
| 7 | $t_{d(SCS-MOSI)}$ | Delay time, $\overline{\text{SPI_SCS[x]}}$ active edge to SPI_D[x] transition | | | 5.5 | ns |
| 8 | $t_{d(SCS-SPICLK)}$ | Delay time, $\overline{\text{SPI_SCS[x]}}$ active to SPI_CLK first edge (1) | MASTER_PHA0 (5) | B-3.5 (6) | | ns |
| | | | MASTER_PHA1 (5) | A-3.5 (7) | | ns |
| 9 | $t_{d(SPICLK-SCS)}$ | Delay time, SPI_CLK last edge to $\overline{\text{SPI_SCS[x]}}$ inactive (1) | MASTER_PHA0 (5) | A-3.5 (7) | | ns |
| | | | MASTER_PHA1 (5) | B-3.5 (6) | | ns |

(1) This timing applies to all configurations regardless of SPI_CLK polarity and which clock edges are used to drive output data and capture input data.
(2) Related to the SPI_CLK maximum frequency.
(3) Maximum frequency = 48 MHz
(4) P = SPICLK period.
(5) SPI_CLK phase is programmable with the PHA bit of the SPI_CH(i)CONF register.
(6) B = (TCS + 0.5) * TSPICLKREF * $F_{ratio}$, where TCS is a bit field of the SPI_CH(i)CONF register and $F_{ratio}$ = Even ≥2.
(7) When P = 20.8 ns, A = (TCS + 1) * TSPICLKREF, where TCS is a bit field of the SPI_CH(i)CONF register. When P > 20.8 ns, A = (TCS + 0.5) * $F_{ratio}$ * TSPICLKREF, where TCS is a bit field of the SPI_CH(i)CONF register.
(8) Maximum frequency = 24 MHz


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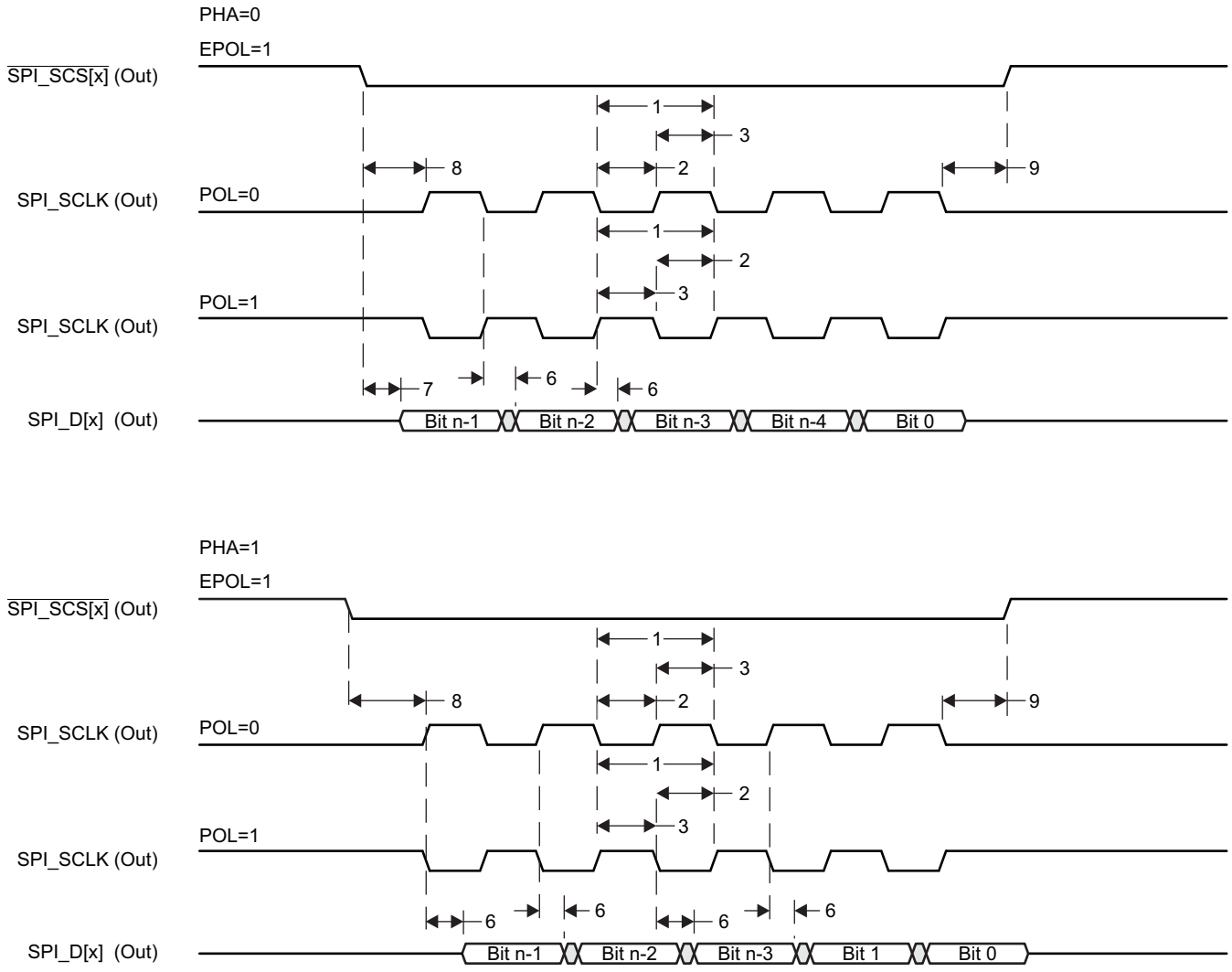


**Figure 9-89. SPI Master Mode Transmit Timing**

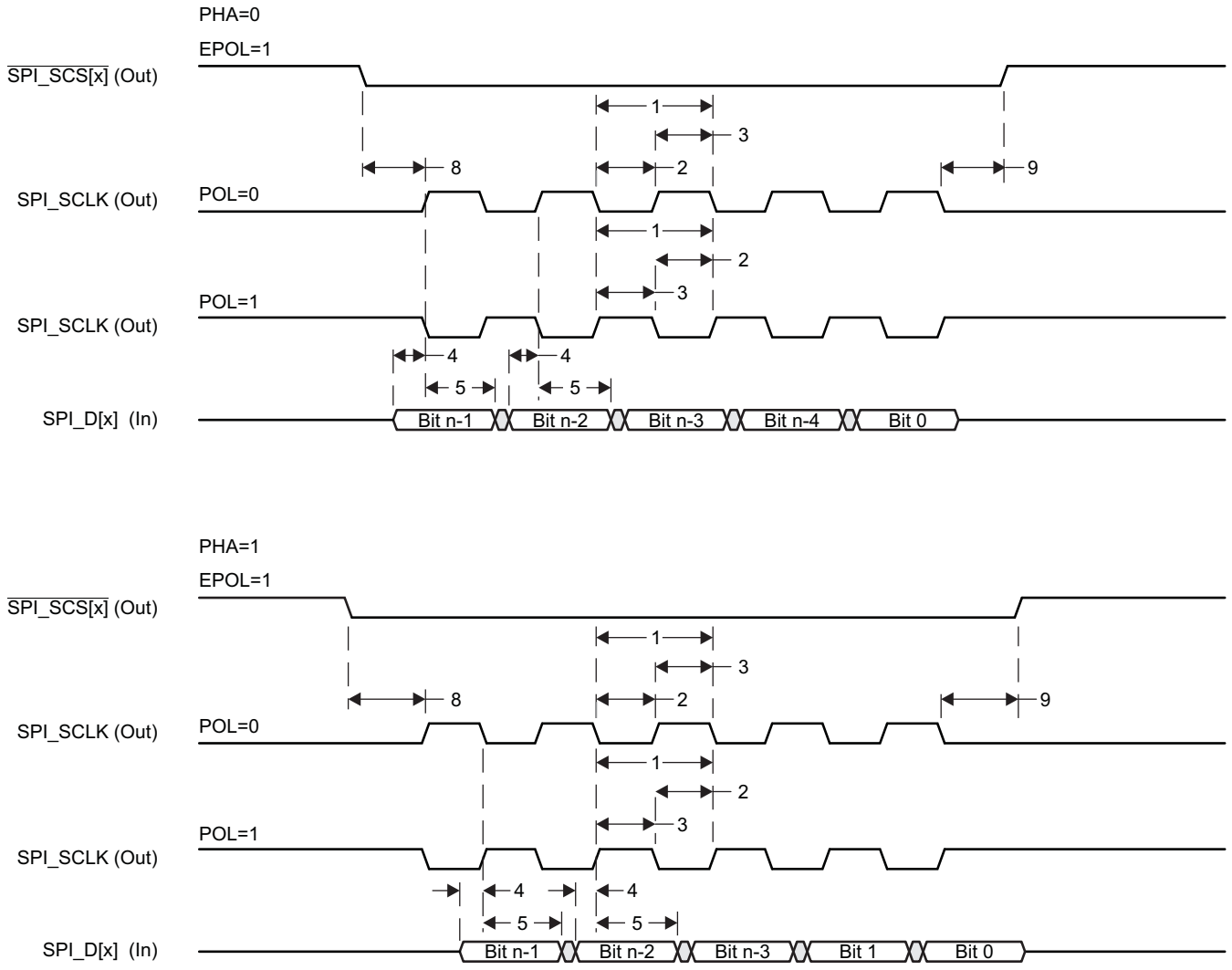


**Figure 9-90. SPI Master Mode Receive Timing**

**Table 9-101. Timing Requirements for SPI - Slave Mode**

(see Figure 9-91 and Figure 9-92)

| NO. | | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{c(SPICLK)}$ | Cycle time, SPI_CLK (1) (2) | 62.5 (3) | | ns |
| 2 | $t_{w(SPICLKL)}$ | Pulse duration, SPI_CLK low (1) | 0.5*P - 3 (4) | | ns |
| 3 | $t_{w(SPICLKH)}$ | Pulse duration, SPI_CLK high (1) | 0.5*P - 3 (4) | | ns |
| 4 | $t_{su(MOSI-SPICLK)}$ | Setup time, SPI_D[x] valid before SPI_CLK active edge (1) | 12.92 | | ns |
| 5 | $t_{h(SPICLK-MOSI)}$ | Hold time, SPI_D[x] valid after SPI_CLK active edge (1) | 12.92 | | ns |
| 6 | $t_{d(SPICLK-MISO)}$ | Delay time, SPI_CLK active edge to SPI_D[x] transition (1) | -4.00 | 17.1 | ns |
| 7 | $t_{d(SCS-MISO)}$ | Delay time, $\overline{\text{SPI_SCS[x]}}$ active edge to SPI_D[x] transition (5) | | 17.1 | ns |
| 8 | $t_{su(SCS-SPICLK)}$ | Setup time, $\overline{\text{SPI_SCS[x]}}$ valid before SPI_CLK first edge (1) | 12.92 | | ns |

(1) This timing applies to all configurations regardless of SPI_CLK polarity and which clock edges are used to drive output data and capture input data.
(2) Related to the input maximum frequency supported by the SPI module.
(3) Maximum frequency = 16 MHz
(4) P = SPICLK period.
(5) PHA = 0; SPI_CLK phase is programmable with the PHA bit of the SPI_CH(i)CONF register.


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**Table 9-101. Timing Requirements for SPI - Slave Mode (continued)**

(see Figure 9-91 and Figure 9-92)

| NO. | | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 9 | $t_{h(SPICLK-SCS)}$ | Hold time, $\overline{SPI_SCS[x]}$ valid after SPI_CLK last edge (1) | 12.92 | | ns |

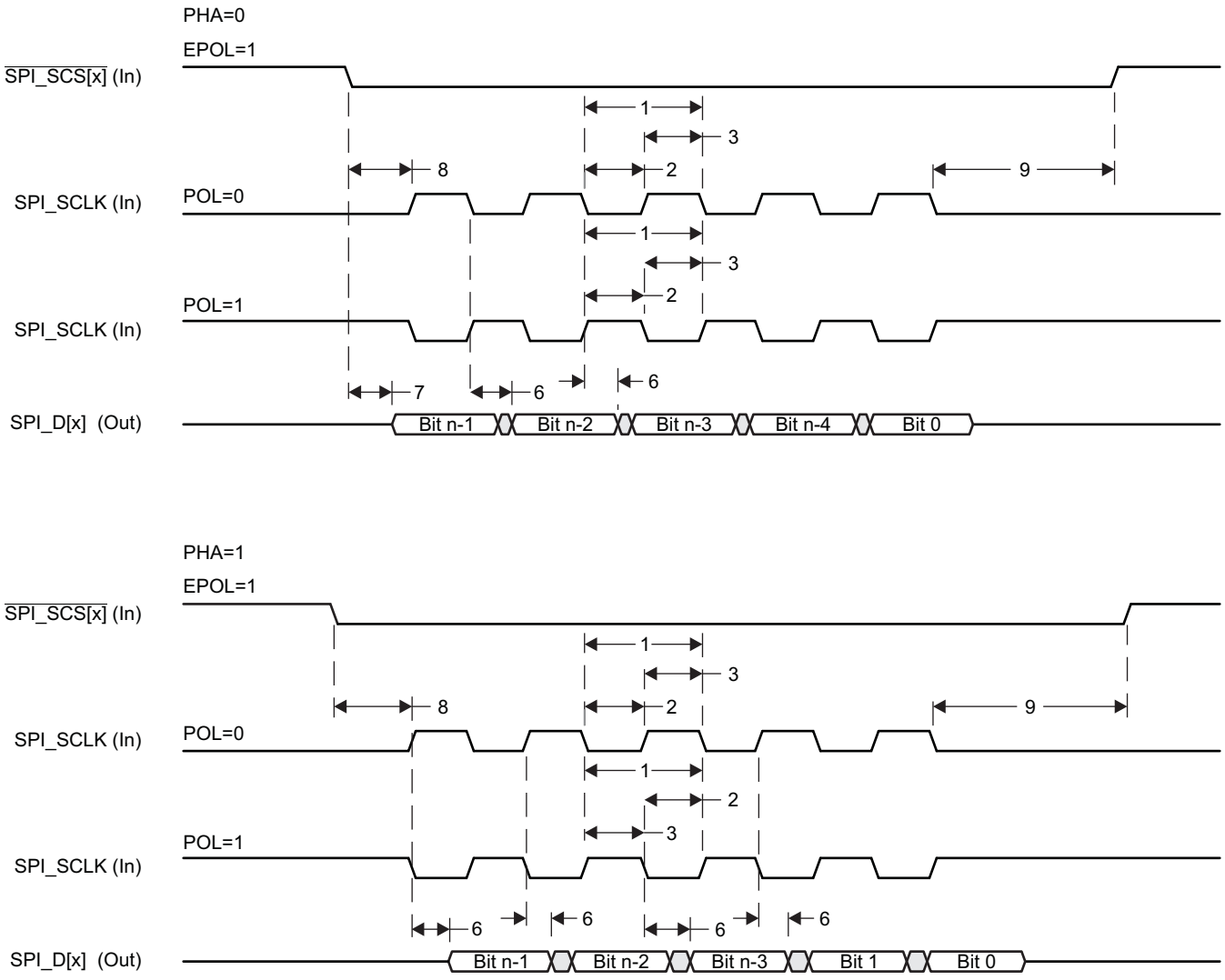


**Figure 9-91. SPI Slave Mode Transmit Timing**

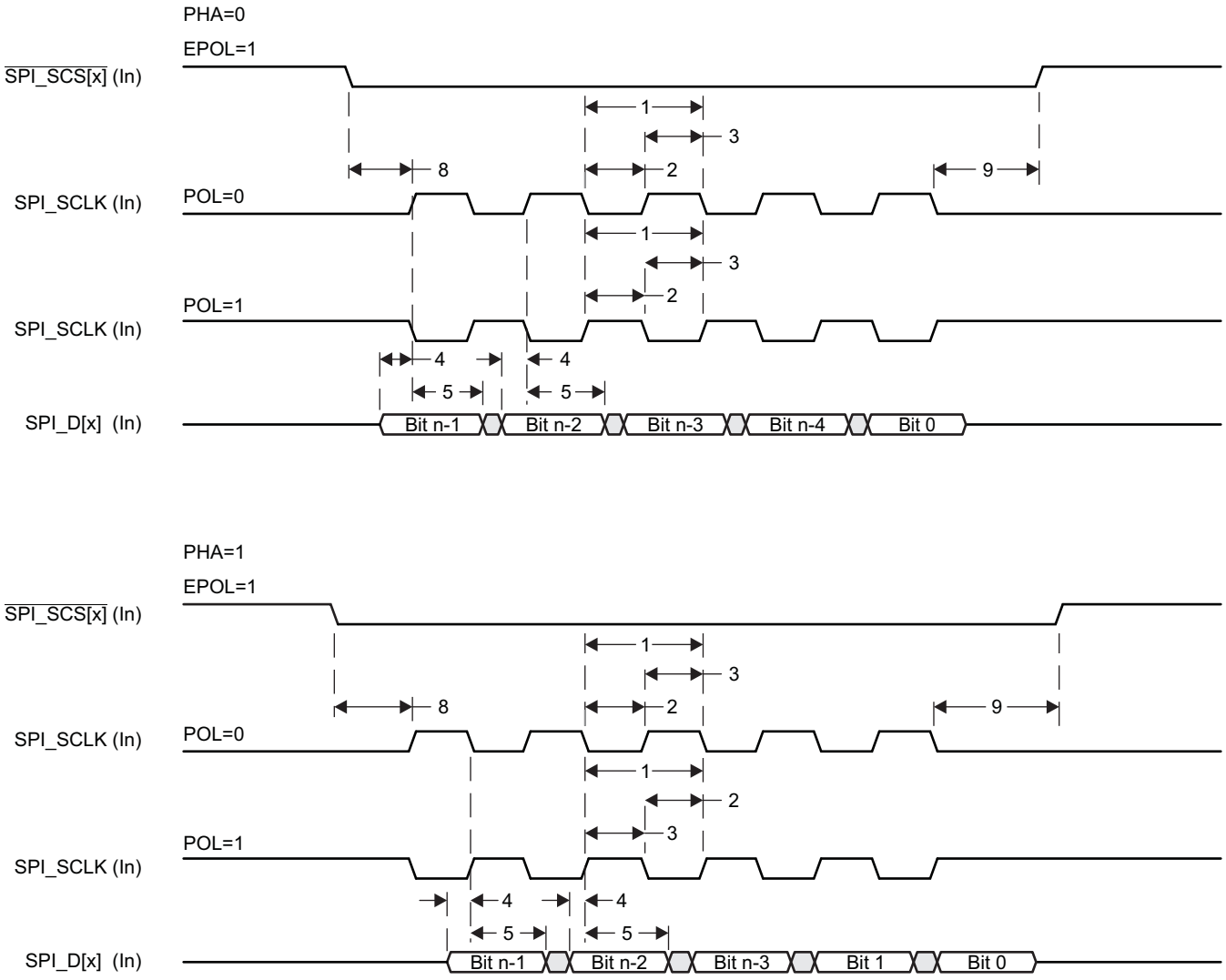


**Figure 9-92. SPI Slave Mode Receive Timing**


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## 9.19 Timers

The device has eight 32-bit general-purpose (GP) timers (TIMER8 - TIMER1) that have the following features:

- TIMER8, TIMER1 are for software use and do not have an external connection
- Dedicated input trigger for capture mode and dedicated output trigger/pulse width modulation (PWM) signal
- Interrupts generated on overflow, compare, and capture
- Free-running 32-bit upward counter
- Supported modes:
  - Compare and capture modes
  - Auto-reload mode
  - Start-stop mode
- TIMER[8:1] functional clock is sourced from either the DEVOSC, AUXOSC, AUD_CLK2/1/0, TCLKIN, or SYSCLK18 27 MHz as selected by the timer clock multiplexers.
- On-the-fly read/write register (while counting)
- Generates interrupts to the ARM and Media Controller.

The device has one system watchdog timer that have the following features:

- Free-running 32-bit upward counter
- On-the-fly read/write register (while counting)
- Reset upon occurrence of a timer overflow condition
- The system watchdog timer has two possible clock sources:
  - RCOSC32K oscillator
  - RTCDIVIDER
- The watchdog timer is used to provide a recovery mechanism for the device in the event of a fault condition, such as a non-exiting code loop.

For more detailed information on the GP and Watchdog Timers, see the *Timers* and *Watchdog Timer* chapters of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

### *9.19.1 Timer Peripheral Register Descriptions*

### 9.19.2 Timer Electrical/Data Timing

**Table 9-102. Timing Requirements for Timer**

(see Figure 9-93)

| NO. | | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{w(EVTIH)}$ | Pulse duration, high | 4P(1) | | ns |
| 2 | $t_{w(EVTIL)}$ | Pulse duration, low | 4P(1) | | ns |

(1) P = module clock.

**Table 9-103. Switching Characteristics Over Recommended Operating Conditions for Timer**

(see Figure 9-93)

| NO. | PARAMETER | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 3 | $t_{w(EVTOH)}$ | Pulse duration, high | 4P-3(1) | | ns |
| 4 | $t_{w(EVTOL)}$ | Pulse duration, low | 4P-3(1) | | ns |

(1) P = module clock.

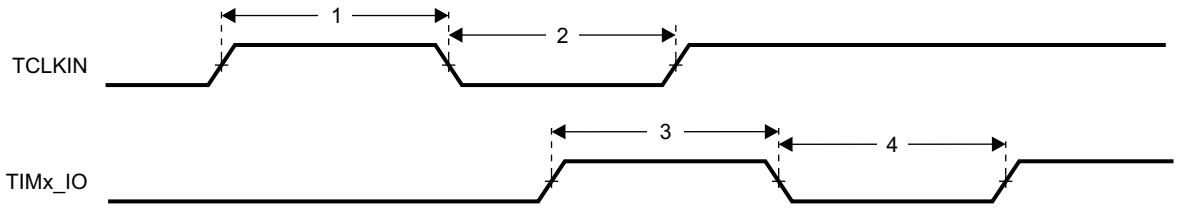


**Figure 9-93. Timer Timing**


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## 9.20 Universal Asynchronous Receiver/Transmitter (UART)

The UART performs serial-to-parallel conversions on data received from a peripheral device and parallel-to-serial conversion on data received from the CPU. The device provides up to six UART peripheral interfaces, depending on the selected pin multiplexing.

Each UART has the following features:

- Selectable UART/IrDA (SIR/MIR)/CIR modes
- Dual 64-entry FIFOs for received and transmitted data payload
- Programmable and selectable transmit and receive FIFO trigger levels for DMA and interrupt generation
- Baud-rate generation based upon programmable divisors N (N=1…16384)
- Two DMA requests and one interrupt request to the system
- Can connect to any RS-232 compliant device.

UART functions include:

- Baud-rate up to 3.6 Mbit/s on UART0, UART1, and UART2
- Baud-rate up to 12 Mbit/s on UART3, UART4, and UART5
- Programmable serial interfaces characteristics
  - 5, 6, 7, or 8-bit characters
  - Even, odd, or no parity-bit generation and detection
  - 1, 1.5, or 2 stop-bit generation
  - Flow control: hardware (RTS/CTS) or software (XON/XOFF)
- Additional modem control functions (UART0_DTR, UART0_DSR, UART0_DCD, and UART0_RIN) for UART0 only; UART1, UART2, UART3, UART4, and UART5 do not support full-flow control signaling.

IR-IrDA functions include:

- Support of IrDA 1.4 slow infrared (SIR, baud-rate up to 115.2 Kbits/s), medium infrared (MIR, baud-rate up to 1.152 Mbits/s) and fast infrared (FIR baud-rate up to 4.0 Mbits/s) communications
- Supports framing error, cyclic redundancy check (CRC) error, illegal symbol (FIR), and abort pattern (SIR, MIR) detection
- 8-entry status FIFO (with selectable trigger levels) available to monitor frame length and frame errors.

IR-CIR functions include:

- Consumer infrared (CIR) remote control mode with programmable data encoding
- Free data format (supports any remote control private standards)
- Selectable bit rate and configurable carrier frequency.

For more detailed information on the UART peripheral, see the *UART/IrDA/CIR Module* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

### *9.20.1 UART Peripheral Register Descriptions*

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### 9.20.2 UART Electrical/Data Timing

**Table 9-104. Timing Requirements for UART**

(see Figure 9-94)

| NO. | | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 4 | $t_{w(RX)}$ | Pulse width, receive data bit, 15/30/100pF high or low | 0.96U(1) | 1.05U(1) | ns |
| 5 | $t_{w(CTS)}$ | Pulse width, receive start bit, 15/30/100pF high or low | 0.96U(1) | 1.05U(1) | ns |
| | $t_{d(RTS-TX)}$ | Delay time, transmit start bit to transmit data | P(2) | | ns |
| | $t_{d(CTS-TX)}$ | Delay time, receive start bit to transmit data | P(2) | | ns |

(1) U = UART baud time = 1/programmed baud rate
(2) P = Clock period of the reference clock (FCLK, usually 48 MHz).

**Table 9-105. Switching Characteristics Over Recommended Operating Conditions for UART**

(see Figure 9-94)

| NO. | PARAMETER | | | OPP100/120/166 | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| | $f_{(baud)}$ | Maximum programmable baud rate | 15 pF (UART0/1/2) | | 5 | MHz |
| | | | 15 pF (UART3/4/5) | | 12 | |
| | | | 30 pF | | 0.23 | |
| | | | 100 pF | | 0.115 | |
| 2 | $t_{w(TX)}$ | Pulse width, transmit data bit, 15/30/100 pF high or low | | U - 2(1) | U + 2(1) | ns |
| 3 | $t_{w(RTS)}$ | Pulse width, transmit start bit, 15/30/100 pF high or low | | U - 2(1) | U + 2(1) | ns |

(1) U = UART baud time = 1/programmed baud rate

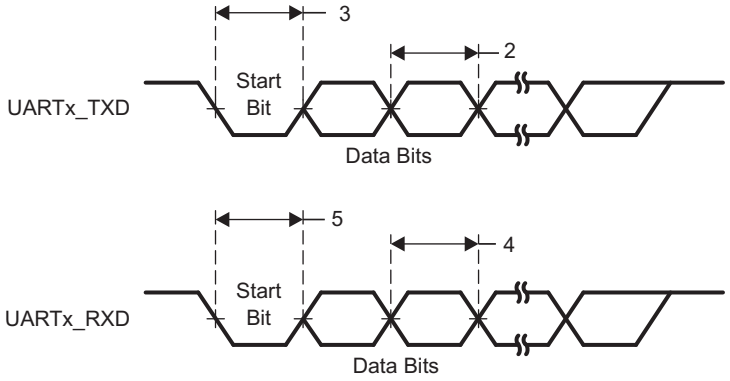


**Figure 9-94. UART Timing**


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## 9.21 Universal Serial Bus (USB2.0)

The device includes two USB2.0 modules which support the *Universal Serial Bus Specification Revision 2.0.* The following are some of the major USB features that are supported:

- USB 2.0 peripheral at high speed (HS: 480 Mbps) and full speed (FS: 12 Mbps)
- USB 2.0 host at HS, FS, and low speed (LS: 1.5 Mbps)
- Each endpoint (other than endpoint 0, control only) can support all transfer modes (control, bulk, interrupt, and isochronous)
- Supports high-bandwidth ISO mode
- Supports 16 Transmit (TX) and 16 Receive (RX) endpoints including endpoint 0
- FIFO RAM
  - 32K endpoint
  - Programmable size
- Includes two integrated PHYs
- RNDIS-like mode for terminating RNDIS-type protocols without using short-packet termination for support of MSC applications.
- USB OTG extensions — session request protocol (SRP) and host negotiation protocol (HNP)

The USB2.0 peripherals do not support the following features:

- On-chip charge pump (VBUS Power must be generated external to the device.)
- RNDIS mode acceleration for USB sizes that are not multiples of 64 bytes
- Endpoint max USB packet sizes that do not conform to the USB 2.0 spec (for FS/LS: 8, 16, 32, 64, – and 1023 are defined; for HS: 64, 128, 512, and 1024 are defined

For more detailed information on the USB2.0 peripheral, see the *Universal Serial Bus (USB)* chapter of the *TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual* (Literature Number: SPRUGZ8).

### 9.21.1 USB2.0 Peripheral Register Descriptions

**Table 9-106. USB2.0 Submodules**

| SUBMODULE ADDRESS OFFSET | SUBMODULE NAME |
|---|---|
| 0x0000 | USBSS registers |
| 0x1000 | USB0 controller registers |
| 0x1800 | USB1 controller registers |
| 0x2000 | CPPI DMA controller registers |
| 0x3000 | CPPI DMA scheduler registers |
| 0x4000 | CPPI DMA Queue Manager registers |

**Table 9-107. USB Subsystem (USBSS) Registers (1)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4740 0000 | REVREG | USBSS REVISION |
| 0x4740 0004 - 0x4740 000C | - | Reserved |
| 0x4740 0010 | SYSCONFIG | USBSS SYSCONFIG |
| 0x4740 0014 - 0x4740 001C | - | Reserved |
| 0x4740 0020 | EOI | USBSS IRQ_EOI |
| 0x4740 0024 | IRQSTATRAW | USBSS IRQ_STATUS_RAW |
| 0x4740 0028 | IRQSTAT | USBSS IRQ_STATUS |

(1) USBSS registers contain the registers that are used to control at the global level and apply to all sub-modules.

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**Table 9-107. USB Subsystem (USBSS) Registers[(1)] (continued)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4740 002C | IRQENABLER | USBSS IRQ_ENABLE_SET |
| 0x4740 0030 | IRQCLEARR | USBSS IRQ_ENABLE_CLR |
| 0x4740 0034 - 0x4740 00FC | - | Reserved |
| 0x4740 0100 | IRQDMATHOLDTX00 | USBSS IRQ_DMA_THRESHOLD_TX0_0 |
| 0x4740 0104 | IRQDMATHOLDTX01 | USBSS IRQ_DMA_THRESHOLD_TX0_1 |
| 0x4740 0108 | IRQDMATHOLDTX02 | USBSS IRQ_DMA_THRESHOLD_TX0_2 |
| 0x4740 010C | IRQDMATHOLDTX03 | USBSS IRQ_DMA_THRESHOLD_TX0_3 |
| 0x4740 0110 | IRQDMATHOLDRX00 | USBSS IRQ_DMA_THRESHOLD_RX0_0 |
| 0x4740 0114 | IRQDMATHOLDRX01 | USBSS IRQ_DMA_THRESHOLD_RX0_1 |
| 0x4740 0118 | IRQDMATHOLDRX02 | USBSS IRQ_DMA_THRESHOLD_RX0_2 |
| 0x4740 011C | IRQDMATHOLDRX03 | USBSS IRQ_DMA_THRESHOLD_RX0_3 |
| 0x4740 0120 | IRQDMATHOLDTX10 | USBSS IRQ_DMA_THRESHOLD_TX1_0 |
| 0x4740 0124 | IRQDMATHOLDTX11 | USBSS IRQ_DMA_THRESHOLD_TX1_1 |
| 0x4740 0128 | IRQDMATHOLDTX12 | USBSS IRQ_DMA_THRESHOLD_TX1_2 |
| 0x4740 012C | IRQDMATHOLDTX13 | USBSS IRQ_DMA_THRESHOLD_TX1_3 |
| 0x4740 0130 | IRQDMATHOLDRX10 | USBSS IRQ_DMA_THRESHOLD_RX1_0 |
| 0x4740 0134 | IRQDMATHOLDRX11 | USBSS IRQ_DMA_THRESHOLD_RX1_1 |
| 0x4740 0138 | IRQDMATHOLDRX12 | USBSS IRQ_DMA_THRESHOLD_RX1_2 |
| 0x4740 013C | IRQDMATHOLDRX13 | USBSS IRQ_DMA_THRESHOLD_RX1_3 |
| 0x4740 0140 | IRQDMAENABLE0 | USBSS IRQ_DMA_ENABLE_0 |
| 0x4740 0144 | IRQDMAENABLE1 | USBSS IRQ_DMA_ENABLE_1 |
| 0x4740 0148 - 0x4740 01FC | - | Reserved |
| 0x4740 0200 | IRQFRAMETHOLDTX00 | USBSS IRQ_FRAME_THRESHOLD_TX0_0 |
| 0x4740 0204 | IRQFRAMETHOLDTX01 | USBSS IRQ_FRAME_THRESHOLD_TX0_1 |
| 0x4740 0208 | IRQFRAMETHOLDTX02 | USBSS IRQ_FRAME_THRESHOLD_TX0_2 |
| 0x4740 020C | IRQFRAMETHOLDTX03 | USBSS IRQ_FRAME_THRESHOLD_TX0_3 |
| 0x4740 0210 | IRQFRAMETHOLDRX00 | USBSS IRQ_FRAME_THRESHOLD_RX0_0 |
| 0x4740 0214 | IRQFRAMETHOLDRX01 | USBSS IRQ_FRAME_THRESHOLD_RX0_1 |
| 0x4740 0218 | IRQFRAMETHOLDRX02 | USBSS IRQ_FRAME_THRESHOLD_RX0_2 |
| 0x4740 021C | IRQFRAMETHOLDRX03 | USBSS IRQ_FRAME_THRESHOLD_RX0_3 |
| 0x4740 0220 | IRQFRAMETHOLDTX10 | USBSS IRQ_FRAME_THRESHOLD_TX1_0 |
| 0x4740 0224 | IRQFRAMETHOLDTX11 | USBSS IRQ_FRAME_THRESHOLD_TX1_1 |
| 0x4740 0228 | IRQFRAMETHOLDTX12 | USBSS IRQ_FRAME_THRESHOLD_TX1_2 |
| 0x4740 022C | IRQFRAMETHOLDTX13 | USBSS IRQ_FRAME_THRESHOLD_TX1_3 |
| 0x4740 0230 | IRQFRAMETHOLDRX10 | USBSS IRQ_FRAME_THRESHOLD_RX1_0 |
| 0x4740 0234 | IRQFRAMETHOLDRX11 | USBSS IRQ_FRAME_THRESHOLD_RX1_1 |
| 0x4740 0238 | IRQFRAMETHOLDRX12 | USBSS IRQ_FRAME_THRESHOLD_RX1_2 |
| 0x4740 023C | IRQFRAMETHOLDRX13 | USBSS IRQ_FRAME_THRESHOLD_RX1_3 |
| 0x4740 0240 | IRQFRAMEENABLE0 | USBSS IRQ_FRAME_ENABLE_0 |
| 0x4740 0244 | IRQFRAMEENABLE1 | USBSS IRQ_FRAME_ENABLE_1 |
| 0x4740 0248 - 0x4740 0FFC | - | Reserved |


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**Table 9-108. USB0 Controller Registers**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4740 1000 | USB0REV | USB0 REVISION |
| 0x4740 1004 - 0x4740 1010 | - | Reserved |
| 0x4740 1014 | USB0CTRL | USB0 Control |
| 0x4740 1018 | USB0STAT | USB0 Status |
| 0x4740 101C | - | Reserved |
| 0x4740 1020 | USB0IRQMSTAT | USB0 IRQ_MERGED_STATUS |
| 0x4740 1024 | USB0IRQEOI | USB0 IRQ_EOI |
| 0x4740 1028 | USB0IRQSTATRAW0 | USB0 IRQ_STATUS_RAW_0 |
| 0x4740 102C | USB0IRQSTATRAW1 | USB0 IRQ_STATUS_RAW_1 |
| 0x4740 1030 | USB0IRQSTAT0 | USB0 IRQ_STATUS_0 |
| 0x4740 1034 | USB0IRQSTAT1 | USB0 IRQ_STATUS_1 |
| 0x4740 1038 | USB0IRQENABLESET0 | USB0 IRQ_ENABLE_SET_0 |
| 0x4740 103C | USB0IRQENABLESET1 | USB0 IRQ_ENABLE_SET_1 |
| 0x4740 1040 | USB0IRQENABLECLR0 | USB0 IRQ_ENABLE_CLR_0 |
| 0x4740 1044 | USB0IRQENABLECLR1 | USB0 IRQ_ENABLE_CLR_1 |
| 0x4740 1048 - 0x4740 106C | - | Reserved |
| 0x4740 1070 | USB0TXMODE | USB0 Tx Mode |
| 0x4740 1074 | USB0RXMODE | USB0 Rx Mode |
| 0x4740 1078 - 0x4740 107C | - | Reserved |
| 0x4740 1080 | USB0GENRNDISEP1 | USB0 Generic RNDIS Size EP1 |
| 0x4740 1084 | USB0GENRNDISEP2 | USB0 Generic RNDIS Size EP2 |
| 0x4740 1088 | USB0GENRNDISEP3 | USB0 Generic RNDIS Size EP3 |
| 0x4740 108C | USB0GENRNDISEP4 | USB0 Generic RNDIS Size EP4 |
| 0x4740 1090 | USB0GENRNDISEP5 | USB0 Generic RNDIS Size EP5 |
| 0x4740 1094 | USB0GENRNDISEP6 | USB0 Generic RNDIS Size EP6 |
| 0x4740 1098 | USB0GENRNDISEP7 | USB0 Generic RNDIS Size EP7 |
| 0x4740 109C | USB0GENRNDISEP8 | USB0 Generic RNDIS Size EP8 |
| 0x4740 10A0 | USB0GENRNDISEP9 | USB0 Generic RNDIS Size EP9 |
| 0x4740 10A4 | USB0GENRNDISEP10 | USB0 Generic RNDIS Size EP10 |
| 0x4740 10A8 | USB0GENRNDISEP11 | USB0 Generic RNDIS Size EP11 |
| 0x4740 10AC | USB0GENRNDISEP12 | USB0 Generic RNDIS Size EP12 |
| 0x4740 10B0 | USB0GENRNDISEP13 | USB0 Generic RNDIS Size EP13 |
| 0x4740 10B4 | USB0GENRNDISEP14 | USB0 Generic RNDIS Size EP14 |
| 0x4740 10B8 | USB0GENRNDISEP15 | USB0 Generic RNDIS Size EP15 |
| 0x4740 10BC - 0x4740 10CC | - | Reserved |
| 0x4740 10D0 | USB0AUTOREQ | USB0 Auto Req |
| 0x4740 10D4 | USB0SRPFIXTIME | USB0 SRP Fix Time |
| 0x4740 10D8 | USB0TDOWN | USB0 Teardown |
| 0x4740 10DC | - | Reserved |
| 0x4740 10E0 | USB0UTMI | USB0 PHY UTMI |
| 0x4740 10E4 | USB0UTMILB | USB0 MGC UTMI Loopback |
| 0x4740 10E8 | USB0MODE | USB0 Mode |
| 0x4740 10E8 - 0x4740 13FF | - | Reserved |
| 0x4740 1400 - 0x4740 1468 | - | USB0 Mentor Core Registers/FIFOs |
| 0x4740 146C | USB0_HWVERS | USB0 Mentor Core Hardware Version Register |
| 0x4740 1470 - 0x4740 159C | - | USB0 Mentor Core Registers/FIFOs |
| 0x4740 15A0 - 0x4740 17FC | - | Reserved |

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**Table 9-109. USB1 Controller Registers**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4740 1800 | USB1REV | USB1 Revision |
| 0x4740 1804 - 0x4740 1810 | - | Reserved |
| 0x4740 1814 | USB1CTRL | USB1 Control |
| 0x4740 1818 | USB1STAT | USB1 Status |
| 0x4740 181C | - | Reserved |
| 0x4740 1820 | USB1IRQMSTAT | USB1 IRQ_MERGED_STATUS |
| 0x4740 1824 | USB1IRQEOI | USB1 IRQ_EOI |
| 0x4740 1828 | USB1IRQSTATRAW0 | USB1 IRQ_STATUS_RAW_0 |
| 0x4740 182C | USB1IRQSTATRAW1 | USB1 IRQ_STATUS_RAW_1 |
| 0x4740 1830 | USB1IRQSTAT0 | USB1 IRQ_STATUS_0 |
| 0x4740 1834 | USB1IRQSTAT1 | USB1 IRQ_STATUS_1 |
| 0x4740 1838 | USB1IRQENABLESET0 | USB1 IRQ_ENABLE_SET_0 |
| 0x4740 183C | USB1IRQENABLESET1 | USB1 IRQ_ENABLE_SET_1 |
| 0x4740 1840 | USB1IRQENABLECLR0 | USB1 IRQ_ENABLE_CLR_0 |
| 0x4740 1844 | USB1IRQENABLECLR1 | USB1 IRQ_ENABLE_CLR_1 |
| 0x4740 1848 - 0x4740 186C | - | Reserved |
| 0x4740 1870 | USB1TXMODE | USB1 Tx Mode |
| 0x4740 1874 | USB1RXMODE | USB1 Rx Mode |
| 0x4740 1878 - 0x4740 187C | - | Reserved |
| 0x4740 1880 | USB1GENRNDISEP1 | USB1 Generic RNDIS Size EP1 |
| 0x4740 1884 | USB1GENRNDISEP2 | USB1 Generic RNDIS Size EP2 |
| 0x4740 1888 | USB1GENRNDISEP3 | USB1 Generic RNDIS Size EP3 |
| 0x4740 188C | USB1GENRNDISEP4 | USB1 Generic RNDIS Size EP4 |
| 0x4740 1890 | USB1GENRNDISEP5 | USB1 Generic RNDIS Size EP5 |
| 0x4740 1894 | USB1GENRNDISEP6 | USB1 Generic RNDIS Size EP6 |
| 0x4740 1898 | USB1GENRNDISEP7 | USB1 Generic RNDIS Size EP7 |
| 0x4740 189C | USB1GENRNDISEP8 | USB1 Generic RNDIS Size EP8 |
| 0x4740 18A0 | USB1GENRNDISEP9 | USB1 Generic RNDIS Size EP9 |
| 0x4740 18A4 | USB1GENRNDISEP10 | USB1 Generic RNDIS Size EP10 |
| 0x4740 18A8 | USB1GENRNDISEP11 | USB1 Generic RNDIS Size EP11 |
| 0x4740 18AC | USB1GENRNDISEP12 | USB1 Generic RNDIS Size EP12 |
| 0x4740 18B0 | USB1GENRNDISEP13 | USB1 Generic RNDIS Size EP13 |
| 0x4740 18B4 | USB1GENRNDISEP14 | USB1 Generic RNDIS Size EP14 |
| 0x4740 18B8 | USB1GENRNDISEP15 | USB1 Generic RNDIS Size EP15 |
| 0x4740 18BC - 0x4740 18CC | - | Reserved |
| 0x4740 18D0 | USB1AUTOREQ | USB1 Auto Req |
| 0x4740 18D4 | USB1SRPFIXTIME | USB1 SRP Fix Time |
| 0x4740 18D8 | USB1TDOWN | USB1 Teardown |
| 0x4740 18DC | - | Reserved |
| 0x4740 18E0 | USB1UTMI | USB1 PHY UTMI |
| 0x4740 18E4 | USB1UTMILB | USB1 MGC UTMI Loopback |
| 0x4740 18E8 | USB1MODE | USB1 Mode |
| 0x4740 18E8 - 0x4740 1BFF | - | Reserved |
| 0x4740 1C00 - 0x4740 1C68 | - | USB1 Mentor Core Registers |
| 0x4740 1C6C | USB1HWVERS | USB1 Mentor Core Hardware Version Register |
| 0x4740 1C70 - 0x4740 1D9C | - | USB1 Mentor Core Registers |
| 0x4740 1DA0 - 0x4740 1FFC | - | Reserved |


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**Table 9-110. CPPI DMA Controller Registers**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4740 2000 | DMAREVID | Revision Register |
| 0x4740 2004 | TDFDQ | Teardown Free Descriptor Queue Control |
| 0x4740 2008 | DMAEMU | Emulation Control Register |
| 0x4740 200C | - | Reserved |
| 0x4740 2010 | DMAMEM1BA | CPPI Mem1 Base Address Register |
| 0x4740 2014 | DMAMEM1MASK | CPPI Mem1 Mask Address Register |
| 0x4740 200C - 0x4740 27FF | - | Reserved |
| 0x4740 2800 | TXGCR0 | Tx Channel 0 Global Configuration Register |
| 0x4740 2804 | - | Reserved |
| 0x4740 2808 | RXGCR0 | Rx Channel 0 Global Configuration Register |
| 0x4740 280C | RXHPCRA0 | Rx Channel 0 Host Packet Configuration Register A |
| 0x4740 2810 | RXHPCRB0 | Rx Channel 0 Host Packet Configuration Register B |
| 0x4740 2814 - 0x4740 281C | - | Reserved |
| 0x4740 2820 | TXGCR1 | Tx Channel 1 Global Configuration Register |
| 0x4740 2824 | - | Reserved |
| 0x4740 2828 | RXGCR1 | Rx Channel 1 Global Configuration Register |
| 0x4740 282C | RXHPCRA1 | Rx Channel 1 Host Packet Configuration Register A |
| 0x4740 2830 | RXHPCRB1 | Rx Channel 1 Host Packet Configuration Register B |
| 0x4740 2834 - 0x4740 283C | - | Reserved |
| 0x4740 2840 | TXGCR2 | Tx Channel 2 Global Configuration Register |
| 0x4740 2844 | - | Reserved |
| 0x4740 2848 | RXGCR2 | Rx Channel 2 Global Configuration Register |
| 0x4740 284C | RXHPCRA2 | Rx Channel 2 Host Packet Configuration Register A |
| 0x4740 2850 | RXHPCRB2 | Rx Channel 2 Host Packet Configuration Register B |
| 0x4740 2854 - 0x4740 285F | - | Reserved |
| 0x4740 2860 | TXGCR3 | Tx Channel 3 Global Configuration Register |
| 0x4740 2864 | - | Reserved |
| 0x4740 2868 | RXGCR3 | Rx Channel 3 Global Configuration Register |
| 0x4740 286C | RXHPCRA3 | Rx Channel 3 Host Packet Configuration Register A |
| 0x4740 2870 | RXHPCRB3 | Rx Channel 3 Host Packet Configuration Register B |
| 0x4740 2880 - 0x4740 2B9F | - | ... |
| 0x4740 2BA0 | TXGCR29 | Tx Channel 29 Global Configuration Register |
| 0x4740 2BA4 | - | Reserved |
| 0x4740 2BA8 | RXGCR29 | Rx Channel 29 Global Configuration Register |
| 0x4740 2BAC | RXHPCRA29 | Rx Channel 29 Host Packet Configuration Register A |
| 0x4740 2BB0 | RXHPCRB29 | Rx Channel 29 Host Packet Configuration Register B |
| 0x4740 2BB4 - 0x4740 2FFF | - | Reserved |

**Table 9-111. CPPI DMA Scheduler Registers**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4740 3000 | DMA_SCHED_CTRL | CPPI DMA Scheduler Control Register |
| 0x4740 3804 - 0x4740 38FF | - | Reserved |
| 0x4740 3800 | WORD0 | CPPI DMA Scheduler Table Word 0 |
| 0x4740 3804 | WORD1 | CPPI DMA Scheduler Table Word 1 |
| … | … | … |
| 0x4740 38F8 | WORD62 | CPPI DMA Scheduler Table Word 62 |
| 0x4740 38FC | WORD63 | CPPI DMA Scheduler Table Word 63 |

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**Table 9-111. CPPI DMA Scheduler Registers (continued)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4740 38FF - 0x4740 3FFF | - | Reserved |

**Table 9-112. CPPI DMA Queue Manager Registers**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4740 4000 | QMGRREVID | Queue Manager Revision |
| 0x4740 4004 | - | Reserved |
| 0x4740 4008 | DIVERSION | Queue Manager Queue Diversion |
| 0x4740 400C - 0x4740 401F | - | Reserved |
| 0x4740 4020 | FDBSC0 | Queue Manager Free Descriptor/Buffer Starvation Count 0 |
| 0x4740 4024 | FDBSC1 | Queue Manager Free Descriptor/Buffer Starvation Count 1 |
| 0x4740 4028 | FDBSC2 | Queue Manager Free Descriptor/Buffer Starvation Count 2 |
| 0x4740 402C | FDBSC3 | Queue Manager Free Descriptor/Buffer Starvation Count 3 |
| 0x4740 4030 | FDBSC4 | Queue Manager Free Descriptor/Buffer Starvation Count 4 |
| 0x4740 4034 | FDBSC5 | Queue Manager Free Descriptor/Buffer Starvation Count 5 |
| 0x4740 4038 | FDBSC6 | Queue Manager Free Descriptor/Buffer Starvation Count 6 |
| 0x4740 403C | FDBSC7 | Queue Manager Free Descriptor/Buffer Starvation Count 7 |
| 0x4740 4030 - 0x4740 407C | - | Reserved |
| 0x4740 4080 | LRAM0BASE | Queue Manager Linking RAM Region 0 Base Address |
| 0x4740 4084 | LRAM0SIZE | Queue Manager Linking RAM Region 0 Size |
| 0x4740 4088 | LRAM1BASE | Queue Manager Linking RAM Region 1 Base Address |
| 0x4740 408C | - | Reserved |
| 0x4740 4090 | PEND0 | Queue Manager Queue Pending 0 |
| 0x4740 4094 | PEND1 | Queue Manager Queue Pending 1 |
| 0x4740 4098 | PEND2 | Queue Manager Queue Pending 2 |
| 0x4740 409C | PEND3 | Queue Manager Queue Pending 3 |
| 0x4740 40A0 | PEND4 | Queue Manager Queue Pending 4 |
| 0x4740 40A4 - 0x4740 4FFF | - | Reserved |
| 0x4740 5000 + 16xR | QMEMRBASE0 | Memory Region 0 Base Address (R ranges from 0 to 15) |
| 0x4740 5000 + 16xR + 4 | QMEMRCTRL0 | Memory Region 0 Control 0 (R ranges from 0 to 15) |
| 0x4740 5000 + 16xR + 8 | - | Reserved |
| 0x4740 5000 + 16xR + C | - | Reserved |
| 0x4740 5010 – 0x4740 50EF | - | ... |
| 0x4740 5000 + 16xR | QMEMRBASE15 | Memory Region 15 Base Address (R ranges from 0 to 15) |
| 0x4740 5000 + 16xR + 4 | QMEMRCTRL15 | Memory Region 15 Control (R ranges from 0 to 15) |
| 0x4740 5000 + 16xR + 8 | - | Reserved |
| 0x4740 5000 + 16xR + C | - | Reserved |
| 0x4740 5080 - 0x4740 5FFF | - | Reserved |
| 0x4740 6000 + 16xN | - | Reserved |
| 0x4740 6000 + 16xN + 4 | - | Reserved |
| 0x4740 6000 + 16xN + 8 | - | Reserved |
| 0x4740 6000 + 16xN + C | CTRLD0 | Queue N Register D (N ranges from 0 to 155) |
| 0x4740 6010 – 0x4740 69AF | - | ... |
| 0x4740 6000 + 16xN | - | Reserved |
| 0x4740 6000 + 16xN + 4 | - | Reserved |
| 0x4740 6000 + 16xN + 8 | - | Reserved |
| 0x4740 6000 + 16xN + C | CTRLD155 | Queue N Register D (N ranges from 0 to 155) |
| 0x4740 69B0 - 0x4740 6FFF | - | Reserved |


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**Table 9-112. CPPI DMA Queue Manager Registers (continued)**

| HEX ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x4740 7000 + 16xN | QSTATA0 | Queue N Status A (N ranges from 0 to 155) |
| 0x4740 7000 + 16xN + 4 | QSTATB0 | Queue N Status B (N ranges from 0 to 155) |
| 0x4740 7000 + 16xN + 8 | QSTATC0 | Queue N Status C (N ranges from 0 to 155) |
| 0x4740 7000 + 16xN + C | - | Reserved |
| 0x4740 7010 – 0x4740 79AF | - | ... |
| 0x4740 7000 + 16xN | QSTATA155 | Queue N Status A (N ranges from 0 to 155) |
| 0x4740 7000 + 16xN + 4 | QSTATB155 | Queue N Status B (N ranges from 0 to 155) |
| 0x4740 7000 + 16xN + 8 | QSTATC155 | Queue N Status C (N ranges from 0 to 155) |
| 0x4740 7000 + 16xN + C | - | Reserved |
| 0x4740 79B0 - 0x4740 7FFF | - | Reserved |

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### 9.21.2 USB2.0 Electrical Data/Timing

**Table 9-113. Switching Characteristics Over Recommended Operating Conditions for USB2.0**

(see Figure 9-95)

| NO. | PARAMETER | | OPP100/120/166 | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | LOW SPEED 1.5 Mbps | | FULL SPEED 12 Mbps | | HIGH SPEED 480 Mbps | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{r(D)}$ | Rise time, USBx_DP and USBx_DM signals(1) | 75 | 300 | 4 | 20 | 0.5 | | ns |
| 2 | $t_{f(D)}$ | Fall time, USBx_DP and USBx_DM signals(1) | 75 | 300 | 4 | 20 | 0.5 | | ns |
| 3 | $t_{rfM}$ | Rise/Fall time, matching(2) | 80 | 125 | 90 | 111 | – | – | % |
| 4 | $V_{CRS}$ | Output signal cross-over voltage(1) | 1.3 | 2 | 1.3 | 2 | – | – | V |
| 5 | $t_{jr(source)NT}$ | Source (Host) Driver jitter, next transition | | 2 | | 2 | | (3) | ns |
| | $t_{jr(FUNC)NT}$ | Function Driver jitter, next transition | | 25 | | 2 | | (3) | ns |
| 6 | $t_{jr(source)PT}$ | Source (Host) Driver jitter, paired transition(4) | | 1 | | 1 | | (3) | ns |
| | $t_{jr(FUNC)PT}$ | Function Driver jitter, paired transition | | 10 | | 1 | | (3) | ns |
| 7 | $t_{w(EOPT)}$ | Pulse duration, EOP transmitter | 1250 | 1500 | 160 | 175 | – | – | ns |
| 8 | $t_{w(EOPR)}$ | Pulse duration, EOP receiver(5) | 670 | | 82 | | – | | ns |
| 9 | $t_{(DRATE)}$ | Data Rate | | 1.5 | | 12 | | 480 | Mbps |
| 10 | $Z_{DRV}$ | Driver Output Resistance | – | – | 28 | 49.5 | 40.5 | 49.5 | Ω |
| 11 | $Z_{INP}$ | Receiver Input Impedance(6) | 300 | | 300 | – | – | – | kΩ |

(1) Low Speed: $C_L$ = 200 pF, Full Speed: $C_L$ = 50 pF, High Speed: $C_L$ = 50 pF
(2) $t_{RFM} = (t_r/t_f) \times 100$. [Excluding the first transaction from the Idle state.]
(3) For more detailed information, see the Universal Serial Bus Specification Revision 2.0, Chapter 7, *Electrical*.
(4) $t_{jr} = t_{px(1)} - t_{px(0)}$
(5) Must accept as valid EOP.
(6) These values do not include the external resistors required per USB 2.0 specification.

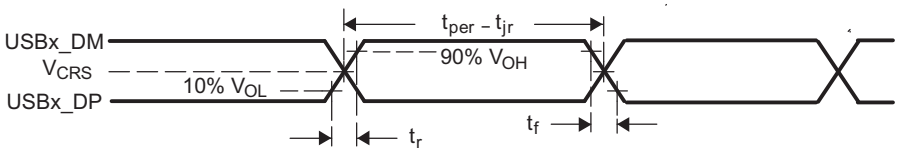


**Figure 9-95. USB2.0 Integrated Transceiver Interface Timing**

For more detailed information on USB2.0 board design, routing, and layout guidelines, see the *USB 2.0 Board Design and Layout Guidelines* Application Report (Literature Number: SPRAAR7).


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# 10 Device and Documentation Support

## 10.1 Device Support

### 10.1.1 Development Support

TI offers an extensive line of development tools, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules. The support documentation for the tools is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE).

The following products support development of TMS320DM8127 processor applications:

**Software Development Tools:** Code Composer Studio™ Integrated Development Environment (IDE): including Editor C/C++/Assembly Code Generation, and Debug plus additional development tools Scalable, Real-Time Foundation Software (DSP/BIOS™), which provides the basic run-time target software needed to support any DaVinci Digital Media Processor application.

**Hardware Development Tools:** Extended Development System (XDS™) Emulator

For a complete listing of development-support tools for the DM8127 DaVinci™ Digital Media Processor platform, visit the Texas Instruments website at www.ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

### 10.1.2 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP + ARM devices and support tools. Each DSP + ARM commercial family member has one of three prefixes: TMX, TMP, or TMS (for example, TMS320DM8127BCYE1). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

**TMX** Experimental device that is not necessarily representative of the final device's electrical specifications.

**TMP** Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification.

**TMS** Fully-qualified production device.

Support tool development evolutionary flow:

**TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing.

**TMDS** Fully qualified development-support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

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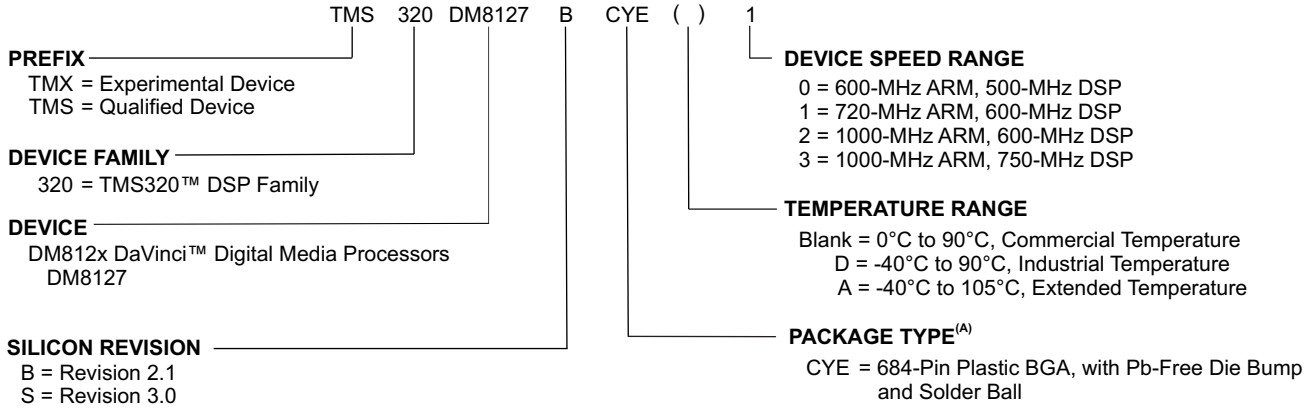
TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, CYE), the temperature range (for example, "Blank" is the commercial temperature range), and the device speed range in megahertz (for example, "Blank" is the default [600-MHz ARM, 500-MHz DSP]).

Figure 10-1 provides a legend for reading the complete device name for any TMS320DM8127 platform member.

For device part numbers and further ordering information of TMS320DM8127 devices in the CYE package type, see the TI website (www.ti.com) or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the *TMS320DM8127 DaVinci™ Digital Media Processors Silicon Errata (Silicon Revisions 3.0, 2.1)* (Literature Number: SPRZ385).




A. BGA = Ball Grid Array
B. For actual device part numbers (P/Ns) and ordering information, contact your nearest TI Sales Representative.
C. The TEMPERATURE RANGE values are specified over operating junction temperature.

**Figure 10-1. Device Nomenclature(B)(C)**

## 10.2 Documentation Support

The following document describes the DM8127 DaVinci™ Digital Media Processors.

**SPRUGZ8** ***TMS320DM814x DaVinci Digital Media Processors Technical Reference Manual.***

## 10.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**TI Embedded Processors Wiki** ***Texas Instruments Embedded Processors Wiki.*** Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.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# 11 Mechanical

The device package has been specially engineered with a new technology called Via Channel™. The Via Channel technology allows larger than normal PCB via sizes and reduced PCB signal layers to be used in a PCB design with this 0.8-mm pitch package, and will substantially reduce PCB costs. Via Channel also allows PCB routing in only two signal layers (four layers total) due to the increased layer efficiency of the Via Channel™ BGA technology.

## 11.1 Thermal Data for CYE-04 (Top Hat)

**Table 11-1. Thermal Resistance Characteristics (PBGA Package) [CYE-04] (Thinner Top Hat)**

| NO. | | | °C/W(1) | AIR FLOW (m/s)(2) |
|---|---|---|---|---|
| 1 | $R\Theta_{JC}$ | Junction-to-case | 0.39 | N/A |
| 2 | $R\Theta_{JB}$ | Junction-to-board | 3.87 | N/A |
| 3 | $R\Theta_{JA}$ | Junction-to-free air | 11.67 | 0.00 |
| 5 | $R\Theta_{JMA}$ | Junction-to-moving air | 8.59 | 1.00 |
| 6 | | | 7.80 | 2.00 |
| 7 | | | 7.33 | 3.00 |
| 8 | $Psi_{JT}$ | Junction-to-package top | 0.19 | 0.00 |
| 10 | | | 0.20 | 1.00 |
| 11 | | | 0.20 | 2.00 |
| 12 | | | 0.21 | 3.00 |
| 13 | $Psi_{JB}$ | Junction-to-board | 3.44 | 0.00 |
| 15 | | | 3.37 | 1.00 |
| 16 | | | 3.26 | 2.00 |
| 17 | | | 3.17 | 3.00 |

(1) These measurements were conducted in a JEDEC defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] measurement, which was conducted in a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Packages*

Power dissipation of 2 W and an ambient temperature of 70ºC is assumed.

(2) m/s = meters per second

## 11.2 Packaging Information

The following packaging information and addendum reflect the most current data available for the designated device(s). This data is subject to change without notice and without revision of this document.

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TMS320DM8127BCYE0 | OBSOLETE | FCBGA | CYE | 684 | | TBD | Call TI | Call TI | 0 to 90 | TMS320DM8127BCYE0 | |
| TMS320DM8127BCYE1 | OBSOLETE | FCBGA | CYE | 684 | | TBD | Call TI | Call TI | 0 to 90 | TMS320DM8127BCYE1 | |
| TMS320DM8127BCYE2 | OBSOLETE | FCBGA | CYE | 684 | | TBD | Call TI | Call TI | 0 to 90 | TMS320DM8127BCYE2 | |
| TMS320DM8127BCYE3 | ACTIVE | FCBGA | CYE | 684 | | Green (RoHS & no Sb/Br) | SNAGCU | Level-4-250C-72 HR | 0 to 90 | TMS320DM8127BCYE3 | Samples |
| TMS320DM8127BCYED1 | OBSOLETE | FCBGA | CYE | 684 | | Green (RoHS & no Sb/Br) | SNAGCU | Level-4-250C-72 HR | -40 to 90 | TMS320DM8127BCYED1 | |
| TMS320DM8127BCYED3 | OBSOLETE | FCBGA | CYE | 684 | | Green (RoHS & no Sb/Br) | SNAGCU | Level-4-250C-72 HR | -40 to 90 | TMS320DM8127BCYED3 | |
| TMS320DM8127SCYE0 | ACTIVE | FCBGA | CYE | 684 | 60 | Green (RoHS & no Sb/Br) | SNAGCU | Level-4-250C-72 HR | 0 to 90 | TMS320DM8127SCYE0 | Samples |
| TMS320DM8127SCYE1 | ACTIVE | FCBGA | CYE | 684 | 60 | Green (RoHS & no Sb/Br) | SNAGCU | Level-4-250C-72 HR | 0 to 90 | TMS320DM8127SCYE1 | Samples |
| TMS320DM8127SCYE2 | ACTIVE | FCBGA | CYE | 684 | 60 | Green (RoHS & no Sb/Br) | SNAGCU | Level-4-250C-72 HR | 0 to 90 | TMS320DM8127SCYE2 | Samples |
| TMS320DM8127SCYE3 | ACTIVE | FCBGA | CYE | 684 | 60 | Green (RoHS & no Sb/Br) | SNAGCU | Level-4-250C-72 HR | 0 to 90 | TMS320DM8127SCYE3 | Samples |
| TMS320DM8127SCYE3H | ACTIVE | FCBGA | CYE | 684 | 60 | Green (RoHS & no Sb/Br) | SNAGCU | Level-4-250C-72 HR | | TMS320DM8127SCYE3H | Samples |
| TMS320DM8127SCYED0 | ACTIVE | FCBGA | CYE | 684 | 60 | Green (RoHS & no Sb/Br) | SNAGCU | Level-4-250C-72 HR | -40 to 90 | TMS320DM8127SCYED0 | Samples |
| TMS320DM8127SCYED1 | ACTIVE | FCBGA | CYE | 684 | 60 | Green (RoHS & no Sb/Br) | SNAGCU | Level-4-250C-72 HR | | TMS320DM8127SCYED1 | Samples |
| TMS320DM8127SCYED2 | ACTIVE | FCBGA | CYE | 684 | 60 | Green (RoHS & no Sb/Br) | SNAGCU | Level-4-250C-72 HR | -40 to 90 | TMS320DM8127SCYED2 | Samples |
| TMS320DM8127SCYED3 | ACTIVE | FCBGA | CYE | 684 | 60 | Green (RoHS & no Sb/Br) | SNAGCU | Level-4-250C-72 HR | -40 to 90 | TMS320DM8127SCYED3 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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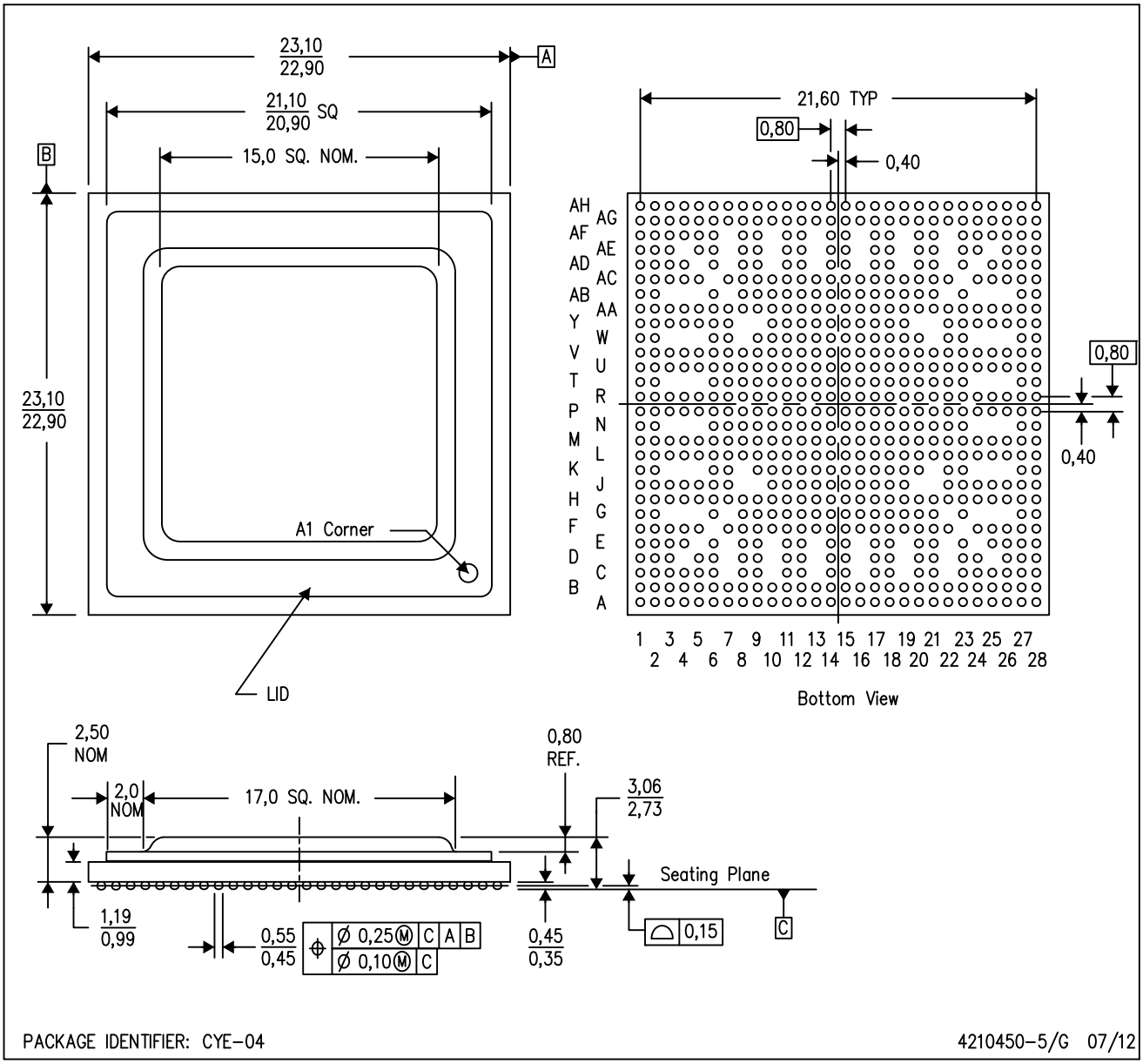
CYE (S–PBGA–N684) PLASTIC BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Flip chip application only.
D. Thermally enhanced plastic package with lid.
E. Pb–free die bump and solder ball.

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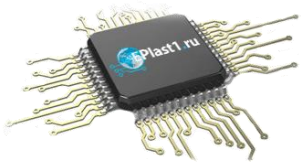


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