

MOSFETs Silicon P-Channel MOS (U-MOSVI)

SSM3J168F

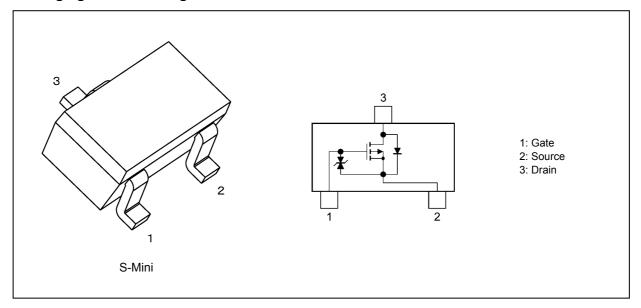
1. Applications

- · High-Speed Switching
- · Analog Switches
- · Interfacing

2. Features

- (1) 4.0 V drive
- (2) Low drain-source on-resistance
 - : $R_{DS(ON)} = 1.6 \Omega$ (typ.) ($V_{GS} = -4.0 \text{ V}$)
 - $R_{\rm DS(ON)} = 1.4 \ \Omega \ {\rm (typ.)} \ {\rm (V_{GS}} = -4.5 \ {\rm V)}$
 - $R_{\mathrm{DS(ON)}} = 1.3~\Omega$ (typ.) ($V_{\mathrm{GS}} = -10~\mathrm{V}$)

3. Packaging and Pin Assignment





4. Absolute Maximum Ratings (Note) (Unless otherwise specified, T_a = 25 °C)

Characteristics			Symbol	Rating	Unit
Drain-source voltage			V _{DSS}	-60	V
Gate-source voltage			V _{GSS}	-20/+10	
Drain current (DC)		(Note 1)	I _D	-400	mA
Drain current (pulsed)		(Note 1)	I _{DP}	-800	
Power dissipation		(Note 2)	P _D	600	mW
Power dissipation	t ≤ 1s	(Note 2)		1200	
Channel temperature			T _{ch}	150	ů
Storage temperature			T _{stg}	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Ensure that the channel temperature does not exceed 150 °C.

Note 2: Device mounted on a 25.4 mm × 25.4 mm × 1.6 mm FR4 glass epoxy board (Cu pad: 645 mm²)

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

Note: The MOSFETs in this device are sensitive to electrostatic discharge. When handling this device, the worktables, operators, soldering irons and other objects should be protected against anti-static discharge.

Note: The channel-to-ambient thermal resistance, R_{th(ch-a)}, and the drain power dissipation, P_D, vary according to the board material, board area, board thickness and pad area. When using this device, be sure to take heat dissipation fully into account.



5. Electrical Characteristics

5.1. Static Characteristics (Unless otherwise specified, Ta = 25 °C)

Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current		I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = -16 \text{ V}/+10 \text{ V}$	_	_	±10	μА
Drain cut-off current		I _{DSS}	V _{DS} = -60 V, V _{GS} = 0 V	_	_	-10	
Drain-source breakdown voltage		V _{(BR)DSS}	$I_D = -1 \text{ mA}, V_{GS} = 0 \text{ V}$	-60	_	_	٧
Drain-source breakdown voltage	(Note 1)	V _{(BR)DSX}	I _D = -1 mA, V _{GS} = 10 V	-50	_	_	
Gate threshold voltage	(Note 2)	V _{th}	V _{DS} = -10 V, I _D = -1 mA	-0.8	_	-2.0	
Drain-source on-resistance	(Note 3)	R _{DS(ON)}	I_D = -100 mA, V_{GS} = -4.0 V	_	1.6	2.0	Ω
			I _D = -100 mA, V _{GS} = -4.5 V	_	1.4	1.9	
			I _D = -200 mA, V _{GS} = -10 V	_	1.3	1.55	

Note 1: If a reverse bias is applied between gate and source, this device enters $V_{(BR)DSX}$ mode. Note that the drain-source breakdown voltage is lowered in this mode.

Note 2: Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to below (-1 mA for this device). Then, for normal switching operation, $V_{GS(ON)}$ must be higher than V_{th} , and $V_{GS(OFF)}$ must be lower than V_{th} . This relationship can be expressed as: $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$.

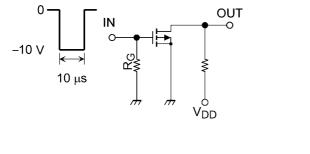
Take this into consideration when using the device.

Note 3: Pulse measurement.

5.2. Dynamic Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Input capacitance	C _{iss}	$V_{DS} = -10 \text{ V}$, $V_{GS} = 0 \text{ V}$,	_	82	_	pF
Reverse transfer capacitance	C _{rss}	f = 1 MHz	_	5.5		
Output capacitance	C _{oss}			13		
Switching time (turn-on time)	t _{on}	$V_{DD} = -30 \text{ V}, I_D = -0.1 \text{ A},$ $V_{GS} = 0 \text{ to } -10 \text{ V}, R_G = 50 \Omega$	_	4.3		ns
Switching time (turn-off time)	t _{off}	Duty \leq 1 %,V _{IN} : t _r , t _r < 5 ns, Common source, See Chapter 5.3.	_	31.7	_	

5.3. Switching Time Test Circuit



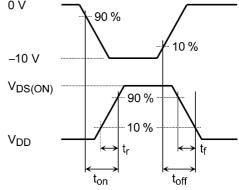


Fig. 5.3.1 Switching Time Test Circuit

Fig. 5.3.2 Input Waveform/Output Waveform

5.4. Gate Charge Characteristics (Unless otherwise specified, Ta = 25 °C)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Qg	$V_{DD} = -48 \text{ V}, I_{D} = -0.4 \text{ A},$	_	3.0		nC
Gate-source charge 1	Q _{gs1}	V _{GS} = -10 V	_	0.4	_	
Gate-drain charge	Q _{gd}		_	1.1	_	

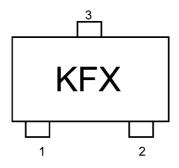


5.5. Source-Drain Characteristics (Unless otherwise specified, T_a = 25 °C)

	Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Diod	le forward voltage	(Note 1)	V_{DSF}	I _D = 400 mA, V _{GS} = 0 V	_	0.87	1.2	V

Note 1: Pulse measurement.

6. Marking



7. Characteristics Curves (Note)

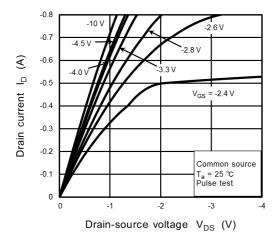


Fig. 7.1 I_D - V_{DS}

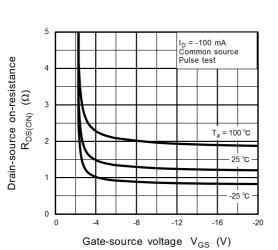


Fig. 7.3 R_{DS(ON)} - V_{GS}

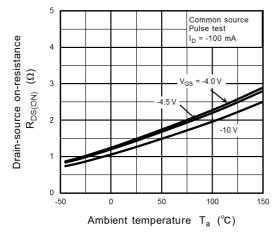


Fig. 7.5 $R_{DS(ON)}$ - T_a

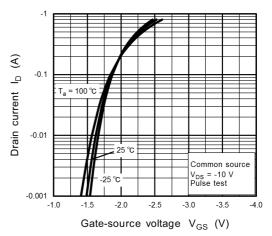


Fig. 7.2 I_D - V_{GS}

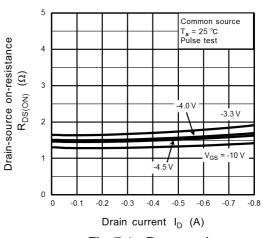


Fig. 7.4 R_{DS(ON)} - I_D

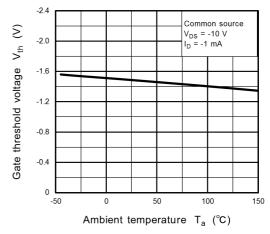


Fig. 7.6 V_{th} - T_a

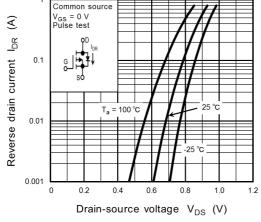


Fig. 7.7 IDR - VDS

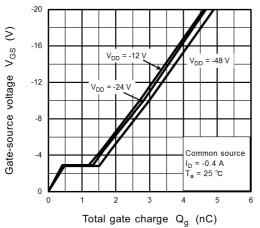


Fig. 7.9 Dynamic Input Characteristics

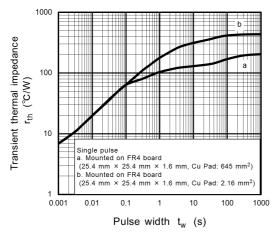


Fig. 7.11 r_{th} - t_w

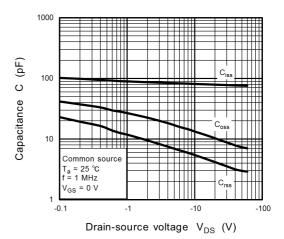


Fig. 7.8 C - V_{DS}

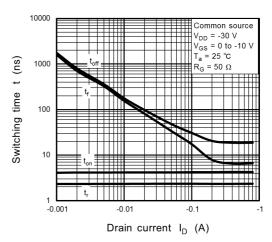


Fig. 7.10 t-I_D

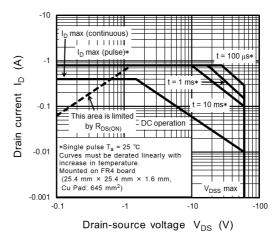


Fig. 7.12 Safe Operationg Area

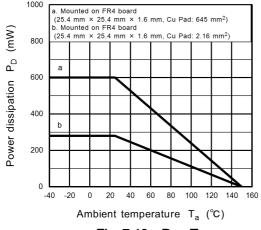


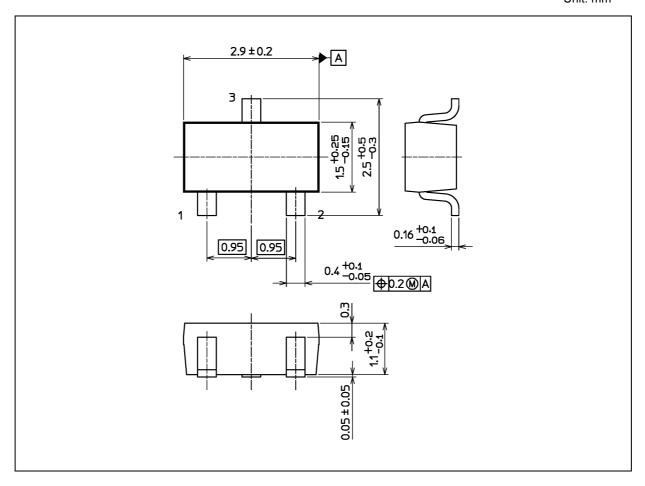
Fig. 7.13 P_D - T_a

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



Package Dimensions

Unit: mm



Weight: 12 mg (typ.)

	Package Name(s)
JEDEC: SOT-346	
Nickname: S-Mini	



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Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: <u>org@eplast1.ru</u>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина,

дом 2, корпус 4, литера А.