

MC74HCT365A

Hex 3-State Noninverting Buffer with Common Enables and LSTTL Compatible Inputs

High-Performance Silicon-Gate CMOS

The MC74HCT365A is identical in pinout to the LS365. The device inputs are compatible with LSTTL outputs.

This device is a high-speed hex buffer with 3-state outputs and two common active-low Output Enables. When either of the enables is high, the buffer outputs are placed into high-impedance states. The HCT365A has noninverting outputs.

Features

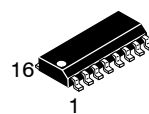
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 90 FETs or 22.5 Equivalent Gates
- These are Pb-Free Devices*



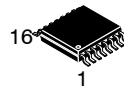
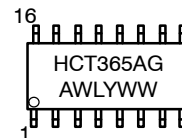
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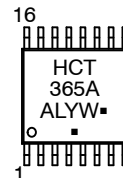
MARKING DIAGRAMS



SOIC-16
D SUFFIX
CASE 751B



TSSOP-16
DT SUFFIX
CASE 948F



A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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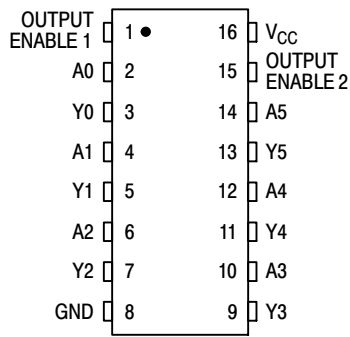


Figure 1. Pin Assignment

FUNCTION TABLE

| Inputs | | | Output |
|----------|----------|---|--------|
| Enable 1 | Enable 2 | A | Y |
| L | L | L | L |
| L | L | H | H |
| H | X | X | Z |
| X | H | X | Z |

X = don't care

Z = high impedance

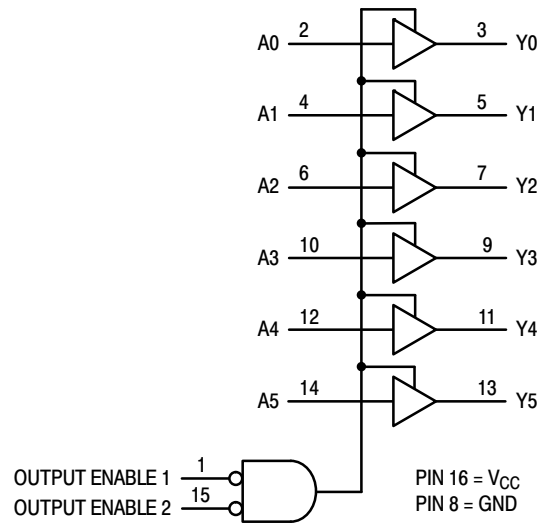


Figure 2. Logic Diagram

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|------------------|------------------------|-----------------------|
| MC74HCT365ADG | SOIC-16 (Pb-Free) | 48 Units / Rail |
| MC74HCT365ADR2G | SOIC-16 (Pb-Free) | 2500 Units / Reel |
| MC74HCT365ADTG | TSSOP-16* (Pb-Free) | 96 Units / Rail |
| MC74HCT365ADTR2G | TSSOP-16* (Pb-Free) | 2500 Units / Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

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MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|-----------|---|-------------------------|------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | - 0.5 to + 7.0 | V |
| V_{in} | DC Input Voltage (Referenced to GND) | - 0.5 to $V_{CC} + 0.5$ | V |
| V_{out} | DC Output Voltage (Referenced to GND) | - 0.5 to $V_{CC} + 0.5$ | V |
| I_{in} | DC Input Current, per Pin | ± 20 | mA |
| I_{out} | DC Output Current, per Pin | ± 25 | mA |
| I_{CC} | DC Supply Current, V_{CC} and GND Pins | ± 50 | mA |
| P_D | Power Dissipation in Still Air, SOIC Package† TSSOP Package† | 500 450 | mW |
| T_{stg} | Storage Temperature | - 65 to + 150 | °C |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating — SOIC Package: - 7 mW/°C from 65° to 125°C
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|----------------------|--|-----|----------|------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | 4.5 | 5.5 | V |
| V_{in} , V_{out} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V_{CC} | V |
| T_A | Operating Temperature Range, All Package Types | -55 | +125 | °C |
| t_r , t_f | Input Rise/Fall Time (Figure 1) | 0 | 500 | ns |

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | V_{CC} V | Guaranteed Limit | | | Unit |
|-----------------|--|--|---------------|------------------|-------------|-----------|---------|
| | | | | - 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| V_{IH} | Minimum High-Level Input Voltage | $V_{out} = V_{CC} - 0.1$ V $ I_{out} \leq 20$ μ A | 4.5 to 5.5 | 2.0 | 2.0 | 2.0 | V |
| V_{IL} | Maximum Low-Level Input Voltage | $V_{out} = 0.1$ V $ I_{out} \leq 20$ μ A | 4.5 to 5.5 | 0.8 | 0.8 | 0.8 | V |
| V_{OH} | Minimum High-Level Output Voltage | $V_{in} = V_{IH}$ $ I_{out} \leq 20$ μ A | 4.5 | 4.4 | 4.4 | 4.4 | V |
| | | $V_{in} = V_{IH}$ $ I_{out} \leq 6.0$ mA | 4.5 | 3.98 | 3.84 | 3.70 | |
| V_{OL} | Maximum Low-Level Output Voltage | $V_{in} = V_{IL}$ $ I_{out} \leq 20$ μ A | 4.5 | 0.1 | 0.1 | 0.1 | V |
| | | $V_{in} = V_{IL}$ $ I_{out} \leq 6.0$ mA | 4.5 | 0.26 | 0.33 | 0.40 | |
| I_{in} | Maximum Input Leakage Current | $V_{in} = V_{CC}$ or GND | 4.5 | ± 0.1 | ± 1.0 | ± 1.0 | μ A |
| I_{OZ} | Maximum Three-State Leakage Current | Output in High-Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND | 4.5 | ± 0.5 | ± 5.0 | ± 10 | μ A |
| I_{CC} | Maximum Quiescent Supply Current (per Package) | $V_{in} = V_{CC}$ or GND $I_{out} = 0$ μ A | 4.5 | 4 | 40 | 160 | μ A |
| ΔI_{CC} | Additional Quiescent Supply Current | $V_{in} = 2.4$ V, Any One Input $V_{in} = V_{CC}$ or GND, Other Inputs $I_{out} = 0$ μ A | 5.5 | ≥ -55°C | 25 to 125°C | | mA |
| | | | | 2.9 | 2.4 | | |

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AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

| Symbol | Parameter | V _{CC} V | Guaranteed Limit | | | Unit |
|--|--|----------------------|------------------|--------|---------|------|
| | | | - 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3) | 4.5 | 24 | 30 | 36 | ns |
| t _{PLZ} , t _{PHZ} | Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4) | 4.5 | 44 | 55 | 66 | ns |
| t _{PZL} , t _{PZH} | Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4) | 4.5 | 44 | 55 | 66 | ns |
| t _{T LH} , t _{T HL} | Maximum Output Transition Time, Any Output (Figures 1 and 3) | 4.5 | 12 | 15 | 18 | ns |
| C _{in} | Maximum Input Capacitance | — | 10 | 10 | 10 | pF |
| C _{out} | Maximum Three-State Output Capacitance (Output in High-Impedance State) | — | 15 | 15 | 15 | pF |

| C _{PD} | Power Dissipation Capacitance (Per Buffer)* | Typical @ 25°C, V _{CC} = 5.0 V | | pF |
|-----------------|---|---|--|----|
| | | 60 | | |
| | | | | |

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

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SWITCHING WAVEFORMS

($V_I = 0$ to 3 V, $V_M = 1.3$ V)

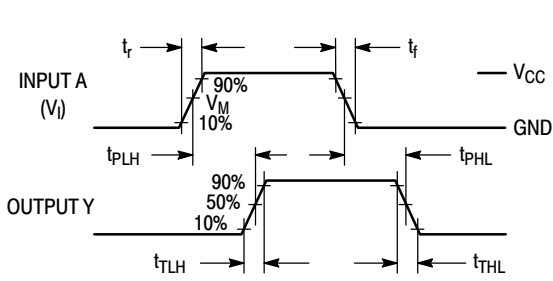


Figure 1.

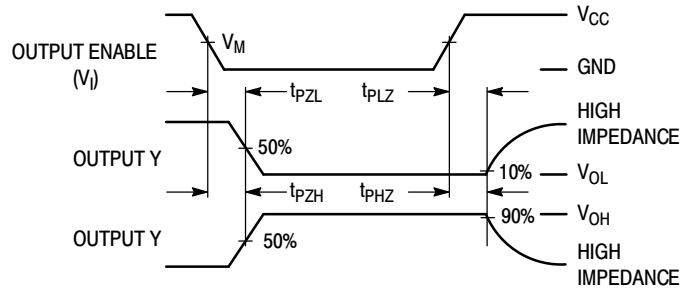
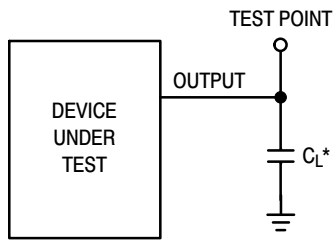


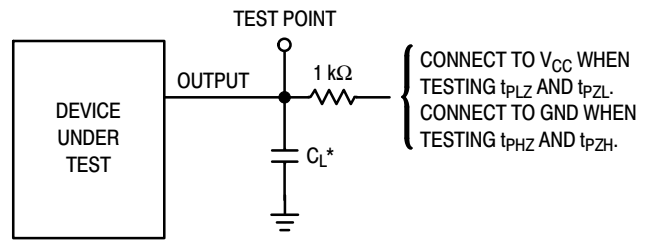
Figure 2.

TEST CIRCUITS



*Includes all probe and jig capacitance

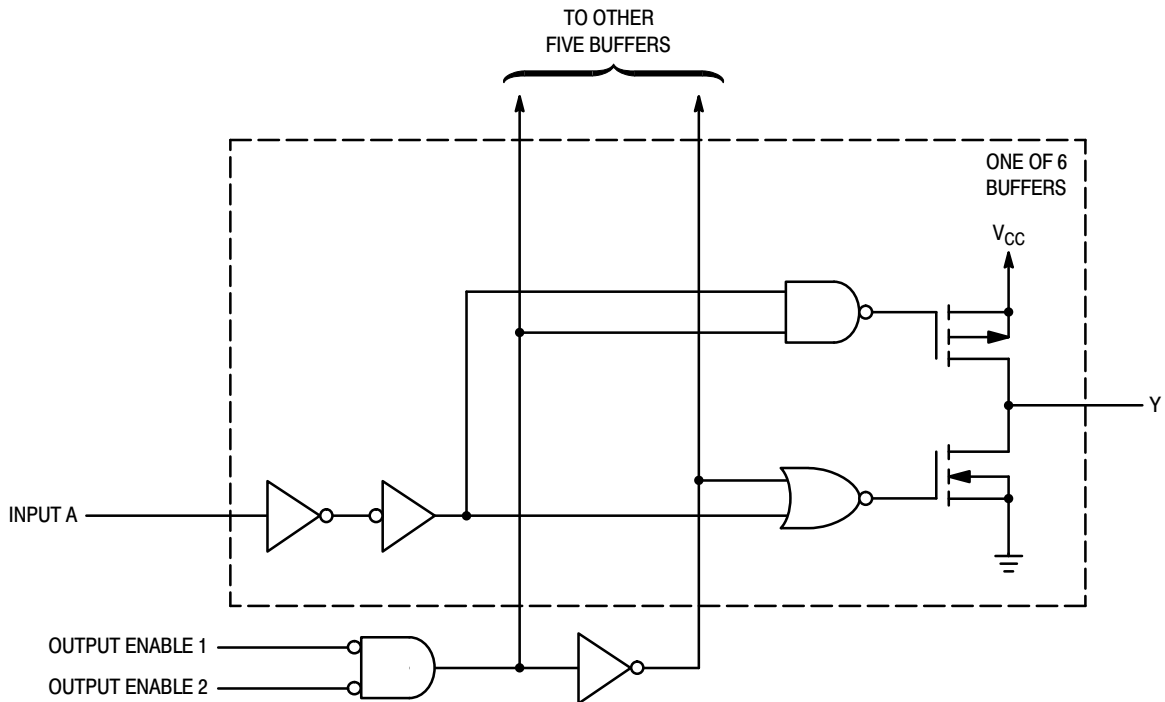
Figure 3.



*Includes all probe and jig capacitance

Figure 4.

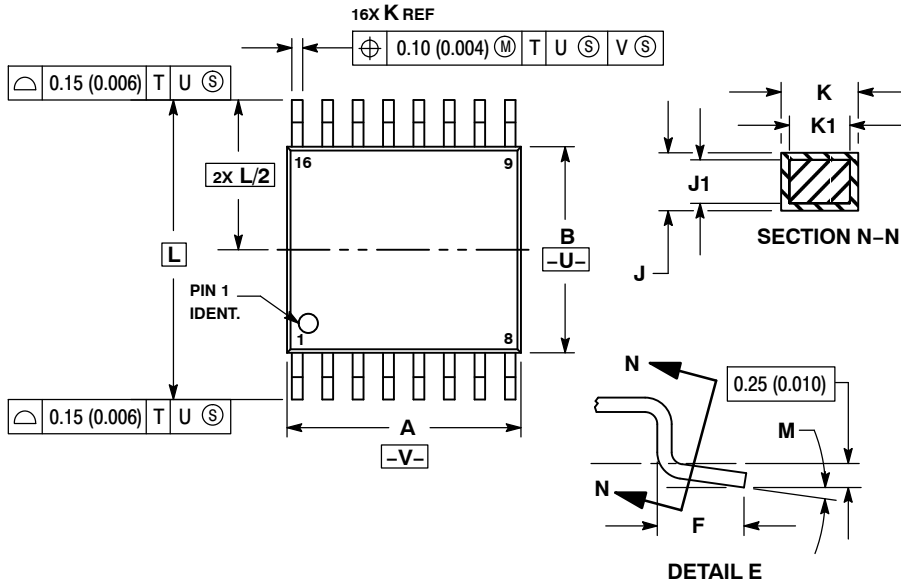
LOGIC DETAIL



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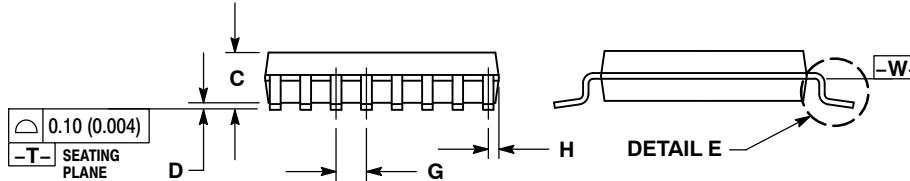
PACKAGE DIMENSIONS

TSSOP-16
DT SUFFIX
CASE 948F-01
ISSUE B

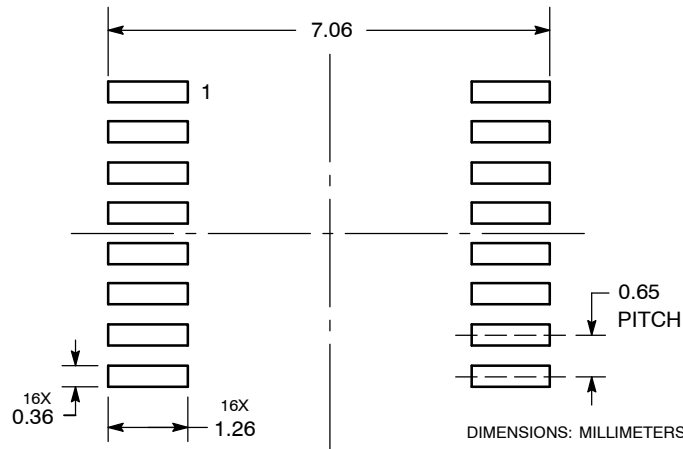


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |



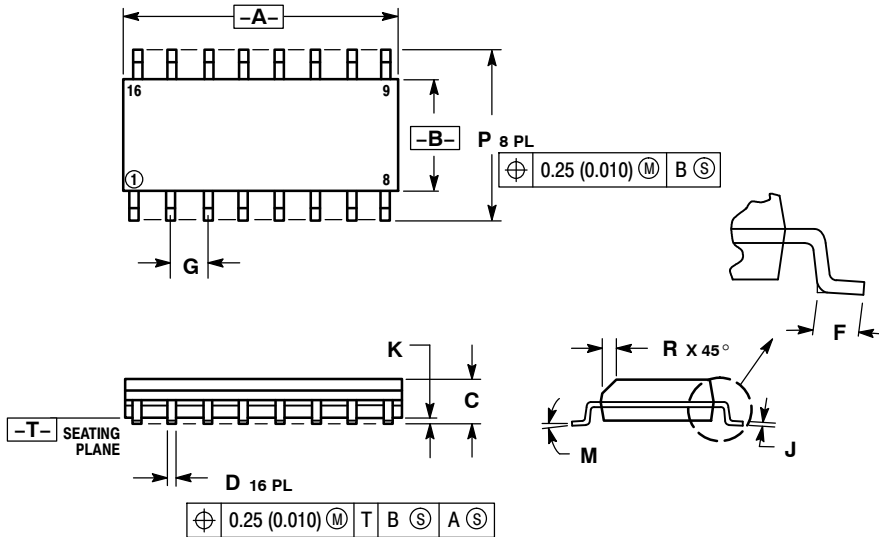
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PACKAGE DIMENSIONS

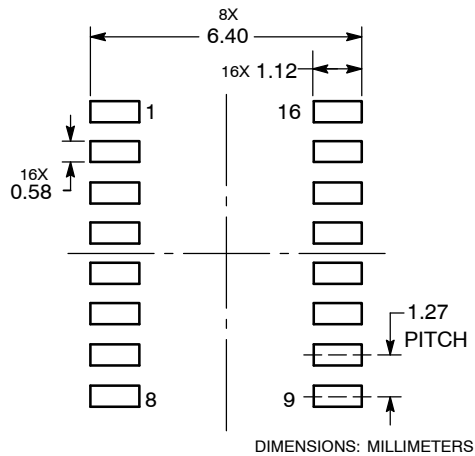
SOIC-16
D SUFFIX
CASE 751B-05
ISSUE K



- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 - CONTROLLING DIMENSION: MILLIMETER.
 - DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 - MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 - DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

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