60V Synchronous Buck Multi-Chemistry Battery Charger

FEATURES

- **Wide Input Voltage Range: 4.5V to 60V**
- **Wide Battery Voltage Range: 0V to 60V**
- **Built-In Charge Algorithms for Lead-Acid and Li-Ion**
- **±0.5% Float Voltage Accuracy**
- **±5% Charge Current Accuracy**
- Maximum Power Point Tracking Input Control
- NTC Temperature Compensated Float Voltage
- Two Open Drain Status Pins
- Thermally Enhanced 28-Lead 4mm × 5mm QFN Package

APPLICATIONS

- Battery Backup for Lighting, UPS Systems, Security Cameras, Computer Control Panels
- Portable Medical Equipment
- Solar-Powered Systems
- Industrial Battery Charging

DESCRIPTION

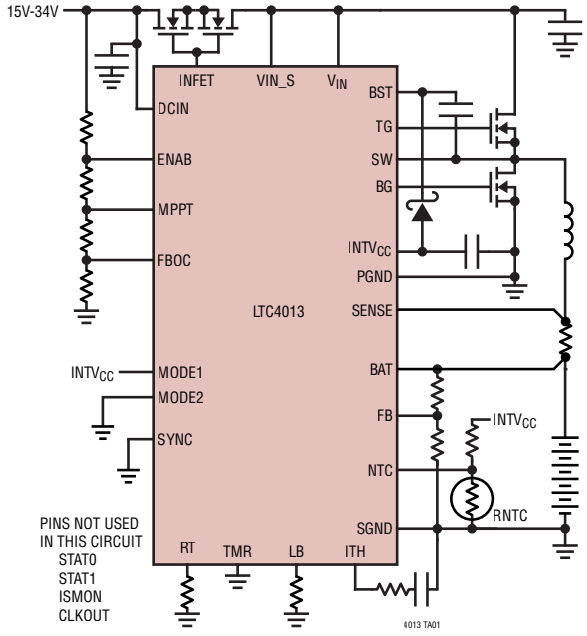
The LTC®4013 is a high voltage battery charger controller that supports float, absorption and equalization lead-acid and constant-current/constant-voltage Li-Ion charging algorithms. It is particularly well suited for charging a wide range of lead-acid batteries, including both vented and sealed type. The LTC4013 also supports Li-Ion/Polymer, $LiFePO_4$, NiMH, NiCd and other battery types.

Charging is performed with a high efficiency synchronous buck (step-down) converter that uses external N-channel MOSFETs. Switching frequency is programmed with a resistor or synchronized with an external clock for use in multiphase applications. Charge current is set with an external sense resistor.

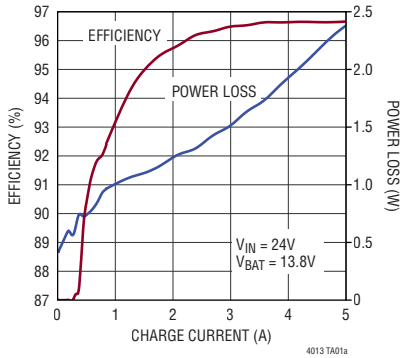
The device includes maximum power point tracking input voltage regulation for limited power inputs such as solar panels. Other features include user-programmable absorption and equalization times, temperature-adjusted regulation voltages and an external NFET isolation diode.

TYPICAL APPLICATION

15V-34V to 6 Cell Lead-Acid (12.6V) 5A Step-Down Battery Charger



Efficiency and Power Loss vs Charge Current



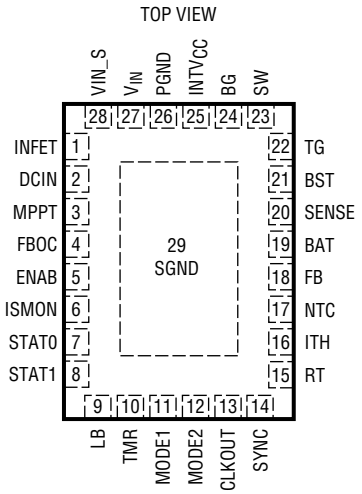
BASED ON APPLICATION ON BACK PAGE

ABSOLUTE MAXIMUM RATINGS

(Note 1)

DCIN, V_{IN}, VIN_S, ENAB, STAT0, STAT1 .... –0.3V to 60V
INFET ..... –0.3V to 73V
BST ..... –0.3V to 66V
STAT0, STAT1 .....5mA
SENSE, BAT ..... –0.3V to 60V
SENSE-BAT ..... –0.3V to 0.3V
FBOC, MPPT, FB, MODE1, MODE2, SYNC,
$INTV_{CC}$, NTC ..... –0.3V to 6V
TMR, LB, ITH ..... –0.3V to 3V
Operating Junction Temperature Range
(Note 2) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W, θ_{JC} = 3.4°C/W
EXPOSED PAD (PIN 29) IS SGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LTC4013#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4013EUFD#PBF	LTC4013EUFD#TRPBF	4013	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LTC4013IUFD#PBF	LTC4013IUFD#TRPBF	4013	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). DCIN, V_{IN}, VIN_S = 18V, ENAB = 1.4V, SYNC = 0V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range (DCIN, V_{IN})		●	4.5		60	V
Battery Voltage Range (BAT)		●			60	V
ENAB Pin Threshold (Rising) Threshold Hysteresis		●	1.175	1.220 170	1.275	V mV
ENAB Pin Bias Current				10		nA
VIN UVLO	V_{IN} Rising, Power Enabled V_{IN} Rising, Power Disabled			3.45 3.08		V V
DCIN Pin Operating Current DCIN Pin Shutdown Current	Not Switching ENAB = 0V	 ●		480 4	625 7.9	µA µA
V_{IN} Pin Operating Current V_{IN} Pin Shutdown Current	Not Switching (Notes 3 and 4) ENAB = 0V, RT = 40.2k	 ●		2.1 32	2.8 80	mA µA
BAT Pin Operating Current BAT Pin Shutdown Current	Not Switching ENAB = 0V	 ●		6.2 0.5	9.3 1.5	µA µA
SENSE Pin Operating Current SENSE Pin Shutdown Current	Not Switching ENAB = 0V	 ●		5.3 0.4	8.1 2.5	µA µA
SW Pin Current in Shutdown	ENAB = 0V, SW = 60V, BST = 66V			0.25		µA
STAT0, STAT1 Enabled Voltage	STAT0, STAT1 Pin Current =1mA STAT0, STAT1 Pin Current = 5mA			0.14 0.77	0.2 1.0	V V
STAT0, STAT1 Leakage Current	STAT0, STAT1 Pin Voltage = 60V	●			1	µA
FB Regulation Voltage (See Tables 2-5)						
Battery Float Voltage $V_{FB(FL)}$	MODE1 = L, H MODE2 = L, H	 ●	2.256 2.244	2.267 2.267	2.278 2.291	V V
	MODE1 = M, MODE2 = L, H	 ●	2.189 2.178	2.200 2.200	2.211 2.223	V V
	MODE1 = L, MODE2 = M	 ●	2.320 2.309	2.332 2.332	2.344 2.356	V V
Battery Absorption Voltage $V_{FB(ABS)}$	MODE1 = H, MODE2 = L, H MODE1 = L, MODE2 = H	 ●	2.355 2.343	2.367 2.3670	2.380 2.392	V V
	MODE1 = M, MODE2 = L, H	 ●	2.388 2.376	2.400 2.400	2.412 2.425	V V
Battery Equalization Voltage $V_{FB(EQ)}$	MODE1 = L, H, MODE2 = H, TMR = Cap	 ●	2.487 2.475	2.500 2.500	2.513 2.526	V V
	MODE1 = M, MODE2 = H, TMR = Cap	 ●	2.587 2.574	2.600 2.600	2.613 2.627	V V
Battery Charge Voltage $V_{FB(CHG)}$	MODE1 = H, MODE2 = M	 ●	2.355 2.343	2.367 2.367	2.38 2.392	V V
	MODE1 = M, MODE2 = M	 ●	2.388 2.376	2.400 2.400	2.412 2.425	V V
Battery Recharge Voltage $V_{FB(RECHG)}$	MODE1 = M, H MODE2 = M	 ●	2.284 2.272	2.295 2.295	2.306 2.319	V V
NTC Amplifier Gain	$\Delta V_{FB(FL)}/\Delta V_{NTC}$			0.21		V/V
NTC Amplifier Offset	$\Delta V_{FB(FL)}$ with V_{NTC} = $INTV_{CC}/2$		–15	0	15	mV
FB Pin Current	V_{FB} = 3V			10		nA
LB Pin Current	V_{LB} = 2V		19.6	20	20.4	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). DCIN, V_{IN}, VIN_S = 18V, ENAB = 1.4V, SYNC = 0V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Error Amp						
Error Amp Transconductance	$\Delta I_{ITH}/\Delta(V_{SENSE}–V_{BAT})$ V_{ITH} = 1.8V		1300	1800	2300	µmho
Error Amp Current Source	V_{ITH} =1.8V, V_{FB} = 2.0V, (Float) MODE1 = H, MODE2 = L		–6.5	–10	–13.5	µA
Error Amp Current Sink	V_{ITH} =1.8V, V_{FB} = 2.4V, (Float) MODE1 = H, MODE2 = L		18	27	35	µA
Current Sense (all measured as V_{SENSE} – V_{BAT} unless otherwise noted)						
Maximum Charging Sense Resistor Voltage	In Absorption, Float, Li-Ion Charge, BAT = 14V	●	48	50	52	mV
Equalization and Low Battery Charging Sense Resistor Voltage	BAT = 14V	●	8	10	12.5	mV
Current Sense C/10 Threshold	Termination when TMR = 0	●	2.0	4.6	7.0	mV
Constant Voltage (CV) Threshold	$V_{FB(ABS,EQ)}$ – V_{FB}, Timeout Initiation with Cap on TMR	●		15.6	24.5	mV
Overcurrent Charging Turnoff		●		100	106	mV
ISMON Fullscale Output Voltage	V_{SENSE} – V_{BAT} = 50mV			1.00		V
SENSE Input UVLO	V_{SENSE} Rising (Charging Enabled)	●	1.86	1.97	2.07	V
SENSE Input UVLO Hysteresis	V_{SENSE} Rising to Falling (Charging Disabled)			100		mV
Configuration Pins						
MODE1, MODE2 Pin, Low Threshold		●			0.8	V
MODE1, MODE2 Pin, Mid Threshold		●	1.3		1.8	V
MODE1, MODE2 Pin, High Threshold		●	2.5			V
Timer						
TMR Oscillator High Threshold				1.5		V
TMR Oscillator Low Threshold				0.97		V
Safety Timer Turn on Voltage	TMR Voltage Rising	●	0.45	0.5	0.65	V
Safety Timer Turn on Hysteresis Voltage				250		mV
TMR Source/Sink Current	TMR = 1.25V		8.5	10.0	11.5	µA
TMR Pin Period	CTMR = 0.2µF			20.8		ms
End of Charge Termination Time, t_{EOC}	CTMR = 0.2µF			3.03		hr
Equalization Charge Termination Time	CTMR = 0.2µF, MODE1 = M, H CTMR = 0.2µF, MODE1 = L			0.379 0.758		hr hr
$INTV_{CC}$ Regulator ($INTV_{CC}$ Pin)						
$INTV_{CC}$ Regulation Voltage				5.00		V
$INTV_{CC}$ Dropout Voltage	DCIN = 4.5V, $INTV_{CC}$ = 5mA			4.46		V
$INTV_{CC}$ Supply Short-Circuit Current	$INTV_{CC}$ = 0V		100	175		mA
NMOS FET Drivers						
Non-Overlap Time TG to BG				40		ns
Non-Overlap Time BG to TG				74		ns
Minimum On-Time BG				38		ns
Minimum On-Time TG				37		ns
Minimum Off-Time BG				65		ns
Top Gate Driver Switch On Resistance	BST – SW = 5V, Pull Up BST – SW = 5V, Pull Down			2.3 1.3		Ω Ω
Bottom Gate Driver Switch On Resistance	$INTV_{CC}$ = 5V, Pull Up $INTV_{CC}$ = 5V, Pull Down			2.3 1		Ω Ω

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). DCIN, V_{IN}, VIN_S = 18V, ENAB = 1.4V, SYNC = 0V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
BST UVLO	TG Enabled (Rising) TG Disabled (Falling)			4.25 3.81		V V
OSC						
Switching Frequency	R_T = 40.2kΩ R_T = 232kΩ	●	950	1000 200	1050	kHz kHz
SYNC Pin Threshold (Falling Edge)			1.3	1.4	1.5	V
SYNC Pin Hysteresis				190		mV
CLK Output Logic Level	High Low		4.5		 0.5	V V
Input PowerPath Control						
Reverse Turn-Off Threshold Voltage	DCIN – V_{IN}	●	–7.3	–4.4	–1.3	mV
Forward Turn-On Threshold Voltage	DCIN – V_{IN}	●	–7.1	–4.2	–1.1	mV
Forward Turn-On Hysteresis Voltage	DCIN – V_{IN}			0.2		mV
INFET Turn-Off Current	INFET = V_{IN} + 1.5V			–9.0		mA
INFET Turn-On Current	INFET = V_{IN} + 1.5V			60		µA
INFET Clamp Voltage	I_{INFET} = 2µA , DCIN = 12V to 60V V_{IN} = DCIN – 0.1V Measure VINFET – DCIN	●		11.0	12.5	V
INFET Off Voltage	I_{INFET} = –2µA , DCIN = 12V to 59.9V V_{IN} = DCIN +0.1V Measure VINFET – DCIN	●		–2.2	–1.6	V
DCIN to BAT UVLO	Switching Regulator Turn Off (V_{DCIN} – V_{BAT} Falling)			69		mV
	Switching Regulator Turn On (V_{DCIN} – V_{BAT} Rising)			99		mV
MPPT Regulation						
FBOC Voltage Range		●	1.0		3.0	V
MPPT Sample Period				10.2		s
MPPT Sample Pulse Width				271		µs
Regulation Input Offset	Set FBOC Look at MPPT Regulation		–40		40	mV
MPPT Input Burst Mode Turn On Threshold	V_{MPPT} – V_{FBOC} (Converted) , V_{FBOC} = 1.5 V_{SENSE} – V_{BAT} < C/10 Part Enter Burst Mode	●	–45	–32	–15	mV
MPPT Input Burst Mode Hysteresis	FBOC = 1.5, V_{SENSE} – V_{BAT} < C/10 MPPT Turn Off – Turn On	●	35	62	85	mV

Note 1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

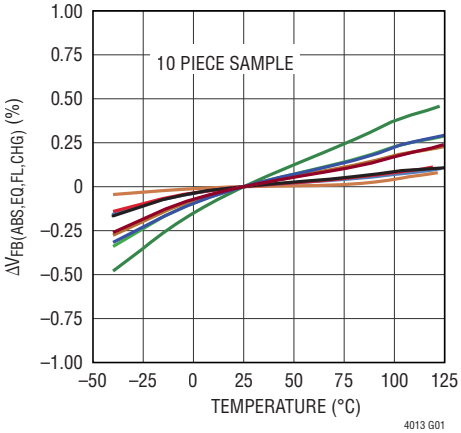
Note 2. The LTC4013 is tested under pulse loaded conditions such that $T_J \approx T_A$. The LTC4013E is guaranteed to meet performance specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC4013I is guaranteed over the full –40°C to 125°C operating junction temperature range. The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D in Watts) according to the formula: $T_J = T_A + P_D \bullet \theta_{JA}$ where θ_{JA} (in °C/W) is the package thermal impedance. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors. This IC includes over temperature protection that is intended to protect the device during momentary overload. Junction temperature will exceed 125°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 3. V_{IN} does not include switching currents. V_{BST} = $INTV_{CC}$ and V_{SW} = 0V for testing.

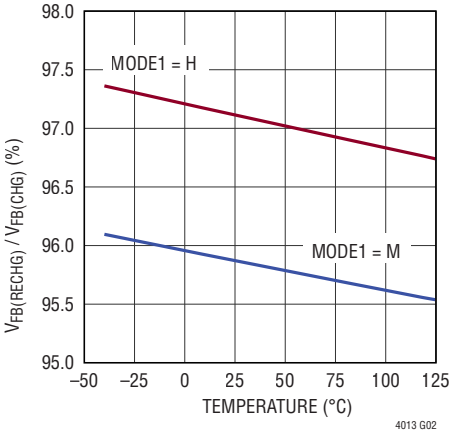
Note 4. I_{VIN} current also includes current that charges capacitance on CLKOUT. This current is approximately $C_{CLKOUT} \bullet 5V \bullet f_{SW}$. For this test C_{CLKOUT} was 100pF, f_{SW} was 1MHz (R_T = 40.2k) so the current included is 0.5mA. In normal operation the CLKOUT capacitance is much less.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

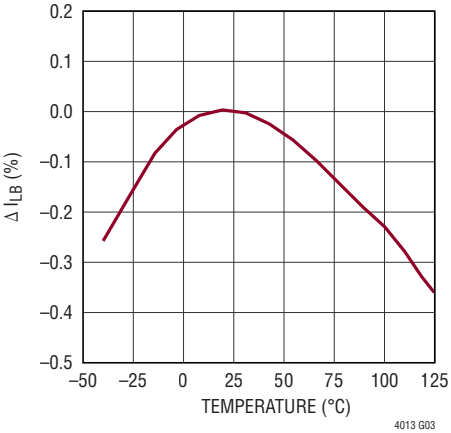
Change in Absorption, Equalization, Float and Li-Ion Charge Voltages vs Temperature



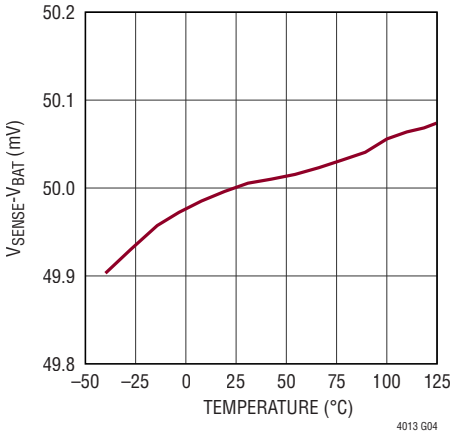
Li-Ion Recharge% vs Temperature



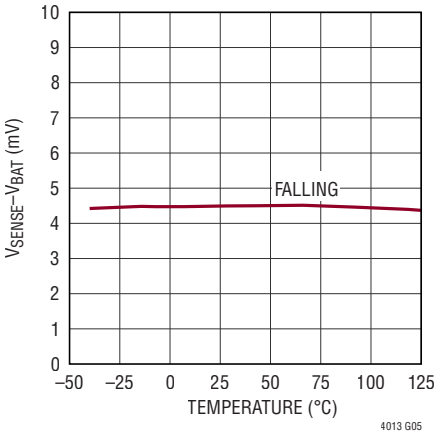
Low Battery (LB) Current vs Temperature



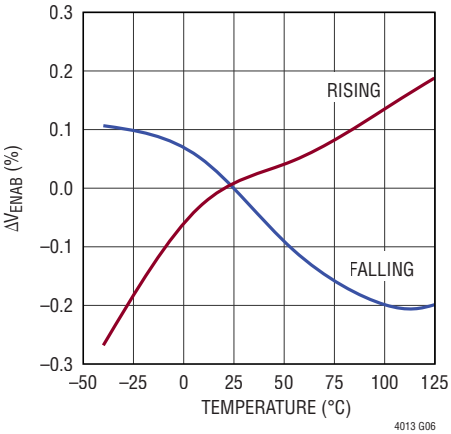
Maximum Sense Voltage vs Temperature



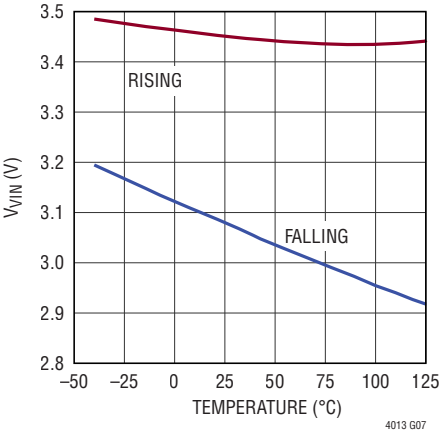
C/10 Thresholds vs Temperature



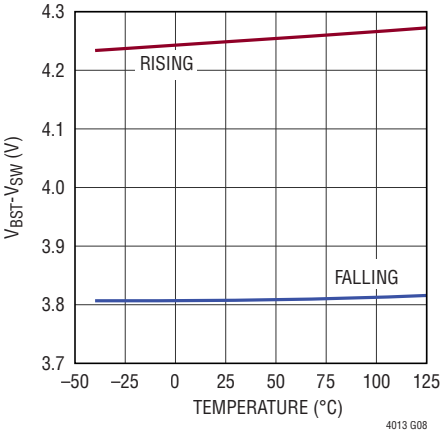
Change in ENAB Voltage vs Temperature



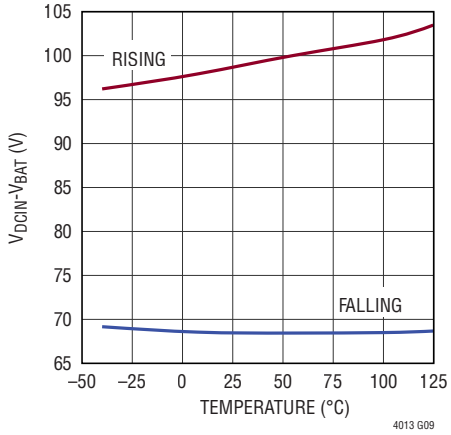
VIN UVLO vs Temperature



BST UVLO vs Temperature

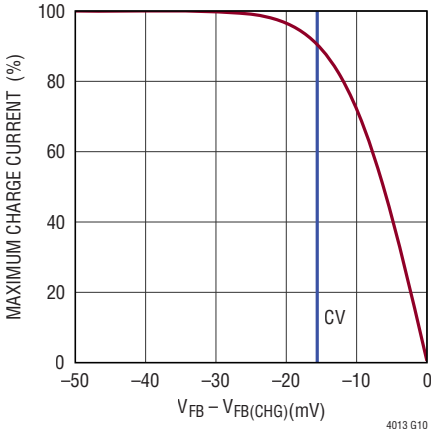


DCIN to BAT UVLO Voltage vs Temperature

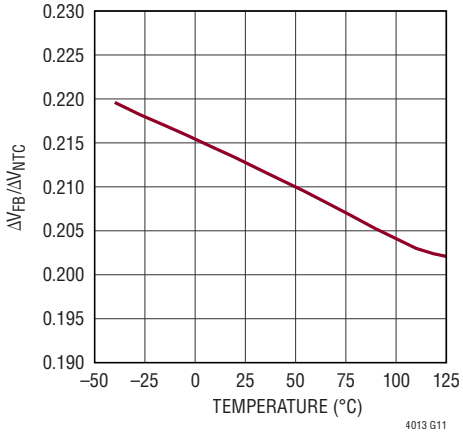


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

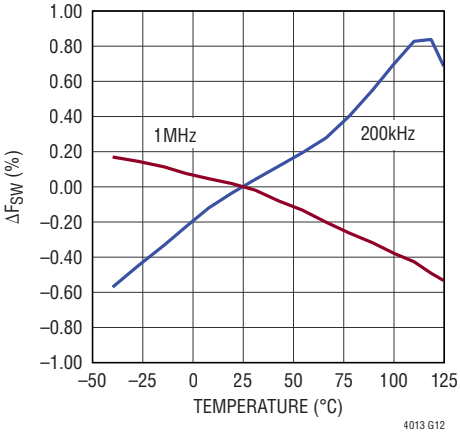
Maximum Charge Current vs ΔV from V_{CHARGE}



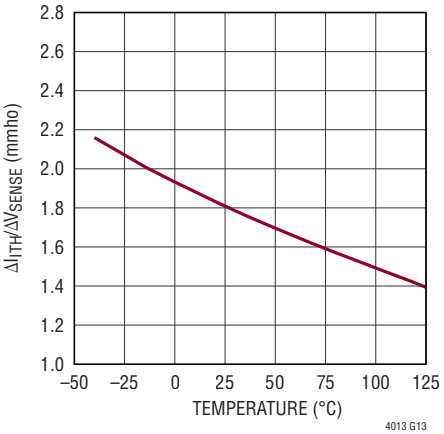
NTC Amplifier Gain vs Temperature



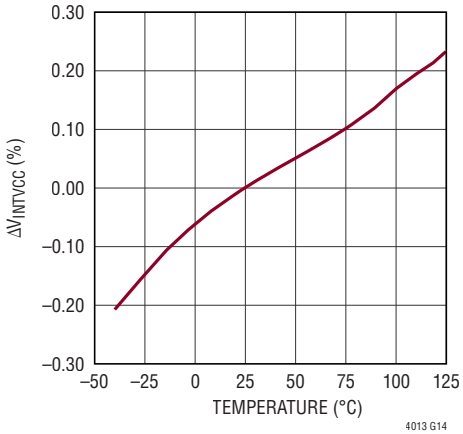
Change in Switching Regulator Frequency vs Temperature



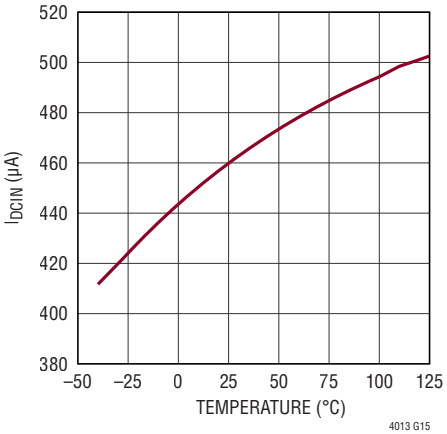
Error Amp Transconductance vs Temperature



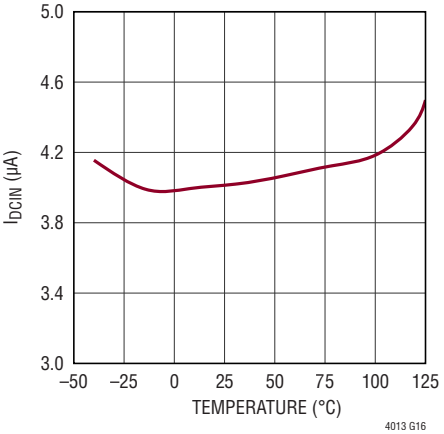
Change in V_{INTVCC} vs Temperature



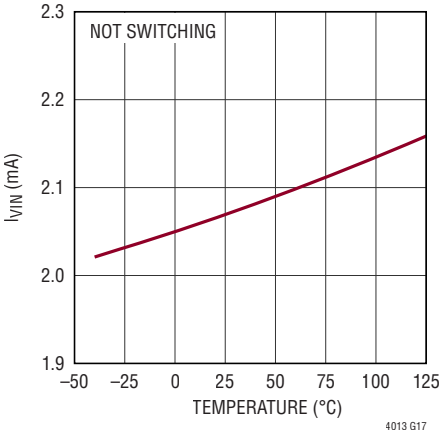
DCIN Operating Current vs Temperature



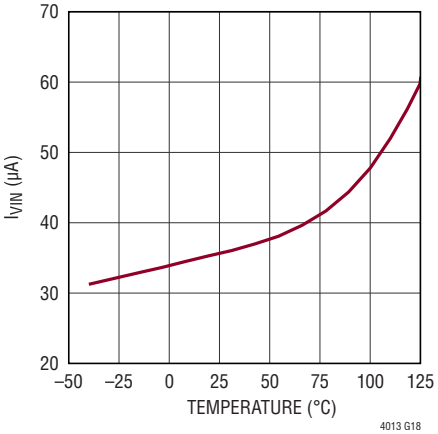
DCIN Current in Shutdown vs Temperature (Note 3)



V_{IN} Operating Current vs Temperature (Note 4)



V_{IN} Current in Shutdown vs Temperature



PIN FUNCTIONS

INFET (Pin 1): Input PowerPath MOSFET Gate Drive. An internal charge pump provides turn on drive for this pin. This pin is connected to the gate of an external N-channel MOSFET(s) used to prevent the battery discharge in the event that DCIN is less than the battery voltage.

DCIN (Pin 2): Input Supply Pin. This pin is used to sense the input voltage and determines whether the external input MOSFET (INFET) is turned on. It also supplies power to the internal charge pump that drives INFET.

MPPT, FBOC (Pins 3, 4): These pins are the inputs for the Maximum Peak Power Tracking (MPPT) regulation loop. This loop regulates charge current in order to maintain maximum power charging in the presence of a power limited source such as a solar panel. A three resistor divider is placed from the input supply to MPPT to FBOC and then to ground. These pins are used to program an input voltage regulation loop as a percentage of the input open circuit voltage. During normal operation, if the input voltage falls below the programmed percentage of the open-circuit voltage, the MPPT loop will reduce charge current to maintain the target voltage at DCIN. If the voltage regulation feature is not used, connect FBOC to $INTV_{CC}$. See the Applications section for more details.

ENAB (Pin 5): Precision Threshold Enable Pin. Enable threshold is 1.22V (rising), with 170mV of input hysteresis. When in shutdown, all charging functions are disabled and input supply current is reduced. Typical ENAB pin input bias current is 10nA.

ISMON (Pin 6): Output of Current Sense Amplifier. The voltage on this pin is twenty times the differential voltage between SENSE and BAT.

STAT0, STAT1 (Pins 7, 8): Open drain outputs indicate the charger status. They are capable of sinking 5mA of current when on, enabling them to drive an LED. Specific states are detailed in Table 6.

LB (Pin 9): A resistor on this pin to ground is used to set the detection voltage for a "discharged" battery. If the battery stays below this voltage for 1/8 of the absorption timeout period, charging is stopped. Charging is reinitiated through an ENAB toggle or swapping out the battery. A 20µA current sourced from the pin through an external resistor from ground sets the voltage on the pin. This voltage is then compared to the FB pin voltage to ascertain the battery condition.

TMR (Pin 10): Battery End of Charge Time Set. A capacitor on this pin to ground sets the time the charger spends during various charging stages. Absorption and Li-Ion charge time is set as three hours per 0.2µF. The equalization timeout is a ratio of this time, either one fourth or one eight of the absorption time, depending on the MODE pins settings.

MODE1 (Pin 11) MODE2 (Pin 12): These pins set the charging algorithm used. See Tables 2 to 5 for a complete listing. The part supports 2, 3, 4-stage lead-acid and Li-Ion charging algorithms with and without time termination.

CLKOUT (Pin 13): This output pin has a signal that can be used to synchronize the oscillator on another LTC4013 or other circuitry. See the applications section for more detail.

SYNC (Pin 14): Frequency Synchronization Pin. This pin is used for paralleling multiple LTC4013 for higher currents. This pin allows the switching frequency to be synchronized to an external clock. The R_T resistor is chosen to operate the internal clock at 20% slower than the SYNC pulse frequency. Ground this pin when not in use. When laying out the PC board, avoid noise coupling to or from SYNC trace.

RT (Pin 15): A resistor to ground sets the switching frequency between 200kHz and 1MHz. This pin is current limited to 60µA. Do not leave this pin open.

ITH (Pin 16): This pin provides loop compensation for the switching regulator control loops. See the applications section for further information.

PIN FUNCTIONS

NTC (Pin 17): This pin connects to an external resistor divider string that contains an NTC resistor. The voltage difference between V_{NTC} and $INTV_{CC}/2$ is converted to an offset in the switching regulator charge voltages. Place the NTC resistor as close to the battery as possible, with good Kelvin ground connection. See the Applications section for more details.

FB (Pin 18): This pin provides feedback for regulating battery voltage during charging. A resistor divider from the battery to this pin sets the input to the charger voltage error amp. Use care in connections to provide a good Kelvin connection and to insure accurate measurement. See applications section for more details.

BAT, SENSE (Pins 19, 20): Battery charge current is monitored and regulated via a resistor connected between SENSE and BAT. Maximum voltage across these pins during charge current regulation is 50mV. The switching regulator inductor is connected between SW and SENSE. Take care to insure that the signal between these pins is not corrupted with noise. Overcurrent shutdown occurs when the voltage across SENSE and BAT exceeds 100mV.

BST (Pin 21): The BST pin provides a floating 5V regulated supply for the high-side MOSFET driver. Connect a 0.22µF capacitor from this pin to SW. Connect a 1A Schottky diode cathode to this pin, anode to $INTV_{CC}$ pin.

TG (Pin 22): This pin drives the gate of the top side external N-channel MOSFET.

SW (Pin 23): This pin connects to the switch mode power supply switch node. It connects to one side of the switching regulator inductor, the source of the top side MOSFET and the drain of the bottom side MOSFET as well as the boost capacitor. This pin has high current associated with the turn off of the high side MOSFET.

BG (Pin 24): This pin drives the gate of the external bottom side N-channel MOSFET.

$INTV_{CC}$ (Pin 25): This pin is the output of a regulated 5V output and is current limited to 100mA. Connect a ceramic capacitor from this pin to PGND. The BST pin refresh diode anode is connected to this pin.

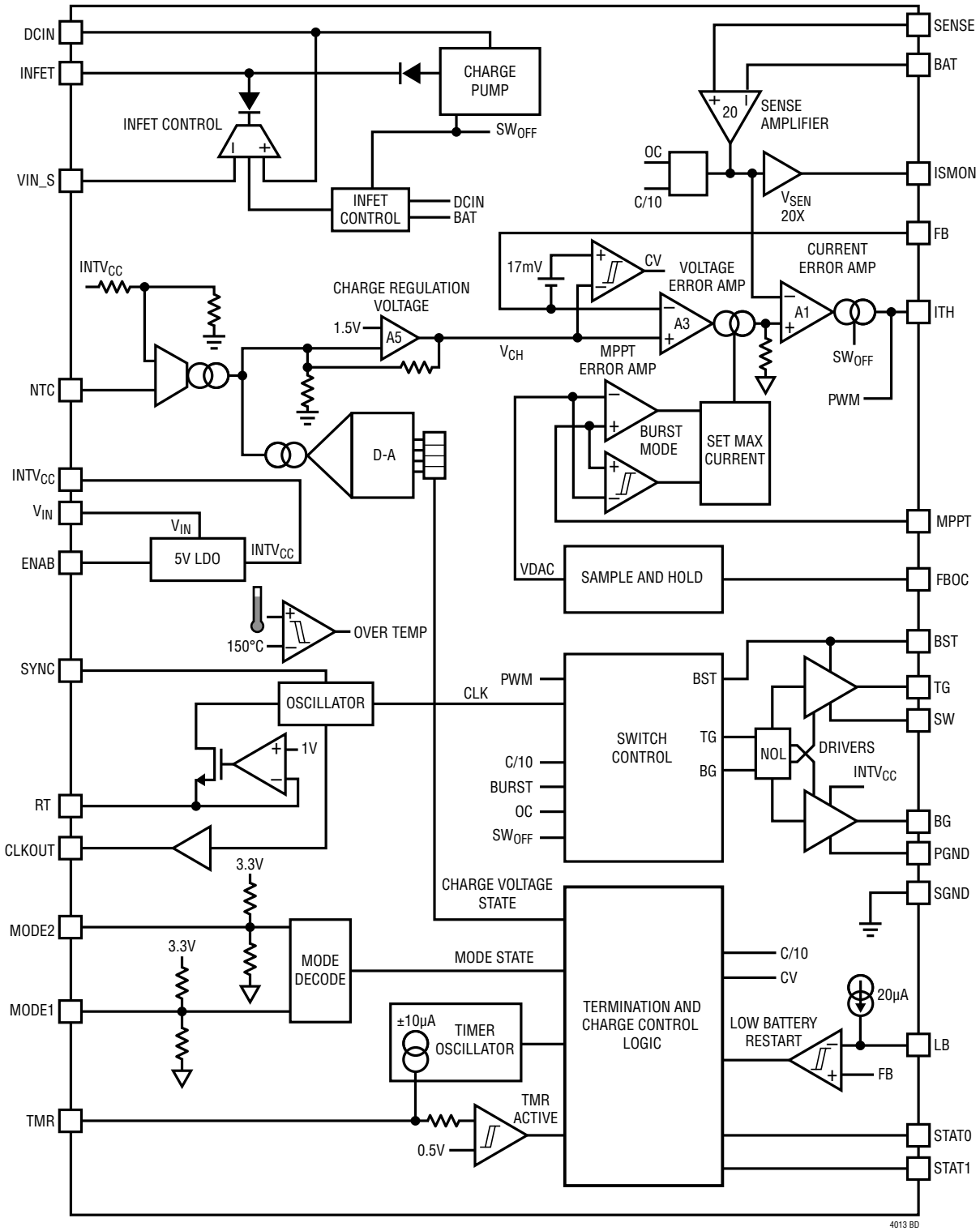
PGND (Pin 26): This pin is the ground return for high current paths for the part. This is primarily the low side gate drive.

V_{IN} (Pin 27): High current input supply pin that provides power to the IC. This pin provides power to the $INTV_{CC}$ internal 5V regulator. It is usually tied to the switching regulator high side MOSFET. This pin must be bypassed with a low ESR capacitor to ground. See the applications section for sizing information.

VIN_S (Pin 28): This pin provides a Kelvin input for the V_{IN} connection of the input PowerPath circuitry.

SGND (Exposed Pad Pin 29): Signal Ground Reference. This pin is the “quiet” ground used as a reference point for critical resistor dividers such as battery feedback, MPPT dividers and NTC resistor. Connect to the output decoupling capacitor negative terminal and battery negative terminal. Solder the exposed pad to PCB ground (SGND) for electrical connection and rated thermal performance.

BLOCK DIAGRAM



OPERATION

OVERVIEW

The LTC4013 is a high voltage multi-chemistry battery charger with specific focus on lead-acid batteries. It incorporates a step-down (buck) DC/DC synchronous converter controller using external N channel mosfets for high efficiency. The LTC4013 accommodates a wide range of battery voltages from 2.4V to 60V. The device is aimed for high current charging applications. The upper limit is determined from efficiency (power loss) which is mostly limited by strength of gate drives, switch losses and current sense voltages. Major features include:

- Selectable charger profiles:
  - 2-stage charging: constant current to constant voltage with and without timeout.
  - 3-stage lead-acid charging: absorption, float with low battery restart and either charge current (C/10) or safety time termination.
  - 4-stage lead-acid charging: absorption, equalization, float with low battery restart and safety time termination.
  - Li-Ion constant current to constant voltage charging with either charge current (C/10) or safety time termination.
- User adjustable maximum power point tracking (MPPT) circuitry that allows simple power optimization for power limited sources such as solar panels. Includes improved high efficiency operation during MPPT operation.
- Continuous temperature adjustment of charge voltages (programmable).
- External input MOSFET (INFET) to prevent battery discharge with a shorted input.
- Maximum battery charge current programmable using an external sense resistor.
- DC/DC switching regulator frequency adjustable using external resistor and externally synchronizable.
- A precision ENAB pin that controls turn on with an external resistor divider.

Current control is maintained throughout the charge cycle by using an average current control scheme. The charger has an input voltage range of 4.5V to 60V. A resistor divider from the battery to FB adjusts the charge voltage with a practical range of 2.4V to 58V.

The LTC4013 also provides three monitor pins. STAT0 and STAT1 are open drain outputs that can drive an LED to provide visual indication of charge status and fault conditions. The ISMON pin provides analog information about charge current.

DC/DC OPERATION

(See Block Diagram)

The LTC4013 uses a fixed frequency, average current mode DC/DC converter architecture to regulate inductor current (and thus charge current) independent of battery voltage. The control loop will regulate current to an accuracy of ±5%. When the battery reaches the charge voltage, current is reduced by a voltage regulation loop. The charge voltage accuracy is ±0.5%.

Note a general switching regulator overview is found in Linear Technology application notes, AN-19 and AN-140.

The inductor current is sensed via the sense resistor placed between SENSE and BAT. The amplified signal is compared to a voltage that represents the maximum allowable charge current. The error amp regulates the average inductor current by controlling duty cycle on the output switches. A single frequency compensation point (ITH pin) is used to provide stability of the loop.

When the battery voltage is below the programmed charge voltage, the control loop servos the differential voltage between SENSE and BAT to 50mV. The charge current at 50mV is referred to as I_{CHGMAX}. When the battery voltage reaches the programmed charge voltage, error amplifier A3 continuously adjusts the average inductor current to servo the battery voltage to the programmed charge voltage. This error amplifier can reduce the battery current to zero, if necessary.

OPERATION

This control loop has additional features. At startup the maximum current is ramped over approximately 1.6ms to provide a soft start function. There is an additional burst mode feature used for maximum power point transfer as described below.

The charge voltage is determined by amplifier A5 and the charge algorithm. The voltage is made a continuous function of temperature by use of the NTC pin. The NTC pin controls a transconductance amp that linearly adjusts the charge regulation voltage. In normal operation a resistor divider with a bottom NTC resistor sets the temperature coefficient of the voltage. See the Temperature Compensation section for more details.

The switching regulator oscillator frequency is set by a resistor from the RT pin to ground. There is an option to synchronize the clock frequency to an external oscillator by using the SYNC pin.

The switching regulator uses external low $R_{DS(ON)}$ MOSFETs for both high and low side switches. It operates in synchronous step-down (Buck) mode at high currents. When the current level falls below $I_{CHGMAX}/10$ the bottom MOSFET is disabled and switching operation is discontinuous with the bottom side MOSFET body diode used for low side conduction. This insures the battery is not discharged.

Drive voltage for the top gate drive is generated by a boost circuit that uses an external diode and boost cap that is charged via the diode from $INTV_{CC}$. The bottom side MOSFET is disabled when current is below $I_{CHGMAX}/10$. If BST – SW is below 3.8V (e.g. at startup), the bottom side MOSFET is enabled to charge the BST cap.

Maximum Power Point Tracking

If the MPPT function is enabled (FBOC pin voltage < 3V) the LTC4013 employs a MPPT circuit that compares a stored open-circuit input voltage measurement against the instantaneous DCIN voltage while charging. The LTC4013 automatically reduces the charge current if the DCIN voltage falls below the user defined percentage of the open-circuit voltage. This algorithm lets the LTC4013 optimize power transfer for a variety of different input sources.

When MPPT is enabled the LTC4013 periodically measures the open-circuit input voltage. About once every 10.2s the LTC4013 pauses charging, samples the input voltage as measured through a resistor divider at the FBOC pin, and outputs this value via a digital to analog converter (DAC). When charging resumes, the DAC voltage, (VDAC) is compared against the MPPT pin voltage that is programmed with a resistor divider. If the MPPT voltage falls below VDAC, the charge current is reduced to regulate the input voltage at that level. This regulation loop maintains the input voltage at or above a user defined level that corresponds to the peak power available from the applied source. Input sampling is useful, for instance, for first order temperature compensation of a solar panel.

When charging resumes after the sampling period, the input voltage drops if the source cannot support the demanded charge current. When the input voltage drops to VDAC, the charge current is reduced to maintain DCIN at VDAC.

The sampling timing is fixed internally. Switching stops for approximately 1ms every 10.2s. There is an initial 720µs delay allowing the DCIN node to rise to its open circuit voltage. During the next 300µs, the FBOC pin voltage is sampled and stored. The ITH pin is high impedance during the sample period. The sampling of DCIN is done at an extremely low duty cycle so as to have minimum impact on the average charge current. Figure 1 shows a picture of MPPT timing.

Keep capacitance low on DCIN to ensure that DCIN achieves open circuit voltage during the initial MPPT delay. The time constant is set by the capacitor and the impedance of the input source.

OPERATION

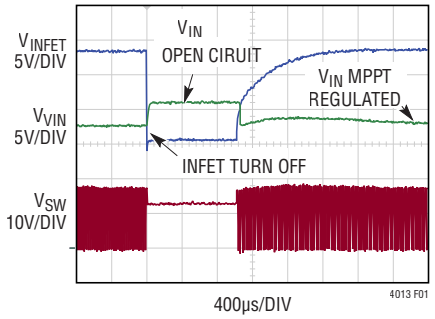


Fig 1. MPPT Timing

MPPT Burst Mode Operation

If input power levels drop during MPPT operation it is desirable to improve switching regulator efficiency in order to deliver the most power. The LTC4013 contains proprietary circuitry that improves overall switching regulator efficiency during these conditions. Efficiency is improved by reducing the maximum switching regulator current and disabling the switching regulator for part of the operation, producing a burst mode operation. Entrance to burst mode occurs when MPPT is below the sampled FBOC voltage by approximately 32mV and the current is below $I_{CHGMAX}/10$ (SENSE-BAT <5mV). The part stays in burst mode operation until the next sampling period when it is reevaluated. If, when resampled, MPPT is above the sampled FBOC voltage by approximately 31mv then burst mode is exited. The net result is that in burst mode the DCIN voltage has approximately a 63mV hysteretic ripple at the FBOC pin. During burst mode maximum current is set to approximately $I_{CHGMAX}/5$ (SENSE-BAT = 10mV).

ISMON Current Monitor

Sense resistor current is monitored via the ISMON pin. The ISMON voltage is $20 \bullet (V_{SENSE} - V_{BAT})$.

BATTERY CHARGER OPERATION

(See Block Diagram)

The battery charge voltage is regulated via the FB pin. The FB voltage regulation levels are appropriate for a single cell lead-acid battery. For instance a 2.267V single cell float voltage corresponds to a 6 cell battery voltage of $6 \bullet 2.267V = 13.6V$

The battery charge current is determined by the battery voltage. When the battery voltage is below the charge voltage, battery current is limited to the programmed charge current. As the battery voltage approaches the charge voltage current falls off to maintain the battery at the charge voltage.

In addition the LTC4013 contains a charge cycle timer that is used for time based control of a charge cycle. The timer is activated by connecting a capacitor from the TMR pin to ground. Grounding TMR disables all timer functions. This timer is used for absorption timeout in 3- and 4-stage lead-acid charging, equalization timeout in 4-stage lead-acid charging, and timeout in Li-Ion or constant current charging.

The LB pin provides a user adjustable voltage that is used to set the restart voltage in some modes and low battery fault in others.

Lead-Acid Battery Charger Basics

Lead-acid batteries can be charged in a number of ways. The simplest is a 2-stage method where a constant current is applied until the battery voltage reaches the float voltage. Float voltage is the electrochemical voltage generated by the cell under no charging or load. The disadvantages of this scheme is that it doesn't fully charge the battery and battery capacity drops over time. The battery capacity loss is because of the increase of deposits on the electrodes. In this mode maximum charge current is limited for safety and falls as the battery voltage approaches the charge voltage.

OPERATION

The most popular charging method is called 3-stage charging cycle (see Figure 2). In this method the battery is initially charged with a constant current (CC) until the battery voltage achieves the absorption voltage. This helps to increase the amount of stored charge in the battery. Because the voltage is above the electrochemical float level, the time that the battery stays in this condition is usually limited, either by a timer (the safest method) or just waiting for the charge current to diminish. After absorption is complete the charger voltage drops back to the float voltage. Minor gassing of water from the battery can occur from charging the battery above the float voltage, so choosing an appropriate absorption voltage is important for best battery life. Always consult the battery manufacturer for their recommendations.

A 4-stage charging algorithm adds an additional stage to the 3-stage method after absorption called equalization. Equalization voltage is significantly higher than the absorption voltage and works in two ways. One is to purposely introducing gassing which stirs the battery electrolyte and reduces electrolyte stratification. Equalization also electrochemically eliminates sulfates on the electrodes which is the main cause of battery performance degradation (sulfates form in heavily discharged batteries). Equalization is not done with sealed batteries because of the gassing. If loss of water is significant it degrades the battery if not replaced. In equalization the maximum current is reduced to approximately $I_{CHGMAX}/5$.

Equalization Cycle

Equalization should not be performed frequently and is always done with a timer to limit excessive battery stress. If MODE2 is high, then only one equalization cycle is initiated per power up without further user intervention.

Table 1 summarizes the various charging methods.

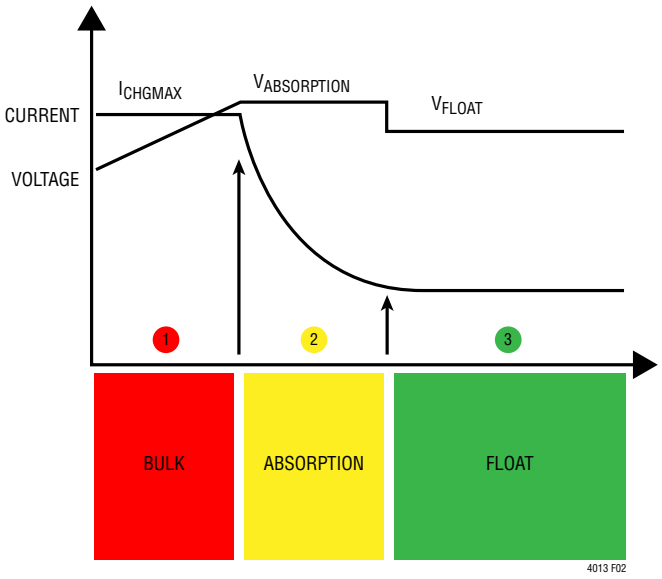


Figure 2. 3-Stage Charge Cycle

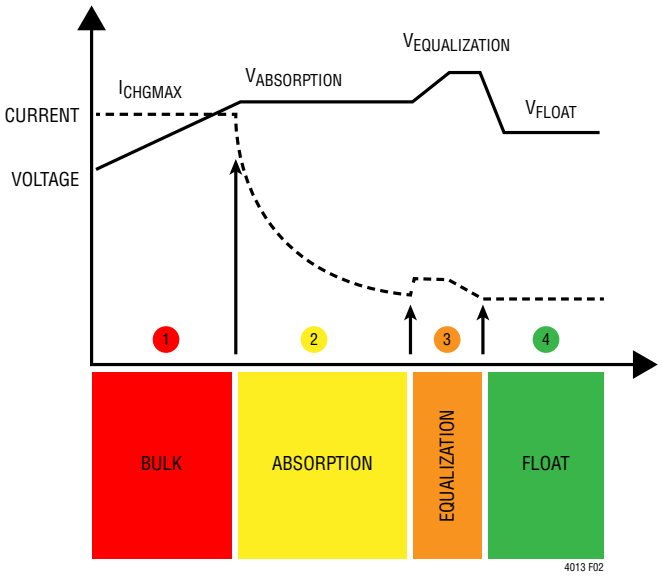


Figure 3. 4-Stage Charge Cycle

OPERATION

Table 1. Battery Charging Stages

Mode	Charge Algorithm	Duration and Additional Details
2-Stage Charging	Charge current is set to I_{CHGMAX}. Charge voltage is set to the float voltage	If no TMR cap, charger continual charges at float voltage. With the cap charging terminates after timeout. The timer starts after float voltage is reached
3-Stage Charging	Charge current is initially set to I_{CHGMAX}. Charge voltage is set to the absorption voltage	Terminates by either current reducing to $I_{CHGMAX}/10$ or timeout set by timer (TMR). Charge voltage is then changed to the float voltage
4-Stage Charging	Similar to 3-stage but at the end of the absorption cycle the charge voltage is increased to the equalization voltage and the maximum current is set at $I_{CHGMAX}/5$	Terminates by timeout set by timer (TMR). Charge voltage is then changed to the float voltage
Li-Ion	Charge at I_{CHGMAX} to the charge voltage. Charger turns off when either the charge current reduces to $I_{CHGMAX}/10$ or timeout set by TMR.	When charger turns off, charge voltage is then changed to the recharge voltage. When the battery voltage drops below this voltage, charging is reinitiated.
Low Battery Restart (all modes)	If FB voltage drops to recharge threshold the charge cycle is reinitiated. Maximum charge current is set to $I_{CHGMAX}/5$.	If the timer is active on 3,4-stage and Li-Ion then charging is terminated if below the low battery threshold for longer than $t_{EOC}/8$

Battery Charge Voltages

The LTC4013 allows for several different options for setting float, absorption and equalization voltages. In normal mode, single cell absorption is approximately 100mV above float (600mV for 6 cells), equalization is then approximately 133mV above absorption (800mV for 6 cells). Another option uses a wider voltage spread where single cell absorption voltage is 200mV above float (1.2V for 6 cells) and equalization is 200mV above absorption (1.2V for 6 cells). Absolute voltages are adjusted through the FB resistor divider to shift voltages up proportionately. It is important that you consult your battery manufacture for what they suggest for the charging voltages. There is no industry consensus and it depends heavily on the type of battery and anticipated usage.

Figure 4 shows how the FB resistor divider allows for the range of charge settings for the normal and wide spread voltage modes.

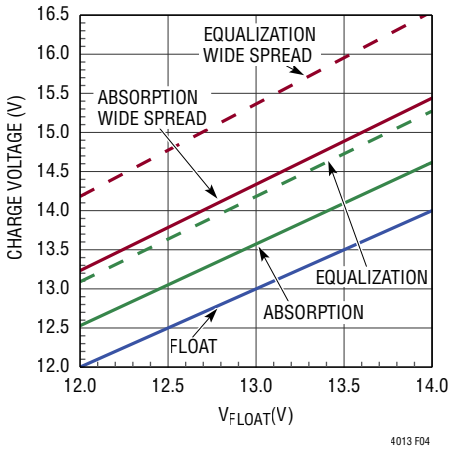


Figure 4. 6 Cell Lead-Acid Charge Voltages with R_{FB1}/R_{FB2} Change

Restart, Low Battery Pin

For lead-acid a normal charge cycle completes with the battery at the float voltage. A new cycle is initiated if the FB referred battery voltage drops below the voltage on the programmable LB pin. The user defines this voltage by setting the resistor from LB to ground. The LB pin sources 20µA. For instance 100k to ground sets the LB pin to 2.0V.

Note a commonly used low battery voltage for 6 cell lead-acid is 10.4V which represents the voltage with one of 6 cells shorted. This LB voltage is set with an 88.6k resistor for 1.73V, (10.4V/6) if you are using a 6-to-1 FB divider. Restart is disabled when using 2-stage charging with timeout (TMR pin active). When the FB voltage is below the LB voltage then maximum charge current is set to 20% of the programmed maximum current.

When the charge timer is active a low battery fault is signaled if the battery remains below the LB referred low battery voltage for 1/8 of the normal absorption end of charge time (t_{EOC}). The fault is indicated by STAT0 turning off and STAT1 turning on. Charging is also stopped.

OPERATION

Lead-Acid Battery Types

There is a wide variety of lead-acid batteries available for use. It is beyond the scope of this data sheet to detail all of them. There are numerous online resources and books available for further education. A good starting point is found at www.batteryuniversity.com. Many of the battery manufacturers also provide detailed information. The following sections outline the various charge modes in detail.

2-Stage Charging

2-stage charging is useful for lead-acid charging with no absorption preconditioning. It is also useful for other battery types (NiCd, NiMH) or supercapacitor charging. In this mode the LTC4013 charges with constant current (CC) (I_{CHGMAX}) until the battery reaches the programmed charge voltage. The charge current is reduced to maintain the battery at the charge float voltage.

When the TMR pin is used the charge cycle terminates after a fixed time period determined by the LTC4013 timer, so there is only a single charge cycle.

In 2-stage charging without the timer, the STAT1 pin indicates a change from constant current (CC) to constant voltage (CV). When the FB voltage rises to 16mV below $V_{FB(FL)}$, STAT1 pulls down indicating the CC to CV transition. The battery charger continues to provide current during the float charge phase and responds to any changes in load while maintaining the battery voltage at the programmed float charge voltage.

There are two different voltage settings for 2-stage charging as noted in Table 2.

If the timer is enabled (cap on TMR pin), the constant-current/constant-voltage algorithm is unchanged, but the timer starts counting when the battery voltage reaches the float voltage. At the end of the timeout period, t_{EOC}, charging stops. Charging is reinitiated only after the FB referred battery voltage drops below the restart voltage (set by the LB pin) or the part is powered off and back on (ENAB).

Low battery protection is enabled if the timer is activated. The charge cycle terminates if the battery voltage remains below the low battery voltage (set by the LB voltage) longer than 1/8 of the normal timeout period (t_{EOC}).

Table 2 shows the MODE pin settings and float voltage in this mode. L means the pin is grounded, H means the pin voltage is above 2.5V (tie to $INTV_{CC}$), M means the pin is midrange (leave unconnected).

Table 2. 2-Stage Charging Settings

2-Stage	Settings			V_{FLOAT}
Termination	MODE1	MODE2	TMR	WRT V_{FB}
No Termination	L	L	0V	2.267V
	L	M	0V	2.332V
Timeout	L	L	Cap	2.267V
	L	M	Cap	2.332V

Note: For nickel-chemistry batteries (e.g. NiCd or NiMH), the possibility of overcharging must be considered. A typical method is to charge with low currents for a long period of time. NiCd and NiMH batteries can absorb a C/300 charge rate indefinitely. Shorter duration charging is possible using a timed current source charge algorithm. It is recommended to ensure a depleted battery before charging, and then subsequently charge the battery to no more than 125% capacity. For example, a depleted 2000mAh NiMH battery is charged with 2.5A for one hour.

3- and 4-Stage Charging

A more common lead-acid battery charging method is 3-stage (absorption) or 4-stage (absorption and equalization) charging as discussed above. Equalization always uses a timer and there is an option to have the equalization timeout be 1/8 or 1/4 of the normal absorption timeout period.

For the 3-stage cycle, charging is initiated on power up or when the battery drops below the LB restart voltage. The battery then charges toward the absorption voltage. As the battery voltage approaches absorption the current falls. When it reaches I_{CHGMAX}/10, STAT1 turns on. When the battery voltage reaches CV (approximately 16mV from the FB referred absorption voltage) the internal charge voltage changes to the float voltage. The charging

OPERATION

remains active at the float voltage. If the battery voltage (FB referred) subsequently drops below the LB pin or the part is powered off and back on (ENAB) a new 3-stage charge cycle is initiated.

Timeout is added to the 3-stage cycle by placing a capacitor on TMR. With timeout, when the voltage then reaches CV (16mV from the absorption voltage) the timer starts and the charge voltage remains at absorption for the set timer period. At the end of that time period the charge voltage changes to the float voltage. The charging remains active at the float voltage.

There are options for different absorption and float voltages. Table 3 details the MODE pins settings and FB voltages. Figure 4 shows a graph that indicates the relationship between float and absorption voltages for a 6 cell battery.

Table 3. 3-Stage Mode Settings

3-Stage	Settings			V_{FLOAT}	V_{ABS}
Absorption to Float	MODE1	MODE2	TMR	WRT V_{FB}	WRT V_{FB}
100mV	H	L	0V	2.267V	2.367V
100mV + Timeout	H	L	Cap		
200mV	M	L	0V	2.200V	2.400V
200mV + Timeout	M	L	Cap		

4-Stage Cycle

The 4-stage cycle is similar to the 3-stage cycle. However at the end of absorption charging the charge voltage is increased to the equalization voltage. The 4-stage cycle always requires the use of the timer (cap on TMR) as a safety precaution to insure that charging time at the high equalization voltage is limited. If the TMR pin is grounded inadvertently the charge cycle will revert to 3-stage. Not all batteries can be charged with a 4-stage cycle so you must consult with your battery manufacturer as to its use and recommended charge voltage.

Charging is initiated when the part is enabled. The battery then starts charging toward the absorption voltage. As the battery voltage approaches the absorption voltage the current falls. When the voltage then reaches CV (16mV from the absorption voltage) the timer starts and the charge voltage remains at absorption for the set timer period. At the end of the timer period the internal charge voltage changes to the equalization voltage. The timer is immediately restarted and charging at $I_{CHGMAX}/5$ occurs with the equalization voltage until the end of equalization timeout, either 1/4 or 1/8 of the absorption timeout period, t_{EOC}. After equalization timeout the charge voltage is reduced to the float voltage. At the end of equalization STAT1 turns on (STAT0 is already on).

The charging remains active at the float voltage and charging responds to battery load. If the battery voltage (FB referred) subsequently drops below the LB pin or the part is powered off and back on (ENAB) a new charge cycle is initiated. Only one equalization cycle is allowed per power on cycle. A full 4-stage cycle can be restarted by cycling the part with the ENAB pin.

Figure 4 shows a graph that indicates the relationship between float, absorption and equalization voltages for a 6 cell battery as the FB resistor divider is changed.

Table 4. 4-Stage Mode Settings

4-Stage (Requires Timer)		Settings			V_{FLOAT}	V_{ABS}	V_{EQ}
Absorption to Float	Timeout	MODE1	MODE2	TMR	WRT V_{FB}	WRT V_{FB}	WRT V_{FB}
100mV	1/4 t_{EOC}	L	H	Cap	2.267V	2.367V	2.500V
	1/8 t_{EOC}	H	H	Cap			
200mV	1/8 t_{EOC}	M	H	Cap	2.200V	2.400V	2.600V

OPERATION

Charging with a Battery Load

Typically, maintaining a battery at float voltage requires little charge current. However, when the LTC4013 is in a float charging state it maintains the capability to increase current to the full charge current in the event there is load on the battery. If the load on the battery does not exceed this current then battery voltage is maintained. If the battery load exceeds the constant current, the battery supplies the difference and is discharged. At the low battery threshold a new charge cycle is initiated but still only at the full charge current so reducing the load is required for charging to occur.

Li-Ion Charging

The LTC4013 can charge higher capacity Li-Ion batteries (including Li-Polymer, and $LiFePO_4$). A resistor divider from the battery to FB sets the desired charge voltage. The Li-Ion charge algorithm charges the battery at I_{CHGMAX} to the charge voltage. When the charge current drops to $I_{CHGMAX}/10$ or the timer times out (timer active), the charger turns off and the charge voltage drops to the lower recharge voltage. When the battery voltage drops below this recharge level, charging is reinitiated. Table 5 shows MODE pin settings for Li-Ion charging.

In this mode, after charge termination a new charge cycle occurs at the recharge voltage. The recharge voltage is 97.0% or 95.6% of the charge voltage depending on MODE state. The wider difference is useful for $LiFePO_4$ batteries to avoid constant recharge events. The shift to recharge can occur with and without timeout.

STAT1 turns on sinking current at charge termination. Without a timer (TMR = 0V) this happens when the charge current drops to $I_{CHGMAX}/10$. If the timer is active (capacitor on TMR) timeout starts when the FB voltage reaches approximately 16mV from $V_{FB(CHG)}$. Termination is then indicated after the end of charge termination time (t_{EOC}).

Status Pins

As previously mentioned there are 2 status pins that indicate charger status. Table 6 details that information. On implies that the STAT0/1 pin is actively pulled down. Off implies the STAT0/1 pins are open circuit.

INFET Behavior

The LTC4013 supports an input MOSFET that provides a blocking path to prevent discharging the battery if the input voltage is below the battery voltage. Secondly it allows the input to be disconnected from the charger so that measurement of the input voltage is done with no load. This measurement is used in conjunction with the Maximum Power Point Tracking (MPPT) function to determine the optimal set point for that function.

Table 5. Li-Ion Charge Settings

	Settings		V_{CHG}	V_{RECHRG}				
% Recharge	MODE1	MODE2	WRT V_{FB}	WRT V_{FB}	3.6V V_{CHG}	3.8V V_{CHG}	4.1V V_{CHG}	4.2V V_{CHG}
97.0%	H	M	2.367V	2.295V	3.490V	3.684V	3.975V	4.072V
95.6%	M	M	2.400V	2.295V	3.443V	3.634V	3.921V	4.016V

OPERATION

Table 6. Status Pin Indications

STAT0	STAT1	CHARGING MODE
Off	**Off**	Not Charging in Standby or Shutdown
On	**Off**	Battery Charge Cycle Active Termination Not Achieved
On	**On**	Charge Cycle Complete Charge Voltage Set to $V_{FB(FL)}$ or for Li-Ion $V_{FB(RECHG)}$
Off	**On**	Bad Battery or Over Temp Fault

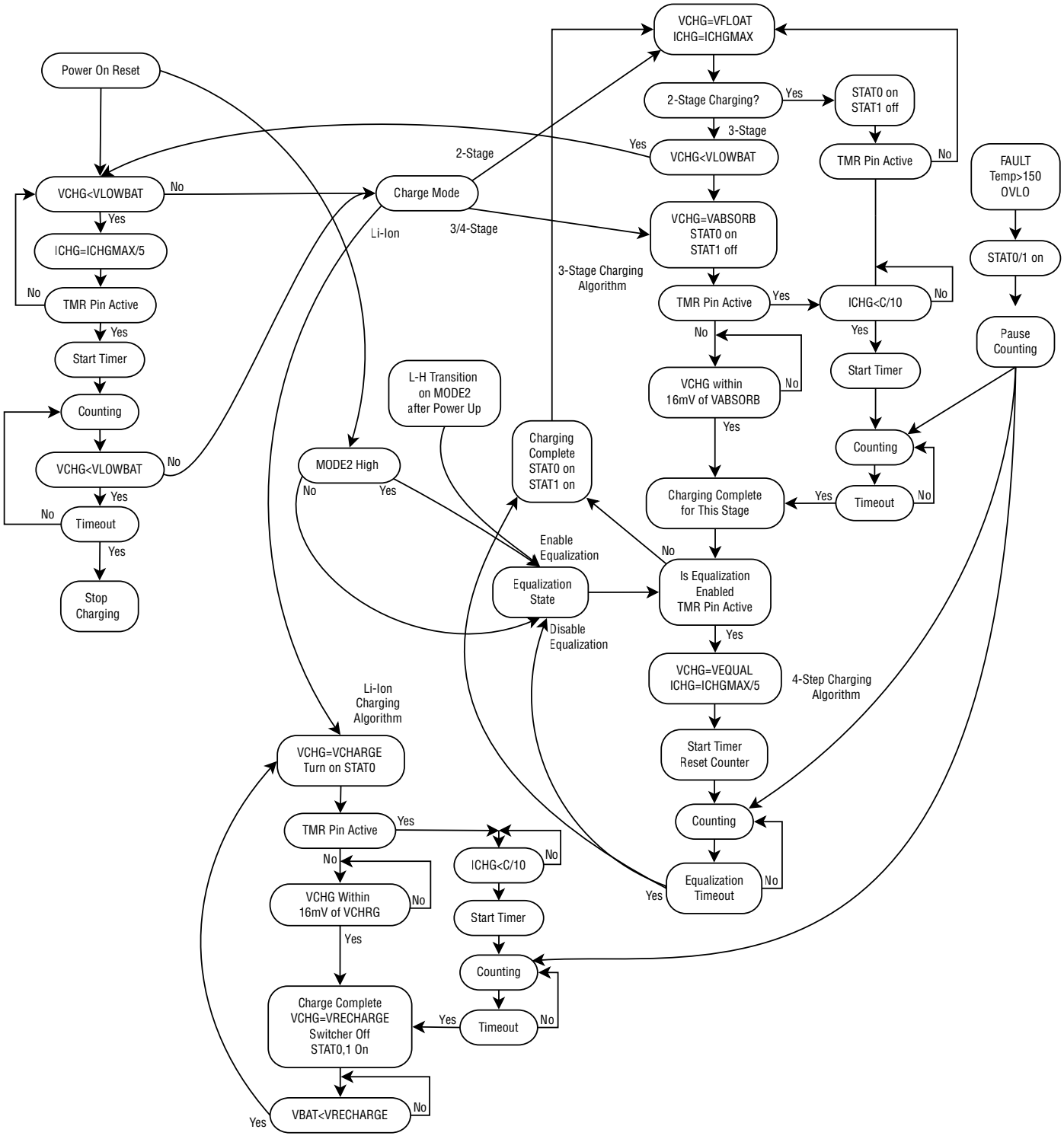
The input MOSFET(s) are controlled via the INFET pin which is connected to the MOSFET gate. The input MOSFETs are turned on with an on chip charge pump sourced through INFET. The charge pump is activated when the part is enabled via the ENAB pin.

The INFET MOSFETs are not allowed to turn on unless DCIN can support charging of the battery. This is accomplished by two comparators, one looks to ensure that DCIN is larger than BAT and the other looks to see if DCIN is greater than V_{IN}. The DCIN to BAT comparator also ensures that the battery is not discharged when DCIN is below BAT. Specifically the comparators check that DCIN is approximately 99mV above BAT and that DCIN is larger than 4mV below V_{IN}. The slight negative voltage on the later helps to reduce ringing when INFET is turned off.

When ENAB and the comparators allow, both the PowerPath and the switching regulator are enabled. If any condition is not met then the input MOSFETs are turned off and the switching regulator disabled. Turn off occurs by INFET sinking current and pulling the INFET voltage to approximately 1.8V below the lower voltage of DCIN or V_{IN}.

The input PowerPath MOSFETs are also turned off when measuring the no load open circuit input voltage when using the MPPT function.

BATTERY CHARGER FLOW CHART



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SWITCHING REGULATOR

Setting Maximum Charge Current

Maximum charge current, I_{CHGMAX}, is determined by the sense resistor. The maximum SENSE – BAT voltage for normal operation is 50mV. The maximum charge current is $50mV/R_{SENSE}$. So for instance if you want a 10A maximum then R_{SENSE} is set to 5mΩ. Accuracy requires the use of 4 terminal sense resistors or careful attention to insure a solid Kelvin connection to the sense resistor. Fig 17 shows examples. Remember to size the resistor for power dissipation with $P_{RSENSE} = I_{CHGMAX} \bullet 50mV$. As an example for the above 10A charger the sense resistor needs to be rated greater than 0.5W. Susumu, Panasonic and Vishay offer a wide variety of accurate sense resistors.

Resistance associated with board traces can add up quickly (2oz copper is approximately 0.24mΩ /square). Review trace width for all high current paths.

Inductor Selection

Size the inductor so that the peak-to-peak ripple current is approximately 30% of the maximum charging current. This is a reasonable tradeoff between inductor size and ripple. Inductance can be computed with the following equation:

$$L = \frac{V_{IN} \bullet V_{BAT} - V_{BAT}^2}{0.3 \bullet f_{SW} \bullet I_{CHGMAX} \bullet V_{IN}}$$

where V_{BAT} is the battery voltage, V_{IN} is the input voltage, I_{CHGMAX} is the maximum charge current in the inductor and f_{SW} is the switching frequency. Choose the saturation current for the inductor to be at least 20% higher than the maximum charge current.

There is an overcurrent comparator which terminates switching when the voltage between the SENSE and BAT pins exceeds 100mV to protect against faults. When tripped switching is stopped for 4 switch cycles.

Switching Regulator MOSFET Selection

MOSFET selection is done with the goal of giving the best efficiency and lowest cost. The key parameters are: total gate charge (QG), on-resistance ($R_{DS(ON)}$), gate to drain charge (Q_{GD}), gate-to-source charge (Q_{GS}), gate resistance (R_G), breakdown voltages (maximum V_{GS} and V_{DS}) and drain current (maximum ID). The following guidelines provide information to make the selection process easier, and Table 7 lists some recommended manufacturers.

The rated drain current for both MOSFETs must be greater than the maximum inductor current. Peak inductor current is approximately:

$$I_{LMAX} = I_{CHGMAX} + \frac{V_{IN} \bullet V_{BAT} - V_{BAT}^2}{2 \bullet f_{SW} \bullet L \bullet V_{IN}}$$

The rated drain current is temperature dependent, and most data sheets include a table or graph of the rated drain current versus temperature.

The rated V_{DS} must be higher than the maximum input voltage (including transients) for both MOSFETs. As for the rated VGS, the signals driving the gates of the switching MOSFETs have a maximum voltage of 5V ($INTV_{CC}$) with respect to the source. However, during start-up and recovery conditions, the gate drive signals may be as low as 3V. Therefore, to ensure that the LTC4013 recovers properly, use logic level threshold MOSFETs with V_T less than 2V. For a robust design, ensure that the rated VGS is greater than 7V.

Power losses in the switching MOSFETs are related to the on-resistance, $R_{DS(ON)}$; gate resistance, R_G; gate-to-drain charge, Q_{GD} and gate-to-source charge, Q_{GS}. Power lost to the on-resistance is an Ohmic loss, $I^2R_{DS(ON)}$, and usually dominates for input voltages less than 15V. Power lost while charging the gate capacitance typically dominates for voltages greater than 15V. When operating at higher input voltages, efficiency is optimized by selecting a high side MOSFET with higher $R_{DS(ON)}$ and lower Q_G. The total power loss in the high side MOSFET is approximated by the sum of Ohmic losses and transition losses:

$$P_{HIGH\_LOSS} = \frac{V_{BAT}}{V_{IN}} \bullet I_L^2 \bullet R_{DS(ON)} \bullet \rho_T +$$

$$\frac{V_{IN} \bullet I_L}{5V} \bullet (Q_{GD} + Q_{GS}) \bullet (2 \bullet R_G + R_{PU} + R_{PD}) \bullet f_{SW}$$

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I_L is the current in the inductor. ρ_T is a dimensionless temperature dependent factor in the MOSFET's on-resistance. Using 70°C as the maximum ambient operating temperature, ρ_T is roughly equal to 1.3. R_{PD} and R_{PU} are the LTC4013 high side gate driver output impedances: 2.3Ω and 1.3Ω, respectively.

For the low side MOSFET the power loss is approximated by.

$$P_{LOW\_LOSS} = \left(1 - \frac{V_{BAT}}{V_{IN}}\right) \bullet I_L^2 \bullet R_{DS(ON)} \bullet \rho_T +$$

$$\frac{V_{IN} \bullet I_L}{5V} \bullet (Q_{GD} + Q_{GS}) \bullet (2 \bullet R_G + R_{PU} + R_{PD}) \bullet f_{SW}$$

$$+ V_f \bullet 2 \bullet f_{SW} \bullet I_L \bullet tnol$$

Where V_f is the voltage drop of the lower MOSFET bulk diode, typically 0.7V; tnol is the non-overlap time when neither top or bottom gate is on, approximately 50ns. This last term represents the loss due to the bulk diode that is active during the non-overlap time.

In addition to the above, it is desirable that the bottom MOSFET has reduced G-D capacitance as it minimizes problems when the top side switch turns on. Coupling through this capacitance during top side turn on creates a capacitor divider with the bottom MOSFET G-S capacitance. It is possible to momentarily turn on the bottom side MOSFET creating a possible shoot through condition, that at best reduces efficiency, and at worse can destroy the MOSFET.

Consideration must also be given for power dissipation in each MOSFET. While it is possible to get high and low side MOSFETs bonded in a common package, power dissipation concerns may suggest that two separate packages or even multiple high or low side MOSFETS be used to spread the heat over a larger PCB area to improve overall board temperature and efficiency. This is more important at the high power levels associated with higher current and higher voltages.

At lower V_{IN}, the top side is on longer and low $R_{DS(ON)}$ helps lower dissipation but as you go up in voltage the transient losses increase and in fact can dominate. For the bottom side MOSFET the opposite is true. Optimization for best efficiency suggests different top and bottom MOSFETs.

A good approach to MOSFET sizing is to select a high side MOSFET, then select the low side MOSFET. The trade-off between $R_{DS(ON)}$, Q_G, and Q_{GS} for the high side MOSFET is evident in the following example. As an example, charging a 6 cell lead-acid from a 30V source at 20A. V_{BAT} is equal to 14V, f_{SW} = 200kHz.

Starting with two N-channel MOSFETs rated for a V_{DS} of 40V. We start with a BSC018N04LS on the top side with a $R_{DS(ON)}$ of 2.5mΩ at 4.5V, Q_G = 60nC, Q_{GS} = 25nC, Q_{GD} =10nC, RG = 1.3Ω. The bottom side is a BSC093N04LS has a $R_{DS(ON)}$ of 11.0mΩ at 4.5V, Q_G = 8.6nC, Q_{GS} = 4.9nC, Q_{GD} = 2nC, R_G = 1.0Ω. Power loss for the MOSFETs is shown in Figures 5 and 6. Observe that the total power loss at 30V is just over 5W for the top side and about 3.5W for the bottom side.

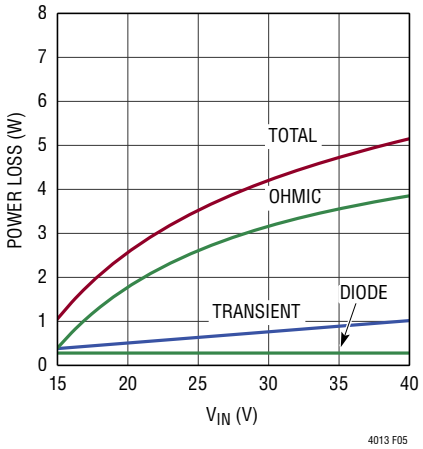

Figure 5. Top MOSFET Power Loss Example

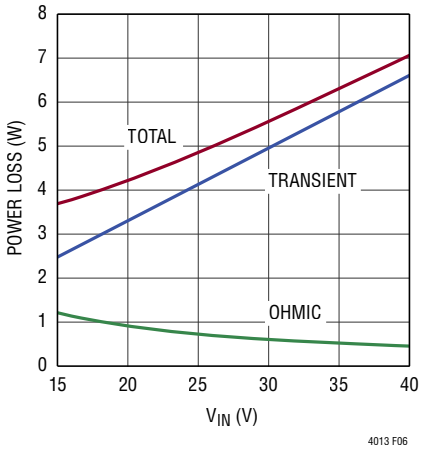

Figure 6. Bottom MOSFET Power Loss Example

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Of course MOSFET choices need to be examined. Normally $R_{DS(ON)}$ and Q_G are inversely related so perhaps finding a top side MOSFET with higher $R_{DS(ON)}$ and lower Q_G might lower top side losses. Conversely the bottom side MOSFET is dominated by ohmic losses so perhaps a larger MOSFET would be better. But of course we also need to watch total Q_{GD} on the bottom side so that presents a limit.

Supplying gate charge current has its own loss most of which is dissipated from the internal LDO and represents a potential limitation at higher voltages. The power dissipated in the IC is: $P_{LDO} = (V_{IN}-5) \times (Q_{GL}+Q_{GH}) \times f_{SW}$ where Q_{GL} is the low side gate charge and Q_{GH} is the high side gate charge.

The $INTV_{CC}$ supply has limitations on the maximum current as well. Figure 7 shows the curve of maximum gate charge current vs V_{IN} for a power loss of 0.5W. This power level would add 22°C of temperature to the die at 43°C/W thermal resistance. Dividing the Y axis value (mA) by f_{SW}(MHz) gives the maximum Q_G (nC) that can be charged (the sum of top and bottom gates.) For instance at 30V and 500kHz Q_G is under 20(mA)/0.5(MHz) = 40(nC).

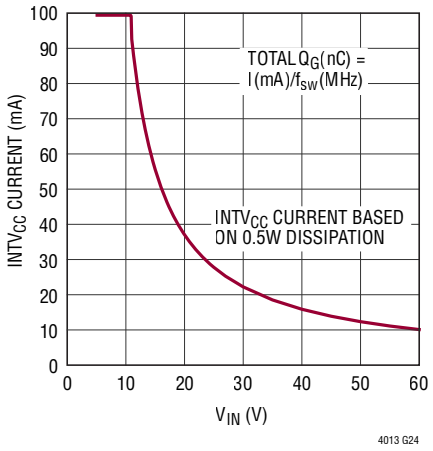

Figure 7. Maximum $INTV_{CC}$ current

If desired operation places the internal 5V regulator out of the allowable region, deriving gate drive power externally is required. This could be done by carefully driving the $INTV_{CC}$ with tight regulation (do not exceed the 6V absmax) or by supplying 5V power for the BST drive (top gate Q_G).

There are many power MOSFET manufacturers that make devices appropriate for this application. Some are listed in Table 7.

Table 7. Suggested MOSFET Suppliers

Manufacturer	Web Site
Infineon	www.infineon.com
Renesas	www.renesas.com
Fairchild	www.fairchildsemi.com
Vishay	www.vishay.com
NXP/Philips	www.nxp.com

Input Supply Capacitor Selection

DCIN provides power to the charge pump and is used for input voltage sensing so high quality capacitance is required on this node. Since most of the switching regulator transients are handled by the V_{IN} capacitor, a smaller capacitor on DCIN is adequate. It primarily needs to handle filtering input voltage when the INFET is off. We recommend starting with a 4.7µF high quality ceramic capacitor.

The LTC4013 receives power from DCIN through the input MOSFET to V_{IN}. V_{IN} then provides power to the switching regulator. This supply provides large currents with fast switching edges, so a high quality, low ESR, low ESL decoupling capacitors are required to minimize voltage glitches on the V_{IN} supply.

The V_{IN} supply decoupling capacitor (C_{VIN}) is intended to absorb the input switching ripple current in the charger, so it must have an adequate ripple current rating.

RMS ripple current ($I_{VIN(RMS)}$) follows the relation:

$$I_{VIN(RMS)} \approx I_{CHGMAX} \bullet DC \bullet \sqrt{\frac{1}{DC} - 1}$$

which has a maximum at DC = 0.5, or $V_{IN} = 2 \bullet V_{OUT}$, where:

$$I_{VIN(RMS)} \approx \frac{I_{CHGMAX}}{2}$$

where I_{CHGMAX} is the maximum charge current is set by R_{SENSE}. The simple worst-case equation is commonly used for design.

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The input capacitance C_{IN} is determined by the desired input ripple voltage (ΔV_{IN}). For step-down operation:

$$C_{IN} \geq \frac{I_{CHGMAX}}{\Delta V_{IN} \bullet f_{SW}} \bullet \frac{V_{BAT(MAX)}}{V_{IN(MIN)}}$$

where f_{SW} is the operating frequency, $V_{BAT(MAX)}$ is the DC/DC converter maximum output voltage and $V_{IN(MIN)}$ is the minimum input operating voltage. Keeping ΔV_{IN} below 100mV is a good starting point. As an example say I_{CHGMAX} = 10A, ΔV_{IN} = 0.1V, f_{SW} = 500k, $V_{BAT(MAX)}$=15V, $V_{IN(MIN)}$ = 18V then C_{IN} is greater than 167µF

At higher voltages meeting all of these requirements probably requires multiple capacitors and perhaps a mixture of cap types. Because of the fast switching edges it is important that the total decoupling capacitance has low ESR and ESL components because they generate sharp voltage spikes. Best practice is to use several low ESR ceramic capacitors as part of the capacitance, with higher density capacitors utilized for bulk requirements. X5R or X7R capacitors maintain their capacitance over a wide range of operating voltages and temperatures. Minimize the loop created by the input capacitor, high side MOSFET, low side MOSFET to reduce radiation components. See Linear application notes AN139 and AN144 for more information on EMI.

Battery Capacitor Selection

The output of the charger is the battery, which represents a large effective capacitance. Because the battery often has significant wiring connecting it to the charger additional decoupling output capacitors at the charger are needed. The BAT node is also used for voltage sensing so better performance is obtained with lower voltage ripple at the BAT and FB pins. The capacitors need to have low ESR to reduce output ripple. To achieve the lowest possible ESR, use several low ESR ceramic capacitors in parallel. Lower output voltage applications may benefit from the use of high density POSCAP capacitors, which are easily destroyed when exposed to overvoltage conditions. To prevent this, select POSCAP capacitors that have a voltage rating that are at least 50% higher than the regulated voltage.

The ripple current on these capacitors is the same as the inductor ripple. Since in general inductor selection is made to have ripple current equal or below 30% of I_{CHGMAX} rating, the BAT capacitors for 40% • I_{CHGMAX} is adequate. The capacitors also need to be surge rated to the maximum output current.

Sizing for output ripple voltage is similar to input decoupling:

$$C_{BAT} \geq \frac{0.4 \bullet I_{CHGMAX}}{\Delta V_{BAT} \bullet f_{SW}}$$

For example if I_{CHGMAX} = 10A, ΔV_{BAT} = 0.1V, f_{SW} = 500k then choose C_{BAT} greater than 80µF.

$INTV_{CC}$ LDO Output, and BST Supply

$INTV_{CC}$ provides power to the IC but also serves to provide charge to the gate drives. The boosted supply pin allows the use of N channel top MOSFET switches for increased conversion efficiency and lower cost. The BST cap is connected from the SW to BST with a low leakage 1A Schottky diode connected from $INTV_{CC}$ and BST. The diode must be rated for a reverse voltage greater than the input supply voltage maximum.

C_{BST} is sized to hold the BST rail reasonably constant when delivering gate charge to the to MOSFET. A good rule of thumb is:

$$C_{BST} > 50 \bullet \frac{Q_{GH}}{V_{GS}} = 10 \bullet Q_{GH}$$

where Q_{GH} is the top side MOSFET Q_G at 5V.

So as an example say that the top gate charge is 20nC, being charged to the $INTV_{CC}$ voltage of 5V then keep the C_{BST} capacitance larger than 0.2µF.

The C_{BST} is charged during the bottom switch on time. The LTC4013 maintains a minimum top gate off time to provide this charge. If the LTC4013 is in discontinuous mode with the bottom switch off and boost voltage drops, the bottom side switch is enabled to provide BST charging.

Since BST cap charge current is drawn from the $INTV_{CC}$ capacitor, that cap needs to be sized to have minimal drop during recharge. A good starting point for high current switching MOSFETs with high gate charge is to set C_{INTVCC} larger than 4.7µF. Connect it as close as possible to the exposed pad underneath the package. Because of the fast

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high current edges use low ESR ceramic, with ESR typically lower than 20mΩ. For driving MOSFETs with gate charges larger than 44nC, size $INTV_{CC}$ with 0.5µF/nC of total gate charge (top and bottom MOSFETs).

Enable

The part has an ENAB pin that allows the part to be enabled when the input voltage reaches a certain threshold. Normally a resistor divider is used from DCIN to ENAB (see Figure 8). The turn on threshold at ENAB is approximately 1.22V (rising), with 170mV of hysteresis. When in shutdown, all charging functions are disabled and input supply current is reduced to around 40µA.

Typical ENAB pin input bias current is 10nA which needs to be accounted for when using high value resistors. So choose R_{EN1} and then:

$$R_{EN2} = R_{EN1} \bullet \left(\frac{V_{ENAB}}{1.22} - 1 \right)$$

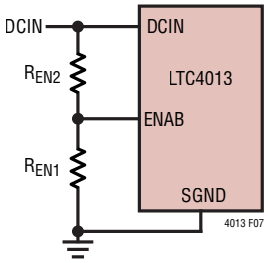

Figure 8. ENAB Resistor Divider

Starting the charger requires that the LTC4013 is enabled, and the DCIN voltage is greater than V_{IN} by about 4mV. DCIN also needs to be greater than V_{BAT} by about 100mV.

Programming Switching Frequency

The LTC4013 has an operational switching frequency range between 200kHz and 1MHz. This frequency is programmed with an external resistor from the RT pin to ground. Do not leave this pin open under any condition. The RT pin is also current-limited to 60µA. See Table 8 for resistor values and the corresponding switching frequencies. An approximate formula is:

$$R_T(k\Omega) = \frac{40.2}{f_{SW}^{1.088}\ (MHz)}$$

Table 8: R_T Resistor Value

Switching Frequency	R_T (Ω)
1MHz	40.2k
750kHz	54.9k
500kHz	86.6k
300kHz	150k
200kHz	232k

Switching Frequency Synchronization

As detailed above the switching frequency of the LTC4013 is set from 200kHz to 1MHz using an R_T resistor. The internal oscillator may also be synchronized to an external clock through the SYNC pin. An external clock applied to the SYNC pin must have a logic low below 1.3V and a logic high above 1.7V. The input sync frequency must be 20% higher than the frequency that would otherwise be determined by the resistor at the RT pin. Input signals outside of these specified parameters cause erratic switching behavior and sub harmonic oscillations. When synchronizing to an external clock, please be aware that there is a fixed delay from the input clock edge to the edge of the signal at the SW pin. Ground the SYNC pin if synchronization to an external clock is not required. When SYNC is grounded, the switching frequency is determined by the resistor R_T.

CLKOUT

Often synchronization is done with an externally generated clock signal. As part of the synchronization capability, a pulse stream is generated on CLKOUT that can be used as the SYNC input to another LTC4013 and produce switching that is approximately 180° out of phase. This allows two LTC4013s to be operated in parallel in a manner that would reduce input current ripple (and thus capacitance).

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Output Current Monitoring

The LTC4013 ISMON pin allows users the capability to monitor the output current as a voltage. The voltage increases linearly from 0V to 1V as the voltage between SENSE and BAT increases from 0mV to 50mV (voltage gain of about 20). The bandwidth on the amplifier is sufficient so that if you want average current you need to filter the ISMON output with a simple RC filter. A 100k resistor from ISMON to a 200pF capacitor to ground is usually sufficient.

Average Current Mode Control Compensation

The LTC4013 uses average current mode control for precise regulation of the inductor/charge current. Figure 9 shows an overview of the control loop. The current is measured via the sense amp and compared against the target value. The error amp with compensation components R_C and C_C sets the duty cycle that controls the inductor current.

A separate voltage amp modulates the maximum current as the battery voltage approaches the charge voltage level, reducing the maximum current.

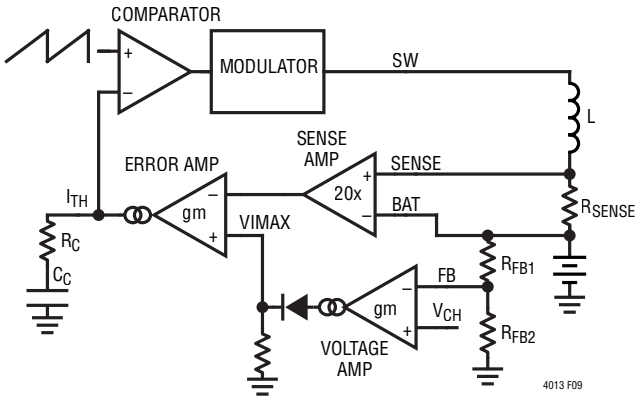

Figure 9. Switching Regulator Control Loop

To design the compensation network, the maximum compensation resistor needs to be calculated. In current mode controllers, the ratio of the sensed inductor current ramp to the slope compensation ramp determines the stability of the current regulation loop above 50% duty cycle. In the same way, average current mode controllers require the slope of the error voltage to not exceed the PWM ramp slope during the switch off time. Since the closed loop gain at the switching frequency produces the error signal slope, the output impedance of the error amplifier is the compensation resistor, R_C. Use the following equation as a good starting point for compensation component sizing:

$$R_C\,(k\Omega) = \frac{L(\mu H) \bullet f_{SW}(kHz)}{V_{BAT}(V) \bullet R_{SENSE}(m\Omega)}$$

$$C_C(nF) = \frac{2000}{f_{SW}(kHz)}$$

where f_{SW} is the switching frequency, L is the inductance value, V_{BAT} is the battery voltage and R_{SENSE} is the sense resistor. C_C is inversely proportion to f_{SW} so lower switching frequencies will need higher C_C. R_C is linearly dependent to inductance, for higher inductance R_C is higher.

An example: DCIN = 24V, V_{BAT} = 14V I_{CHGMAX} = 10A, R_{SENSE} = 5mΩ, f_{SW} = 500kHz, L = 3.6µH then C_C = 4nF, R_C = 25.7kΩ. Of course check stability on the actual physical circuit.

In some circumstances an additional capacitor from I_{TH} to ground is helpful. The capacitance is usually 0.01 to 0.1 times C_C.

Thermal Shutdown

The internal thermal shutdown within the LTC4013 engages at approximately 160°C and disables switching. When the part has cooled to 150°C, the part resumes charging. This feature is not tested but guaranteed by design. Thermal shutdown protects the device from excessive gate drive power and excess internal LDO dissipation but does not protect from excess power dissipation in the external MOSFETS or other external components. Battery over temperature is handled via the use of the external NTC resistor and the NTC function as described below, but does not shutdown the part.

BATTERY CHARGER SECTION

Battery Charge Voltage Programming

The Battery Charger Operation section details how to set the mode switches for the desired charging algorithm. Further tweaking of voltages is done through the resistor divider between the BAT and FB pins as shown in Figure 10.

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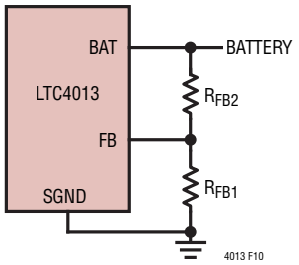

Figure 10. Battery FB Resistor Divider

By way of example consider a 4-stage cycle with MODE1 low and MODE2 high. The associated voltages are shown in Table 9. The first row shows the FB referred voltages.

Table 9. Charge Voltage Examples

	V_{FLOAT}	$V_{ABSORPTION}$	$V_{EQUALIZATION}$
FB	2.267	2.367	2.500
6x	13.6	14.2	15.0
6.043x	13.7	14.3	15.1
6.084x	13.8	14.4	15.2

Generating the divider requires finding resistors that give as close to correct ratio as possible. If we use standard value 1% resistors this may require a bit of searching. For instance, R_{FB1} = 46.4k and R_{FB2} = 232k programs the 6x case with less than 0.015% error for the charge votages shown in Table 9. If more than two resistors are used series and parallel combinations can make it easier. A tool that might help is found at http://reaylabs.com/tools/VoltageRegulator.html

But lets say we want a slightly different float voltage, say 13.7V. Then the divider would be set with:

$$R_{FB2} = R_{FB1} \bullet \left(\frac{V_{FLOAT}}{2.267} - 1 \right) = R_{FB1} \bullet \left(\frac{13.7}{2.267} - 1 \right)$$

$$= R_{FB1} \bullet (6.043 - 1)$$

Absorption and equalization voltages would scale accordingly as shown in the 3rd row of Table 9.

If you are more concerned about obtaining a certain absorption or equalization voltage then the resistor divider would be set based on that ratio. If for instance you want the absorption voltage to be 14.4 then you would use:

$$R_{FB2} = R_{FB1} \bullet \left(\frac{V_{ABS}}{2.367} - 1 \right) = R_{FB1} \bullet \left(\frac{14.4}{2.367} - 1 \right)$$

$$= R_{FB1} \bullet (6.084 - 1)$$

The associated voltages are shown in the 4th row of Table 9.

The MODE pins provide additional options for different charge voltage spreads which may better fit the battery recommendations.

Low Battery Voltage Setting

As described earlier the LB pin provides the user a way to set when low battery conditions occur. The LB pin sources approximately 20µA so placing a resistor from LB to ground generates the LB voltage. Low battery is determined relative to the FB voltage pin. So for instance say we are charging a 6 cell lead acid battery and we want to set the low battery voltage to 10.6V (1.77 V, FB referred). Set the LB resistor to 1.77V/20µA = 88.5k (88.7k is closest 1% value).

Charge Voltage Temperature Compensation

As mentioned the LTC4013 uses a charge voltage method that can be used to shift the charge voltage as a function of temperature. In the simplest view the voltage (V_{NTC}-V_{INTVCC}/2) is multiplied by 0.21 and added to the charge voltage. Figure 11 shows how to configure the pin and Table 10 shows some common temperature coefficient (TC) and associated resistor settings using 10k, B = 3380 NTC resistor. Note TC is with respect to the charge voltage at FB which is roughly 1 cell of a lead acid battery.

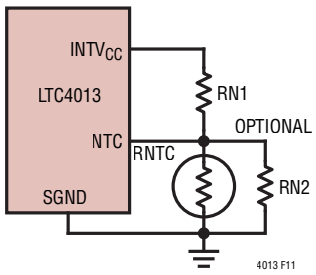

Figure 11. NTC Configuration for Temperature Compensation

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Table 10. Charge Voltage TC Examples Using B=3380 RNTC

TC (WRT V_{FB})	RN1	RN2
–2.5mV/°C	2.49k	3.32k
–5.0mV/°C	4.99k	10.0k
–10mV/°C	10.0k	Open

Since the NTC resistor is used to adjust for changes in battery temperature it is ideally placed in thermal contact with the battery. This is not always practical so the next best thing is to position the resistor for an accurate reading of the battery ambient temperature. Take care to reduce noise pickup on wires and make sure that good Kelvin connections are used.

Charge Termination Timer

The LTC4013 supports timer-based functions, where battery charge cycle control occurs after a specific amount of time. Timer termination is engaged when a capacitor (C_{TMR}) is connected from the TMR pin to ground. C_{TMR} for a desired end-of-cycle time (t_{EOC}) follows the relation:

$$C_{TMR}\ (\mu F) = t_{EOC}\ (Hr) \bullet 0.066$$

Table 11 represents some typical capacitors and associated times.

Table 11. Representative Timer Capacitor Values

Capacitor C_{TMR}	Absorption Time	Equalization Time (MODE1 L/M, H)	Bad Battery Timeout
68nF	1.03 Hrs	15.5, 7.7 Min	7.7 Min
0.22µF	3.33 Hrs	50, 25 Min	25 Min
0.47µF	7.12 Hrs	1.78, 0.89 Hrs	0.89 Hrs

The absorption and Li-Ion timer cycle starts when the charger transitions from constant-current to constant-voltage charging (when V_{FB} is 16mV away from final value). Equalization timing starts immediately upon transition to the equalization charge state. Bad battery timing commences with FB falling below LB.

BATTERY CHARGER FUNCTIONS: FILTERING COMPONENTS

Voltage Regulation Loop (FB)

The charger voltage regulation loop monitors battery voltage, and as such, is controlled by a very slow moving node. Battery ESR, however, can produce significant AC voltages due to ripple currents, causing unstable operation. This ESR effect can be reduced by adding a capacitor to the FB input, producing a low-frequency pole as shown in Figure 12. If ripple suppression proves necessary, the filter frequency is typically set to ~1/1000 of the switching frequency.

$$C_{FB} = \frac{1000 \bullet (R_{FB1} + R_{FB2})}{2\pi \bullet f_{SW} \bullet (R_{FB1} \bullet R_{FB2})}$$

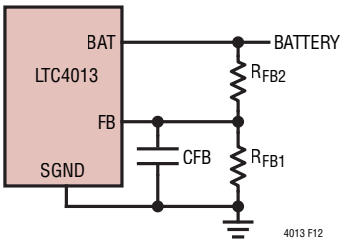

Figure 12. FB Voltage Filtering

Maximum Power Point Tracking (MPPT)

MPPT is used to regulate the input voltage to maximize power transfer from a power limited source. The first step is to determine the maximum power voltage. For a solar panel this can be determined from the data sheet. A resistor divider between the input source and the FBOC and MPPT pins is used to program the LTC4013 to regulate the input source at its maximum power voltage. The FBOC pin is used to sample the input source open circuit voltage when charging is paused while the MPPT pin is used to regulate the maximum power voltage when the charger is running. The MPPT resistor divider should be configured as shown in Figure 13.

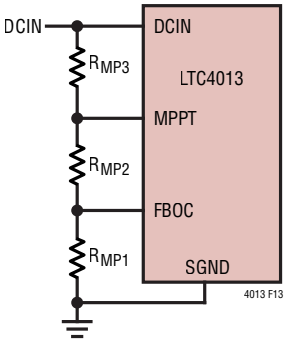

Figure 13. Resistor Divider for MPPT

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Choose the attenuation ratio of FBOC to DCIN voltages (K_F) so V_{FBOC} is between 1.0V and 3.0V when the input voltage is at its highest (i.e. open circuit, $V_{DCIN(OC)}$). The attenuation ratio of MPPT to DCIN voltages is set so that V_{MPPT} equals the chosen V_{FBOC} when DCIN is at the maximum power voltage, $V_{DCIN(MP)}$. The following equations define those conditions:

$$\frac{V_{FBOC}}{V_{DCIN(OC)}} = \frac{R_{MP1}}{R_{MP1}+R_{MP2}+R_{MP3}} = K_F$$

$$\frac{V_{MPPT}}{V_{DCIN(MP)}} = \frac{R_{MP1}+R_{MP2}}{R_{MP1}+R_{MP2}+R_{MP3}}$$

When the MPPT loop is in regulation, the MPPT voltage equals the FBOC voltage as measured during the open circuit interval. Reworking the above equations to define the ratio of the DCIN voltages at regulation and open circuit as K_R gives:

$$\frac{V_{DCIN(MP)}}{V_{DCIN(OC)}} = \frac{R_{MP1}}{R_{MP1}+R_{MP2}} = K_R$$

We can rewrite this equation to solve for R_{MP2} as a function of R_{MP1} and the DCIN ratio K_R:

$$R_{MP2} = R_{MP1} \bullet \left(\frac{1}{K_R} - 1\right)$$

Substitute that for R_{MP2} in the equation for K_F and solve for R_{MP3}:

$$R_{MP3} = R_{MP1} \bullet \left(\frac{1}{K_F} - \frac{1}{K_R}\right)$$

This sets up the design procedure:

1. Choose R_{MP1} such that V_{FBOC} = 1.0V to 3.0V. We recommended a current in the resistor string of 5 to 50µA.
2. Calculate R_{MP2} based on R_{MP1} and the ratio, K_R, between the maximum power voltage and the open circuit voltage.
3. Calculate R_{MP3} based on R_{MP1}, and the K_R and K_F ratios.

As an example, consider a solar panel with an open circuit voltage $V_{DCIN(OC)}$ = 24V and a maximum power voltage $V_{DCIN(MP)}$ = 17V. Choose V_{FBOC} = 1.5V. Then calculate:

$$K_F = \frac{1.5V}{24V} = 0.0625$$

$$K_R = \frac{17V}{24V} = 0.708$$

$$R_{MP1} = \frac{1.5V}{30\mu A} = 50k \text{ (Choose 30µA in Divider)}$$

$$R_{MP2} = 50k \bullet \left(\frac{1}{0.708} - 1\right) = 20.6k$$

$$R_{MP3} = 50k \bullet \left(\frac{1}{0.0625} - \frac{1}{0.708}\right) = 729k$$

Note these are ideal values and adjustments to use actual physical resistor values. The absolute value of V_{FBOC} is not critical so set it to help match ideal values to actual resistor values.

As another example consider charging a battery from a source with an open-circuit voltage of 30V and a source impedance of 5Ω. This resistive supply has a short circuit current of 6A, and the peak available power of 45W occurs with a load of 3A at 50% of V_{OC}. MPPT settings would have $V_{DCIN(OC)}$ = 30V, V_{FBOC} = 1.5V,

$$K_F = \frac{V_{FBOC}}{V_{DCIN(OC)}} = \frac{1.5V}{30V} = 0.05$$

$$K_R = \frac{V_{DCIN(MP)}}{V_{DCIN(OC)}} = \frac{15V}{30V} = 0.5$$

Again with 30µA in R_{MP1}, R_{MP1} = 50k then

$$R_{MP2} = 50k \bullet \left(\frac{1}{0.5} - 1\right) = 50k \text{ and}$$

$$R_{MP3} = 50k \bullet \left(\frac{1}{0.05} - \frac{1}{0.5}\right) = 900k$$

Additional MPPT Considerations

MPPT operation requires the use of back-to-back MOSFETs for the input PowerPath to allow accurate open circuit DCIN voltage measurement. When using back to back MOSFETs the sources are tied together, drains on the outside. If a single MOSFET is used the body diode effectively clamps DCIN to V_{IN} when the input MOSFET

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is off. This could result in inaccurate measurement of the DCIN open circuit voltage.

Because MPPT operation involves large changes of input voltage, it is important to ensure that the programmed maximum power voltage does not violate minimum input operating conditions: 4.5V or 100mV above the battery voltage, whichever is higher.

In general MPPT operation produces no control loop stability issues. If input oscillation is detected a lead capacitor (C_{MPPT}) from DCIN to MPPT can help mitigate problems.

If MPPT is not used the function is disabled by tying FBOC to $INTV_{CC}$.

Battery Stacks

Batteries are stacked serially to increase voltage and reduce load currents. The LTC4013 does allow for charging of higher voltage stacks, up to 60V. However the user needs to carefully consider the need for balancing individual cells of the stack. Cell balancing improves battery life at the expense of additional circuitry. Linear Technology provides ICs that facilitate this task. Some are mentioned in the Related Parts section at the end of this data sheet.

Plugging in a Battery

Care must be taken when hot plugging a battery into the charging circuit. Discharged capacitors on the charger side can cause very high battery discharge current as the battery voltage and the capacitor voltage equalize. Figure 14 shows the current path which has very little series impedance between the battery and capacitor.

As with other Hot Swap issues, the first step is to try and reduce capacitance. It is also possible to partially precharge the capacitors using power from V_{IN}. However, this must be done carefully to avoid a direct current path from the battery back to the input supply. Any application circuit must be bidirectional to support both battery charging through a low impedance path while controlling the reverse current during a hot plug event. See ideal diode application circuit, Figure 18.

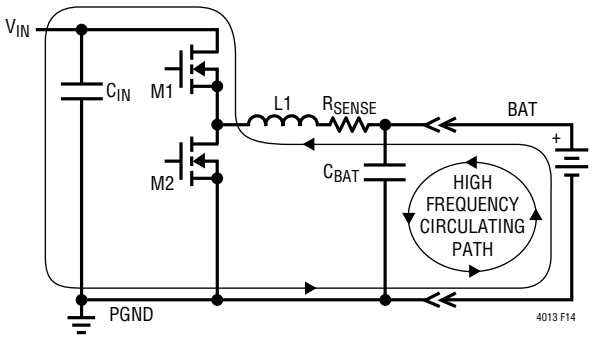

Figure 14. Current Flow During Hot Plugging of Battery

System Load During Charging

If there is a system load on the battery when charging, it can interfere with the charging algorithms. For instance if the load is greater than $I_{CHGMAX}/10$ the charger might not detect an end of charge condition. Careful management of the load can assist. Current is monitored through the sense resistor (and reported on ISMON) so it may be possible to use this signal to help detect this kind of problem.

Starting Without a Battery

The LTC4013 requires the SENSE voltage to be above 1.97V (typ) to run the charger and V_{IN} above VIN UVLO. This insures that the SENSE amp has sufficient headroom to operate. Normally this requirement is met if a battery is present. There are conditions where this may not be met, such as testing without a battery. In order to have the switching regulator start, the voltage on SENSE needs to be pulled up. There is no built in trickle current in the part to do this method. A simple method is in Figure 15. In this case a few mA's of current is taken from $INTV_{CC}$ and used to charge the capacitance on BAT. The time required will depend on the current and size of the capacitor. Once above the UVLO threshold the switching regulator turns on and will charge the node at higher currents, typically C/5 if you are below LB. Once above 4.3V there is not further drain on $INTV_{CC}$.

INFET MOSFETS

The input N channel MOSFETs are used for blocking battery discharge when the input is below battery as well as disconnecting DCIN to V_{IN} for open circuit measurement

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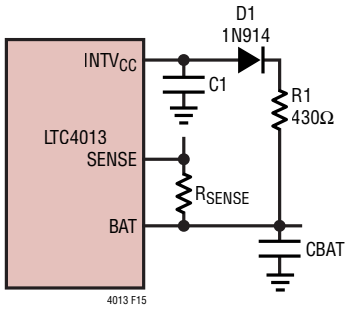

Figure 15. SENSE Precharge

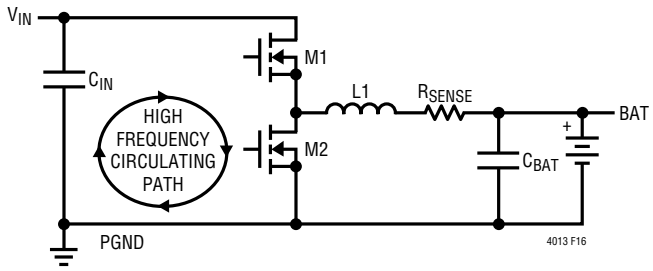

Figure 16. High Frequency Radiation Path

of DCIN in MPPT. This is done with back-to-back MOSFETs but if reverse discharge, or MPPT is not an issue, then a single MOSFET can be used with the source on the DCIN side. If a single MOSFET is used then V_{IN} is charged up initially though the bulk diode of the MOSFET. Take care when using back-to-back MOSFETs as INFET charging of gate turn on is controlled by DCIN to V_{IN} voltage, DCIN to V_{BAT} voltage, the part ENAB voltage and absolute V_{IN} voltage. Pick MOSFETs with low R_{DS} on as they conduct all charger current. Select breakdown voltage to stand off supply voltages.

LAYOUT CONSIDERATIONS

Note a general switching regulator layout overview is found in Linear Technology application notes, AN-136, AN-139 and AN-144.

For high current applications, current path traces need to meet current density guidelines as well as having minimal IR drops. There will also be substantial switching transients. The switch drivers on the IC are designed to drive large capacitances and generate significant transient currents. Carefully consider supply bypass capacitor locations to avoid corrupting the signal ground reference (SGND) used by the IC. Isolate SGND from high current paths and transients from the input supply and any local drive supplies because sensitive circuits such as the error amp reference are referred there. As a general rule keep the high frequency circulation path area as shown in Figure 16 minimized.

Effective grounding is achieved by considering switch current in the ground plane, and the return current paths of each respective bypass capacitor. The V_{IN} bypass return, $INTV_{CC}$ bypass return, and the sources of the ground-referred switch FETs carry PGND currents. SGND originates at the negative terminal of the BAT bypass capacitor, and is the small signal reference for the LTC4013. Do not run small traces to separate ground paths. A good ground plane is important. Orient PGND referred bypass elements such that transient currents in these return paths do not corrupt the SGND reference.

During the dead-time between the synchronous bottom switch and top switch conduction, the body diode of the synchronous FET conducts inductor current. Commutating the body diode requires a significant charge contribution from the top switch during initiation, creating a current spike in the top switch. At the instant the body diode commutates, a current discontinuity is created between the inductor and top switch, with parasitic inductance causing the switch node to transition in response to this discontinuity. High currents and excessive parasitic inductance can generate extremely fast $\delta V/\delta t$ times during this transition. These fast $\delta V/\delta t$ transitions can sometimes cause avalanche breakdown in the synchronous MOSFET body diode, generating shoot-through currents via parasitic turn-on of the synchronous MOSFET. Layout practices and component orientations that minimize parasitic inductance on the switched nodes are critical for reducing these effects.

Orient power path components such that current paths in the ground plane do not cross through signal ground areas. Power ground currents are controlled on the LTC4013 via the PGND pin, and this ground references the high current synchronous switch drive components, as well as the local $INTV_{CC}$ supply. It is important to keep PGND and SGND voltages consistent with each other, do not separate these grounds with thin traces.

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When the bottom side MOSFET is turned off, gate drive currents return to the LTC4013 PGND pin from the MOSFET source. The BST supply refresh surge currents also return through this same path. Orient the MOSFET such that these PGND return currents do not corrupt the SGND reference.

The high $\delta i/\delta t$ loop formed by the switch MOSFETs and the input capacitor (C_{VIN}) should have short wide traces to minimize high frequency noise and voltage stress from inductive ringing. Surface mount components are preferred to reduce parasitic inductances from component leads. Switch path currents can be controlled by orienting switch FETs, the switched inductor, and input and output decoupling capacitors in close proximity to each other. Locate the $INTV_{CC}$, and BST capacitors in close proximity to the IC. These capacitors carry the MOSFET gate drive currents. Locate the small-signal components away from high frequency switching nodes (TG, BG, SW, BST and $INTV_{CC}$). High current switching nodes are oriented across the top of the LTC4013 package to simplify layout and prevent corruption of the SGND reference.

Locate the battery charger feedback resistors, and MPPT resistors in close proximity to the LTC4013 and minimize the length of the high impedance feedback nodes.

Route the SENSE and BAT traces together, keeping them as short as possible, and avoid corruption of these lines by high current switching nodes.

The LTC4013 packaging has been designed to efficiently remove heat from the IC via the exposed backside pad. Solder the pad to a copper footprint on the PCB that contains a large number of vias to the ground plane. This reduces both the electrical ground resistance, as well as the thermal resistance to ambient.

Accurate sensing of charge current is dependent on good printed circuit board layout as shown in Figure 17. 4 terminal sense resistors are the best option but it is possible to get good results with 2 terminal devices.

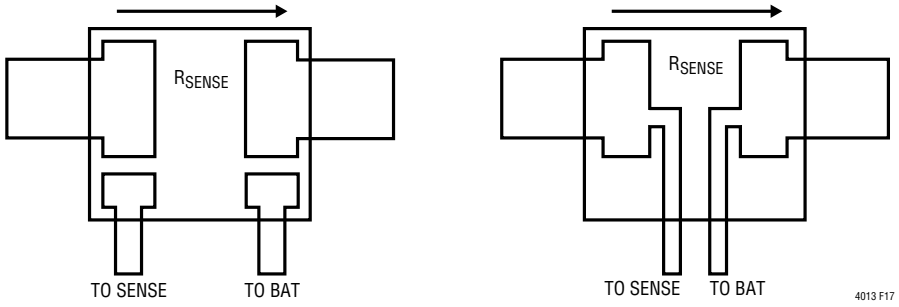

Figure 17. Sense Resistor PCB Layout

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Figure 18. Ideal Diode to Block Current Surge When Hot Plugging Battery

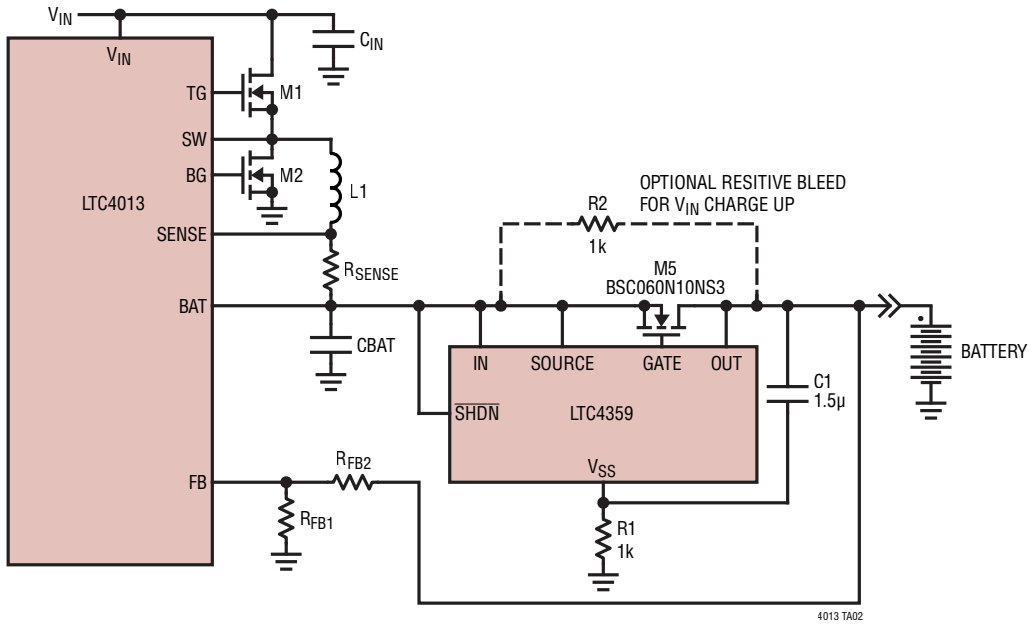
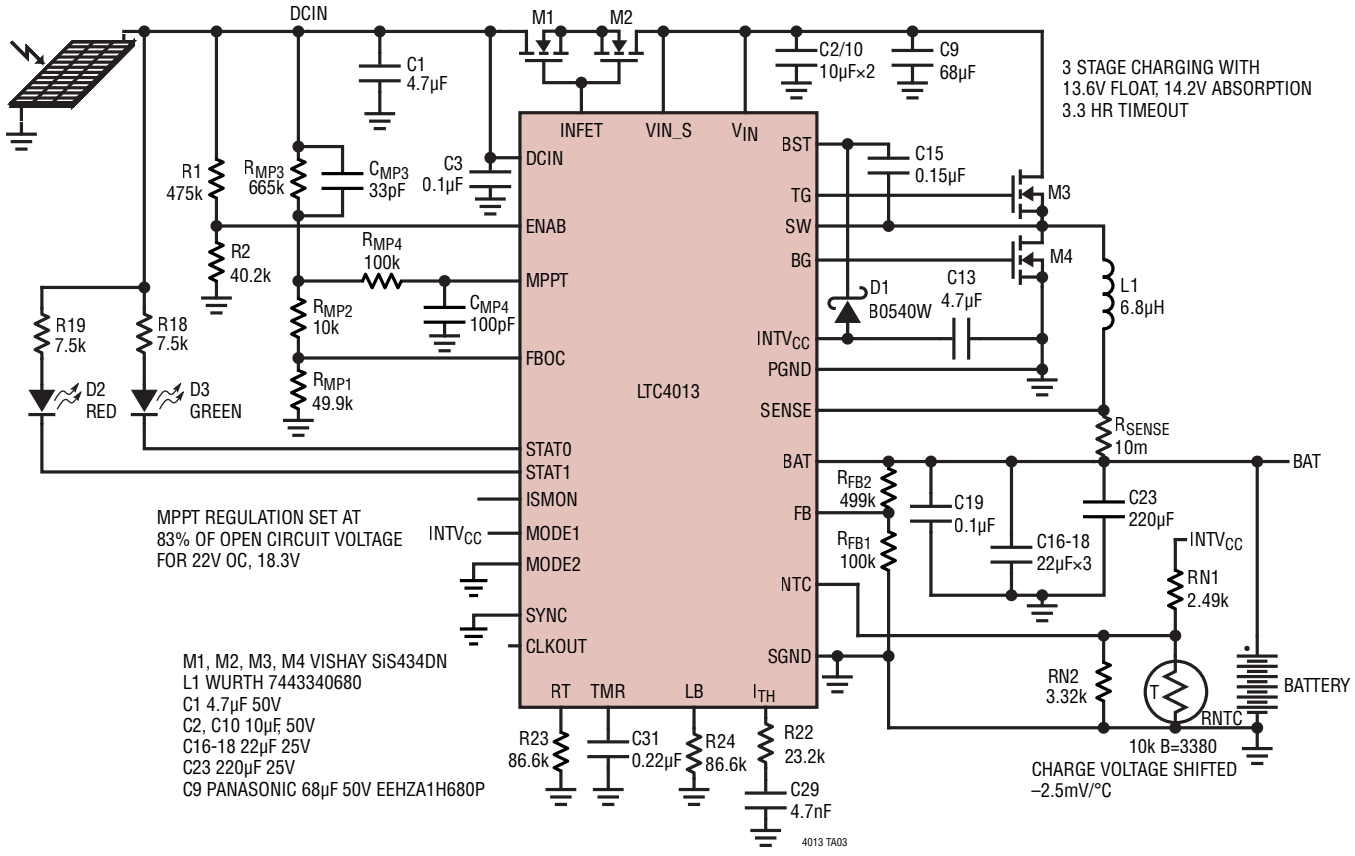
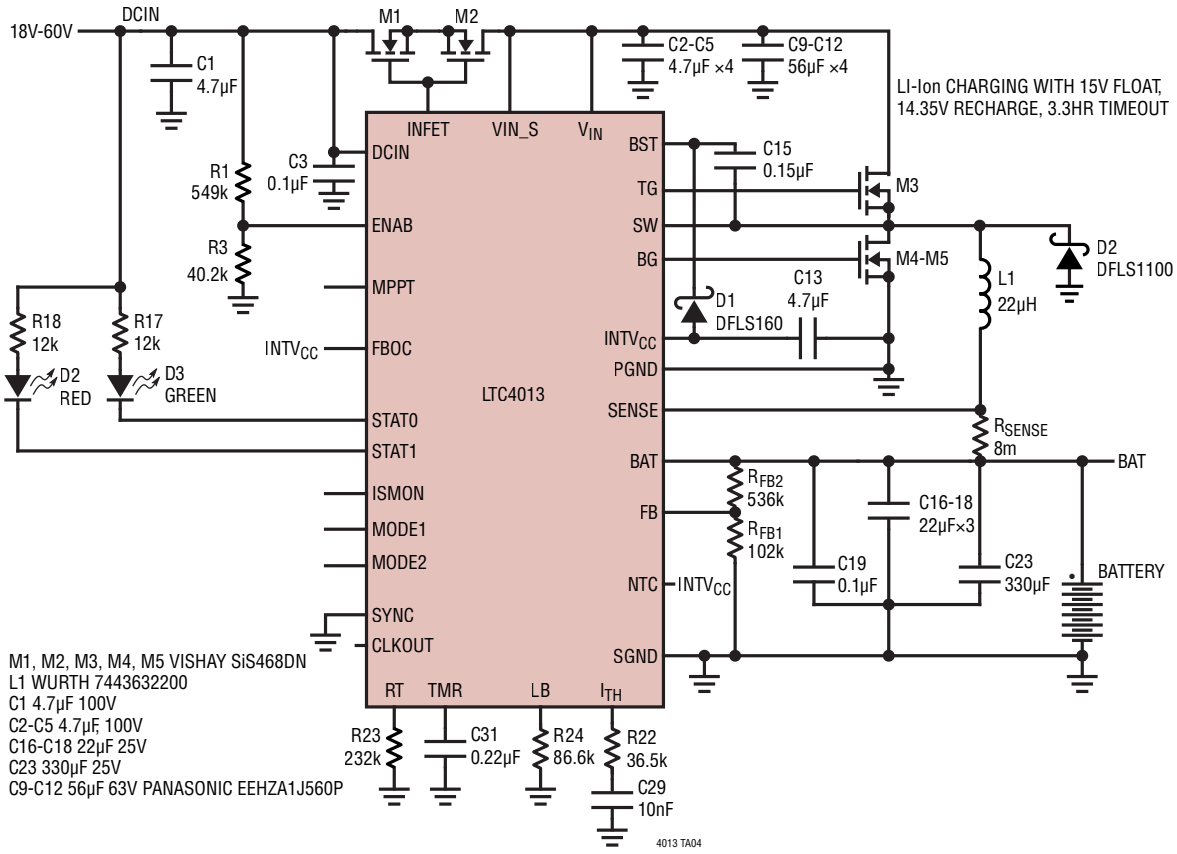


Figure 19. 6 Cell, 5A Lead Acid Charger with 24V Solar Panel Input and MPPT Optimization



APPLICATIONS INFORMATION

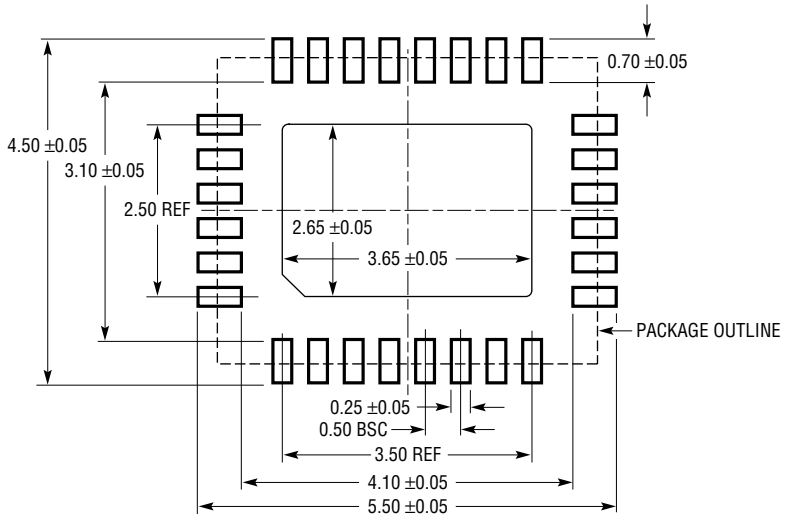
Figure 20. 18V-60V 6.25A LiFePO$_4$ 15V SLA Replacement Battery Charger



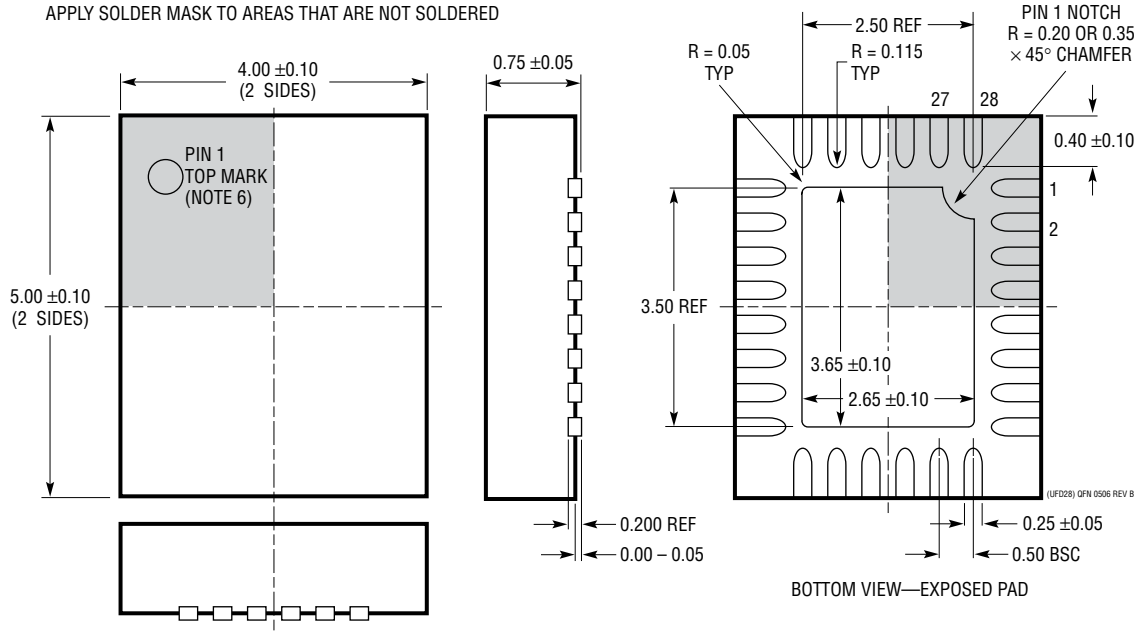
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC4013#packaging for the most recent package drawings.

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

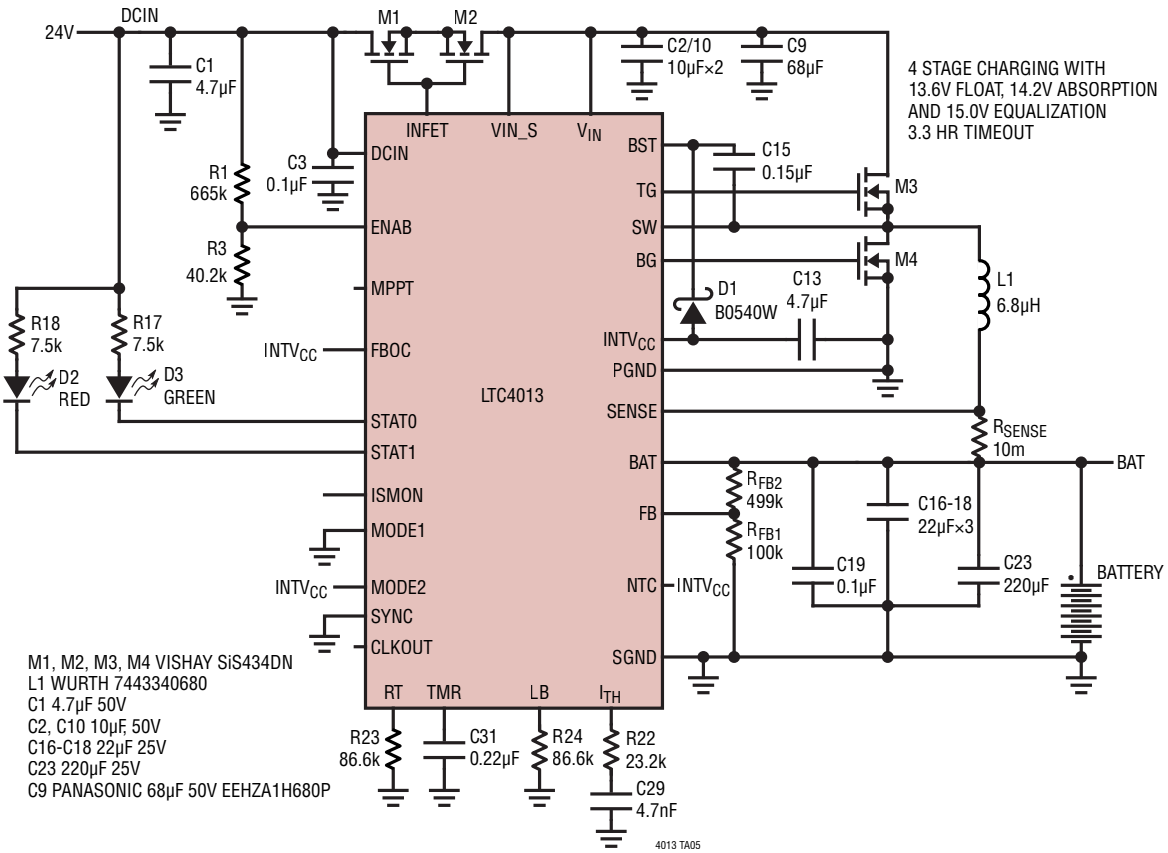


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

Figure 21. 24V 5A 6 Cell Lead Acid Charger with Absorption and Equalization Charging



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC4020	55V Buck-Boost Multi-Chemistry Battery Charger	Li-Ion and Lead Acid Charge Algorithms
LTC4000/LTC4000-1	High Voltage High Current Controller for Battery Charging	3V to 60V Input and Output Voltage. Pair with a DC/DC Converter. LTC4000- 1 Has MPPT
LTC4015	Multichemistry Buck Battery Charger Controller with Digital Telemetry System	4.5V to 35V Synchronous Buck Battery Charger with Multiple System Monitors and Coulomb Counter
LTC3305	Lead Acid Battery Balancer	Balance up to Four 12V Lead Acid Batteries in Series. Stand Alone Operation
LT8710	Synchronous SEPIC/ Inverting/Boost Controller with Output Current Control	2, 3-Stage Lead Acid Charger with C/10 Termination
LT3652/LTC3652HV	2A Battery Charger with Power Tracking	Multi-Chemistry, Onboard Termination, Input Supply Voltage Regulation Loop for Peak Power Tracking. 4.95V to 34V input Up to 2A Charger Current.
LT3651-4.x/LT3651-8.x	Monolithic 4A Switch Mode Synchronous Li-Ion Battery Charger	Standalone, 4.75V ≤ V_{IN} ≤ 32V (40V Abs Max), 4A, Programmable Charge Current Timer or C/10 Termination
LT8490	High Voltage High Current Buck-Boost Controller Battery Charger	6V to 80V Input and Output Voltage. Single Inductor. MPPT

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(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com/LTC4013
LT 0816 • PRINTED IN USA

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- Поставка более 17-ти миллионов наименований электронных компонентов;
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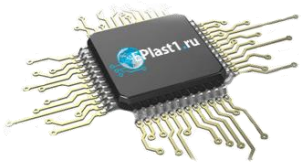
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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