

## FEATURES

- SMPTE 259M compliant
- four isolated outputs (two complimentary pairs), adjustable from 50mV-1000mV into 75Ω loads
- operational from 143Mb/s to 540Mb/s and beyond
- nominal 500ps rise/fall times
- precise  $\pm 7.5\%$  output amplitudes
- 40% system power reduction over GS9007
- 75Ω on-chip input termination resistors
- input hysteresis
- operational down to 80mV input amplitude
- superior output isolation
- "Bus Through" expansion port for fan out requirements

## APPLICATIONS

4fsc, 4:2:2 and 4:4:4 serial digital video co-axial transmission interfaces from 143 to 540Mb/s; General purpose cable driving applications (co-axial cable or UTP).

## DESCRIPTION

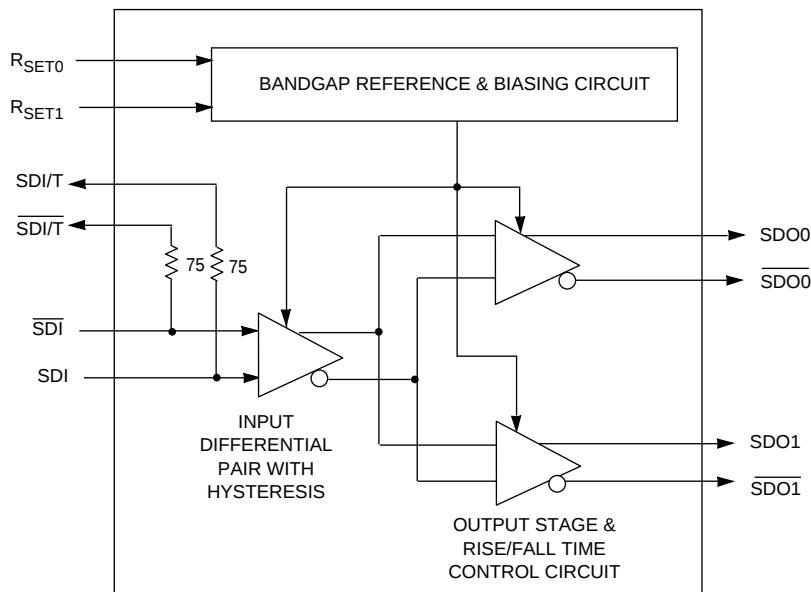
The GS9029 is a second generation bipolar integrated circuit designed to drive four 75Ω co-axial cables.

The GS9029 features two pairs of complementary outputs whose amplitude is controlled within  $\pm 7.5\%$ . The output signal levels are also adjustable from 50mVp-p up to 1000mVp-p with little change in other performance parameters. The amplitude of the output stage is varied by adjusting the  $R_{SET}$  resistor value. The patented current mode outputs ensure superior output return loss and minimal over shoot. The rise/fall time circuitry allows wide range operation and provides symmetrical balanced outputs to reject power supply noise. In addition high output isolation ensures that the cable driver outputs are not affected by the performance or status of other outputs. Operational with input amplitudes as low as 80mV, the GS9029 provides a robust serial interface.

The GS9029 is packaged in a 16 pin narrow SOIC and operates from a single +5 or -5 volt supply. Typical system power consumption is 320mW which is 40% less than the GS9007.

## ORDERING INFORMATION

| PART NUMBER | PACKAGE            | TEMPERATURE |
|-------------|--------------------|-------------|
| GS9029-CKD  | 16 pin SOIC Narrow | 0°C to 70°C |
| GS9029-CTD  | 16 pin SOIC Tap    | 0°C to 70°C |



## BLOCK DIAGRAM

**ABSOLUTE MAXIMUM RATINGS**

| PARAMETER                                  | VALUE                        |
|--------------------------------------------|------------------------------|
| Supply Voltage ( $V_S = V_{CC} - V_{EE}$ ) | 5.5V                         |
| Input Voltage Range (any input)            | -0.3V to ( $V_{CC} + 0.3$ )V |
| Maximum Die Temperature                    | 125°C                        |
| Operating Temperature Range                | 0°C ≤ $T_A$ ≤ 70°C           |
| Storage Temperature Range                  | -65°C ≤ $T_S$ ≤ 150°C        |
| Lead Temperature (soldering, 10 sec)       | 260°C                        |

**DC ELECTRICAL CHARACTERISTICS**

$V_{CC} = 5V$ ,  $V_{EE} = 0V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$  unless otherwise specified. Specifications assume 800mV output amplitude into 75Ω terminated line.

| PARAMETER                        | SYMBOL        | CONDITIONS                                           | MIN                  | TYP                | MAX                     | UNITS | TEST LEVEL |
|----------------------------------|---------------|------------------------------------------------------|----------------------|--------------------|-------------------------|-------|------------|
| Supply Voltage                   | $V_{CC}$      | Operating Range.                                     | 4.75                 | 5.00               | 5.25                    | V     | 1          |
| Power (system power)             | $P_S$         | Driving four 75Ω cables.<br>$R_{SET} = 54.9\Omega$ . | -                    | 320                | 350                     | mW    | 5          |
| Supply Current                   | $I_{CC}$      | Driving four 75Ω cables.<br>$R_{SET} = 54.9\Omega$ . | -                    | 64                 | 70                      | mA    | 1          |
| Common Mode Input Voltage        | $V_{CM\_IN}$  |                                                      | $2.4 + (V_{DIFF}/2)$ | -                  | $V_{CC} - (V_{DIFF}/2)$ | V     | 6, 7       |
| Differential Input Voltage       | $V_{DIFF}$    |                                                      | 80                   | -                  | 1000                    | mV    | 6, 7       |
| Common Mode Output Voltage Range | $V_{CM\_OUT}$ |                                                      | -                    | $V_{CC} - V_{OUT}$ | -                       | V     | 5          |
| Differential Output Voltage      | $V_{OUT}$     | $R_{SET} = 54.9\Omega$                               | 740                  | 800                | 860                     | mV    | 1          |
|                                  |               | $R_{SET} = 43.2\Omega$                               | 925                  | 1000               | 1075                    | mV    | 1          |
| Input Hysteresis                 |               |                                                      | -                    | 25                 | -                       | mV    | 7          |

**TEST LEVELS**

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1,2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.

## AC ELECTRICAL CHARACTERISTICS

$V_{CC} = 5V$ ,  $V_{EE} = 0V$ ,  $T_A = 0^{\circ}C$  TO  $70^{\circ}C$  unless otherwise specified. Specifications assume 800mV output amplitude into  $75\Omega$  terminated line.

| PARAMETER                | SYMBOL     | CONDITIONS    | MIN | TYP | MAX | UNITS       | NOTES | TEST LEVEL |
|--------------------------|------------|---------------|-----|-----|-----|-------------|-------|------------|
| Serial Data Bit Rate     |            |               | 143 | -   | 540 | Mb/s        |       | 1          |
| Additive Jitter          |            | 270Mb/s       | -   | 25  | -   | ps p-p      | 1, 2  | 7          |
|                          |            | 540Mb/s       | -   | 25  | -   | ps p-p      |       |            |
| Output Rise/Fall Times   | $t_R, t_F$ | 20% - 80%     | 400 | 500 | 700 | ps          |       | 1          |
| Rise/Fall Times Mismatch |            |               | -   | 50  | 100 | ps          |       | 5          |
| Overshoot                |            |               | -   | 5   | -   | % $V_{OUT}$ | 2     | 7          |
| Duty Cycle Distortion    |            |               | -   | 50  | 100 | ps          |       | 1          |
| Output Return Loss       |            | 5MHz - 540MHz | -   | 17  | -   | dB          | 2     | 7          |

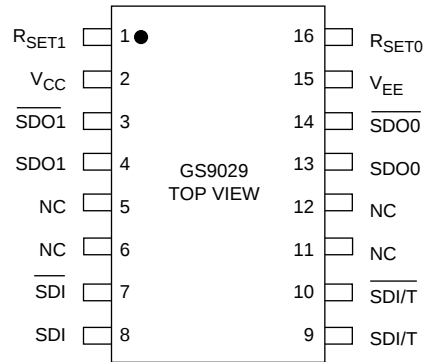
### NOTES

1.  $6\sigma$  additive jitter measuring Pseudo random bit sequence ( $2^{23}-1$ ).
2. Measured with Gennum Evaluation Board (EB9029V1).

### TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1,2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.

PIN CONNECTIONS



PIN DESCRIPTIONS

| NUMBER       | SYMBOL                           | TYPE | DESCRIPTION                                                                                                                                                                                                         |
|--------------|----------------------------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1            | R <sub>SET1</sub>                | I    | Amplitude setting resistor for SDO1, $\overline{\text{SDO1}}$ .                                                                                                                                                     |
| 2            | V <sub>CC</sub>                  |      | Most positive supply voltage.                                                                                                                                                                                       |
| 3, 4         | $\overline{\text{SDO1}}$ , SDO1  | O    | Second differential serial output (inverse and true).                                                                                                                                                               |
| 5, 6, 11, 12 | NC                               |      | No connect.                                                                                                                                                                                                         |
| 7, 8         | $\overline{\text{SDI}}$ , SDI    | I    | Serial data inputs (inverse and true).                                                                                                                                                                              |
| 9, 10        | SDI/T, $\overline{\text{SDI/T}}$ | I    | Dual mode pin:<br>a) "Bus Through" pins for serial data inputs when additional GS9029s are used on the same bus.<br>b) Termination pins when using a single GS9029, or when the device is the last on an input bus. |
| 13, 14       | SDO0, $\overline{\text{SDO0}}$   | O    | First differential serial output (true and inverse).                                                                                                                                                                |
| 15           | V <sub>EE</sub>                  |      | Most negative supply voltage.                                                                                                                                                                                       |
| 16           | R <sub>SET0</sub>                | I    | Amplitude setting resistor for SDO0, $\overline{\text{SDO0}}$ .                                                                                                                                                     |

**TYPICAL PERFORMANCE CURVES** ( $V_S = 5V$ ,  $T_A = 25^\circ C$  unless otherwise shown. Devices guard band tested to  $70^\circ C$  only.)

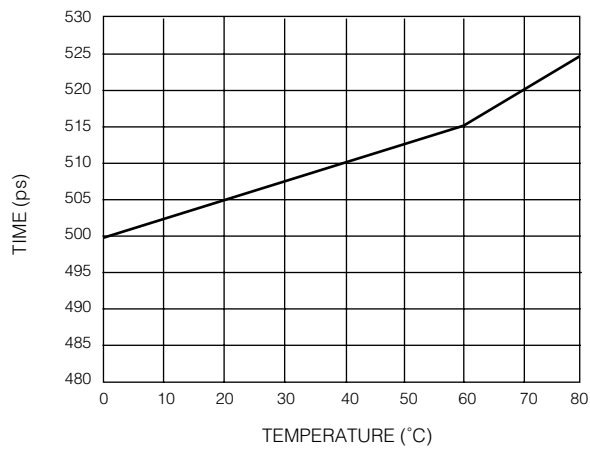


Fig. 1 Rise/Fall vs. Temperature

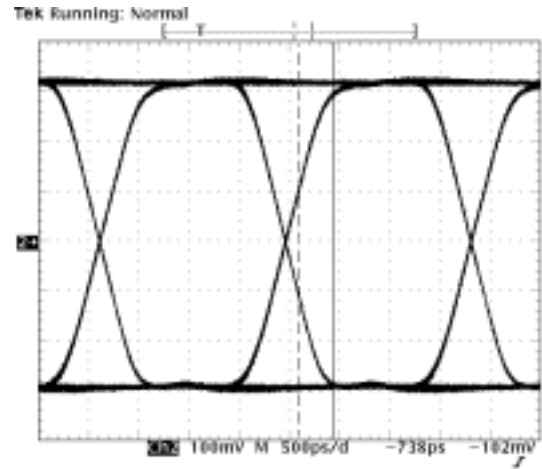


Fig. 4 540Mb/s Eye Diagram

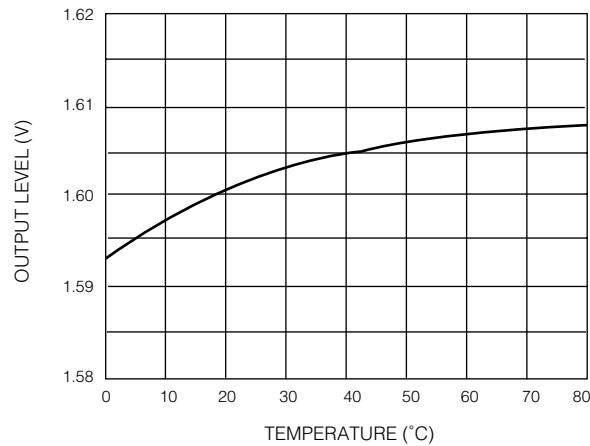


Fig. 2 Serial Data Output Level vs. Temperature

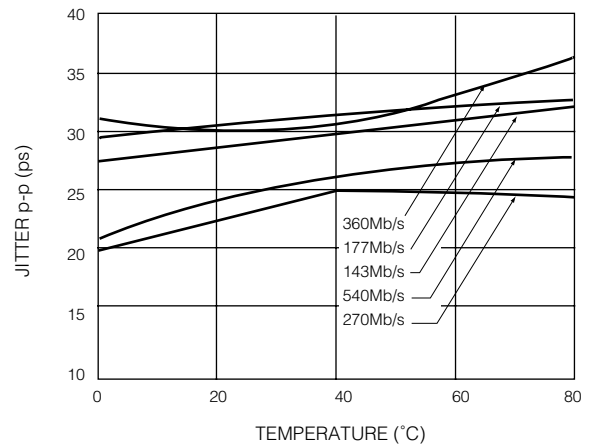


Fig. 5 Peak to Peak Additive Jitter vs. Temperature

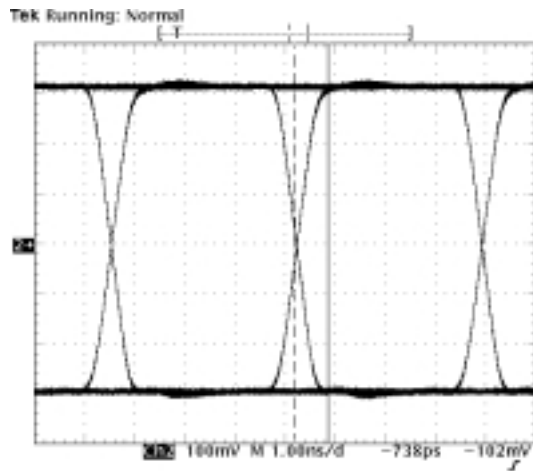


Fig. 3 270Mb/s Eye Diagram

## DETAILED DESCRIPTION

### INPUT INTERFACING

SDI/ $\overline{\text{SDI}}$  are high impedance differential inputs. Two conditions must be observed when interfacing to these inputs:

1. The input signal amplitude must be between 80mV and 1000mV.
2. The common mode voltage range must be as specified in the DC Characteristics Table (page 2). For 800mV input amplitude signals, this corresponds to a common mode voltage range between 2.8 and 4.6 volts.

Figures 6 and 7 illustrate two methods of interfacing the GS9029 to the Gennum GS9024 (Cable Equalizer), GS9035 (Reclocker) or the GS9025 (Receiver).

Figure 6 illustrates the simplest interface and is recommended when the trace lengths between the driver and the GS9029 are less than 0.5 in.

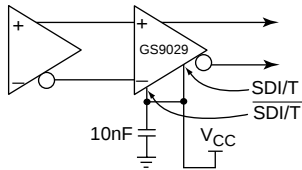


Fig. 6 Interfaces using Internal SDI Terminations

When trace lengths become longer than 0.5in. and data rates greater than 360Mb/s, electromagnetic reflections begin to affect signal integrity. To minimize reflections, controlled impedance traces and source and end terminations should be used as shown in Figure 7. Although terminations on both sides reduce the signal swing by a factor of two, the GS9029 is designed to meet this need with ultra low input amplitude requirements (as low as 80mV).

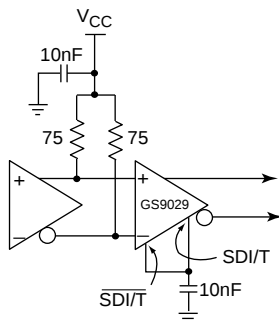


Fig. 7 Interfaces using Internal SDI Terminations  
Connected to AC Ground

The GS9029 can accept AC coupled input signals with no extra configuration required.

### OUTPUT INTERFACING

Figure 8 illustrates the recommended interface for ac coupled outputs.

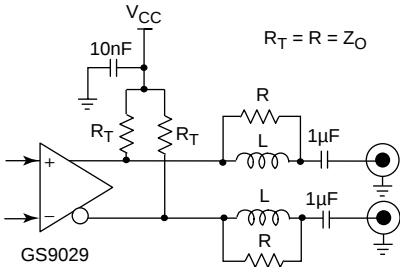


Fig. 8 Interfaces for AC Coupled Outputs

The termination resistor ( $R_T$ ) value should be equal to the characteristic impedance of the cable. Controlled impedance traces should be used for the outputs and the termination resistors should be placed near the GS9029. The inductor (L) and resistor (R) are used to optimize the output return loss and are PCB dependent. Typically, R equals the transmission line characteristic impedance and L is approximately 8.2nH.

### OUTPUT AMPLITUDE ADJUSTMENT

The GS9029 outputs are adjustable from as low as 50mV to as high as 1000 mV. The output amplitudes are set by the  $R_{SET0}$  and the  $R_{SET1}$  resistors respectively. The relationship between the approximate output amplitude ( $V_{OUT}$ ) and  $R_{SET}$  is given by the equation below:

$$R_{SET} = \frac{1.154 \times Z_O}{2 \times V_{OUT}}$$

where  $Z_O$  is in ohms and  $V_{OUT}$  is in volts.

The minimum value of  $R_{SET}$  is 43.2 $\Omega$ . For 75 $\Omega$  cable and 800mV output amplitudes, the value of  $R_{SET}$  is 54.9 $\Omega$ . Also, note that the above formula assumes that the transmission line is properly end terminated.

## INPUT / OUTPUT CIRCUITS

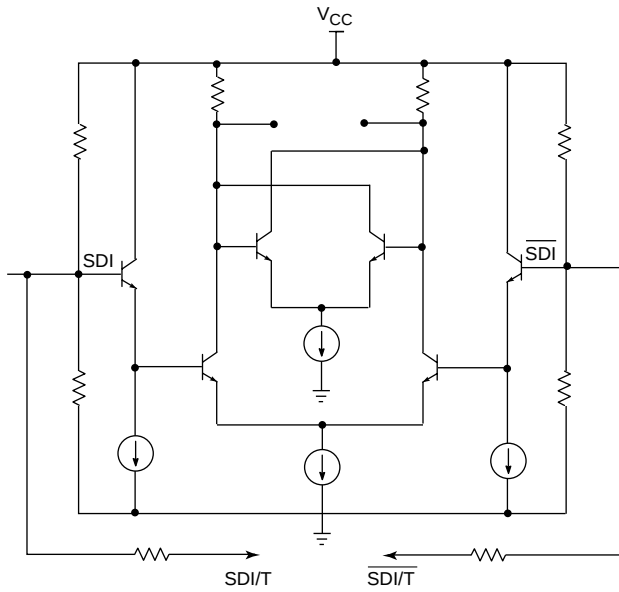


Fig. 9 Input Circuit (SDI,  $\overline{\text{SDI}}$ , SDI/T,  $\overline{\text{SDI/T}}$ )

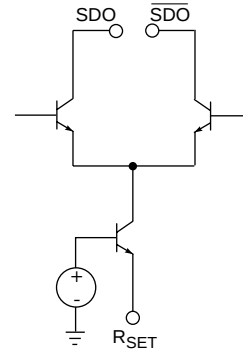


Fig. 10 Output Circuit (SDO1,  $\overline{\text{SDO1}}$ , SDO0,  $\overline{\text{SDO0}}$ )

### NOTES ON INPUT ARCHITECTURE

The input pins of the GS9029 are configured so that two or three GS9029's can easily be connected to a single input bus as shown below. On-chip input termination resistors permit a proper termination by connecting pins 9 to 10 of the last device on the bus. If only one GS9029 is used, it should be connected as the last device in the diagram below.

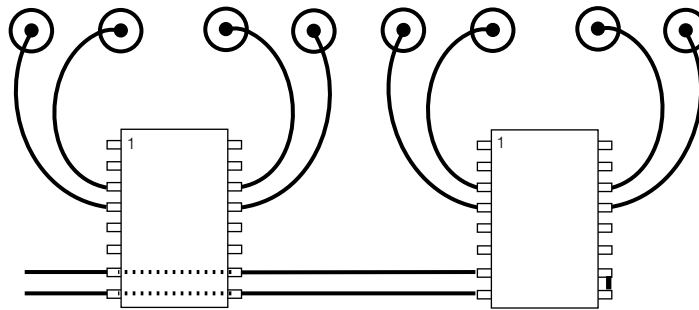
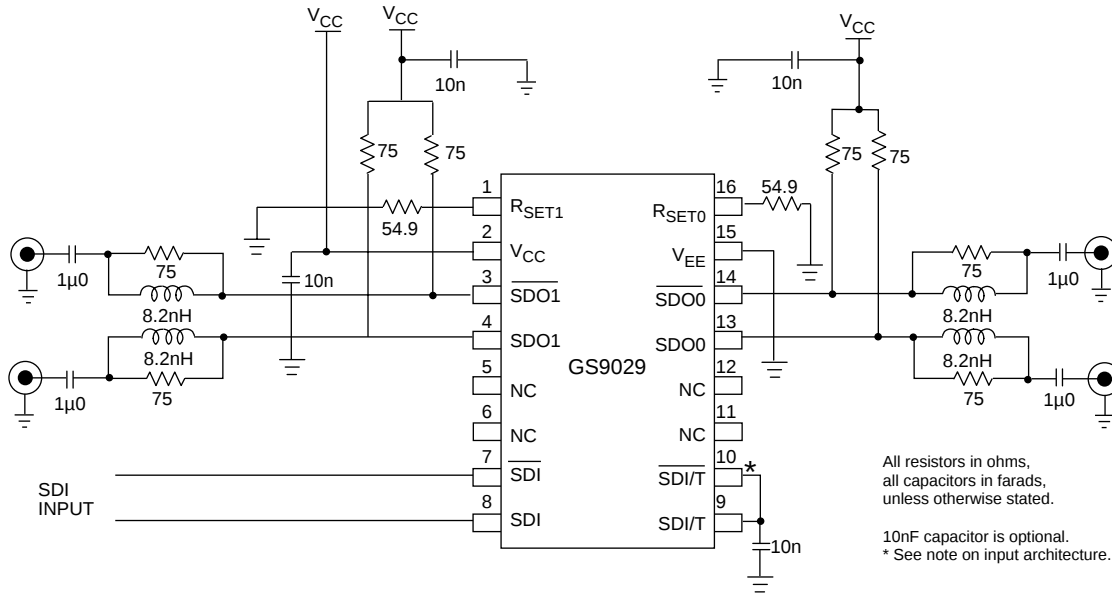


Fig. 11 GS9029 Bussed Connections

## TYPICAL APPLICATION CIRCUIT

GS9029



### CAUTION

ELECTROSTATIC  
SENSITIVE DEVICES

DO NOT OPEN PACKAGES OR HANDLE  
EXCEPT AT A STATIC-FREE WORKSTATION



### DOCUMENT IDENTIFICATION

DATA SHEET

The product is in production. Gennum reserves the right to make changes at any time to improve reliability, function or design, in order to provide the best product possible.

### REVISION NOTES:

Updated serial data bit rate values in Features and Description; Updated AC and DC Electrical Characteristics Tables; Removed Figure 5; Updated Typical Application Circuit.

*For the latest product information, visit [www.gennum.com](http://www.gennum.com).*

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