

Product Summary

V _{BR} (Min)	I _{PP} (Max)	C _T (Typ)
4.5V	45A	2.1pF

Description

The D5V0P4UR6SO is a high-performance device suitable for protecting four high-speed I/Os. These devices are assembled in SOT26 package and have high ESD surge capability and low capacitance.

Applications

Typically used at high-speed ports such as USB 2.0, IEEE1394 (Firewire®, iLink™), Serial ATA, DVI, HDMI and PCI.



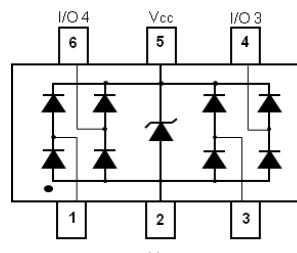
Top View

Features

- Low Clamping Voltage: Typical 7.5V at 12A 100ns, TLP, I/O to V_{SS}; Typical 5.8V at 12A 100ns, TLP, V_{CC} to V_{SS}
- IEC 61000-4-2 (ESD): Air – ±30kV, Contact – ±30kV
- IEC 61000-4-4 (EFT): ±80A (5/50ns)
- IEC 61000-4-5 (Lighting): 20A, I/O to V_{SS}; 45A, V_{CC} to V_{SS}
- TLP Dynamic Resistance: 0.15Ω, I/O to V_{SS}; 0.07Ω, V_{CC} to V_{SS}
- Low Channel Input Capacitance of 2.1pF Typical
- 4 Channels of ESD Protection
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- Halogen and Antimony Free. "Green" Device (Note 3)**

Mechanical Data

- Case: SOT26
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Schematic
- Terminals – Finish – Matte Tin Pleated Leadframe. Solderable per MIL-STD-202, Method 208 (B3)
- Weight: 0.016 grams (Approximate)



Device Schematic

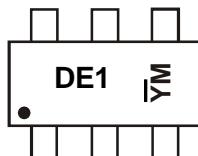
Ordering Information (Note 4)

Product	Compliance	Marking	Reel Size (inches)	Tape Width (mm)	Quantity per Reel
D5V0P4UR6SO-7	Standard	DE1	7	8	3,000/Tape & Reel

Notes:

- No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information



DE1 = Product Type Marking Code

YM = Date Code Marking

Y = Year (ex: D = 2016)

M = Month (ex: 9 = September)

Note: "—" Represents Internal Code

Date Code Key

Year	2016	2017	2018	2019	2020	2021						
Code	D	E	F	G	H	I						
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

FireWire is a registered trademark of Apple Computer, Inc.
iLink is a trademark of CEM Corporation.

D5V0P4UR6SO
Document number: DS38235 Rev. 1 - 2

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Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	Conditions
Peak Pulse Current, per IEC 61000-4-5	I_{PP}	20	A	I/O to V_{SS} , 8/20 μs
Peak Pulse Current, per IEC 61000-4-5	I_{PP}	45	A	V_{CC} to V_{SS} , 8/20 μs
Peak Pulse Power, per IEC 61000-4-5	P_{PP}	180	W	I/O to V_{SS} , 8/20 μs
Operating Supply Voltage (DC)	V_{DC}	3.6	V	V_{CC} to V_{SS}
ESD Protection – Contact Discharge, per IEC 61000-4-2	$V_{ESD_CONTACT}$	± 30	kV	I/O to V_{SS} , V_{CC} to V_{SS}
ESD Protection – Air Discharge, per IEC 61000-4-2	V_{ESD_AIR}	± 30	kV	I/O to V_{SS} , V_{CC} to V_{SS}
Operating Temperature	T_{OP}	-55 to +85	$^\circ\text{C}$	—
Storage Temperature	T_{STG}	-55 to +150	$^\circ\text{C}$	—

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation Typical (Note 5)	P_D	300	mW
Thermal Resistance, Junction to Ambient Typical (Note 5)	$R_{\theta JA}$	417	$^\circ\text{C}/\text{W}$

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Conditions
Reverse Working Voltage	V_{RWM}	—	—	3.3	V	V_{CC} to V_{SS}
Reverse Leakage Current (Note 6)	I_{LEAK}	—	—	5	μA	$V_{CC} = 3.3\text{V}$, V_{CC} to V_{SS}
Channel Leakage Current (Note 6)	I_{CH_LEAK}	—	—	1	μA	$V_{I/O} = 3.3\text{V}$, I/O to V_{SS}
Reverse Breakdown Voltage	V_{BR}	4.5	—	7	V	$I_{BR} = 1\text{mA}$, V_{CC} to V_{SS}
Forward Clamping Voltage	V_F	—	0.8	1.2	V	$I_F = 15\text{mA}$, V_{SS} to V_{CC}
Reverse Clamping Voltage (Note 7)	V_{C_5A}	—	6	—	V	$I_{PP} = 5\text{A}$, I/O to V_{SS} , 8/20 μs
		—	4.8	—	V	$I_{PP} = 5\text{A}$, V_{CC} to V_{SS} , 8/20 μs
ESD Clamping Voltage	V_{ESD}	—	7.5	—	V	TLP, 12A, $t_P = 100\text{ns}$, I/O to V_{SS}
		—	5.8	—		TLP, 12A, $t_P = 100\text{ns}$, V_{CC} to V_{SS}
Dynamic Resistance	R_{DIF}	—	0.15	—	Ω	TLP, 12A, $t_P = 100\text{ns}$, I/O to V_{SS}
		—	0.07	—		TLP, 12A, $t_P = 100\text{ns}$, V_{CC} to V_{SS}
Channel Input Capacitance	$C_{I/O}$	—	2.1	2.5	pF	$V_{I/O} = 1.65\text{V}$, $V_{CC} = 3.3\text{V}$, $f = 1\text{MHz}$
		—	2.4	3.0	pF	$V_{I/O} = 1.65\text{V}$, V_{CC} = floated, $f = 1\text{MHz}$
Variation of Channel Input Capacitance	$\Delta C_{I/O}$	—	0.05	—	pF	$V_{SS} = 0\text{V}$, I/O = 1.65V, $V_{CC} = 3.3\text{V}$, $f = 1\text{MHz}$, I/O_x to V_{SS} – I/O_y to V_{SS}
		—	0.04	—	pF	$V_{SS} = 0\text{V}$, I/O = 1.65V, V_{CC} = floated, $f = 1\text{MHz}$, I/O_x to V_{SS} – I/O_y to V_{SS}

Notes:

5. Device mounted on FR-4 PCB pad layout (2oz copper) as shown on Diodes, Inc. website at <http://www.diodes.com/package-outlines.html>.
6. Short duration pulse test used to minimize self-heating effect.
7. Clamping voltage value is based on an 8x20 μs peak pulse current (I_{PP}) waveform.

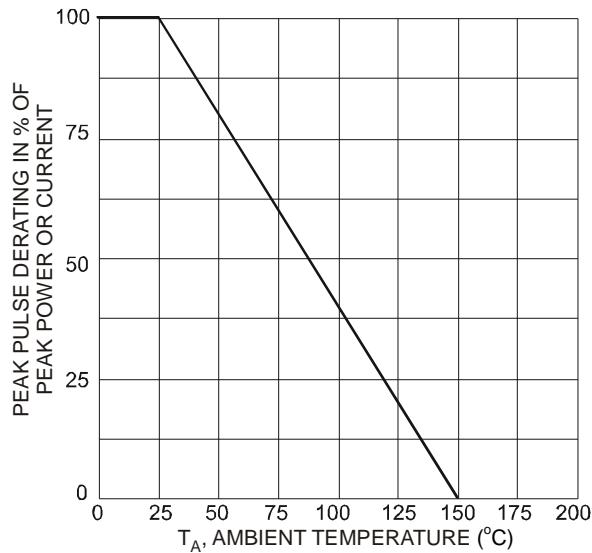


Figure 1 Pulse Derating Curve

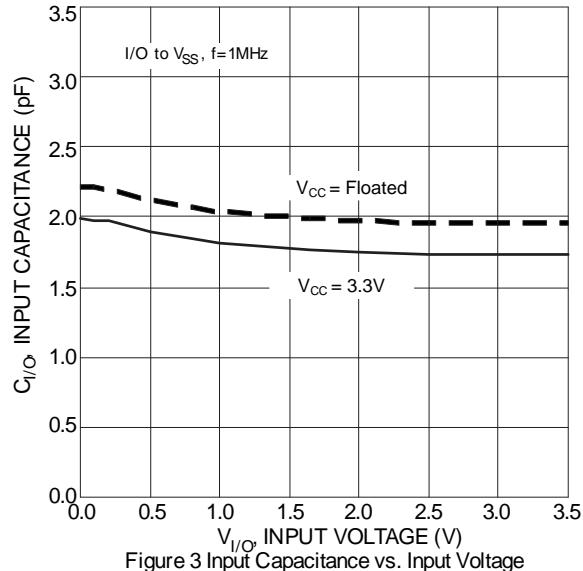


Figure 3 Input Capacitance vs. Input Voltage

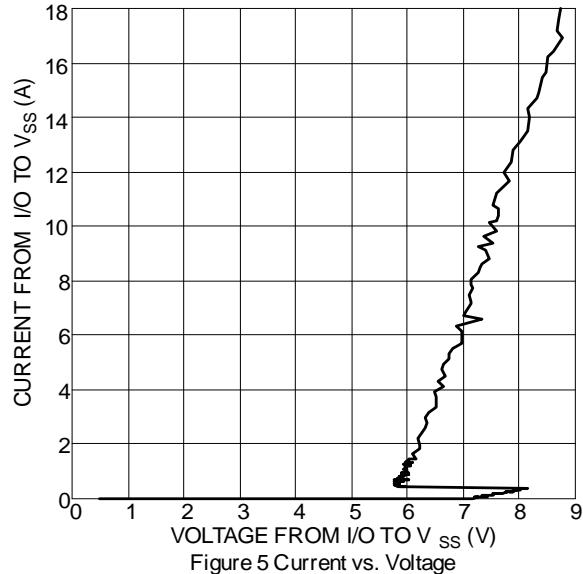


Figure 5 Current vs. Voltage

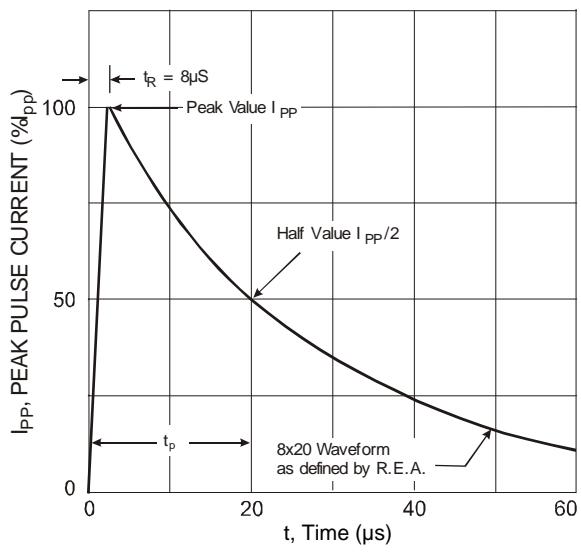


Figure 2 Pulse Waveform

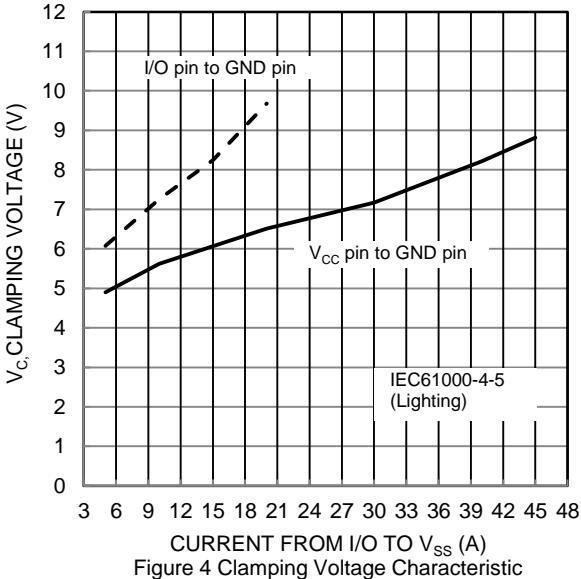


Figure 4 Clamping Voltage Characteristic

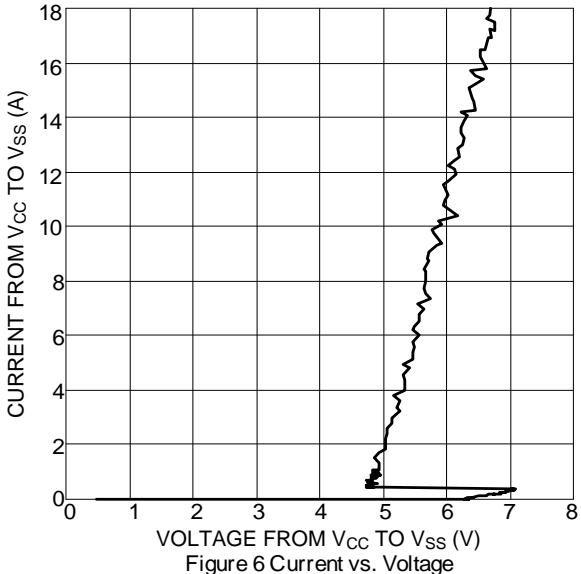
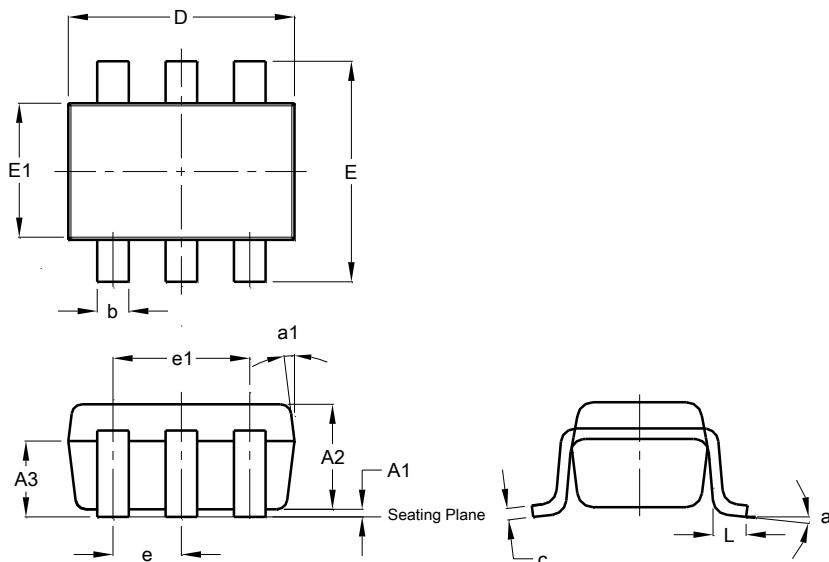


Figure 6 Current vs. Voltage

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

SOT26



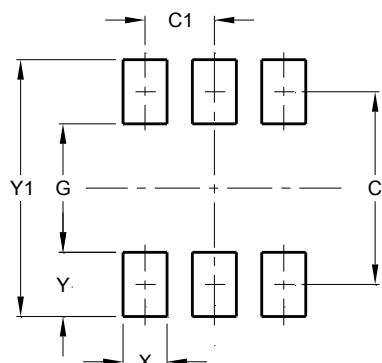
SOT26			
Dim	Min	Max	Typ
A1	0.013	0.10	0.05
A2	1.00	1.30	1.10
A3	0.70	0.80	0.75
b	0.35	0.50	0.38
c	0.10	0.20	0.15
D	2.90	3.10	3.00
e	—	—	0.95
e1	—	—	1.90
E	2.70	3.00	2.80
E1	1.50	1.70	1.60
L	0.35	0.55	0.40
a	—	—	8°
a1	—	—	7°

All Dimensions in mm

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

SOT26



Dimensions	Value (in mm)
C	2.40
C1	0.95
G	1.60
X	0.55
Y	0.80
Y1	3.20

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