11AA010/11LC010 11AA080/11LC080
11AA020/11LC020 11AA160/11LC160
11AA040/11LC040 11AA161/11LC161

1K-16K UNI/O® Serial EEPROM Family Data Sheet

Features:

- Single I/O, UNI/O® Serial Interface Bus
- Low-Power CMOS Technology:
  - 1 mA active current, typical
  - 1 µA standby current (max.) (I-temp)
- 128 x 8 through 2,048 x 8 Bit Organizations
- Schmitt Trigger Inputs for Noise Suppression
- Output Slope Control to Eliminate Ground Bounce
- 100 kbps Max. Bit Rate – Equivalent to 100 kHz Clock Frequency
- Self-Timed Write Cycle (including Auto-Erase)
- Page-Write Buffer for up to 16 Bytes
- STATUS Register for Added Control:
  - Write enable latch bit
  - Write-In-Progress bit
- Block Write Protection:
  - Protect none, 1/4, 1/2 or all of array
- Built-in Write Protection:
  - Power-on/off data protection circuitry
  - Write enable latch
- High Reliability:
  - Endurance: 1,000,000 erase/write cycles
  - Data retention: > 200 years
  - ESD protection: > 4,000V
- 3-lead SOT-23 and TO-92 Packages
- 4-lead Chip Scale Package
- 8-lead PDIP, SOIC, MSOP, TDFN Packages
- Pb-Free and RoHS Compliant
- Available Temperature Ranges:
  - Industrial (I): -40°C to +85°C
  - Automotive (E): -40°C to +125°C

Pin Function Table

Name	Function
SCIO	Serial Clock, Data Input/Output
VSS	Ground
VCC	Supply Voltage

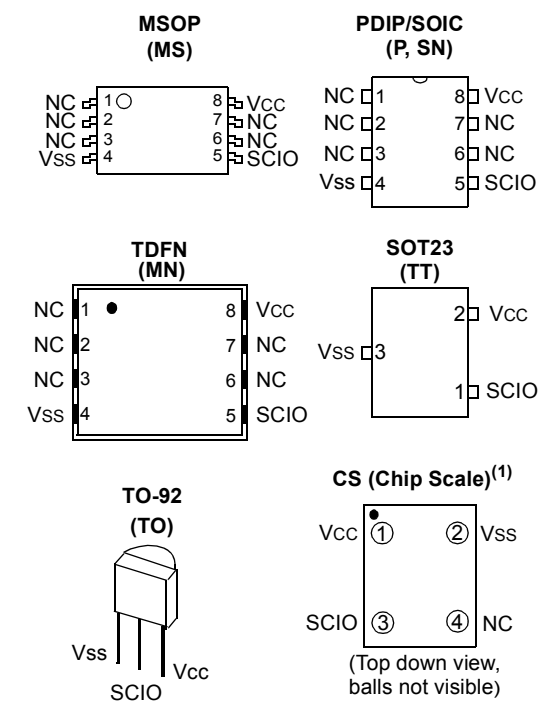
Description:

The Microchip Technology Inc. 11AAXXX/11LCXXX (11XX*) devices are a family of 1 Kbit through 16 Kbit Serial Electrically Erasable PROMs. The devices are organized in blocks of x8-bit memory and support the patented** single I/O UNI/O® serial bus. By using Manchester encoding techniques, the clock and data are combined into a single, serial bit stream (SCIO), where the clock signal is extracted by the receiver to correctly decode the timing and value of each bit.

Low-voltage design permits operation down to 1.8V (for 11AAXXX devices), with standby and active currents of only 1 uA and 1 mA, respectively.

The 11XX family is available in standard packages including 8-lead PDIP and SOIC, and advanced packaging including 3-lead SOT-23, 3-lead TO-92, 4-lead Chip Scale, 8-lead TDFN, and 8-lead MSOP.

Package Types (not to scale)



Note 1: Available in I-temp, "AA" only.

* 11XX is used in this document as a generic part number for the 11 series devices.

** Microchip's UNI/O® Bus products are covered by the following patent issued in the U.S.A.: 7,376,020.

DEVICE SELECTION TABLE

Part Number	Density (bits)	Organization	Vcc Range	Page Size (Bytes)	Temp. Ranges	Device Address	Packages
11LC010	1K	128 x 8	2.5-5.5V	16	I,E	0xA0	P, SN, MS, MN, TO, TT
11AA010	1K	128 x 8	1.8-5.5V	16	I	0xA0	P, SN, MS, MN, TO, TT, CS
11LC020	2K	256 x 8	2.5-5.5V	16	I,E	0xA0	P, SN, MS, MN, TO, TT
11AA020	2K	256 x 8	1.8-5.5V	16	I	0xA0	P, SN, MS, MN, TO, TT, CS
11LC040	4K	512 x 8	2.5-5.5V	16	I,E	0xA0	P, SN, MS, MN, TO, TT
11AA040	4K	512 x 8	1.8-5.5V	16	I	0xA0	P, SN, MS, MN, TO, TT, CS
11LC080	8K	1,024 x 8	2.5-5.5V	16	I,E	0xA0	P, SN, MS, MN, TO, TT
11AA080	8K	1,024 x 8	1.8-5.5V	16	I	0xA0	P, SN, MS, MN, TO, TT, CS
11LC160	16K	2,048 x 8	2.5-5.5V	16	I,E	0xA0	P, SN, MS, MN, TO, TT
11AA160	16K	2,048 x 8	1.8-5.5V	16	I	0xA0	P, SN, MS, MN, TO, TT,CS
11LC161	16K	2,048 x 8	2.5-5.5V	16	I, E	0xA1	P, SN, MS, MN, TO, TT
11AA161	16K	2,048 x 8	1.8-5.5V	16	I	0xA1	P, SN, MS, MN, TO, TT, CS

 © 2010 Microchip Technology Inc.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

V_{CC} 6.5V

SCIO w.r.t. V_{SS} ..... -0.6V to V_{CC}+1.0V

Storage temperature ..... -65°C to 150°C

Ambient temperature under bias ..... -40°C to 125°C

ESD protection on all pins ..... 4 kV

† NOTICE: Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Electrical Characteristics: Industrial (I): V_{CC} = 2.5V to 5.5V, T_A = -40°C to +85°C V_{CC} = 1.8V to 2.5V, T_A = -20°C to +85°C Automotive (E): V_{CC} = 2.5V to 5.5V, T_A = -40°C to +125°C			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
D1	V_{IH}	High-level input voltage	0.7*V_{CC}	V_{CC}+1	V	
D2	V_{IL}	Low-level input voltage	-0.3 -0.3	0.3*V_{CC} 0.2*V_{CC}	V V	$V_{CC} \geq$ 2.5V V_{CC} < 2.5V
D3	V_{HYS}	Hysteresis of Schmitt Trigger inputs (SCIO)	0.05*Vcc	—	V	$V_{CC} \geq$ 2.5V **(Note 1)**
D4	V_{OH}	High-level output voltage	V_{CC} -0.5 V_{CC} -0.5	— —	V V	I_{OH} = -300 μA, V_{CC} = 5.5V I_{OH} = -200 μA, Vcc = 2.5V
D5	V_{OL}	Low-level output voltage	— —	0.4 0.4	V V	I_{OI} = 300 μA, V_{CC} = 5.5V I_{OI} = 200 μA, Vcc = 2.5V
D6	I_O	Output current limit **(Note 2)**	— —	±4 ±3	mA mA	V_{CC} = 5.5V **(Note 1)** Vcc = 2.5V **(Note 1)**
D7	I_{LI}	Input leakage current (SCIO)	—	±1	μA	V_{IN} = V_{SS} or V_{CC}
D8	C_{INT}	Internal Capacitance (all inputs and outputs)	—	7	pF	T_A = 25°C, F_{CLK} = 1 MHz, V_{CC} = 5.0V **(Note 1)**
D9	I_{CC} Read	Read Operating Current	— —	3 1	mA mA	V_{CC}=5.5V; F_{BUS}=100 kHz, C_B=100 pF V_{CC}=2.5V; F_{BUS}=100 kHz, C_B=100 pF
D10	I_{CC} Write	Write Operating Current	— —	5 3	mA mA	V_{CC} = 5.5V V_{CC} = 2.5V
D11	Iccs	Standby Current	— —	5 1	μA μA	V_{CC} = 5.5V, T_A = 125°C V_{CC} = 5.5V, T_A = 85°C
D12	I_{CCI}	Idle Mode Current	—	50	μA	V_{CC} = 5.5V

Note 1: This parameter is periodically sampled and not 100% tested.

2: The SCIO output driver impedance will vary to ensure I_O is not exceeded.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): V_{CC} = 2.5V to 5.5V T_A = -40°C to +85°C V_{CC} = 1.8V to 2.5V T_A = -20°C to +85°C Automotive (E): V_{CC} = 2.5V to 5.5V T_A = -40°C to +125°C			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
1	F_{BUS}	Serial bus frequency	10	100	kHz	—
2	T_E	Bit period	10	100	µs	—
3	T_{IJIT}	Input edge jitter tolerance	—	±0.08	UI	**(Note 3)**
4	F_{DRIFT}	Serial bus frequency drift rate tolerance	—	±0.75	% per byte	—
5	F_{DEV}	Serial bus frequency drift limit	—	±5	% per command	—
6	T_{OJIT}	Output edge jitter	—	±0.25	UI	**(Note 3)**
7	T_R	SCIO input rise time **(Note 1)**	—	100	ns	—
8	T_F	SCIO input fall time **(Note 1)**	—	100	ns	—
9	T_{STBY}	Standby pulse time	600	—	µs	—
10	T_{SS}	Start header setup time	10	—	µs	—
11	T_{HDR}	Start header low pulse time	5	—	µs	—
12	T_{SP}	Input filter spike suppression (SCIO)	—	50	ns	**(Note 1)**
13	T_{WC}	Write cycle time (byte or page)	— —	5 10	ms ms	Write, WRSR commands ERAL, SETAL commands
14	—	Endurance (per page)	1M	—	cycles	25°C, V_{CC} = 5.5V **(Note 2)**

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained on Microchip's web site: www.microchip.com.

3: A Unit Interval (UI) is equal to 1-bit period (T_E) at the current bus frequency.

TABLE 1-3: AC TEST CONDITIONS

AC Waveform:	
V_{LO} = 0.2V	
V_{HI} = V_{CC} - 0.2V	
C_L = 100 pF	
Timing Measurement Reference Level	
Input	0.5 V_{CC}
Output	0.5 V_{CC}

 © 2010 Microchip Technology Inc.

FIGURE 1-1: BUS TIMING – START HEADER

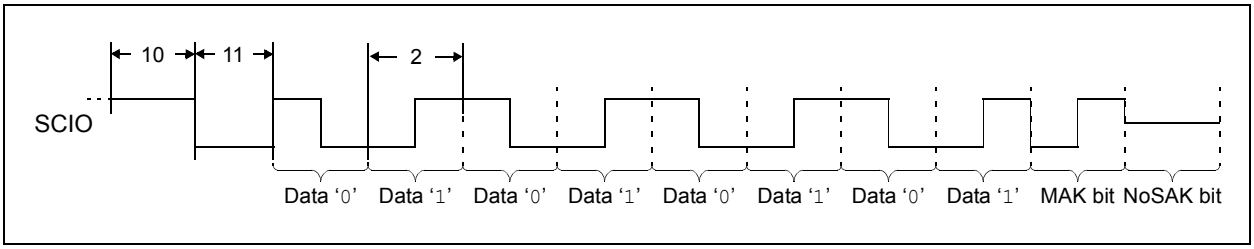


FIGURE 1-2: BUS TIMING – DATA

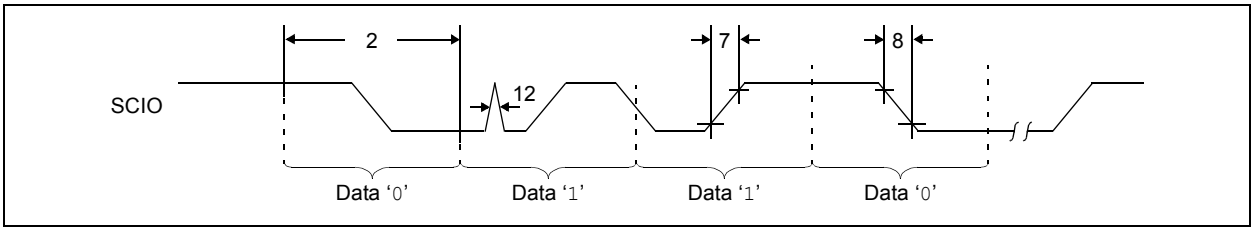


FIGURE 1-3: BUS TIMING – STANDBY PULSE

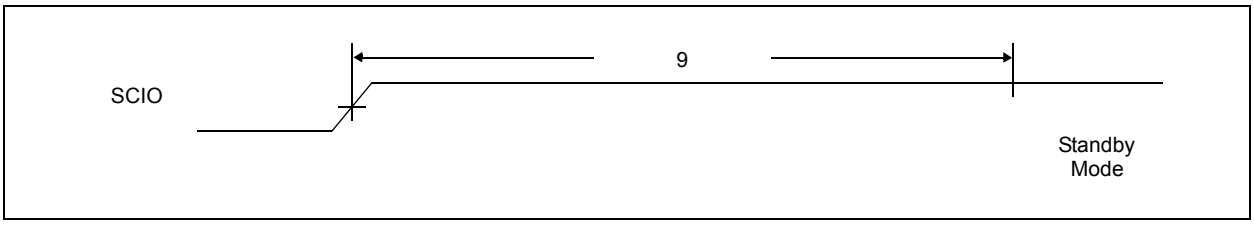
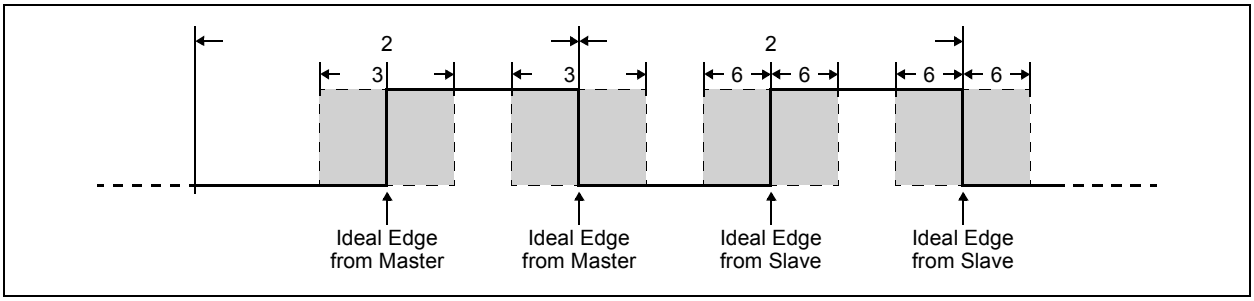


FIGURE 1-4: BUS TIMING – JITTER



2.0 FUNCTIONAL DESCRIPTION

2.1 Principles of Operation

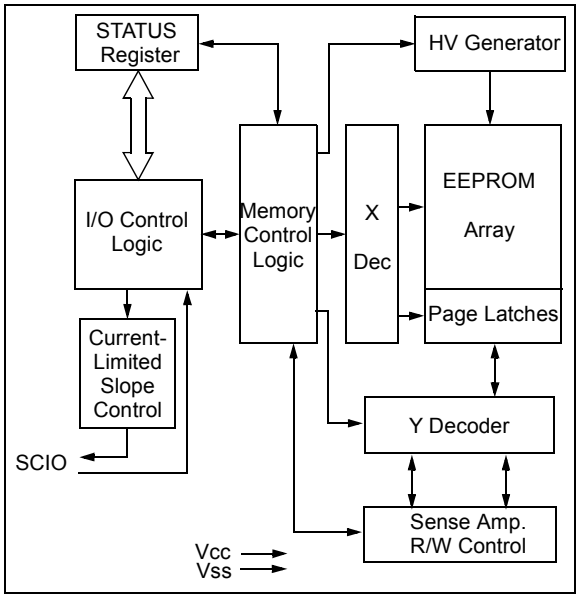
The 11XX family of serial EEPROMs support the UNI/O® protocol. They can be interfaced with microcontrollers, including Microchip's PIC® microcontrollers, ASICs, or any other device with an available discrete I/O line that can be configured properly to match the UNI/O protocol.

The 11XX devices contain an 8-bit instruction register. The devices are accessed via the SCIO pin.

Table 4-1 contains a list of the possible instruction bytes and format for device operation. All instructions, addresses, and data are transferred MSb first, LSb last.

Data is embedded into the I/O stream through Manchester encoding. The bus is controlled by a master device which determines the clock period, controls the bus access and initiates all operations, while the 11XX works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is active.

FIGURE 2-1: BLOCK DIAGRAM



 © 2010 Microchip Technology Inc.

3.0 BUS CHARACTERISTICS

3.1 Standby Pulse

When the master has control of SCIO, a standby pulse can be generated by holding SCIO high for T_{STBY}. At this time, the 11XX will reset and return to Standby mode. Subsequently, a high-to-low transition on SCIO (the first low pulse of the header) will return the device to the active state.

Once a command is terminated satisfactorily (i.e., via a NoMAK/SAK combination during the Acknowledge sequence), performing a standby pulse is not required to begin a new command as long as the device to be selected is the same device selected during the previous command. However, a period of T_{SS} must be observed after the end of the command and before the beginning of the start header. After T_{SS}, the start header (including T_{HDR} low pulse) can be transmitted in order to begin the new command.

If a command is terminated in any manner other than a NoMAK/SAK combination, then the master must perform a standby pulse before beginning a new command, regardless of which device is to be selected.

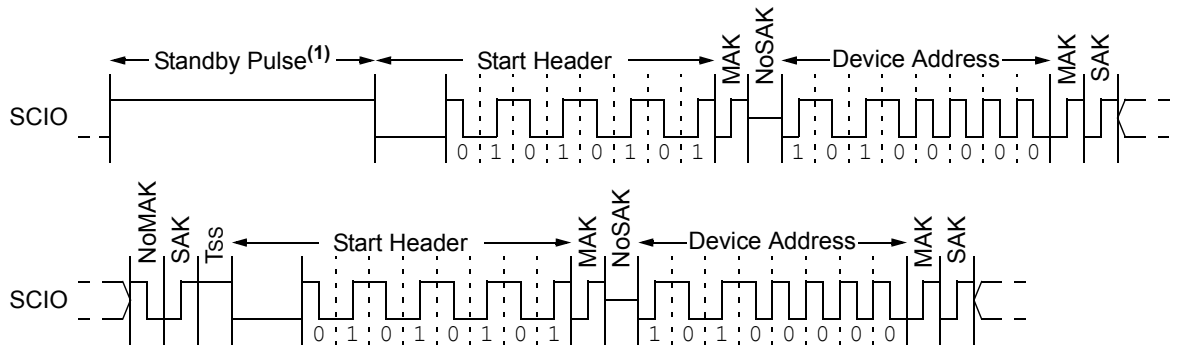
> **Note:** After a POR/BOR event occurs, a low-to-high transition on SCIO must be generated before proceeding with communication, including a standby pulse.

An example of two consecutive commands is shown in Figure 3-1. Note that the device address is the same for both commands, indicating that the same device is being selected both times.

A standby pulse cannot be generated while the slave has control of SCIO. In this situation, the master must wait for the slave to finish transmitting and to release SCIO before the pulse can be generated.

If, at any point during a command, an error is detected by the master, a standby pulse should be generated and the command should be performed again.

FIGURE 3-1: CONSECUTIVE COMMANDS EXAMPLE



Note 1: After a POR/BOR event, a low-to-high transition on SCIO is required to occur before the first standby pulse.

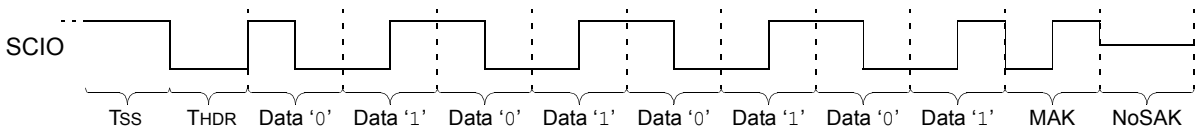
3.2 Start Data Transfer

All operations must be preceded by a start header. The start header consists of holding SCIO low for a period of T_{HDR}, followed by transmitting an 8-bit '01010101' code. This code is used to synchronize the slave's internal clock period with the master's clock period, so accurate timing is very important.

When a standby pulse is not required (i.e., between successive commands to the same device), a period of T_{SS} must be observed after the end of the command and before the beginning of the start header.

Figure 3-2 shows the waveform for the start header, including the required Acknowledge sequence at the end of the byte.

FIGURE 3-2: START HEADER



3.3 Acknowledge

An Acknowledge routine occurs after each byte is transmitted, including the start header. This routine consists of two bits. The first bit is transmitted by the master, and the second bit is transmitted by the slave.

> **Note:** A MAK must always be transmitted following the start header.

The Master Acknowledge, or MAK, is signified by transmitting a '1', and informs the slave that the current operation is to be continued. Conversely, a Not Acknowledge, or NoMAK, is signified by transmitting a '0', and is used to end the current operation (and initiate the write cycle for write operations).

> **Note:** When a NoMAK is used to end a WRITE or WRSR instruction, the write cycle is not initiated if no bytes of data have been received.

The slave Acknowledge, or SAK, is also signified by transmitting a '1', and confirms proper communication. However, unlike the NoMAK, the NoSAK is signified by the lack of a middle edge during the bit period.

> **Note:** In order to guard against bus contention, a NoSAK will occur after the start header.

A NoSAK will occur for the following events:

- Following the start header
- Following the device address, if no slave on the bus matches the transmitted address
- Following the command byte, if the command is invalid, including Read, CRRD, Write, WRSR, SETAL, and ERAL during a write cycle.
- If the slave becomes out of sync with the master
- If a command is terminated prematurely by using a NoMAK, with the exception of immediately after the device address.

See Figure 3.3 and Figure 3-4 for details.

If a NoSAK is received from the slave after any byte (except the start header), an error has occurred. The master should then perform a standby pulse and begin the desired command again.

FIGURE 3-3: ACKNOWLEDGE ROUTINE

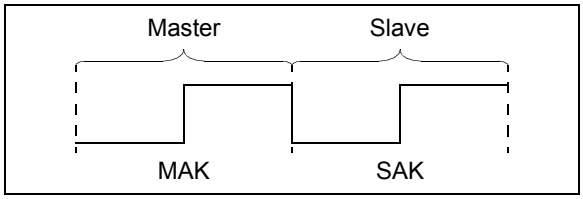
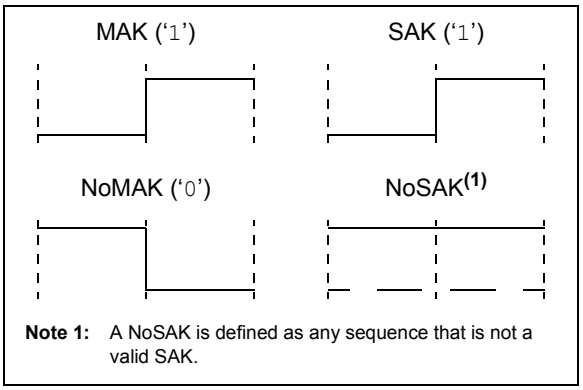


FIGURE 3-4: ACKNOWLEDGE BITS



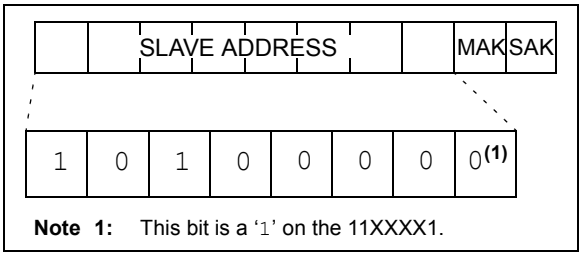
Note 1: A NoSAK is defined as any sequence that is not a valid SAK.

3.4 Device Addressing

A device address byte is the first byte received from the master device following the start header. The device address byte consists of a four-bit family code, for the 11XX this is set as '1010'. The last four bits of the device address byte are the device code, which is hardwired to '0000' on the 11XXXX0 devices.

The device code on 11XXXX1 devices is hardwired to '0001'. This allows both 11XXXX0 and 11XXXX1 devices to be used on the same bus without address conflicts.

FIGURE 3-5: DEVICE ADDRESS BYTE ALLOCATION



Note 1: This bit is a '1' on the 11XXXX1.

3.5 Bus Conflict Protection

To help guard against high current conditions arising from bus conflicts, the 11XX features a current-limited output driver. The I_{OL} and I_{OH} specifications describe the maximum current that can be sunk or sourced, respectively, by the SCIO pin. The 11XX will vary the output driver impedance to ensure that the maximum current level is not exceeded.

 © 2010 Microchip Technology Inc.

3.6 Device Standby

The 11XX features a low-power Standby mode during which the device is waiting to begin a new command. A high-to-low transition on SCIO will exit low-power mode and prepare the device for receiving the start header.

Standby mode will be entered upon the following conditions:

- A NoMAK followed by a SAK (i.e., valid termination of a command)
- Reception of a standby pulse

Note: In the case of the `WRITE`, `WRSR`, `SETAL`, or `ERAL` commands, the write cycle is initiated upon receipt of the NoMAK, assuming all other write requirements have been met.

3.7 Device Idle

The 11XX features an Idle mode during which all serial data is ignored until a standby pulse occurs. Idle mode will be entered upon the following conditions:

- Invalid device address
- Invalid command byte, including Read, CRRD, Write, WRSR, SETAL and ERAL during a write cycle.
- Missed edge transition
- Reception of a MAK following a `WREN`, `WRDI`, `SETAL`, or `ERAL` command byte
- Reception of a MAK following the data byte of a `WRSR` command

An invalid start header will indirectly cause the device to enter Idle mode. Whether or not the start header is invalid cannot be detected by the slave, but will prevent the slave from synchronizing properly with the master. If the slave is not synchronized with the master, an edge transition will be missed, thus causing the device to enter Idle mode.

3.8 Synchronization

At the beginning of every command, the 11XX utilizes the start header to determine the master's bus clock period. This period is then used as a reference for all subsequent communication within that command.

The 11XX features re-synchronization circuitry which will monitor the position of the middle data edge during each MAK bit and subsequently adjust the internal time reference in order to remain synchronized with the master.

There are two variables which can cause the 11XX to lose synchronization. The first is frequency drift, defined as a change in the bit period, T_E. The second is edge jitter, which is a single occurrence change in the position of an edge within a bit period, while the bit period itself remains constant.

3.8.1 FREQUENCY DRIFT

Within a system, there is a possibility that frequencies can drift due to changes in voltage, temperature, etc. The re-synchronization circuitry provides some tolerance for such frequency drift. The tolerance range is specified by two parameters, F_{DRIFT} and F_{DEV}. F_{DRIFT} specifies the maximum tolerable change in bus frequency per byte. F_{DEV} specifies the overall limit in frequency deviation within an operation (i.e., from the end of the start header until communication is terminated for that operation). The start header at the beginning of the next operation will reset the re-synchronization circuitry and allow for another F_{DEV} amount of frequency drift.

3.8.2 EDGE JITTER

Ensuring that edge transitions from the master always occur exactly in the middle or end of the bit period is not always possible. Therefore, the re-synchronization circuitry is designed to provide some tolerance for edge jitter.

The 11XX adjusts its phase every MAK bit, so T_{IJIT} specifies the maximum allowable peak-to-peak jitter relative to the previous MAK bit. Since the position of the previous MAK bit would be difficult to measure by the master, the minimum and maximum jitter values for a system should be considered the worst-case. These values will be based on the execution time for different branch paths in software, jitter due to thermal noise, etc.

The difference between the minimum and maximum values, as a percentage of the bit period, should be calculated and then compared against T_{IJIT} to determine jitter compliance.

Note: Because the 11XX only re-synchronizes during the MAK bit, the overall ability to remain synchronized depends on a combination of frequency drift and edge jitter (i.e., if the MAK bit edge is experiencing the maximum allowable edge jitter, then there is no room for frequency drift). Conversely, if the frequency has drifted to the maximum amount tolerable within a byte, then no edge jitter can be present.

4.0 DEVICE COMMANDS

After the device address byte, a command byte must be sent by the master to indicate the type of operation to be performed. The code for each instruction is listed in Table 4-1.

TABLE 4-1: INSTRUCTION SET

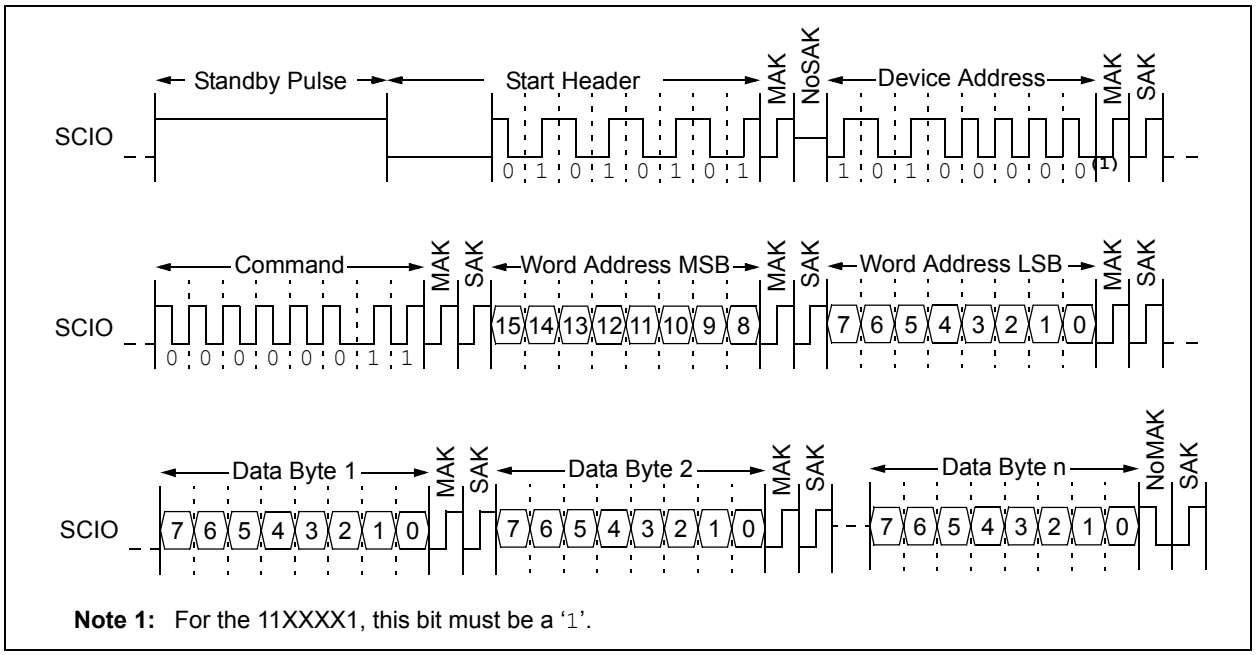
Instruction Name	Instruction Code	Hex Code	Description
READ	0000 0011	0x03	Read data from memory array beginning at specified address
CRRD	0000 0110	0x06	Read data from current location in memory array
WRITE	0110 1100	0x6C	Write data to memory array beginning at specified address
WREN	1001 0110	0x96	Set the write enable latch (enable write operations)
WRDI	1001 0001	0x91	Reset the write enable latch (disable write operations)
RDSR	0000 0101	0x05	Read STATUS register
WRSR	0110 1110	0x6E	Write STATUS register
ERAL	0110 1101	0x6D	Write ‘0x00’ to entire array
SETAL	0110 0111	0x67	Write ‘0xFF’ to entire array

4.1 Read Instruction

The Read command allows the master to access any memory location in a random manner. After the READ instruction has been sent to the slave, the two bytes of the Word Address are transmitted, with an Acknowledge sequence being performed after each byte. Then, the slave sends the first data byte to the master. If more data is to be read, the master sends a MAK, indicating that the slave should output the next data byte. This continues until the master sends a NoMAK, which ends the operation.

To provide sequential reads in this manner, the 11XX contains an internal Address Pointer which is incremented by one after the transmission of each byte. This Address Pointer allows the entire memory contents to be serially read during one operation. When the highest address is reached, the Address Pointer rolls over to address ‘0x000’ if the master chooses to continue the operation by providing a MAK.

FIGURE 4-1: READ COMMAND SEQUENCE



Note 1: For the 11XXXX1, this bit must be a ‘1’.

 © 2010 Microchip Technology Inc.

4.2 Current Address Read (CRRD) Instruction

The internal address counter featured on the 11XX maintains the address of the last memory array location accessed. The CRRD instruction allows the master to read data back beginning from this current location. Consequently, no word address is provided upon issuing this command.

Note that, except for the initial word address, the READ and CRRD instructions are identical, including the ability to continue requesting data through the use of MAKs in order to sequentially read from the array.

As with the READ instruction, the CRRD instruction is terminated by transmitting a NoMAK.

Table 4-2 lists the events upon which the internal address counter is modified.

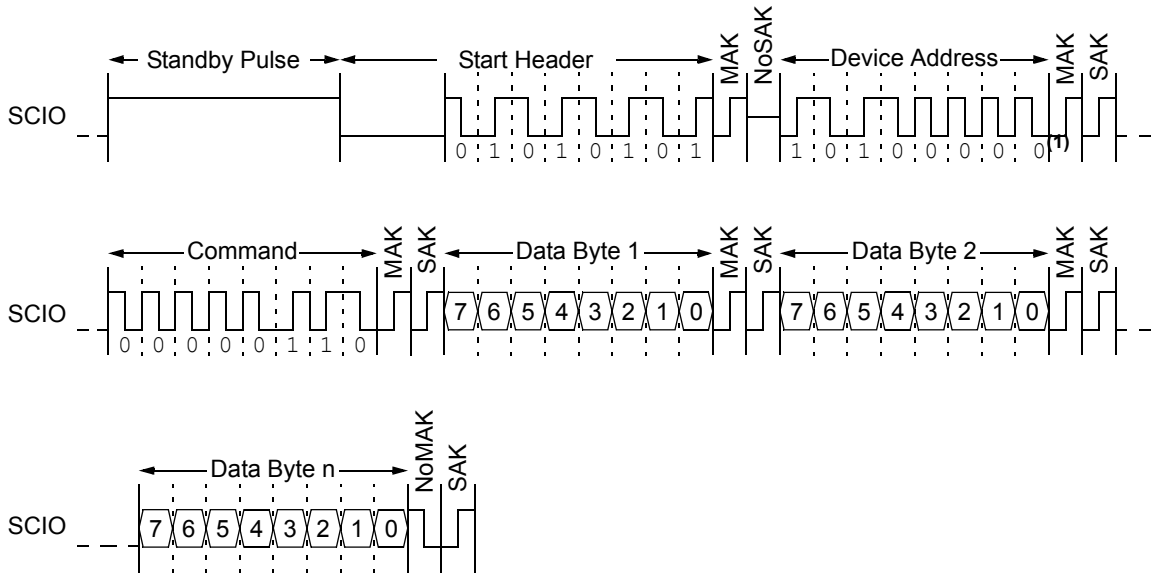
TABLE 4-2: INTERNAL ADDRESS COUNTER

Command	Event	Action
—	Power-on Reset	Counter is undefined
READ or WRITE	MAK edge following each Address byte	Counter is updated with newly received value
READ, WRITE, or CRRD	MAK/NoMAK edge following each data byte	Counter is incremented by 1

Note: If, following each data byte in a READ, WRITE, or CRRD instruction, neither a MAK nor a NoMAK edge is received (i.e., if a standby pulse occurs instead), the internal address counter will not be incremented.

Note: During a Write command, once the last data byte for a page has been loaded, the internal Address Pointer will rollover to the beginning of the selected page.

FIGURE 4-2: CRRD COMMAND SEQUENCE



Note 1: For the 11XXXX1, this bit must be a '1'.

4.3 Write Instruction

Prior to any attempt to write data to the 11XX, the write enable latch must be set by issuing the `WREN` instruction (see Section 4.4).

Once the write enable latch is set, the user may proceed with issuing a `WRITE` instruction (including the header and device address bytes) followed by the MSB and LSB of the Word Address. Once the last Acknowledge sequence has been performed, the master transmits the data byte to be written.

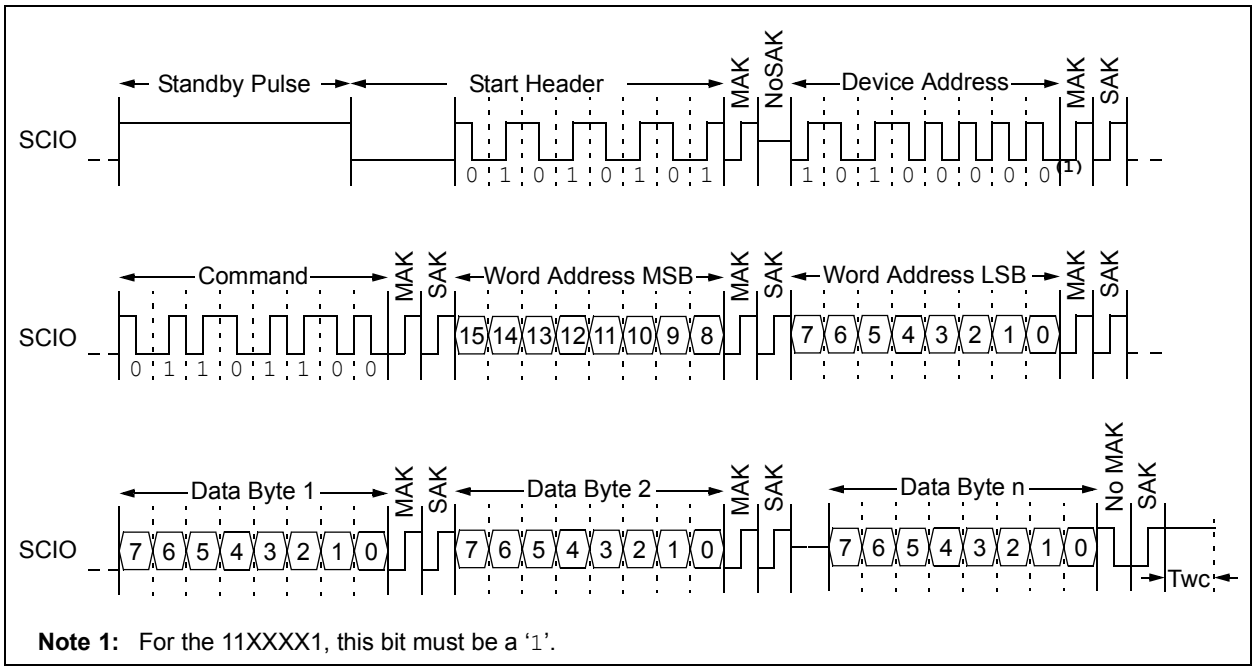
The 11XX features a 16-byte page buffer, meaning that up to 16 bytes can be written at one time. To utilize this feature, the master can transmit up to 16 data bytes to the 11XX, which are temporarily stored in the page buffer. After each data byte, the master sends a MAK, indicating whether or not another data byte is to follow. A NoMAK indicates that no more data is to follow, and as such will initiate the internal write cycle.

> **Note:** If a NoMAK is generated before any data has been provided, or if a standby pulse occurs before the NoMAK is generated, the 11XX will be reset, and the write cycle will not be initiated.

Upon receipt of each word, the four lower-order Address Pointer bits are internally incremented by one. The higher-order bits of the word address remain constant. If the master should transmit data past the end of the page, the address counter will roll over to the beginning of the page, where further received data will be written.

> **Note:** Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page size (16 bytes) and end at addresses that are integer multiples of the page size minus 1. As an example, the page that begins at address 0x30 ends at address 0x3F. If a page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

FIGURE 4-3: WRITE COMMAND SEQUENCE



Note 1: For the 11XXXX1, this bit must be a '1'.

 © 2010 Microchip Technology Inc.

4.4 Write Enable (WREN) and Write Disable (WRDI) Instructions

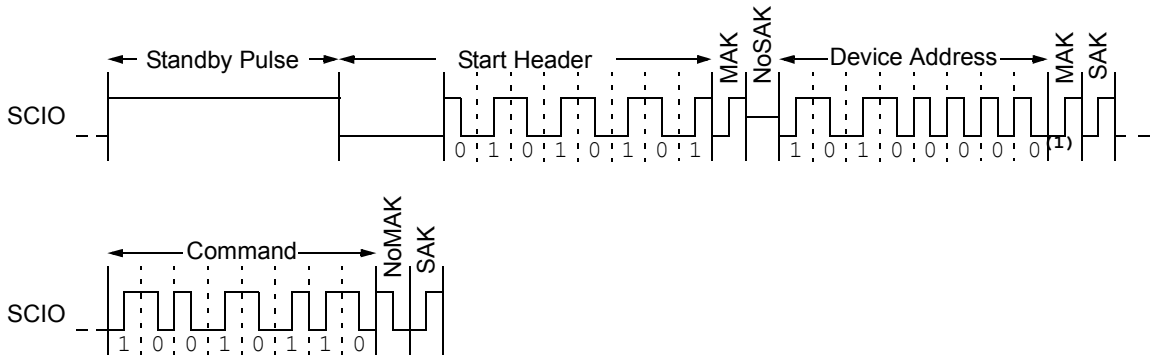
The 11XX contains a write enable latch. See Table 6-1 for the Write-Protect Functionality Matrix. This latch must be set before any write operation will be completed internally. The WREN instruction will set the latch, and the WRDI instruction will reset the latch.

Note: The WREN and WRDI instructions must be terminated with a NoMAK following the command byte. If a NoMAK is not received at this point, the command will be considered invalid, and the device will go into Idle mode without responding with a SAK or executing the command.

The following is a list of conditions under which the write enable latch will be reset:

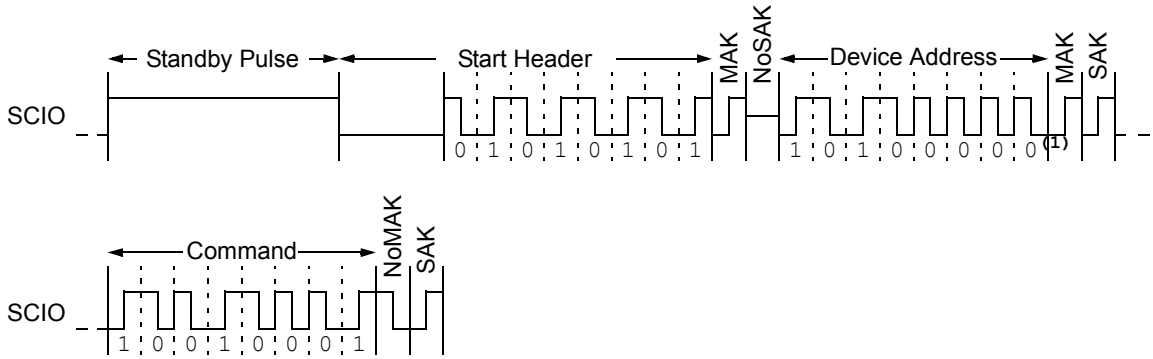
- Power-up
- WRDI instruction successfully executed
- WRSR instruction successfully executed
- WRITE instruction successfully executed
- ERAL instruction successfully executed
- SETAL instruction successfully executed

FIGURE 4-4: WRITE ENABLE COMMAND SEQUENCE



Note 1: For the 11XXXX1, this bit must be a '1'.

FIGURE 4-5: WRITE DISABLE COMMAND SEQUENCE



Note 1: For the 11XXXX1, this bit must be a '1'.

4.5 Read Status Register (RDSR) Instruction

The RDSR instruction provides access to the STATUS register. The STATUS register may be read at any time, even during a write cycle. The STATUS register is formatted as follows:

7	6	5	4	3	2	1	0
X	X	X	X	BP1	BP0	WEL	WIP
Note: Bits 4-7 are don't cares, and will read as '0'.							

The **Write-In-Process (WIP)** bit indicates whether the 11XX is busy with a write operation. When set to a '1', a write is in progress, when set to a '0', no write is in progress. This bit is read-only.

The **Write Enable Latch (WEL)** bit indicates the status of the write enable latch. When set to a '1', the latch allows writes to the array, when set to a '0', the latch prohibits writes to the array. This bit is set and cleared using the WREN and WRDI instructions, respectively. This bit is read-only for any other instruction.

The **Block Protection (BP0 and BP1)** bits indicate which blocks are currently write-protected. These bits are set by the user through the WRSR instruction. These bits are nonvolatile.

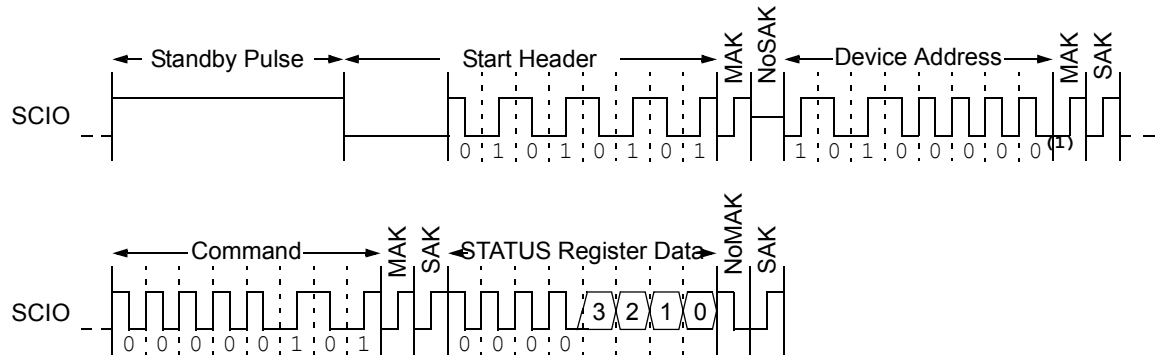
> **Note:** If Read Status Register command is initiated while the 11XX is currently executing an internal write cycle on the STATUS register, the new Block Protection bit values will be read during the entire command.

The WIP and WEL bits will update dynamically (asynchronous to issuing the RDSR instruction). Furthermore, after the STATUS register data is received, the master can provide a MAK during the Acknowledge sequence to request that the data be transmitted again. This allows the master to continuously monitor the WIP and WEL bits without the need to issue another full command.

Once the master is finished, it provides a NoMAK to end the operation.

> **Note:** The current drawn for a Read Status Register command during a write cycle is a combination of the ICC Read and ICC Write operating currents.

FIGURE 4-6: READ STATUS REGISTER COMMAND SEQUENCE



Note 1: For the 11XXXX1, this bit must be a '1'.

Note 2: The STATUS register data can continuously be read, or polled, by transmitting a MAK in place of the NoMAK.

 © 2010 Microchip Technology Inc.

4.6 Write Status Register (WRSR) Instruction

The WRSR instruction allows the user to select one of four levels of protection for the array by writing to the appropriate bits in the STATUS register. The array is divided up into four segments. The user has the ability to write-protect none, one, two, or all four of the segments of the array. The partitioning is controlled as illustrated in Table 4-3.

After transmitting the STATUS register data, the master must transmit a NoMAK during the Acknowledge sequence in order to initiate the internal write cycle.

Note: The WRSR instruction must be terminated with a NoMAK following the data byte. If a NoMAK is not received at this point, the command will be considered invalid, and the device will go into Idle mode without responding with a SAK or executing the command.

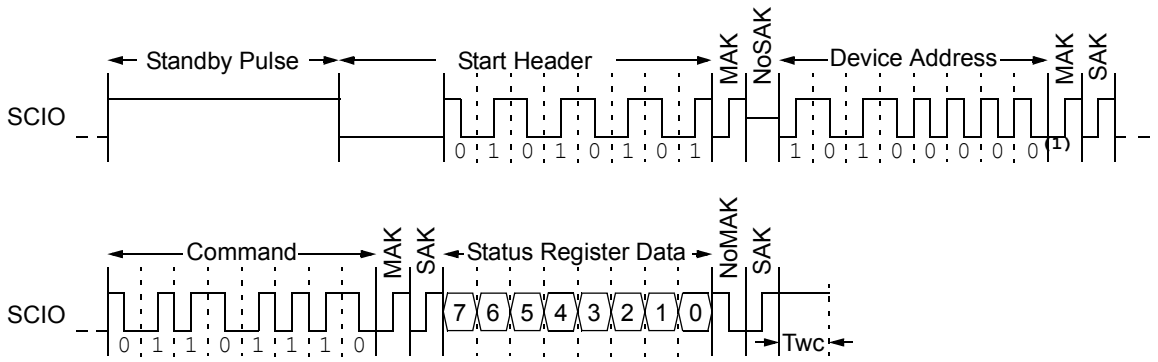
TABLE 4-3: ARRAY PROTECTION

BP1	BP0	Address Ranges Write-Protected	Address Ranges Unprotected
0	0	None	All
0	1	Upper 1/4	Lower 3/4
1	0	Upper 1/2	Lower 1/2
1	1	All	None

TABLE 4-4: PROTECTED ARRAY ADDRESS LOCATIONS

Density	Upper 1/4	Upper 1/2	All Sectors
1K	60h-7Fh	40h-7Fh	00h-7Fh
2K	C0h-FFh	80h-FFh	00h-FFh
4K	180h-1FFh	100h-1FFh	000h-1FFh
8K	300h-3FFh	200h-3FFh	000h-3FFh
16K	600h-7FFh	400h-7FFh	000h-7FFh

FIGURE 4-7: WRITE STATUS REGISTER COMMAND SEQUENCE



Note 1: For the 11XXXX1, this bit must be a '1'.

4.7 Erase All (ERAL) Instruction

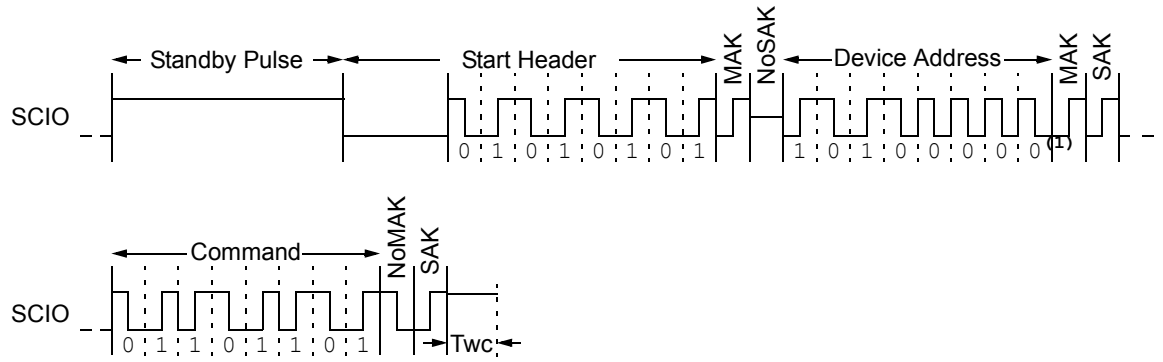
The ERAL instruction allows the user to write ‘0x00’ to the entire memory array with one command. Note that the write enable latch (WEL) must first be set by issuing the WREN instruction.

Once the write enable latch is set, the user may proceed with issuing a ERAL instruction (including the header and device address bytes). Immediately after the NoMAK bit has been transmitted by the master, the internal write cycle is initiated, during which time all words of the memory array are written to ‘0x00’.

The ERAL instruction is ignored if either of the Block Protect bits (BP0, BP1) are not 0, meaning 1/4, 1/2, or all of the array is protected.

> **Note:** The ERAL instruction must be terminated with a NoMAK following the command byte. If a NoMAK is not received at this point, the command will be considered invalid, and the device will go into Idle mode without responding with a SAK or executing the command.

FIGURE 4-8: ERASE ALL COMMAND SEQUENCE



Note 1: For the 11XXXX1, this bit must be a ‘1’.

4.8 Set All (SETAL) Instruction

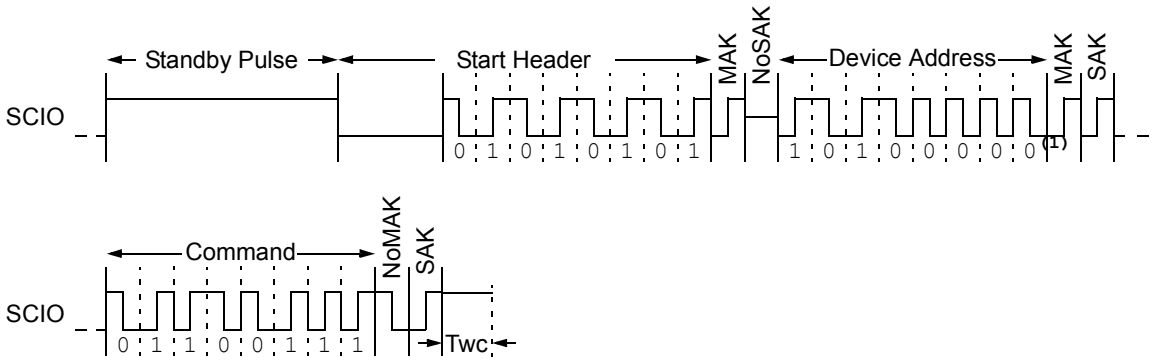
The SETAL instruction allows the user to write ‘0xFF’ to the entire memory array with one command. Note that the write enable latch (WEL) must first be set by issuing the WREN instruction.

Once the write enable latch is set, the user may proceed with issuing a SETAL instruction (including the header and device address bytes). Immediately after the NoMAK bit has been transmitted by the master, the internal write cycle is initiated, during which time all words of the memory array are written to ‘0xFF’.

The SETAL instruction is ignored if either of the Block Protect bits (BP0, BP1) are not 0, meaning 1/4, 1/2, or all of the array is protected.

> **Note:** The SETAL instruction must be terminated with a NoMAK following the command byte. If a NoMAK is not received at this point, the command will be considered invalid, and the device will go into Idle mode without responding with a SAK or executing the command.

FIGURE 4-9: SET ALL COMMAND SEQUENCE



Note 1: For the 11XXXX1, this bit must be a ‘1’.

 © 2010 Microchip Technology Inc.

5.0 DATA PROTECTION

The following protection has been implemented to prevent inadvertent writes to the array:

- The Write Enable Latch (WEL) is reset on power-up
- A Write Enable (`WREN`) instruction must be issued to set the write enable latch
- After a write, ERAL, SETAL, or WRSR command, the write enable latch is reset
- Commands to access the array or write to the status register are ignored during an internal write cycle and programming is not affected

6.0 POWER-ON STATE

The 11XX powers on in the following state:

- The device is in low-power Shutdown mode, requiring a low-to-high transition on SCIO to enter Idle mode
- The Write Enable Latch (WEL) is reset
- The internal Address Pointer is undefined
- A low-to-high transition, standby pulse and subsequent high-to-low transition on SCIO (the first low pulse of the header) are required to enter the active state

TABLE 6-1: WRITE PROTECT FUNCTIONALITY MATRIX

WEL	Protected Blocks	Unprotected Blocks	Status Register
0	Protected	Protected	Protected
1	Protected	Writable	Writable

7.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 7-1.

TABLE 7-1: PIN FUNCTION TABLE

Name	3-pin SOT-23	3-pin TO-92	4-pin CS	8-pin PDIP/SOIC/ MSOP/TDFN	Description
SCIO	1	2	3	5	Serial Clock, Data Input/Output
VCC	2	3	1	8	Supply Voltage
VSS	3	1	2	4	Ground
NC	—	—	4	1,2,3,6,7	No Internal Connection

7.1 Serial Clock, Data Input/Output (SCIO)

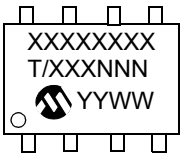
SCIO is a bidirectional pin used to transfer commands and addresses into, as well as data into and out of, the device. The serial clock is embedded into the data stream through Manchester encoding. Each bit is represented by a signal transition at the middle of the bit period.

 © 2010 Microchip Technology Inc.

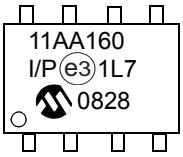
8.0 PACKAGING INFORMATION

8.1 Package Marking Information

8-Lead PDIP



Example:

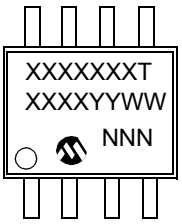


8-Lead PDIP Package Marking (Pb-Free)			
Device	**Line 1 Marking**	**Device**	**Line 1 Marking**
11AA010	11AA010	11LC010	11LC010
11AA020	11AA020	11LC020	11LC020
11AA040	11AA040	11LC040	11LC040
11AA080	11AA080	11LC080	11LC080
11AA160	11AA160	11LC160	11LC160
11AA161	11AA161	11LC161	11LC161
Note: T = Temperature Grade (I, E)			

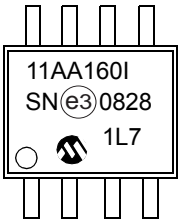
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead SOIC



Example:

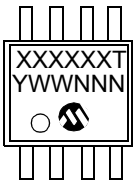


8-Lead SOIC Package Marking (Pb-Free)			
Device	**Line 1 Marking**	**Device**	**Line 1 Marking**
11AA010	11AA010T	11LC010	11LC010T
11AA020	11AA020T	11LC020	11LC020T
11AA040	11AA040T	11LC040	11LC040T
11AA080	11AA080T	11LC080	11LC080T
11AA160	11AA160T	11LC160	11LC160T
11AA161	11AA161T	11LC161	11LC161T
Note: T = Temperature Grade (I, E)			

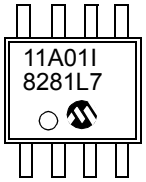
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.	

 © 2010 Microchip Technology Inc.

8-Lead MSOP (150 mil)



Example:

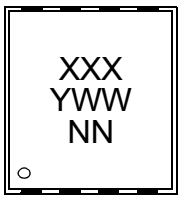


8-Lead MSOP Package Marking (Pb-Free)			
Device	**Line 1 Marking**	**Device**	**Line 1 Marking**
11AA010	11A01T	11LC010	11L01T
11AA020	11A02T	11LC020	11L02T
11AA040	11A04T	11LC040	11L04T
11AA080	11A08T	11LC080	11L08T
11AA160	11AAT	11LC160	11LAT
11AA161	11AA1T	11LC161	11LA1T
Note: T = Temperature Grade (I, E)			

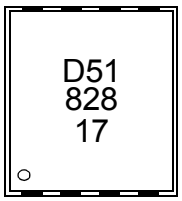
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead 2x3 TDFN



Example:

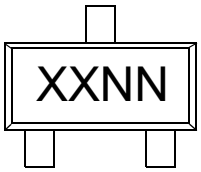


8-Lead 2x3 TDFN Package Marking (Pb-Free)				
Device	**I-Temp Marking**	**Device**	**I-Temp Marking**	**E-Temp Marking**
11AA010	D11	11LC010	D14	D15
11AA020	D21	11LC020	D24	D25
11AA040	D31	11LC040	D34	D35
11AA080	D41	11LC080	D44	D45
11AA160	D51	11LC160	D54	D55
11AA161	D5D	11LC161	D5G	D5H

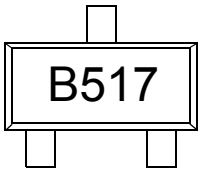
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.	

 © 2010 Microchip Technology Inc.

3-Lead SOT-23



Example:



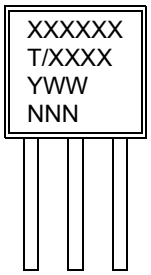
3-Lead SOT-23 Package Marking (Pb-Free)				
Device	**I-Temp Marking**	**Device**	**I-Temp Marking**	**E-Temp Marking**
11AA010	B1NN	11LC010	M1NN	N1NN
11AA020	B2NN	11LC020	M2NN	N2NN
11AA040	B3NN	11LC040	M3NN	N3NN
11AA080	B4NN	11LC080	M4NN	N4NN
11AA160	B5NN	11LC160	M5NN	N5NN
11AA161	B0NN	11LC161	M0NN	N0NN

Legend:

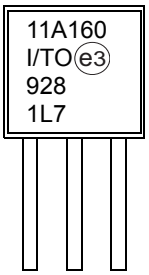
XX...X	Customer-specific information
Y	Year code (last digit of calendar year)
YY	Year code (last 2 digits of calendar year)
WW	Week code (week of January 1 is week ‘01’)
NNN	Alphanumeric traceability code
(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

3-Lead TO-92



Example:



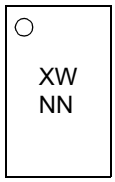
3-Lead TO-92 Package Marking (Pb-Free)			
Device	**Line 1 Marking**	**Device**	**Line 1 Marking**
11AA010	11A010	11LC010	11L010
11AA020	11A020	11LC020	11L020
11AA040	11A040	11LC040	11L040
11AA080	11A080	11LC080	11L080
11AA160	11A160	11LC160	11L160
11AA161	11A161	11LC161	11L161
Note: T = Temperature Grade (I, E)			

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

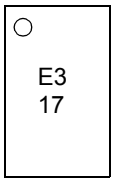
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

 © 2010 Microchip Technology Inc.

4-Lead Chip Scale



Example:



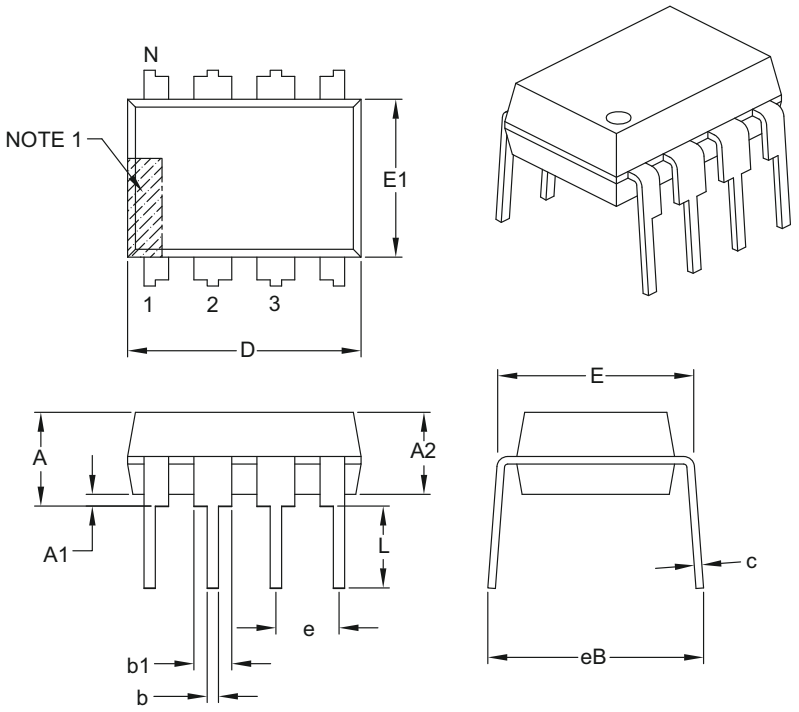
4-Lead Chip Scale Package Marking (Pb-Free)	
Device	**Line 1 Marking**
11AA010	AW
11AA020	BW
11AA040	CW
11AA080	DW
11AA160	EW
11AA161	HW

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

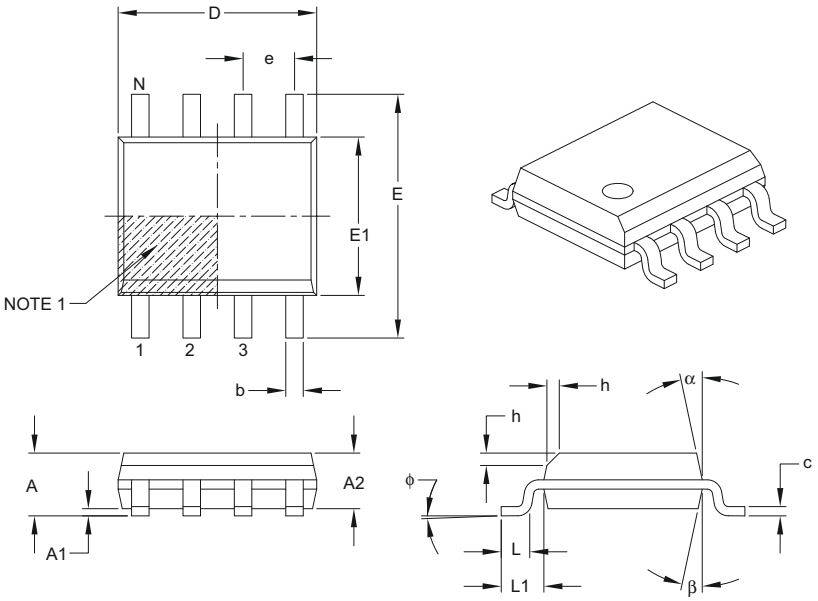
Notes:
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

 © 2010 Microchip Technology Inc.

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1	1.04 REF		
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

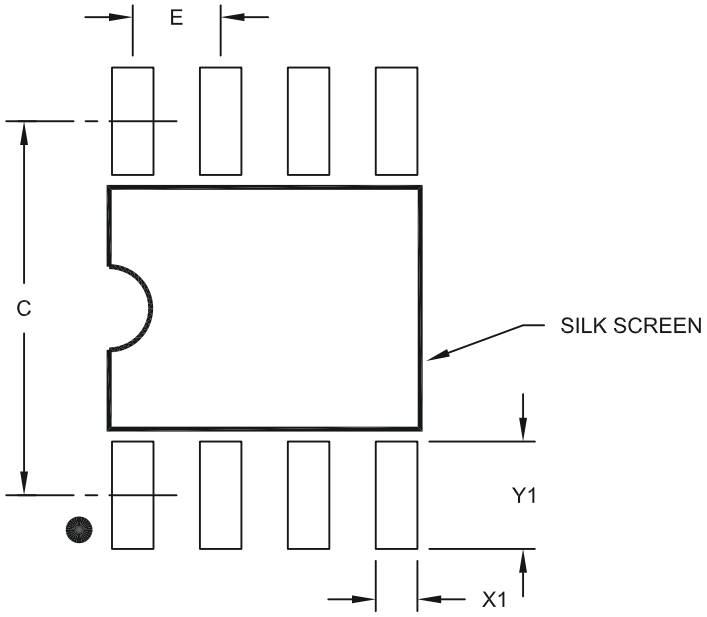
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

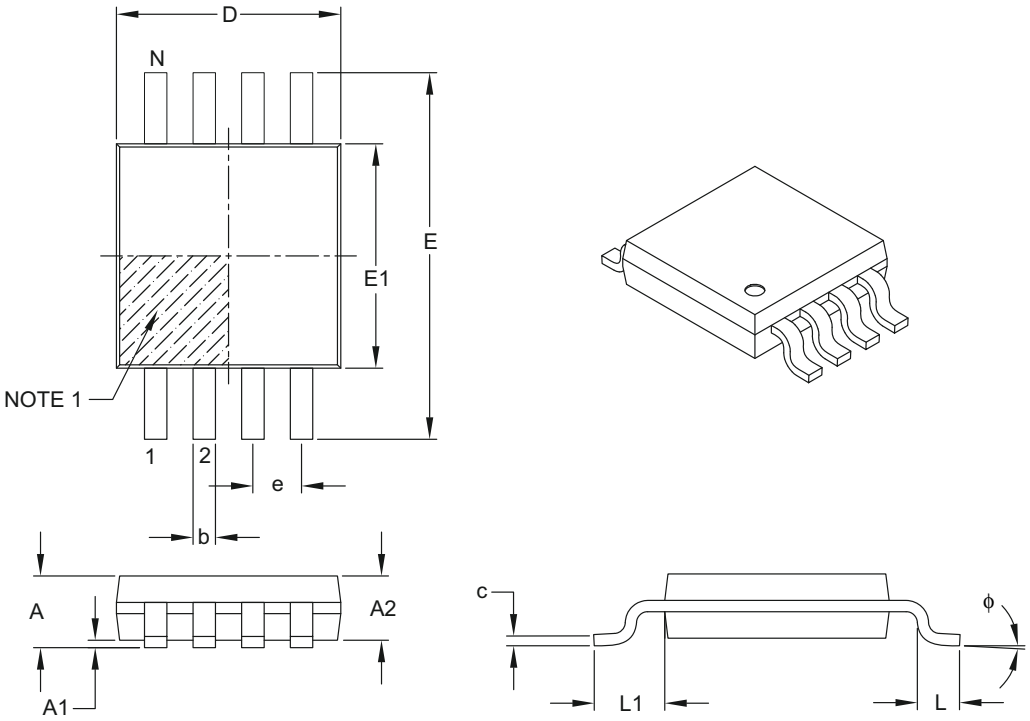
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

 © 2010 Microchip Technology Inc.

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	–	0.15
Overall Width	E	4.90 BSC		
Molded Package Width	E1	3.00 BSC		
Overall Length	D	3.00 BSC		
Foot Length	L	0.40	0.60	0.80
Footprint	L1	0.95 REF		
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.08	–	0.23
Lead Width	b	0.22	–	0.40

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

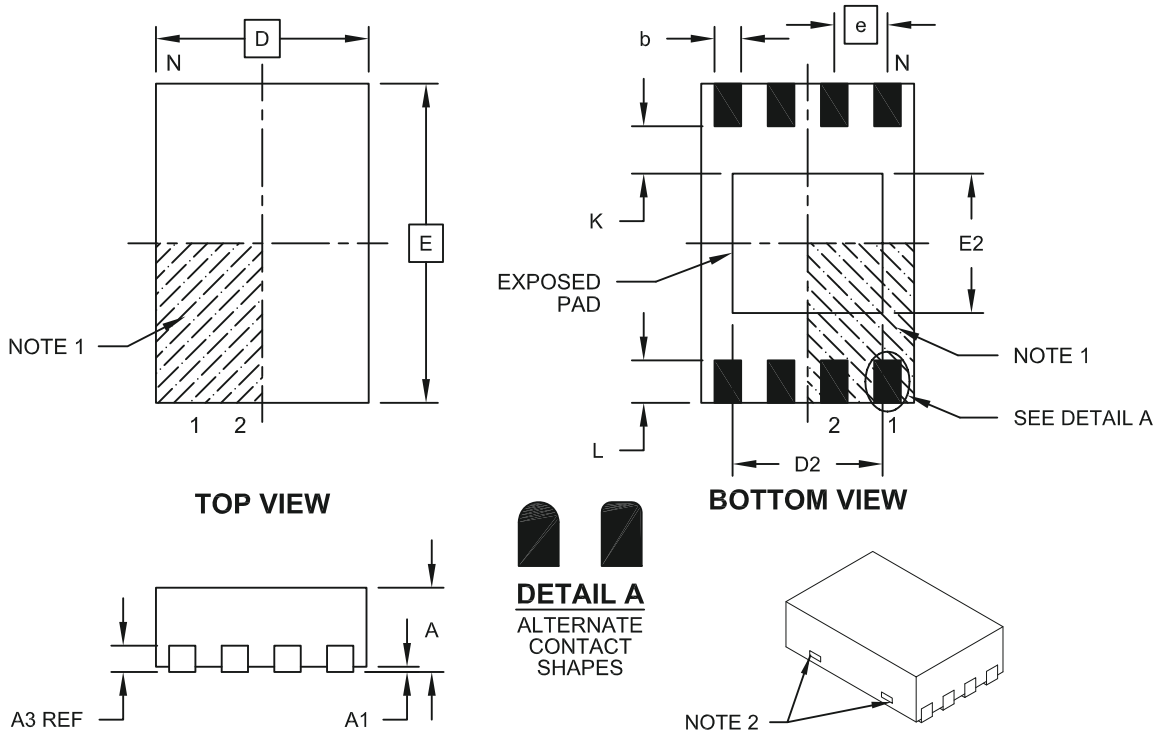
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75 mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.50 BSC		
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Length	D	2.00 BSC		
Overall Width	E	3.00 BSC		
Exposed Pad Length	D2	1.20	-	1.60
Exposed Pad Width	E2	1.20	-	1.60
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.25	0.30	0.45
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

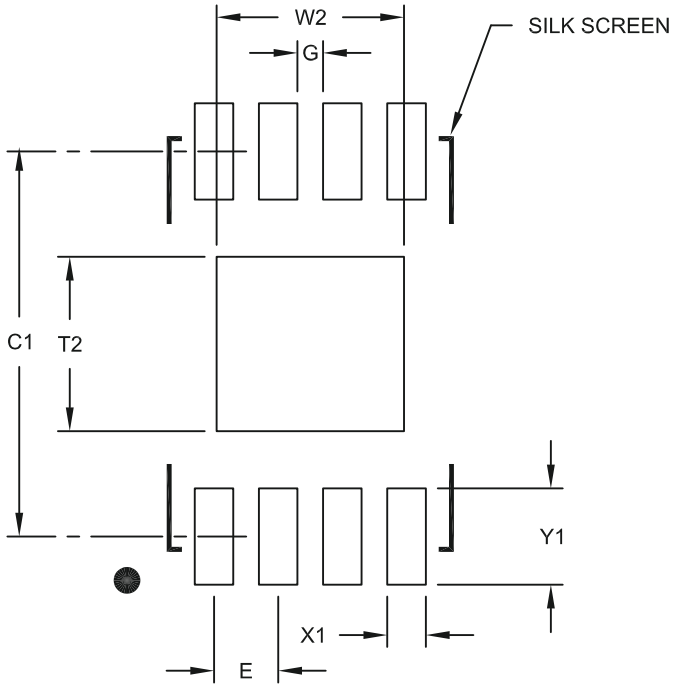
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-129B

 © 2010 Microchip Technology Inc.

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75 mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			1.46
Optional Center Pad Length	T2			1.36
Contact Pad Spacing	C1		3.00	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.20		

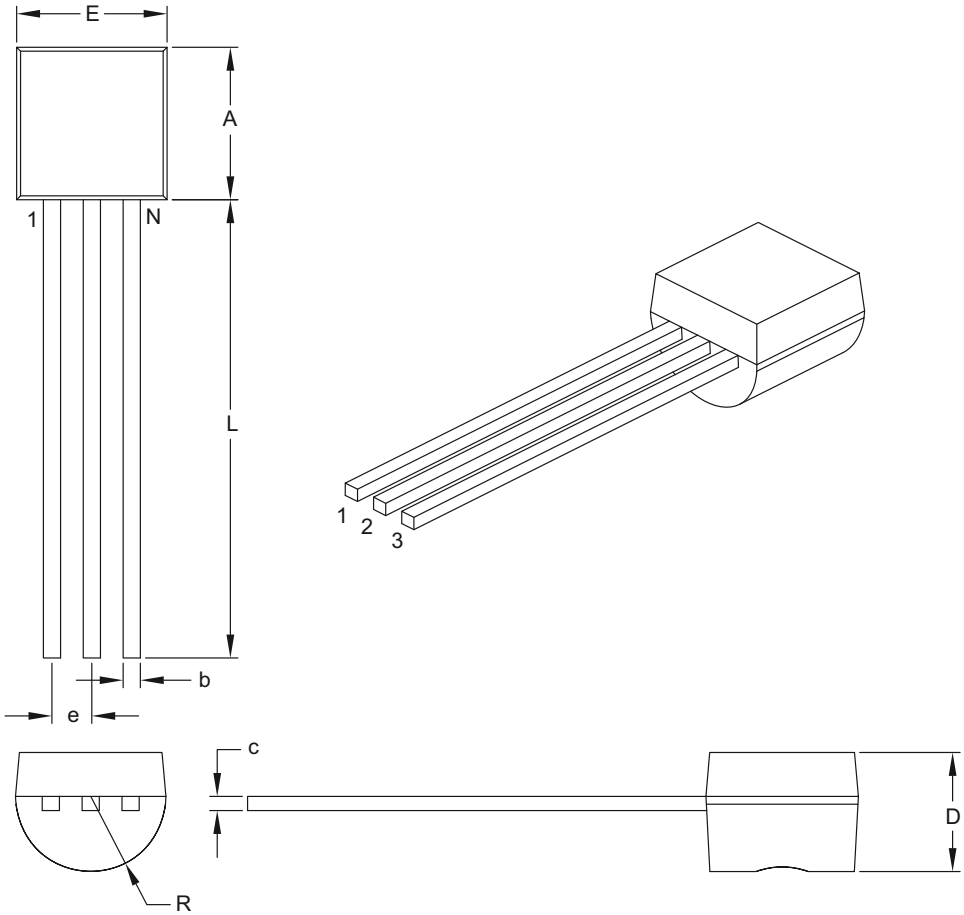
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2129A

3-Lead Plastic Transistor Outline (TO) [TO-92]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES	
Dimension Limits		MIN	MAX
Number of Pins	N	3	
Pitch	e	.050 BSC	
Bottom to Package Flat	D	.125	.165
Overall Width	E	.175	.205
Overall Length	A	.170	.210
Molded Package Radius	R	.080	.105
Tip to Seating Plane	L	.500	–
Lead Thickness	c	.014	.021
Lead Width	b	.014	.022

Notes:

1. Dimensions A and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

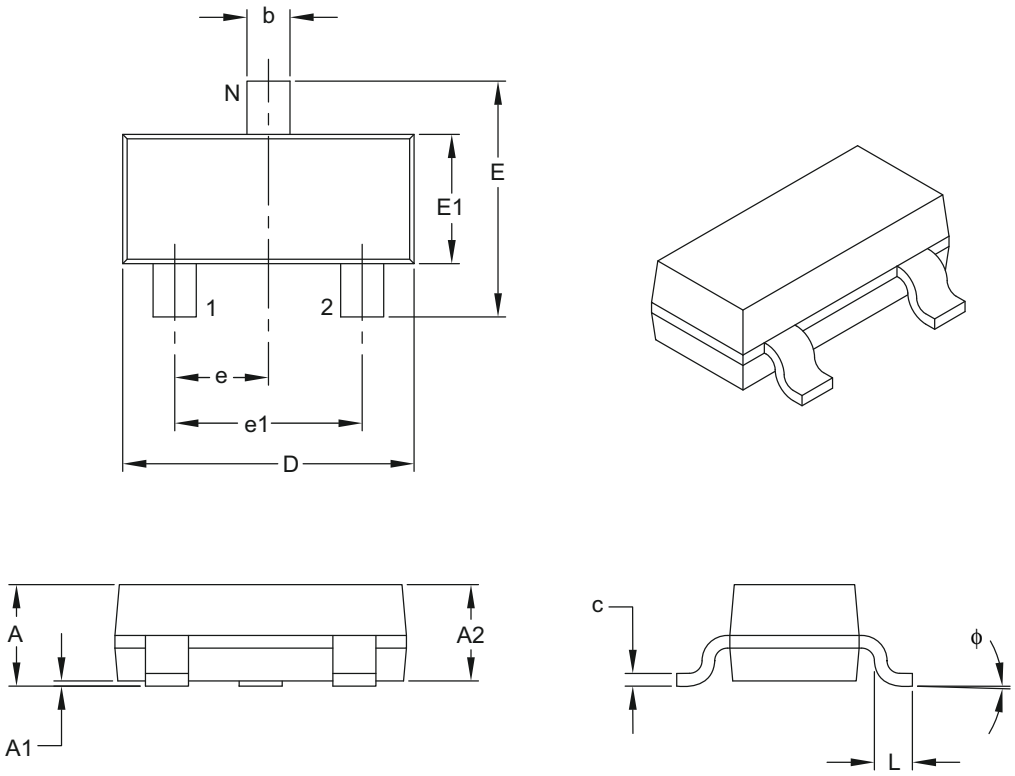
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-101B

 © 2010 Microchip Technology Inc.

3-Lead Plastic Small Outline Transistor (TT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	3		
Lead Pitch	e	0.95 BSC		
Outside Lead Pitch	e1	1.90 BSC		
Overall Height	A	0.89	–	1.12
Molded Package Thickness	A2	0.79	0.95	1.02
Standoff	A1	0.01	–	0.10
Overall Width	E	2.10	–	2.64
Molded Package Width	E1	1.16	1.30	1.40
Overall Length	D	2.67	2.90	3.05
Foot Length	L	0.13	0.50	0.60
Foot Angle	ϕ	0°	–	10°
Lead Thickness	c	0.08	–	0.20
Lead Width	b	0.30	–	0.54

Notes:

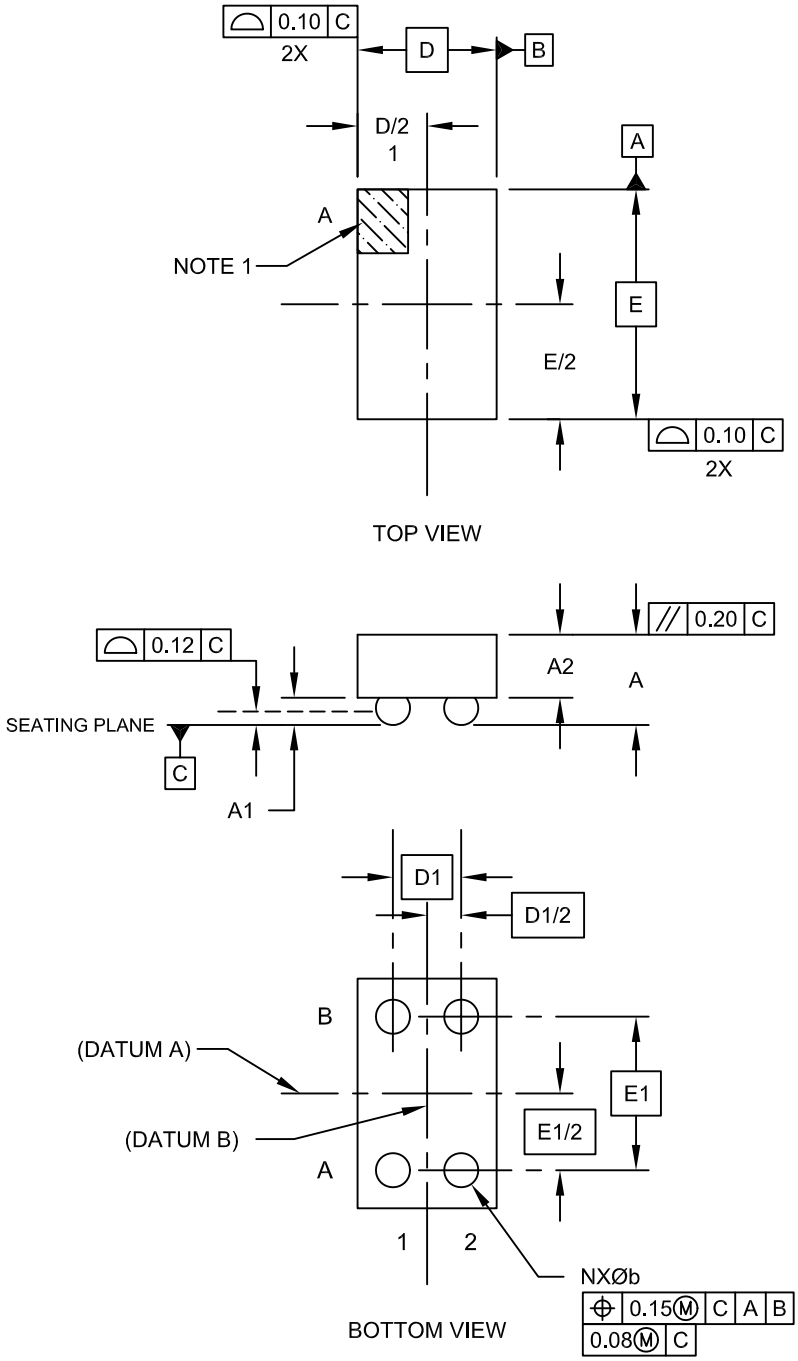
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-104B

4-Lead Chip Scale Package (CS) - [CSP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

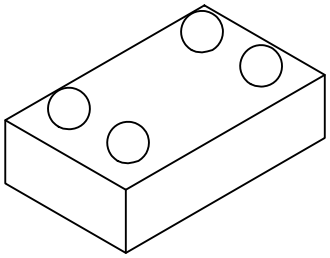


Microchip Technology Drawing C04-6008A Sheet 1 of 2

 © 2010 Microchip Technology Inc.

4-Lead Chip Scale Package (CS) - [CSP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Contacts	N		4	
Adjacent Column X-Pitch	D1	0.400 BSC		
Adjacent Row Y-Pitch	E1	0.900 BSC		
Overall Height	A	0.47	0.51	0.55
Die Height	A2	0.33	0.35	0.37
Bump Height	A1	0.14	0.16	0.18
Overall Width	D	NOTE 4		
Overall Length	E	NOTE 4		
Ball Diameter	b	0.18	0.20	0.22

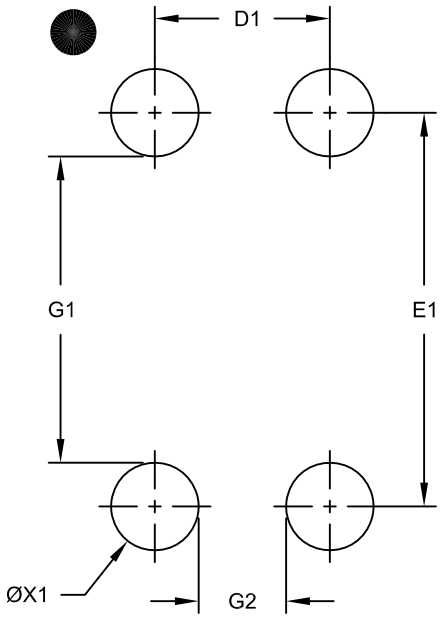
Notes:

1. Orientation reference feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
4. Package size varies with specific devices. Please see the specific Product Data Sheet.

Microchip Technology Drawing C04-6008A Sheet 2 of 2

4-Lead Chip Scale Package (CS) - [CSP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Contacts	N		4	
Contact Pad Spacing	D1		0.40	
Contact Pad Spacing	E1		0.90	
Contact Pad Diameter (X4)	ØX1		0.20	
Distance Between Pads	G1		0.70	
Distance Between Pads	G2		0.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-8008A

 © 2010 Microchip Technology Inc.

APPENDIX A: REVISION HISTORY

Revision A (10/07)

Original release of this document.

Revision B (01/08)

Revised SOT-23 Package Type; Revised DFN package to TDFN; Section 3.3 (added new bullet item); Section 4.5 note; Table 7-1.

Revision C (03/08)

Removed patent pending notice; Revised Tables 1-1 and 1-2; Section 3.3 (bullet 3) and 3.7 (bullet 2); Product ID System.

Revision D (04/08)

Revised document status to Preliminary; General updates.

Revision E (09/08)

Updated UNI/O trademark; Revised Table 1-2, parameters 3 and 5; Updated package drawings.

Revision F (10/09)

Added 3-lead TO-92 Package.

Revision G (12/09)

Added 11AA161/11LC161 device.

Revision H (03/10)

Added 4-lead Chip Scale package.

NOTES:

 © 2010 Microchip Technology Inc.

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com, click on Customer Change Notification and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support
- Development Systems Information Line

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://support.microchip.com

READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this document.

To: Technical Publications Manager Total Pages Sent _____

RE: Reader Response

From: Name _____

Company _____

Address _____

City / State / ZIP / Country _____

Telephone: (_____) _____ - _____ FAX: (_____) _____ - _____

Application (optional):

Would you like a reply?____Y ____N

Device: 11AAXXX/11LCXXX Literature Number: DS22067H

Questions:

1. What are the best features of this document?

_____

_____

2. How does this document meet your hardware and software development needs?

_____

_____

3. Do you find the organization of this document easy to follow? If not, why?

_____

_____

4. What additions to the document do you think would enhance the structure and subject?

_____

_____

5. What deletions from the document could be made without affecting the overall usefulness?

_____

_____

6. Is there any incorrect or misleading information (what and where)?

_____

_____

7. How would you improve this document?

_____

_____

 © 2010 Microchip Technology Inc.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	X	—	X	/XXX
Device	Device Address	Tape & Reel		Temperature Range	Package

Device:

11AA01 =	1 Kbit, 1.8V UNI/O Serial EEPROM	
11LC01 =	1 Kbit, 2.5V UNI/O Serial EEPROM	
11AA02 =	2 Kbit, 1.8V UNI/O Serial EEPROM	
11LC02 =	2 Kbit, 2.5V UNI/O Serial EEPROM	
11AA04 =	4 Kbit, 1.8V UNI/O Serial EEPROM	
11LC04 =	4 Kbit, 2.5V UNI/O Serial EEPROM	
11AA08 =	8 Kbit, 1.8V UNI/O Serial EEPROM	
11LC08 =	8 Kbit, 2.5V UNI/O Serial EEPROM	
11AA16 =	16 Kbit, 1.8V UNI/O Serial EEPROM	
11LC16 =	16 Kbit, 2.5V UNI/O Serial EEPROM	

Device Address:

0	=	Standard Address – 0xA0
1	=	Alternate Address – 0xA1 (11XX161 only)

Tape & Reel:

T	=	Tape and Reel
Blank	=	Tube

Temperature Range:

I	=	-40°C to +85°C	(Industrial)
E	=	-40°C to +125°C	(Extended)

Package:

P	=	8-lead Plastic DIP (300 mil body)
SN	=	8-lead Plastic SOIC (3.90 mm body)
MS	=	8-lead Plastic Micro Small Outline (MSOP)
MNY(1)	=	8-lead 2x3 mm TDFN
TO	=	3-lead Plastic TO-92
TT	=	3-lead SOT-23 (Tape and Reel only)
CS16K(2)	=	Chip Scale (CS), 4-lead (I-temp, “AA”, Tape and Reel only)

Note 1: “Y” indicates a Nickel Palladium Gold (NiPdAu) finish.

2: “16K” indicates 160K technology.

Examples:

a) 11AA010-I/P = 1 Kbit, 1.8V Serial EEPROM, Industrial temp., Standard address, PDIP package

b) 11LC160T-E/TT = 16 Kbit, 2.5V Serial EEPROM, Extended temp., Tape & Reel, SOT-23 package

c) 11AA080-I/MS = 8 Kbit, 1.8V Serial EEPROM, Industrial temp., Standard address, MSOP package

d) 11LC020T-I/SN = 2 Kbit, 2.5V Serial EEPROM, Industrial temp., Tape & Reel, Standard Address, SOIC package

e) 11AA040T-I/MNY = 4 Kbit, 1.8V Serial EEPROM, Industrial temp., Tape and Reel, Standard Address, 2x3 mm TDFN package, Nickel Palladium Gold finish

f) 11LC161-I/SN = 16 Kbit, 2.5V Serial EEPROM, Industrial temp., Alternate address, SOIC package

g) 11AA020T-I/CS16K = 2 Kbit, 1.8V Serial EEPROM, Industrial temp., Standard address, Chip Scale package

NOTES:

 © 2010 Microchip Technology Inc.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, PIC32 logo, rfPIC and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MXDEV, MXLAB, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Octopus, Omniscient Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICkit, PICtail, REAL ICE, rfLAB, Select Mode, Total Endurance, TSHARC, UniWinDriver, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2010, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

Printed on recycled paper.

ISBN:978-1-60932-042-3

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO/TS 16949:2002

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://support.microchip.com
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo
Kokomo, IN
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8528-2100
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Yokohama
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-6578-300
Fax: 886-3-6578-370

Taiwan - Kaohsiung
Tel: 886-7-536-4818
Fax: 886-7-536-4803

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

01/05/10

© 2010 Microchip Technology Inc.

Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.