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NDS351N

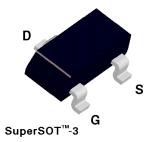
N-Channel Logic Level Enhancement Mode Field Effect Transistor

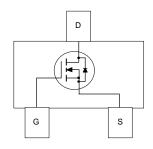
General Description

These N-Channel logic level enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications in notebook computers, portable phones, PCMCIA cards, and other battery powered circuits where fast switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

- $\qquad \text{1.1A, 30V. } \mathsf{R}_{\mathrm{DS(ON)}} = 0.25 \Omega \ @ \mathsf{V}_{\mathrm{GS}} = 4.5 \mathsf{V}.$
- Proprietary package design using copper lead frame for superior thermal and electrical capabilities.
- High density cell design for extremely low R_{DS(ON)}.
- Exceptional on-resistance and maximum DC current capability.
- Compact industry standard SOT-23 surface mount package.





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS351N	Units	
V _{DSS}	Drain-Source Voltage		30	V	
V _{GSS}	Gate-Source Voltage - Continuous		20	V	
I _D	Maximum Drain Current - Continuous	(Note 1a)	± 1.1	А	
	- Pulsed		± 10		
P _D	Maximum Power Dissipation	(Note 1a)	0.5	W	
		(Note 1b)	0.46		
T _J ,T _{STG}	Operating and Storage Temperature Range		-55 to 150	°C	
THERMA	L CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)		250	°C/W	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	75	°C/W	

Symbol	Parameter	Conditions		Min	Тур	Max	Units
OFF CHA	RACTERISTICS	·					
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$		30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V				1	μΑ
			T _J =125°C			10	μΑ
I _{GSSF}	Gate - Body Leakage, Forward	$V_{GS} = 12 \text{ V}, V_{DS} = 0 \text{ V}$				100	nA
I _{GSSR}	Gate - Body Leakage, Reverse	V _{GS} = -12 V, V _{DS} = 0 V				-100	nA
ON CHAF	RACTERISTICS (Note 2)	·					
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$		8.0	1.6	2	V
			T _J =125°C	0.5	1.3	1.5	
R _{DS(ON)}	Static Drain-Source On-Resistance	$V_{GS} = 4.5 \text{ V}, I_{D} = 1.1 \text{ A}$			0.185	0.25	Ω
			T _J =125°C		0.26	0.37	
		$V_{GS} = 10 \text{ V}, I_{D} = 1.4 \text{ A}$			0.135	0.16	
I _{D(ON)}	On-State Drain Current	$V_{GS} = 4.5 \text{ V}, \ V_{DS} = 5 \text{ V}$		5			Α
g _{FS}	Forward Transconductance	$V_{DS} = 5 \text{ V}, I_{D} = 1.1 \text{ A}$			2.5		S
DYNAMIC	CHARACTERISTICS						
C _{iss}	Input Capacitance	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1.0 MHz			140		pF
C _{oss}	Output Capacitance				80		pF
C _{rss}	Reverse Transfer Capacitance				18		pF
SWITCHI	NG CHARACTERISTICS (Note 2)						
$\mathbf{t}_{d(on)}$	Turn - On Delay Time	$V_{DD} = 10 \text{ V}, \ I_{D} = 1 \text{ A},$ $V_{GS} = 10 \text{ V}, \ R_{GEN} = 50 \Omega$			9	15	ns
t _r	Turn - On Rise Time				16	30	ns
$t_{d(off)}$	Turn - Off Delay Time				26	50	ns
t _f	Turn - Off Fall Time				19	40	ns
Q_g	Total Gate Charge	$V_{DS} = 10 \text{ V}, I_{D} = 1.1 \text{ A}, V_{GS} = 5 \text{ V}$			2	3.5	nC
Q_{gs}	Gate-Source Charge					1	nC
Q_{gd}	Gate-Drain Charge					2	nC

Electrical Characteristics (T _A = 25°C unless otherwise noted)							
Symbol	Parameter	Conditions	Min	Тур	Max	Units	
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
Is	Maximum Continuous Drain-Source Diode Forward Current				0.6	Α	
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current				5	Α	
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 1.1 A (Note 2)		0.8	1.2	V	

Notes:

1. R_{gut} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{gut} is guaranteed by design while R_{gut} is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta J} A(t)} = \frac{T_J - T_A}{R_{\theta J} d^* R_{\theta C} A(t)} = I_D^2(t) \times R_{DS (ON)} \varrho_{TJ}$$

Typical $R_{_{\theta^{J\!A}}}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 250°C/W when mounted on a 0.02 in² pad of 2oz cpper.

b. 270°C/W when mounted on a 0.001 in $^{\!2}$ pad of 2oz cpper.





Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2.0%.

Typical Electrical Characteristics

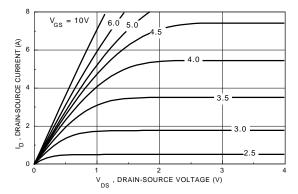


Figure 1. On-Region Characteristics

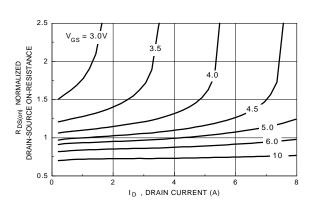


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

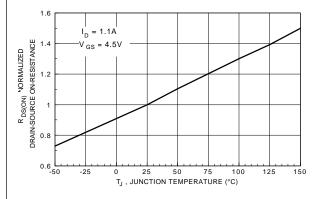


Figure 3. On-Resistance Variation with Temperature

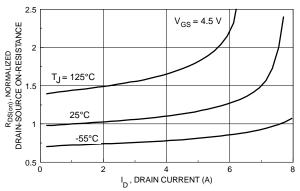


Figure 4. On-Resistance Variation with Drain Current and Temperature

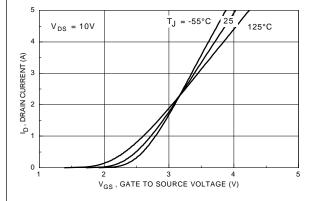


Figure 5. Transfer Characteristics

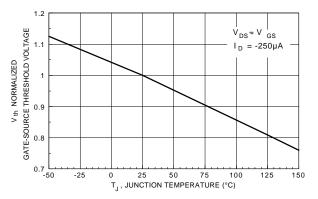


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

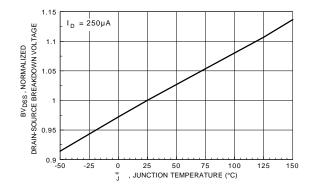


Figure 7. Breakdown Voltage Variation with Temperature

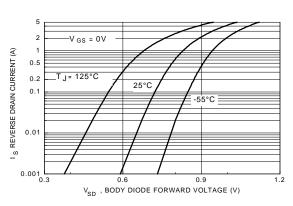


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

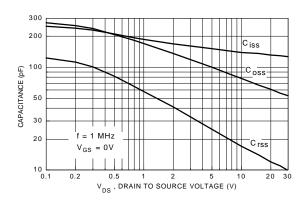


Figure 9. Capacitance Characteristics

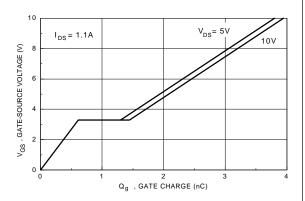


Figure 10. Gate Charge Characteristics

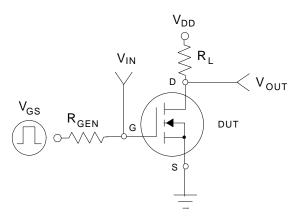


Figure 11. Switching Test Circuit

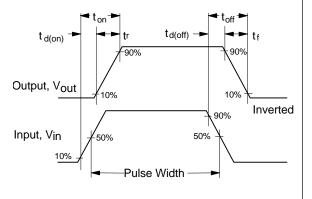
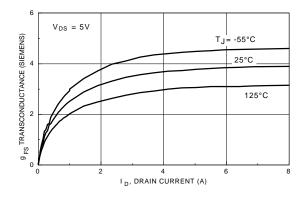


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)



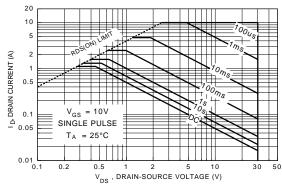


Figure 13. Transconductance Variation with Drain Current and Temperature

Figure 14. Maximum Safe Operating Area

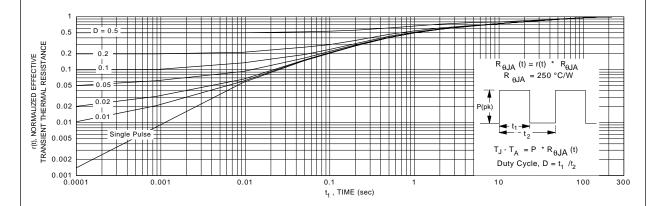


Figure 15. Transient Thermal Response Curve

Note: Characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

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Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: <u>org@eplast1.ru</u>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина,

дом 2, корпус 4, литера А.