MAX14949

5kV$_{RMS}$ Isolated 500kbps Half-Duplex RS-485/RS-422 Transceiver with ±30kV ESD Protection and Integrated Transformer Driver

General Description

The MAX14949 isolated RS-485/RS-422 transceiver provides 5000V$_{RMS}$ (60s) of galvanic isolation between the cable-side (RS-485/RS-422 driver/receiver-side) and the UART-side of the device. Isolation improves communication by breaking ground loops and reduces noise when there are large differences in ground potential between ports. This device allows for robust communication up to 500kbps.

The device includes an integrated 450kHz transformer driver for power transfer to the cable-side of the transceiver using an external transformer. An integrated LDO provides a simple and space-efficient architecture for providing power to the cable-side of the IC.

The device includes one half-duplex driver/receiver channel. The receiver is 1/8-unit load, allowing up to 256 transceivers on a common bus.

Integrated true fail-safe circuitry ensures a logic-high on the receiver output when inputs are shorted or open. Undervoltage lockout disables the driver when cable-side or UART-side power supplies are below functional levels.

The driver outputs/receiver inputs are protected from ±30kV electrostatic discharge (ESD) to GNDB on the cable-side, as specified by the Human Body Model (HBM).

The MAX14949 is available in a wide body 16-pin SOIC package and operates over the -40°C to +85°C temperature range.

Applications

- Industrial Automation Equipment
- Programmable Logic Controllers
- HVAC
- Power Meters

Safety Regulatory Approvals Pending

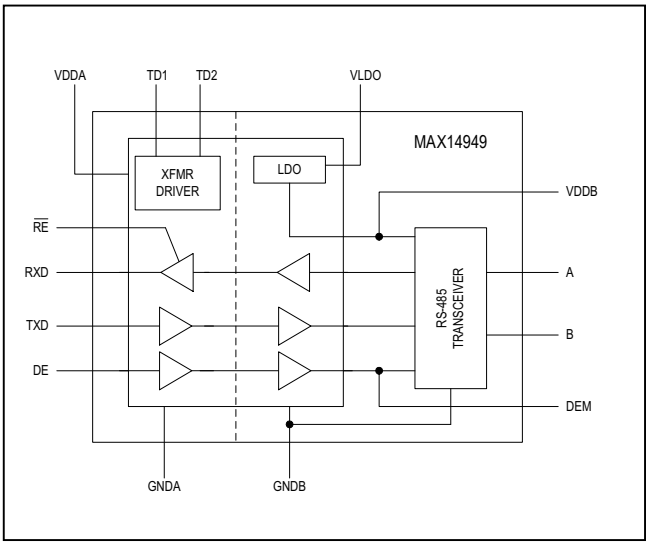
- UL According to UL1577
- cUL According to CSA Bulletin 5A
- VDE 0884-10

Ordering Information appears at end of data sheet.

Benefits and Features

- High Integration Simplifies Designs
  - Integrated LDO for Cable-Side Power
  - Integrated Transformer Driver for Power Transfer to Cable-Side Has Up to 80% Efficiency at 150mA Load
- High-Performance Transceiver Enables Flexible Designs
  - Compliant with RS-485 EIA/TIA-485 Standard
  - 500kbps (max) Data Rate
  - Up to 256 Devices on the Bus
- Integrated Protection for Robust Communication
  - ±30kV ESD (HBM) on Driver Outputs/Receiver Inputs
  - 5kV$_{RMS}$ Withstand-Isolation Voltage for 60 Seconds (V$_{ISO}$)
  - 1200V$_{PEAK}$ Maximum Repetitive Peak-Isolation Voltage (V$_{IORM}$)
  - 848V$_{RMS}$ Maximum Working-Isolation Voltage (V$_{IOWM}$)
  - >30 Years Lifetime at Rated Working Voltage
  - Withstands ±10kV Surge per IEC 61000-4-5
  - Thermal Shutdown

Functional Diagram



maxim integrated™

Absolute Maximum Ratings

V_{DDA} to GNDA .....-0.3V to +6V
V_{DDB} to GNDB.....-0.3V to +6V
V_{LDO} to GNDB.....-0.3V to +16V
TD1, TD2 to GNDA .....-0.3V to +12V
TXD, DE, $\overline{RE}$, RXD to GNDA .....-0.3V to +6V
DEM to GNDB .....-0.3V to +6V
A, B to GNDB.....-8V to +13V
TD1, TD2 Continuous Current .....±1.4A
Short-Circuit Duration (RXD to GNDA, A, B, DEM, V_{DDB} to GNDB).....Continuous

Continuous Power Dissipation (T_A = +70°C)
16-pin Wide SOIC
(derate 14.1mW/°C above +70°C) 1126.8mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

Junction-to-Ambient Thermal Resistance (θ_{JA}).....71°C/W

Junction-to-Case Thermal Resistance (θ_{JC}).....23°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC Electrical Characteristics

(V_{DDA} - V_{GNDA} = 3.0V to 5.5V, V_{DDB} - V_{GNDB} = 4.5V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 5V, V_{GNDA} = V_{GNDB}, and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER						
Supply Voltage	V_{DDA}		3.0		5.5	V
	V_{DDB}		4.5		5.5	
Supply Current	I_{DDA}	V_{DDA} = 5V, DE = high, $\overline{RE}$ = TXD = low, RXD unconnected, no bus load, TD1/TD2 unconnected		4.7	7.7	mA
	I_{DDB}	DE = high, $\overline{RE}$ = TXD = low, RXD unconnected, no bus load, V_{DDB} = 5V		6.3	12.5	
Undervoltage-Lockout Threshold	V_{UVLOA}	$\overline{RE}$, RXD, DE, TXD, V_{DDA} rising	1.50	1.58	1.65	V
		TD1/TD2 driver, V_{DDA} rising	2.55	2.7	2.85	
	V_{UVLOB}	V_{DDB} rising	2.55	2.7	2.85	
Undervoltage-Lockout-Threshold Hysteresis	$V_{UVHYSTA}$	$\overline{RE}$, RXD, DE, TXD		50		mV
		TD1/TD2 driver		200		
	$V_{UVHYSTB}$			200		
TRANSFORMER DRIVER						
Output Resistance	R_O	TD1/TD2 = low, I_{OUT} = 300mA		0.6	1.5	Ω
TD1, TD2 Current Limit	I_{LIM}	4.5V ≤ V_{DDA} ≤ 5.5V	540	785	1300	mA
		3.0V ≤ V_{DDA} ≤ 3.6V	485	730	1170	
Switching Frequency	f_{SW}		350	450	550	kHz
Duty Cycle	D			50		%
Crossover Dead Time	t_{DEAD}			50		ns

DC Electrical Characteristics (continued)

(V_{DDA} - V_{GNDA} = 3.0V to 5.5V, V_{DDB} - V_{GNDB} = 4.5V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 5V, V_{GNDA} = V_{GNDB}, and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LDO						
LDO Supply Voltage	V_{LDO}	Relative to GNDB, LDO is on (Note 4)	4.68		14	V
LDO Supply Current	I_{LDO}	DE = high, TXD = low, no bus load, V_{LDO} = 5.5V		6.4	12.9	mA
LDO Output Voltage	V_{DDB}		4.5	5	5.5	V
LDO Current Limit				300		mA
Load Regulation		V_{LDO} = 5.68V, I_{LOAD} = 20mA to 40mA		0.19	1.7	mV/mA
Line Regulation		V_{LDO} = 5.68V to 14V, I_{LOAD} = 20mA		0.12	1.8	mV/V
Dropout Voltage		V_{LDO} = 4.68V, I_{DDB} = 120mA		100	180	mV
Load Capacitance		Nominal value (Note 5)	1		10	µF
LOGIC INTERFACE (TXD, RXD, DE, $\overline{RE}$, DEM)						
Input High Voltage	V_{IH}	$\overline{RE}$, TXD, DE to GNDA	0.7 x V_{DDA}			V
Input Low Voltage	V_{IL}	$\overline{RE}$, TXD, DE to GNDA			0.8	V
Input Hysteresis	V_{HYS}	$\overline{RE}$, TXD, DE to GNDA		220		mV
Input Capacitance	C_{IN}	$\overline{RE}$, TXD, DE, f = 1MHz		2		pF
Input Pullup Current	I_{PU}	TXD	-10	-4.5	-1.5	µA
Input Pulldown Current	I_{PD}	DE, $\overline{RE}$	1.5	4.5	10	µA
Output Voltage High	V_{OH}	RXD to GNDA, I_{OUT} = -4mA	V_{DDA} -0.4			V
		DEM to GNDB, I_{OUT} = -4mA	V_{DDB} -0.4			
Output Voltage Low	V_{OL}	RXD to GNDA, I_{OUT} = 4mA			0.40	V
		DEM to GNDB, I_{OUT} = 4mA			0.40	
Short-Circuit Output Pullup Current	I_{SH_PU}	0V ≤ V_{RXD} ≤ V_{DDA}, V_A - V_B > -50mV, $\overline{RE}$ = low	-42			mA
		0V ≤ V_{DEM} ≤ V_{DDB}, DE = high	-42			
Short-Circuit Output Pulldown Current	I_{SH_PD}	0V ≤ V_{RXD} ≤ V_{DDA}, V_A - V_B < -200mV, $\overline{RE}$ = low			+40	mA
		0V ≤ V_{DEM} ≤ V_{DDB}, DE = low			+40	
Three-State Output Current	I_{OZ}	0V ≤ V_{RXD} ≤ V_{DDA}, $\overline{RE}$ = high	-1		+1	µA

DC Electrical Characteristics (continued)

(V_{DDA} - V_{GNDA} = 3.0V to 5.5V, V_{DDB} - V_{GNDB} = 4.5V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 5V, V_{GNDA} = V_{GNDB}, and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DRIVER							
Differential-Driver Output	$\|V_{OD}\|$	R_L = 54Ω, TXD = high or low, DE = high, Figure 1a		2			V
		R_L = 100Ω, TXD = high or low, DE = high, Figure 1a		3			
		-7V ≤ V_{CM} ≤+12V, Figure 1b		1.5		5	
Change in Magnitude of Differential-Driver Output Voltage	ΔV_{OD}	R_L = 100Ω or 54Ω, Figure 1b (Note 6)				0.2	V
Driver Common-Mode Output Voltage	V_{OC}	R_L = 100Ω or 54Ω, Figure 1a			V_{DDB}/2	3	V
Change in Magnitude of Common-Mode Voltage	ΔV_{OC}	R_L = 100Ω or 54Ω, Figure 1a (Note 6)				0.2	V
Driver Short-Circuit Output Current	I_{OSD}	GNDB ≤ V_{OUT} ≤ +12V, output low (Note 7)				+250	mA
		-7V ≤ V_{OUT} ≤ V_{DDB}, output high (Note 7)		-250			
Driver Short-Circuit Foldback Output Current	I_{OSDF}	(V_{DDB} - 1V) ≤ V_{OUT} ≤ +12V, output low (Note 5, 7)		+20			mA
		-7V ≤ V_{OUT} ≤ +1V, output high (Note 5, 7)				-20	
RECEIVER							
Input Current (A and B)	$I_{A,B}$	DE = GNDA, V_{DDB} = GNDB or +5.5V	V_{IN} = +12V			+125	μA
			V_{IN} = -7V	-100			
Receiver Differential-Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ +12V		-200	-125	-50	mV
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V			15		mV
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ +12V, DE = low		96			kΩ
PROTECTION							
Thermal-Shutdown Threshold	T_{SHDN}	Temperature rising			+160		°C
Thermal-Shutdown Hysteresis	T_{HYST}				15		°C
ESD Protection (A and B Pins to GNDB)		Human Body Model			±30		kV
		IEC 61000-4-2 Air-Gap Discharge			±15		
		IEC 61000-4-2- Contact Discharge			±10		
ESD Protection (All Other Pins)		Human Body Model			±4		kV

Switching Electrical Characteristics

(V_{DDA} - V_{GNDA} = 3.0V to 5.5V, V_{DDB} - V_{GNDB} = 4.5V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 5V, V_{GNDA} = V_{GNDB}, and T_A = +25°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC						
Common-Mode Transient Immunity	CMTI	(Note 8)		35		kV/µs
Glitch Rejection		TXD, DE, RXD	10	17	29	ns
DRIVER						
Driver Propagation Delay	t_{DPLH}, t_{DPHL}	R_L = 54Ω, C_L = 50pF, Figure 2 and Figure 3			1040	ns
Differential Driver Output Skew $\lvert t_{DPLH} - t_{DPHL} \rvert$	t_{DSKEW}	R_L = 54Ω, C_L = 50pF, Figure 2 and Figure 3			144	ns
Driver Differential-Output Rise or Fall Time	t_{LH}, t_{HL}	R_L = 54Ω, C_L = 50pF, Figure 2 and Figure 3			900	ns
Maximum Data Rate	DR_{MAX}		500			kbps
Driver Enable to Output High	t_{DZH}	R_L = 500Ω, C_L = 50pF, Figure 4			2540	ns
Driver Enable to Output Low	t_{DZL}	R_L = 500Ω, C_L = 50pF, Figure 5			2540	ns
Driver Disable Time From Low	t_{DLZ}	R_L = 500Ω, C_L = 50pF, Figure 5			140	ns
Driver Disable Time From High	t_{DHZ}	R_L = 500Ω, C_L = 50pF, Figure 4			140	ns
RECEIVER						
Receiver Propagation Delay	t_{RPLH}, t_{RPHL}	C_L = 15pF, Figure 6 and Figure 7 (Note 9)			240	ns
Receiver Output Skew	t_{RSKEW}	C_L = 15pF, Figure 6 and Figure 7 (Note 9)			34	ns
Maximum Data Rate	DR_{MAX}		500			kbps
Receiver Enable to Output High	t_{RZH}	R_L = 1kΩ, C_L = 15pF, S2 closed, Figure 8			20	ns
Receiver Enable to Output Low	t_{RZL}	R_L = 1kΩ, C_L = 15pF, S1 closed, Figure 8			30	ns
Receiver Disable Time from Low	t_{RLZ}	R_L = 1kΩ, C_L = 15pF, S1 closed, Figure 8			20	ns
Receiver Disable Time from High	t_{RHZ}	R_L = 1kΩ, C_L = 15pF, S2 closed, Figure 8			20	ns

Note 2: All devices are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.

Note 3: All currents into the device are positive. All currents out of the device are negative. All voltages are referenced to their respective ground (GNDA or GNDB), unless otherwise noted.

Note 4: V_{LDO} max indicates voltage capability of the circuit. Power-dissipation requirements may limit V_{LDO} max to a lower value.

Note 5: Not production tested. Guaranteed by design.

Note 6: ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC}, respectively, when the TXD input changes state.

Note 7: The short-circuit output current applies to the peak current just prior to foldback-current limiting. The short-circuit foldback output current applies during current limiting to allow a recovery from bus contention. See TOC 6 and TOC 7 in the *Typical Operating Characteristics* section.

Note 8: CMTI is the maximum sustainable common-mode voltage slew rate while maintaining the correct output states. CMTI applies to both rising and falling common-mode voltage edges. Tested with the transient generator connected between GNDA and GNDB. ΔV_{CM} = 1kV.

Note 9: Capacitive load includes test probe and fixture capacitance.

Insulation Characteristics

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Partial Discharge Test Voltage	V_{PR}	Method B1 = V_{IORM} x 1.875 (t = 1s, partial discharge <5pC)	2250	V_P
Maximum Repetitive Peak Withstand Voltage	V_{IORM}	(Note 10)	1200	V_P
Maximum Working-Isolation Voltage	V_{IOWM}	(Note 10)	848	V_{RMS}
Maximum Transient Isolation Voltage	V_{IOTM}	t = 1s	8400	V_P
Maximum Withstand-Isolation Voltage	V_{ISO}	t = 60s, f_{SW} = 60Hz (Notes 10, 11)	5000	V_{RMS}
Maximum Surge Isolation Voltage	V_{IOSM}	Basic insulation	10	kV
Insulation Resistance	R_S	T_A = +150°C, V_{IO} = 500V	>10^9	Ω
Barrier Capacitance Input to Output	CIO	f_{SW} = 1MHz	2	pF
Minimum Creepage Distance	CPG	Wide SOIC	8	mm
Minimum Clearance Distance	CLR	Wide SOIC	8	mm
Internal Clearance		Distance through insulation	0.015	mm
Comparative Tracking Resistance Index	CTI	Material Group II (IEC 60112)	575	
Climatic Category			40/125/21	
Pollution Degree (DIN VDE 0110, Table 1)			2	

Note 10: V_{IORM}, V_{IOWM}, V_{ISO} are defined by the IEC 60747-5-5 standard
Note 11: Product is qualified V_{ISO} for 60s. 100% production tested at 120% of V_{ISO} for 1s.

Safety Regulatory Approvals (Pending)

UL
The MAX14949 is certified under UL1577. For more details, see File E351759.
Rate up to 5000V$_{RMS}$ isolation voltage for basic insulation.
cUL
Pending
VDE
Pending
TUV
Pending

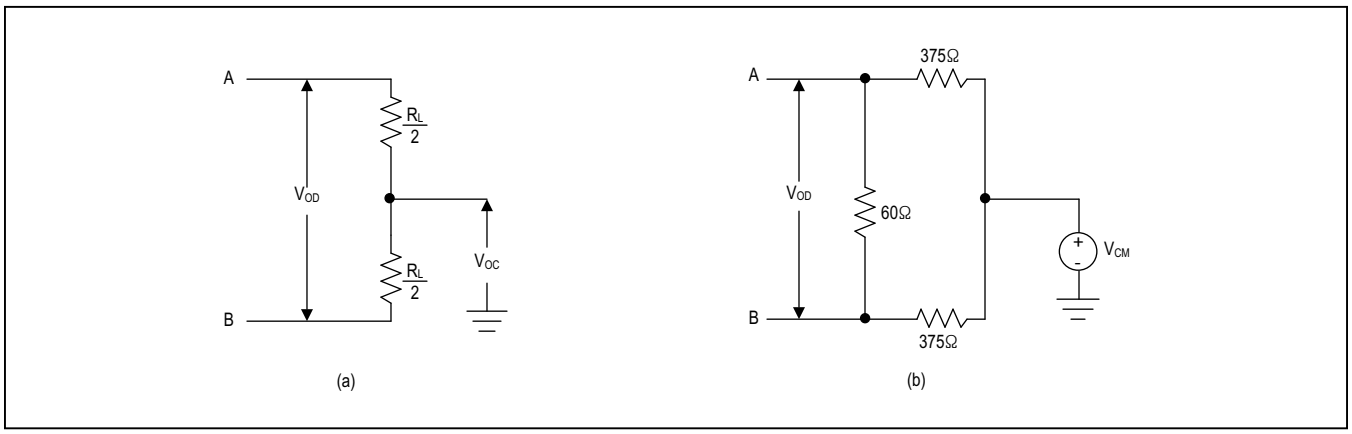


Figure 1. Driver DC Test Load

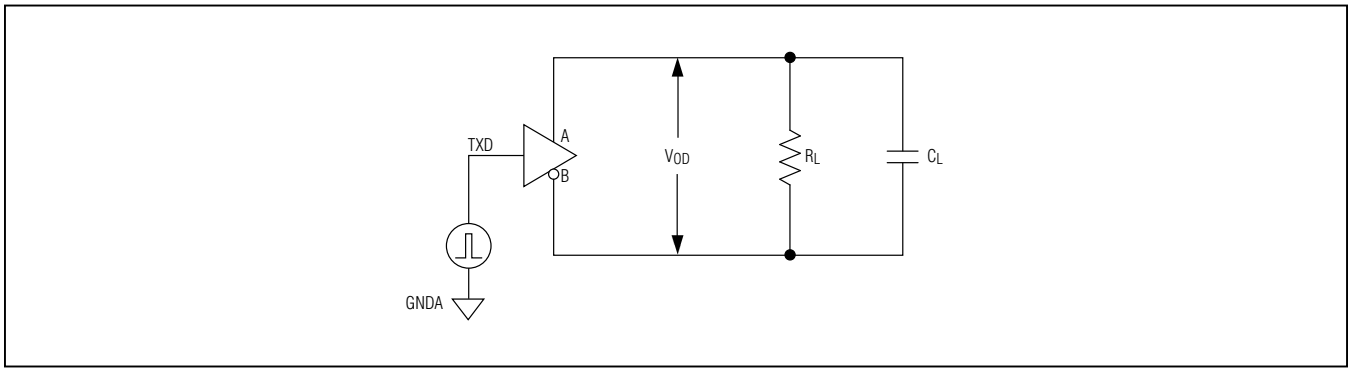


Figure 2. Driver Timing Test Circuit

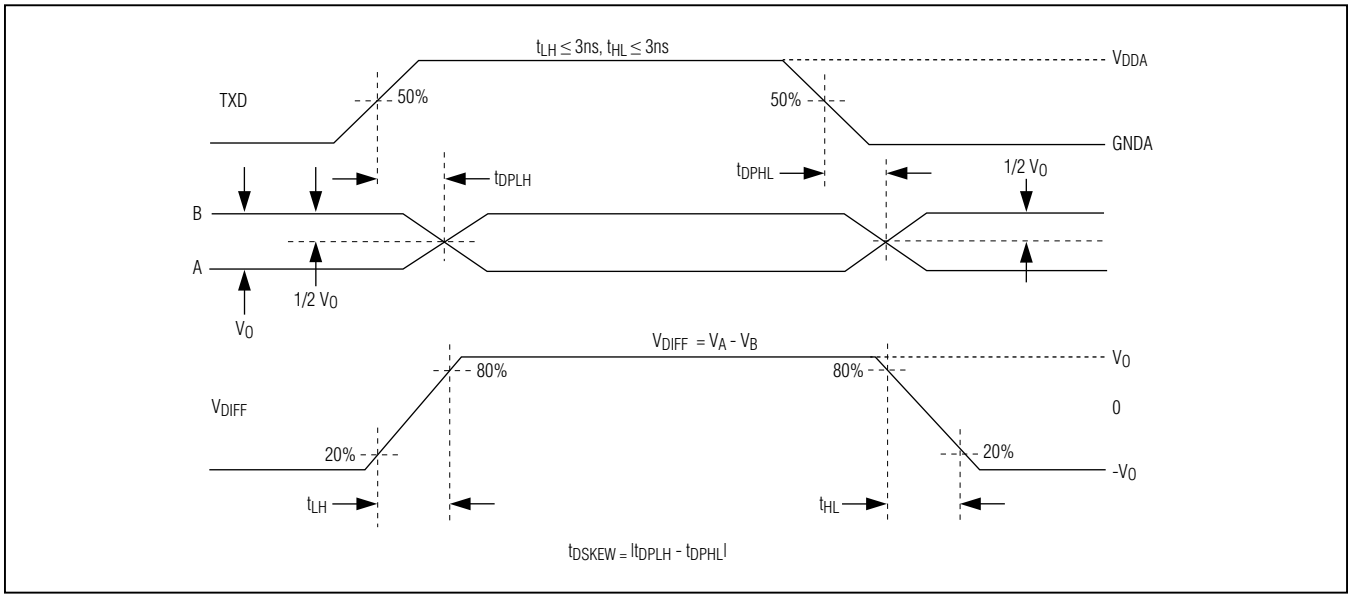


Figure 3. Driver Propagation Delays

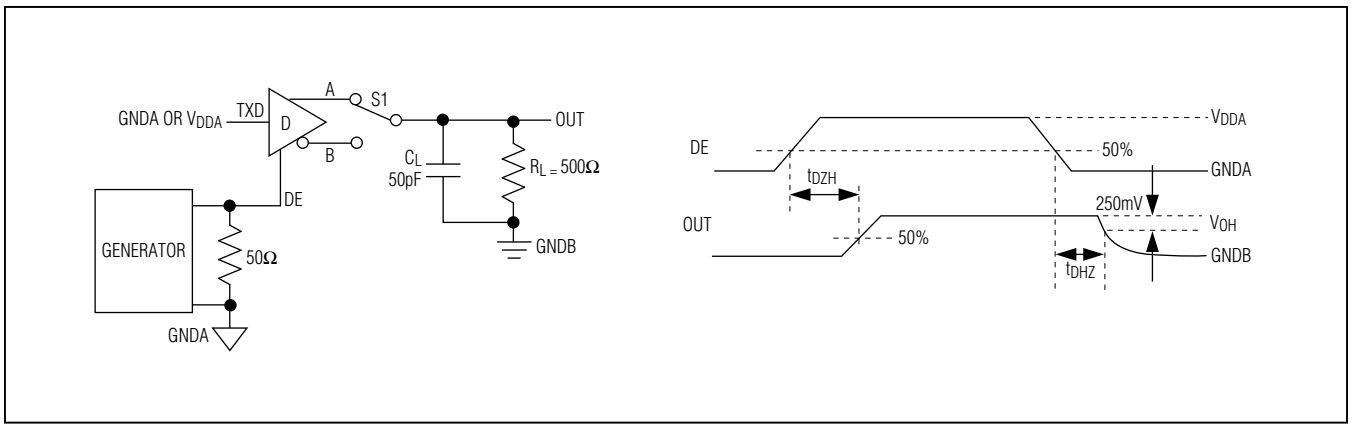


Figure 4. Driver Enable and Disable Times (t_{DZH}, t_{DHZ})

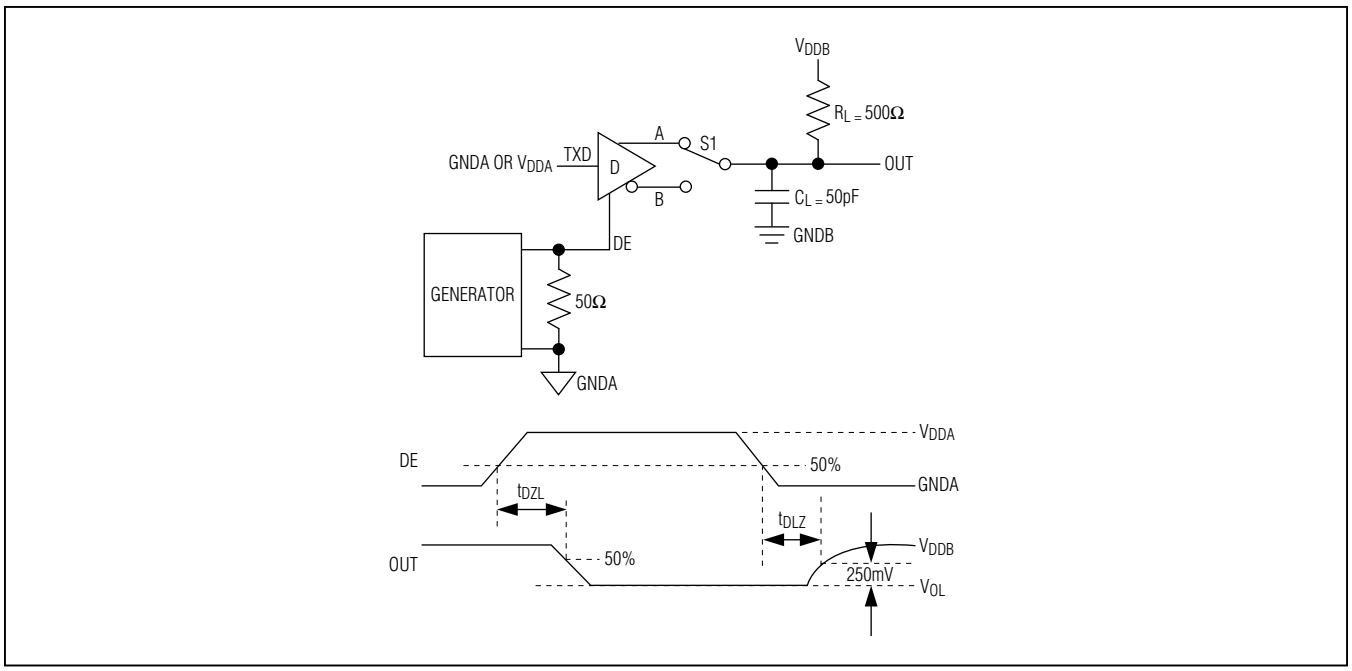


Figure 5. Driver Enable and Disable Times (t_{DZL}, t_{DLZ})

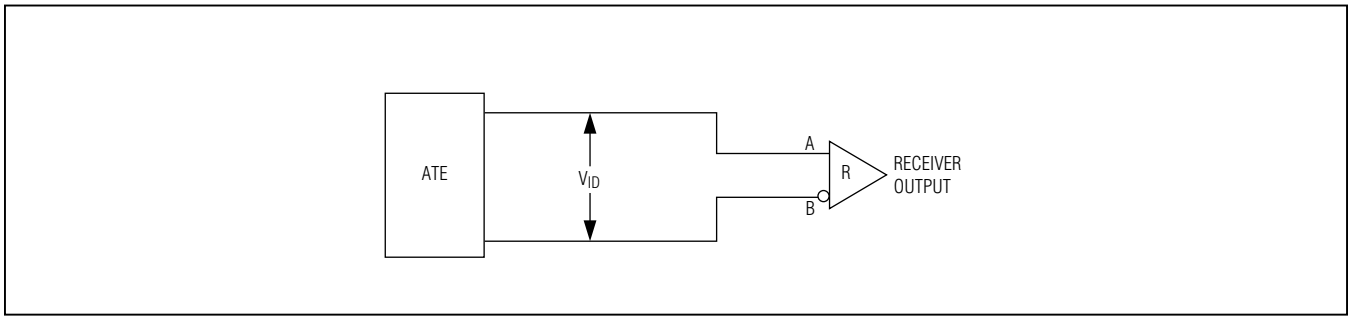


Figure 6. Receiver Propagation-Delay Test Circuit

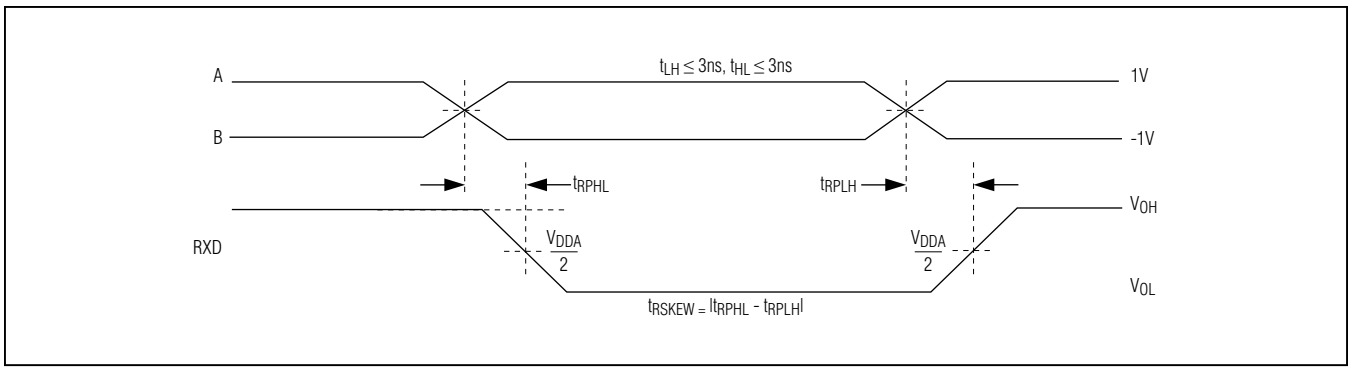


Figure 7. Receiver Propagation Delays

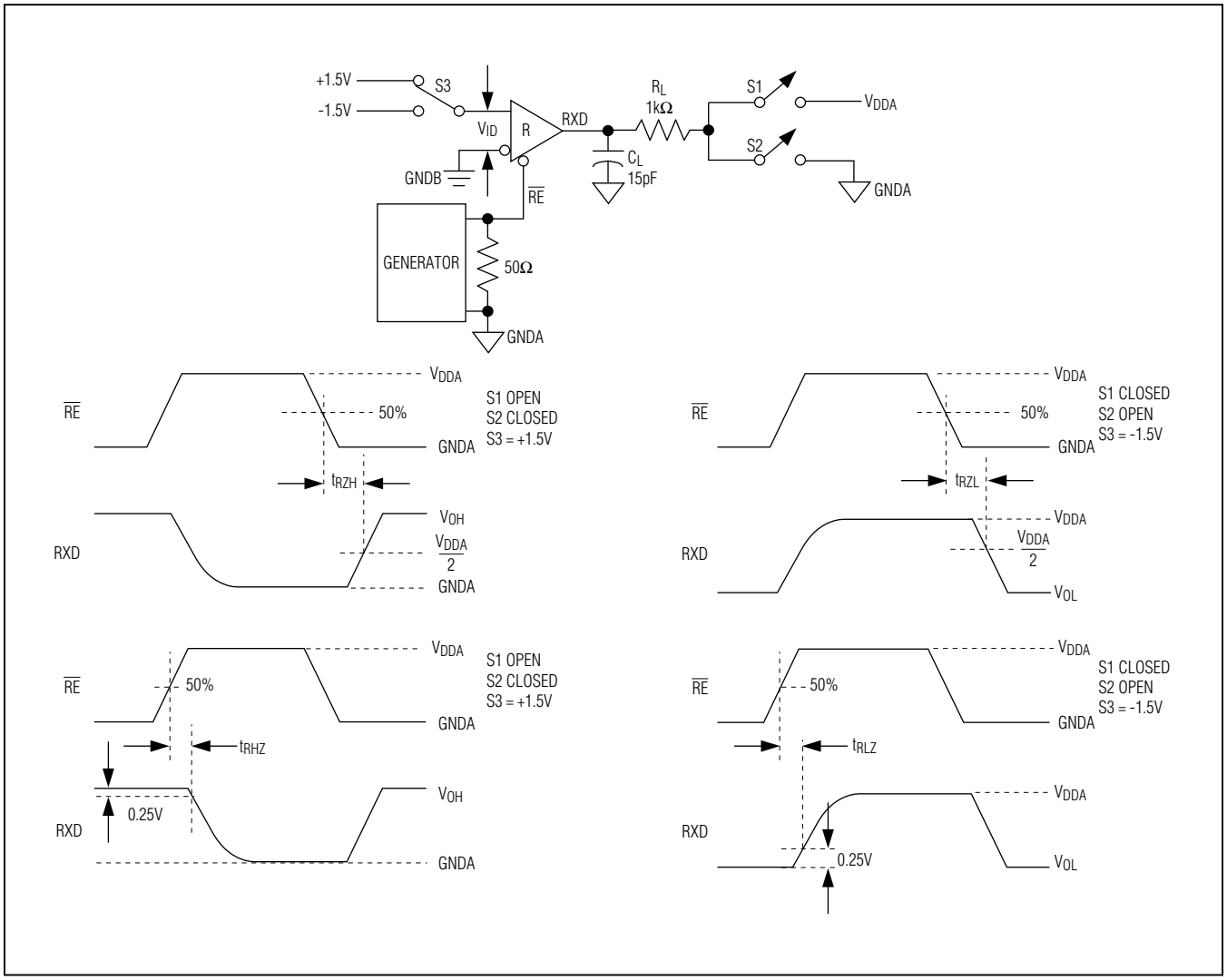
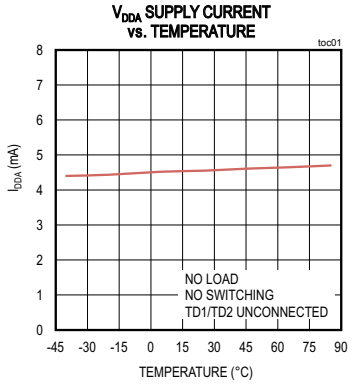
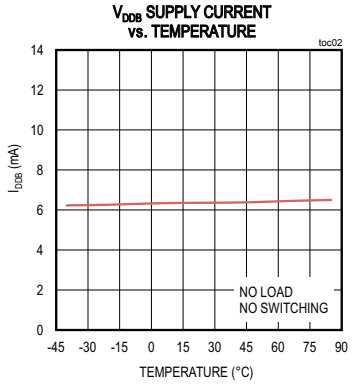


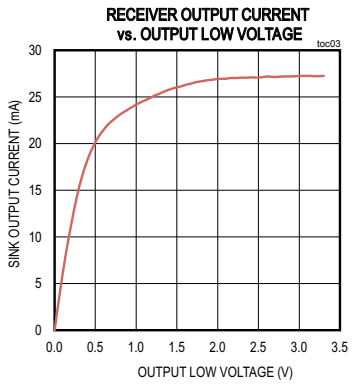
Figure 8. Receiver Enable and Disable Times

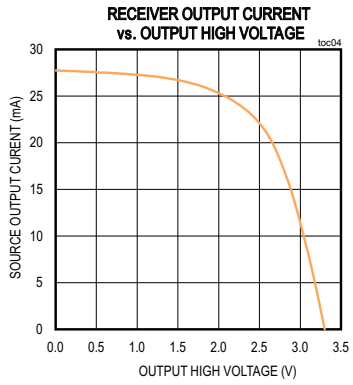
Typical Operating Characteristics

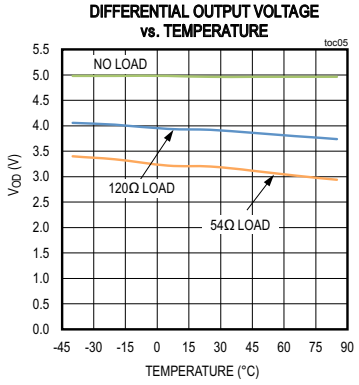
(V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 5V, V_{GNDA} = V_{GNDB}, and T_A = +25°C, unless otherwise noted.)

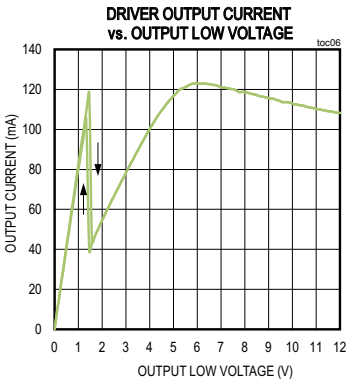


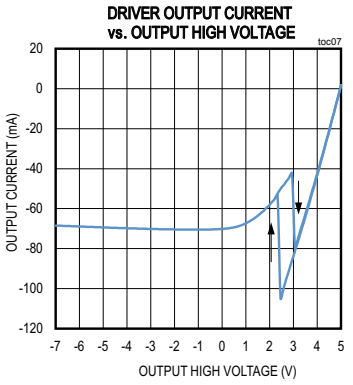


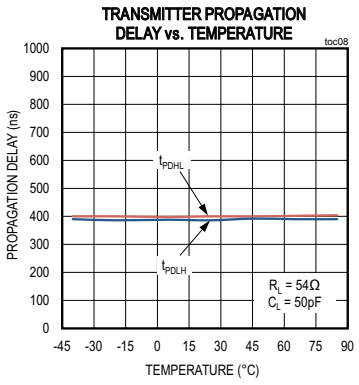


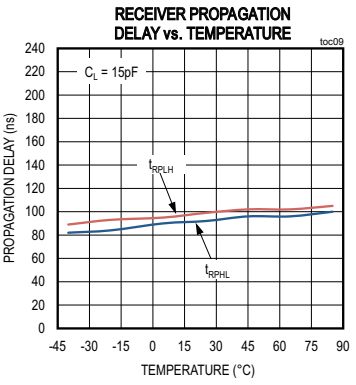






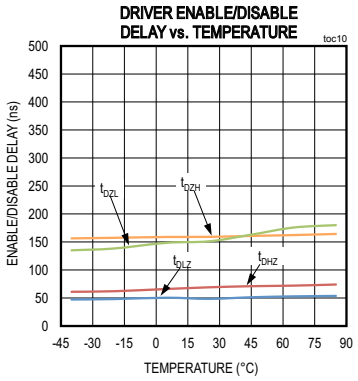


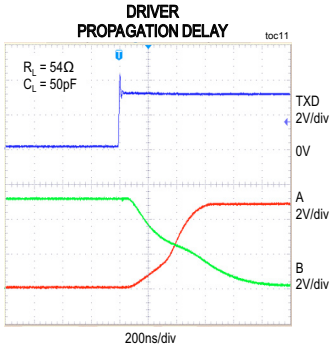


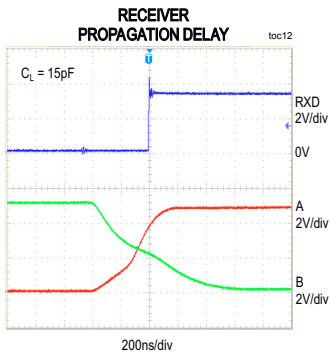


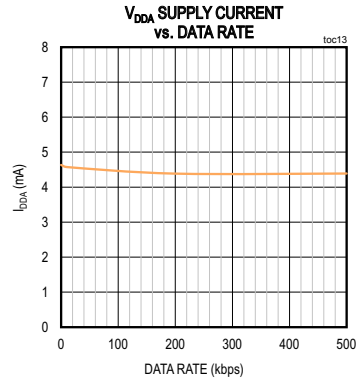
Typical Operating Characteristics (continued)

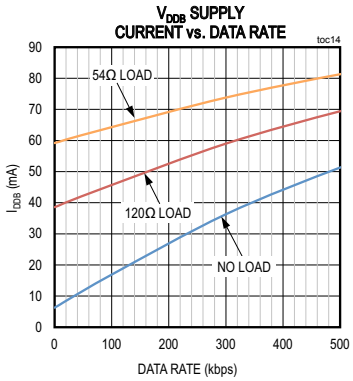
(V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 5V, V_{GNDA} = V_{GNDB}, and T_A = +25°C, unless otherwise noted.)

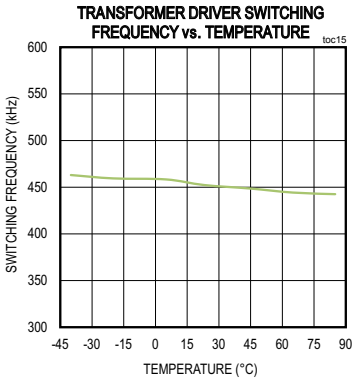


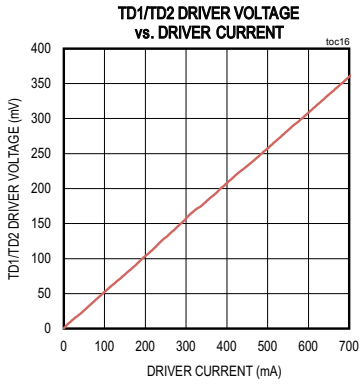


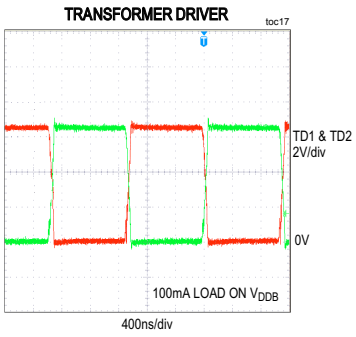




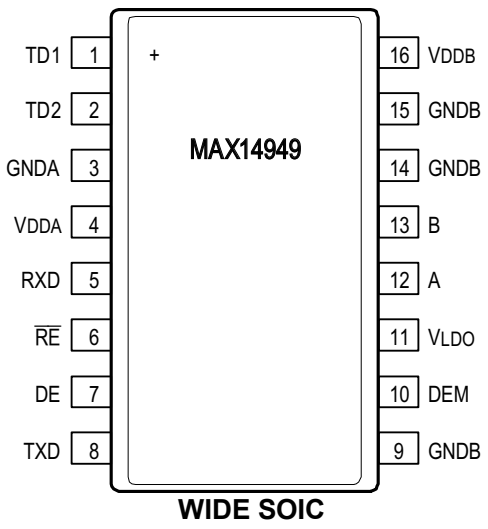








Pin Configuration



Pin Description

PIN	NAME	REFERENCE	FUNCTION
1	TD1	GNDA	Transformer Driver Output 1
2	TD2	GNDA	Transformer Driver Output 2
3	GNDA	—	UART/Logic-Side Ground. GNDA is the ground reference for digital signals and the transformer driver.
4	V_{DDA}	GNDA	Logic-Side Power Input. Bypass V_{DDA} to GNDA with both 0.1µF and 1µF capacitors as close as possible to the device.
5	RXD	GNDA	Receiver Data Output. Drive $\overline{RE}$ low to enable RXD. With $\overline{RE}$ low, RXD is high when (V_A - V_B) > -50mV and is low when (V_A - V_B) < -200mV. RXD is high when V_{DDB} is less than V_{UVLOB}. RXD is high impedance when $\overline{RE}$ is high.
6	$\overline{RE}$	GNDA	Receiver Output Enable. Drive $\overline{RE}$ low or connect to GNDA to enable RXD. Drive $\overline{RE}$ high to disable RXD. RXD is high impedance when $\overline{RE}$ is high. $\overline{RE}$ has an internal 4.5µA pull-down to GNDA.
7	DE	GNDA	Driver Output Enable. Drive DE high to enable bus driver outputs A and B. Drive DE low or connect to GNDA to disable A and B. A and B are high impedance when DE is low. DE has an internal 4.5µA pulldown to GNDA.
8	TXD	GNDA	Driver Input. With DE high, a low on TXD forces the noninverting output (A) low and the inverting output (B) high. Similarly, a high on TXD forces the noninverting output high and the inverting output low. TXD has an internal 4.5µA pullup to V_{DDA}.
9, 14, 15	GNDB	—	Cable-Side Ground. GNDB is the ground reference for the internal LDO, the DEM output, and the RS-485/RS-422 bus signals.

Pin Description (continued)

PIN	NAME	REFERENCE	FUNCTION
10	DEM	GNDB	Driver Enable Monitor Output. DEM is high when the transmitter is enabled. See the *Function Tables* for more information.
11	V_{LDO}	GNDB	LDO Power Input. Connect a minimum voltage of 4.68V to V_{LDO} to power the cable-side of the transceiver. Bypass V_{LDO} to GNDB with both 0.1µF and 1µF capacitors as close as possible to the device. To disable the internal LDO, leave V_{LDO} unconnected or connect to GNDB.
12	A	GNDB	Noninverting Receiver Input and Noninverting Driver Output
13	B	GNDB	Inverting Receiver Input and Inverting Driver Output
16	V_{DDB}	GNDB	Cable-Side Power Input/Isolated LDO Power Output. Bypass V_{DDB} to GNDB with both 0.1µF and 1µF capacitors as close as possible to the device. V_{DDB} is the output of the internal LDO when power is applied to V_{LDO}. When the internal LDO is not used (V_{LDO} is unconnected or connected to GNDB), V_{DDB} is the positive supply input for the cable-side of the IC.

Function Tables

TRANSMITTING						
INPUTS				OUTPUTS		
V_{DDA}	V_{DDB}	DE*	TXD	A	B	DEM
≥ V_{UVLOA}	≥ V_{UVLOB}	1	1	1	0	1
≥ V_{UVLOA}	≥ V_{UVLOB}	1	0	0	1	1
≥ V_{UVLOA}	≥ V_{UVLOB}	0	X	High-Z	High-Z	0
< V_{UVLOA}	≥ V_{UVLOB}	X	X	High-Z	High-Z	0
≥ V_{UVLOA}	< V_{UVLOB}	X	X	High-Z	High-Z	0
< V_{UVLOA}	< V_{UVLOB}	X	X	High-Z	High-Z	0

**Drive DE low to disable the transmitter outputs. Drive DE high to enable the transmitter outputs. DE has an internal pulldown to GNDA.*

X = Don't care.

RECEIVING				
INPUTS				OUTPUTS
V_{DDA}	V_{DDB}	$\overline{RE}$*	(V_A - V_B)	RXD
≥ V_{UVLOA}	≥ V_{UVLOB}	0	> -50mV	1
≥ V_{UVLOA}	≥ V_{UVLOB}	0	< -200mV	0
≥ V_{UVLOA}	≥ V_{UVLOB}	0	Open/Short	1
≥ V_{UVLOA}	≥ V_{UVLOB}	1	X	High-Z
< V_{UVLOA}	≥ V_{UVLOB}	X	X	High-Z
≥ V_{UVLOA}	< V_{UVLOB}	0	X	1
< V_{UVLOA}	< V_{UVLOB}	X	X	High-Z

**Drive RE high to disable the receiver output. Drive $\overline{RE}$ low to enable the receiver output. $\overline{RE}$ has an internal pulldown to GNDA.*

X = Don't care.

Detailed Description

The MAX14949 isolated RS-485/RS-422 transceiver provides 5000V$_{RMS}$ (60s) of galvanic isolation between the RS-485/RS-422 cable-side of the transceiver and the UART-side. This device allows up to 500kbps communication across an isolation barrier when a large potential exists between grounds on each side of the barrier.

Isolation

Both data and power can be transmitted across the isolation barrier. Data isolation is achieved using integrated capacitive isolation that allows data transmission between the UART-side and the cable-side of the transceiver.

To achieve power isolation, the device features an integrated transformer driver to drive an external center-tapped transformer, allowing the transfer of operating power from the UART-side across the isolation barrier to the cable-side. Connect the primary side of the external transformer to the device's transformer driver outputs (TD1 and TD2). Connect the primary center tap to V_{DDA}.

Integrated LDO

The device includes an internal low-dropout regulator with a set 5V (typ) output that is used to power the cable-side of the IC. The output of the LDO is V_{DDB}. The LDO has a 300mA (typ) current limit. If the LDO is unused, connect V_{LDO} to GNDB and apply +5V directly to V_{DDB}.

True Fail-Safe

The device guarantees a logic-high on the receiver output when the receiver inputs are shorted or open, or when connected to a terminated transmission line with all drivers disabled. The receiver threshold is fixed between -50mV and -200mV. If the differential receiver input voltage (V_A - V_B) is greater than or equal to -50mV, RXD is logic-high. In the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage is pulled to zero by the termination resistors. Due to the receiver thresholds of the device, this results in a logic-high at RXD.

Driver Output Protection

Two mechanisms prevent excessive output current and power dissipation caused by faults or by bus contention. The first, a foldback-mode current limit on the output stage, provides immediate protection against short circuits over the entire common-mode voltage range. The second, a thermal-shutdown circuit, forces the driver outputs into a high-impedance state if the die temperature exceeds +160°C (typ).

Thermal Shutdown

The device is protected from overtemperature damage by integrated thermal shutdown circuitry. When the junction temperature (T_J) exceeds +160°C (typ), the driver outputs go high impedance. The device resumes normal operation when T_J falls below +145°C (typ).

Transformer Driver

Overcurrent Limiting

The device features overcurrent limiting to protect the integrated transformer driver from excessive currents when charging large capacitive loads or driving into short circuits. Current limiting is achieved in two stages: internal circuitry monitors the output current and detects when the peak current rises above 1.2A. When the 1.2A threshold is exceeded, internal circuitry reduces the output current to the 730mA current limit. The device monitors the driver current on a cycle-by-cycle basis and limits the current until the short is removed.

The transformer driver on the device can dissipate large amounts of power during overcurrent limiting, causing the IC to enter thermal shutdown. When the junction temperature of the driver exceeds the thermal-shutdown threshold, the TD1 and TD2 driver outputs are disabled. The driver resumes normal operation when the temperature falls below the thermal-shutdown hysteresis.

Transformer Selection

The integrated push-pull transformer driver allows the transmission of operating power from the UART-side, across the isolation barrier, to the isolated cable-side of the device. The 450kHz transformer driver operates with center-tapped primary transformers. Select a transformer with an ET product greater than or equal to the ET of the driver to ensure that the transformer does not enter saturation. E is the voltage applied to the transformer and T is the maximum time it is applied during any one cycle. Calculate the minimum ET product for the transformer primary as:

$$ET = V_{MAX}/(2 \times f_{MIN})$$

where V_{MAX} is the worst-case maximum supply voltage on V_{DDA} and f_{MIN} is the minimum frequency at that supply voltage. For example, using 5.5V and 350kHz, the required minimum ET product is 7.9Vµs. Table 1 includes a list of recommended transformers.

Table 1. Recommended Transformers

MANUFACTURER PART NUMBER	APPLICATION	CONFIGURATION	ISOLATION (V_{RMS})	DIMENSIONS
HALO TGMR-1450V6LF	5V to 3.3V	1CT:1CT	5000	9.45 x 10.87 x 10.03
HALO TGMR-1455V6LF	3.3V to 3.3V	1CT:1.5CT	5000	9.45 x 10.87 x 10.03
WURTH 750315229	5V to 3.3V	1CT:1.1CT	5000	9.14 x 8.00 x 7.62
WURTH 750315230	3.3V to 3.3V	1CT:1.3CT	5000	9.14 x 8.00 x 7.62
WURTH 750315231	3.3V to 3.3V	1CT:1.7CT	5000	9.14 x 8.00 x 7.62

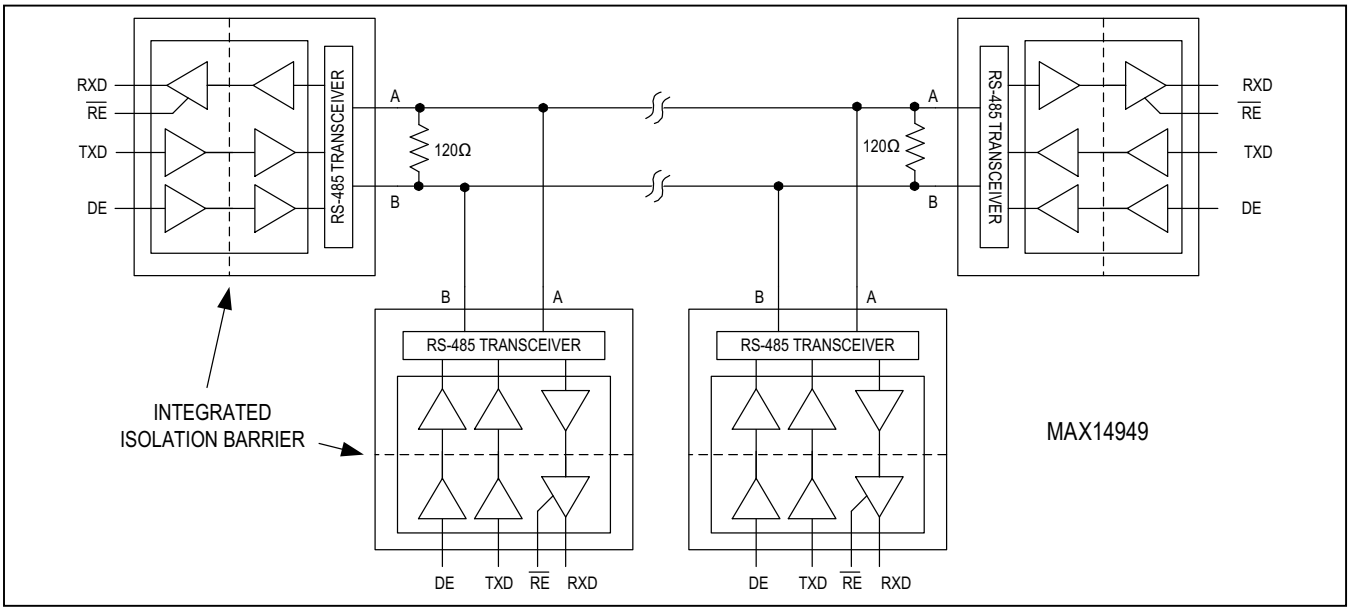


Figure 9. Typical Isolated Half-Duplex RS-485 Application

Applications Information

256 Transceivers on the Bus

The standard RS-485 receiver input impedance is one unit load, and a standard driver can drive up to 32 unit loads. The device transceiver has a 1/8-unit load receiver, which allows up to 256 transceivers connected in parallel on one communication line. Connect any combination of these devices, and/or other RS-485/RS-422 devices, for a maximum of 32 unit loads to the line.

Typical Application

The transceiver is designed for bidirectional data communications on multipoint bus-transmission lines. Figure 9 and Figure 10 show typical network application circuits. To minimize reflections, the bus should be terminated at both ends in its characteristics impedance, and stub lengths off the main line should be kept as short as possible.

Layout Considerations

It is recommended to design an isolation or keep out channel underneath the isolator that is free from ground and signal planes. Any galvanic or metallic connection between the cable-side and UART-side defeats the isolation.

Ensure that the decoupling capacitors between V_{DDA} and GNDA and between V_{LDO}, V_{DDB}, and GNDB are located as close as possible to the IC to minimize inductance.

Route important signal lines close to the ground plane to minimize possible external influences. On the cable-side of the device, it is good practice to have the bus connectors and termination resistor as close as possible to the A and B pins.

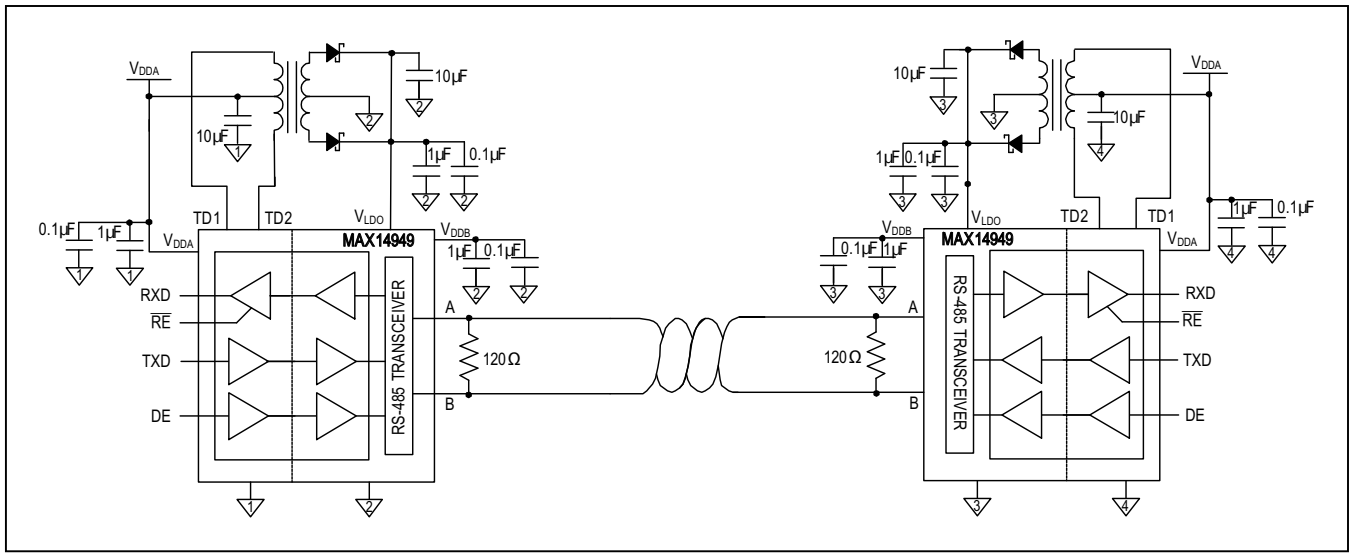


Figure 10. Typical Isolated Half-Duplex RS-485 Application with Integrated Transformer Driver

Extended ESD Protection

ESD-protection structures are incorporated on all pins to protect against electrostatic discharge encountered during handling and assembly. The driver outputs and receiver inputs of the MAX14949 have extra protection against static electricity. The ESD structures withstand high ESD in normal operation and when powered down. After an ESD event, the devices keep working without latchup or damage.

Bypass V_{DDA} to GNDA and bypass V_{DDB} and V_{LDO} to GNDB with 0.1µF and 1µF capacitors to ensure maximum ESD protection.

ESD protection can be tested in various ways. The transmitter outputs and receiver inputs of the device are characterized for protection to the cable-side ground (GNDB) to the following limits:

- ±30kV HBM
- ±15kV using the Air-Gap Discharge method specified in IEC 61000-4-2
- ±10kV using the Contact Discharge method specified in the IEC 61000-4-2

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model (HBM)

Figure 11 shows the HBM test model and Figure 12 shows the current waveform it generates when discharged in a low-impedance state. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged in to the test device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The device helps in designing equipment to meet IEC 61000-4-2 without the need for additional ESD-protection components.

The major difference between tests done using the HBM and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the HBM.

Figure 13 shows the IEC 61000-4-2 model and Figure 14 shows the current waveform for IEC 61000-4-2 ESD Contact Discharge Test.

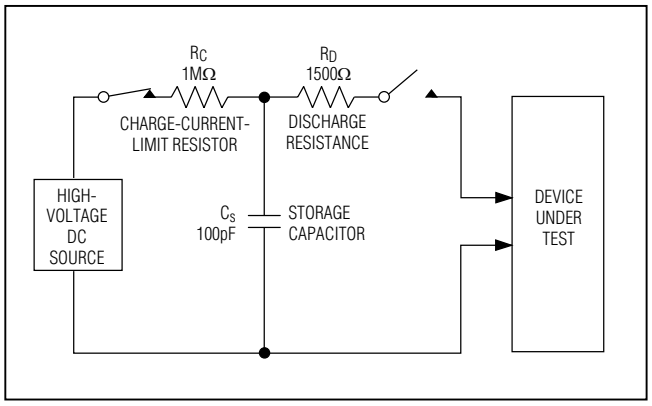


Figure 11. Human Body ESD Test Model

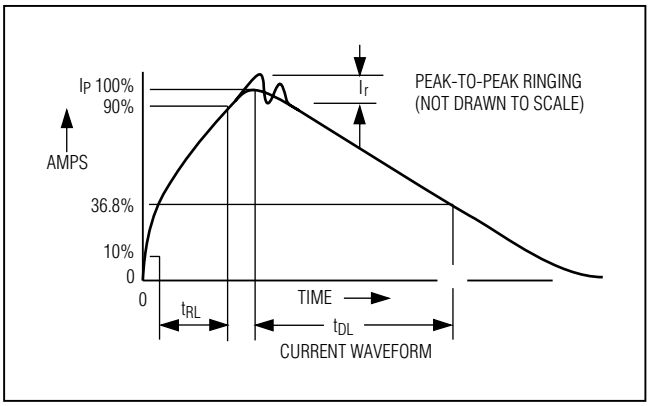


Figure 12. Human Body Current Waveform

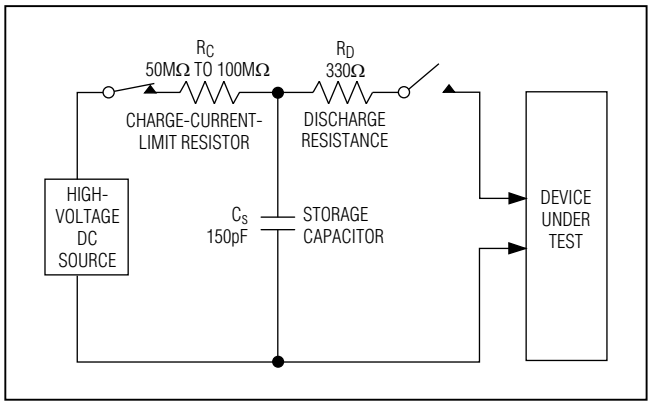


Figure 13. IEC 61000-4-2 ESD Test Model

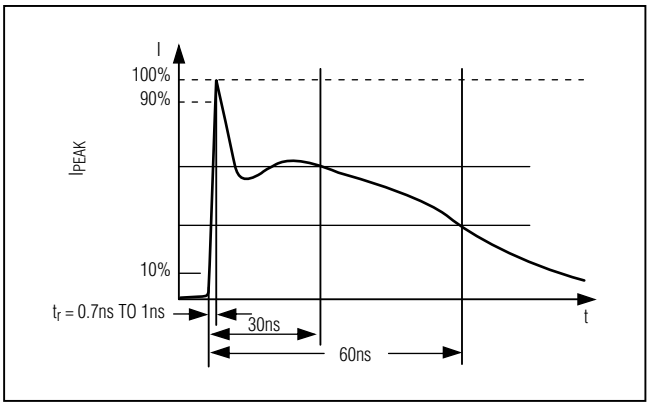
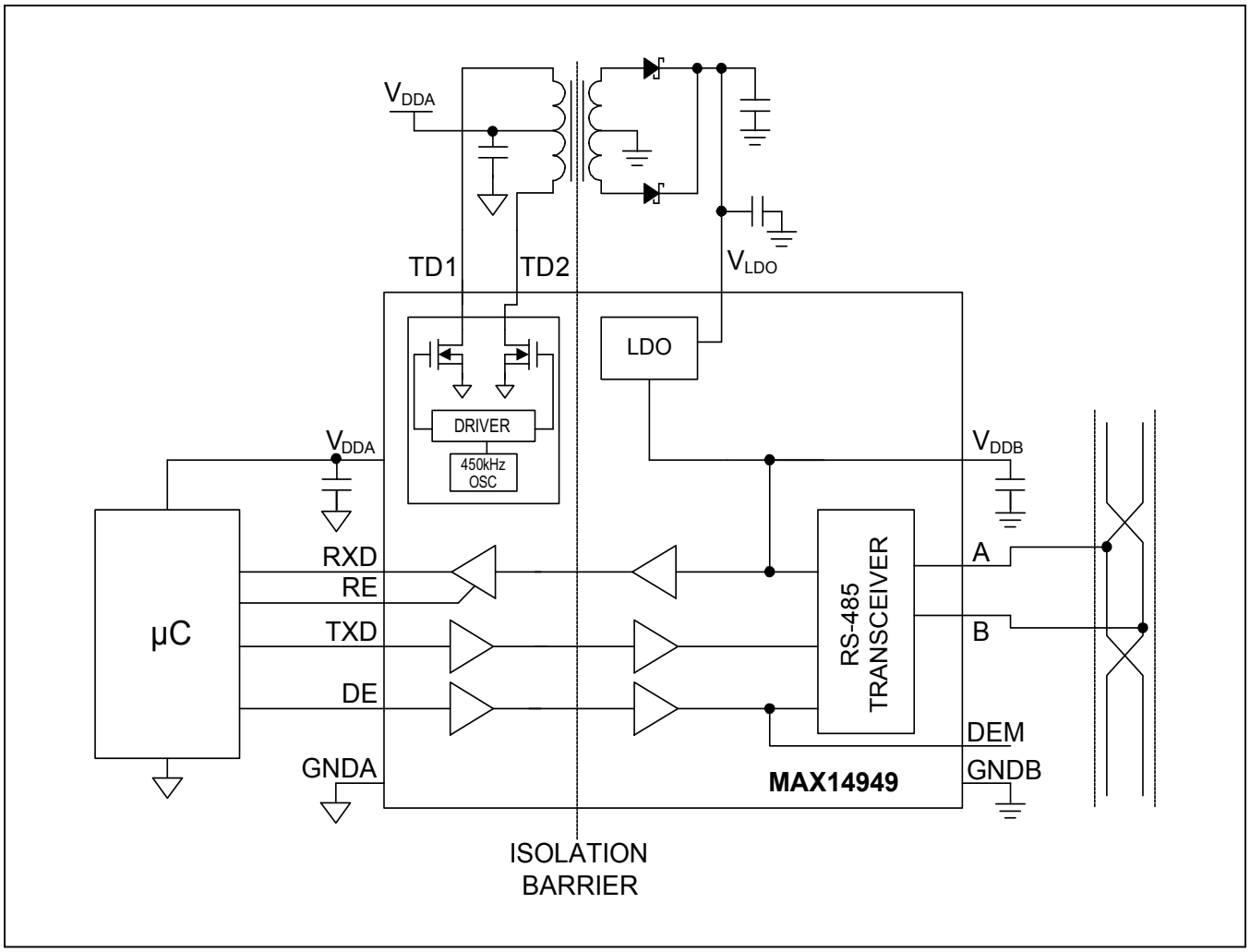


Figure 14. IEC 61000-4-2 ESD Generator Current Waveform

Typical Application Circuit



Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 SOIC	W16M+10	21-0042	90-0107

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14949EWE+	-40°C to +85°C	16 SOIC (W)
MAX14949EWE+T	-40°C to +85°C	16 SOIC (W)

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/15	Initial release	—

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- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

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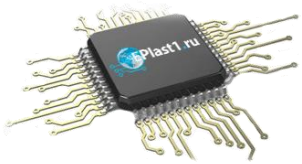
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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