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Power management integrated circuit (PMIC) for i.MX 7 and i.MX 6 SoloLite/SoloX/UltraLite processors

PF3001

POWER MANAGEMENT

EP SUFFIX
98ASA00719D
48 QFN 7.0 X 7.0

ES SUFFIX
98ASA00933D
48 QFN 7.0 X 7.0

The PF3001 is a SMARTMOS power management integrated circuit (PMIC) designed specifically for always ON applications with the NXP i.MX 7 and i.MX 6 SoloLite/SoloX/UltraLite application processors. With up to three buck converters, six linear regulators, RTC supply, and coin-cell charger, the PF3001 can provide power for a complete system, including applications processors, memory, and system peripherals.

Features:

- Three adjustable high efficiency buck regulators: 2.75 A, 1.5 A, 1.25 A
  - Selectable modes: PWM, PFM, APS
  - Programmable output voltage, PWM switching frequency, current limit
- Six adjustable general purpose linear regulators
- Input voltage range: 2.8 V to 4.5 V or 3.7 V to 5.5 V
- I^2C control
- Coin cell charger and always ON RTC supply
- -40 °C to +125 °C Operating Junction Temperature

Applications:

- IPTV
- Set top boxes
- POS terminals
- Industrial control
- Medical monitoring
- Home automation/security/energy management

Figure 1. PF3001 simplified application diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

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1 Orderable parts

The PF3001 is available with pre-programmed OTP memory configurations. The devices are identified using the program codes from Table 1. Details of the start-up programming for each device can be found in Table 32.

Table 1. Orderable part variations

Part number	Temperature (T_A)	Package	Programming options	Notes
MC32PF3001A1EP	-40 °C to 85 °C (For use in consumer applications)	98ASA00719D, 48 QFN 7.0 mm x 7.0 mm with exposed pad	1 (i.MX 7 with DDR3L)	(1)
MC32PF3001A2EP			2 (i.MX 7 with LPDDR3)	
MC32PF3001A3EP			3 (i.MX 6SX with DDR3L)	
MC32PF3001A4EP			4 (i.MX 6SX with DDR3)	
MC32PF3001A5EP			5 (i.MX 6SL with LPDDR2)	
MC32PF3001A6EP			6 (i.MX 6UL with LPDDR2)	
MC32PF3001A7EP			7 (i.MX 6UL with DDR3L)	
MC33PF3001A6ES	-40 °C to 105 °C (For use in automotive applications)	98ASA00933D, 48 QFN 7.0 mm x 7.0 mm WF-type (wettable flank)	6 (i.MX 6UL with LPDDR2)	(1)
MC33PF3001A7ES			7 (i.MX 6UL with DDR3L)	
MC34PF3001A1EP	-40 °C to 105 °C (For use in industrial applications)	98ASA00719D, 48 QFN 7.0 mm x 7.0 mm with exposed pad	1 (i.MX 7 with DDR3L)	(1)
MC34PF3001A2EP			2 (i.MX 7 with LPDDR3)	
MC34PF3001A3EP			3 (i.MX 6SX with DDR3L)	
MC34PF3001A4EP			4 (i.MX 6SX with DDR3)	
MC34PF3001A5EP			5 (i.MX 6SL with LPDDR2)	
MC34PF3001A6EP			6 (i.MX 6UL with LPDDR2)	
MC34PF3001A7EP			7 (i.MX 6UL with DDR3L)	

Notes
1. For Tape and Reel add an R2 suffix to the part number.

2 General description

The PF3001 is the power management integrated circuit (PMIC) designed primarily for use with NXP's i.MX series of multi-media application processors. It is also capable of providing full power solutions to i.MX 6SL, 6SX, 6UL, and i.MX7processors.

2.1 Features

This section summarizes the PF3001 features.

- Input voltage range to PMIC: 2.8 V to 4.5 V, or 3.7 V to 5.5 V [(2)]
  - Buck regulators
    - SW1, 2.75 A; 0.7 V to 1.425 V, 1.8 V, 3.3 V
    - SW2, 1.25 A; 1.50 V to 1.85 V, or 2.50 V to 3.30 V
    - SW3, 1.5 A; 0.90 V to 1.65 V
    - Dynamic voltage scaling
    - Modes: PWM, PFM, APS
    - Programmable output voltage
    - Programmable current limit
    - Programmable PWM switching frequency
  - LDOs
    - VCC_SD, 1.8 V to 1.85 V, or 2.85 V to 3.30 V, 100 mA based on SD_VSEL
    - V33, 2.85 V to 3.30 V, 350 mA
    - VLDO1, 1.8 V to 3.3 V, 100 mA
    - VLDO2, 0.80 V to 1.55 V, 250 mA
    - VLDO3, 1.8 V to 3.3 V, 100 mA
    - VLDO4, 1.8 V to 3.3 V, 350 mA
- Always ON RTC regulator/switch VSNVS 3.0 V, 1.0 mA
- Battery backed memory including coin cell charger
- I^2C interface

Notes

2. 2.8 V to 4.5 V when VIN is used at input. 3.7 V to 5.5 V when VPWR is used as input.

2.2 Functional block diagram

Figure 2. PF3001 functional block diagram

3 Internal Block Diagram

Figure 3. PF3001 simplified internal block diagram

4 Pin connections

4.1 Pinout diagram

Figure 4. PF3001 pinout diagram

4.2 Pin definitions

Table 2. Pin definitions

Pin number	Pin name	Pin function	Type	Definition
1	INTB	O	Digital	Open drain interrupt signal to processor
2	SD_VSEL	I/O	Digital	Input from i.MX processor to select VCC_SD regulator voltage • SD_VSEL=0, VCC_SD = 2.85 V to 3.3 V • SD_VSEL= 1, VCC_SD = 1.8 V to 1.85 V
3	RESETBMCU	O	Digital	Open drain reset output to processor
4	GND	I	GND	Ground reference. Connect to ground.
5	ICTEST1	I	Digital and Analog	Reserved pin. Connect to GND in application
6	SW1FB [(3)]	I	Analog	SW1 output voltage feedback pin. Route this trace separately from the high current path and terminate at the output capacitance or near the load, if possible for best regulation
7	SW1IN [(3)]	I	Analog	Input to SW1 regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible
8	SW1LX [(3)]	O	Analog	Switcher 1 switch node connection. Connect to SW1LX and connect to SW1 inductor
9	SW1LX [(3)]	O	Analog	Switcher 1 switch node connection. Connect to SW1LX and connect to SW1 inductor
10	SW1IN [(3)]	I	Analog	Input to SW1 regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible
11	NC	–	Reserved	Leave floating
12	GNDREF1	GND	GND	Ground reference for SW1. Connect to GND. Keep away from high current ground return paths
13	VLDO1IN	I	Analog	VLDO1 input supply. Bypass with a 1.0 µF decoupling capacitor as close to the pin as possible
14	VLDO1	O	Analog	VLDO1 regulator output. Bypass with a 2.2 µF ceramic output capacitor
15	VLDO2	O	Analog	VLDO2 regulator output. Bypass with a 4.7 µF ceramic output capacitor
16	VLDO2IN	I	Analog	VLDO2 input supply. Bypass with a 1.0 µF decoupling capacitor as close to the pin as possible
17	SW2LX [(3)]	O	Analog	Switcher 2 switch node connection. Connect to SW2 inductor
18	SW2IN [(3)]	I	Analog	Input to SW2 regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible
19	SW2FB [(3)]	I	Analog	SW2 output voltage feedback pin. Route this trace separately from the high current path and terminate at the output capacitor or near the load, if possible for best regulation
20	VLDO3	O	Analog	VLDO3 regulator output. Bypass with a 2.2 µF ceramic output capacitor
21	VLDO34IN	I	Analog	VLDO3 and VLDO4 input supply. Bypass with a 1.0 µF decoupling capacitor as close to the pin as possible
22	VLDO4	O	Analog	VLDO4 regulator output. Bypass with a 2.2 µF ceramic output capacitor
23	NC	–	Reserved	Leave floating
24	GND	GND	GND	Ground reference. Connect to ground. Keep away from high current ground return paths
25	NC	–	Reserved	Leave floating
26	GNDREF2	GND	GND	Reference ground for SW2 and SW3 regulators. Connect to GND. Keep away from high current ground return paths
27	SW3FB [(3)]	I	Analog	SW3 output voltage feedback pin. Route this trace separately from the high current path and terminate at the output capacitor or near the load, if possible for best regulation
28	SW3IN [(3)]	I	Analog	Input to SW3 regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible

Table 2. Pin definitions (continued)

Pin number	Pin name	Pin function	Type	Definition
29	SW3LX [(3)]	O	Analog	Switcher 3 switch node connection. Connect the SW3 inductor
30	LDOG	O	Analog	Connect to gate of front-end LDO external pass P-MOSFET. Leave floating if VPWR LDO is not used
31	VPWR	I	Analog	Input to optional front-end VPWR LDO for systems with input voltage > 4.5 V
32	V33	O	Analog	V33 regulator output. Bypass with a 4.7 μF ceramic output capacitor
33	VCC_SD	O	Analog	Output of VCC_SD regulator. Bypass with a 2.2 μF ceramic output capacitor.
34	VSNVS	O	Analog	VSNVS regulator/switch output. Bypass with 0.47 μF capacitor to ground.
35	NC	–	Reserved	Leave floating
36	LICELL	I/O	Analog	Coin cell supply input/output. Bypass with 0.1 μF capacitor. Connect to optional coin cell.
37	NC	–	Reserved	Leave floating
38	VIN2	I	Analog	Input to VCC_SD, V33 regulators. Connect to VIN rail and bypass with 10 μF capacitor
39	ICTEST2	I	Digital & Analog	Reserved pin. Connect to GND in application
40	GNDREF	GND	GND	Ground reference for IC core circuitry. Connect to ground. Keep away from high current ground return paths
41	VCORE	O	Analog	Internal analog core supply. Bypass with 1.0 μF capacitor to ground
42	VIN	I	Analog	Main IC supply. Bypass with 1.0 μF capacitor to ground. Connect to system input supply if voltage ≤ 4.5 V. Connect to drain of external PFET when VPWR LDO is used for systems with input voltage > 4.5 V
43	VCOREDIG	O	Analog	Internal digital core supply. Bypass with 1.0 μF capacitor to ground
44	VCOREREF	O	Analog	Main band gap reference. Bypass with 220 nF capacitor to ground
45	SDA	I/O	Digital	I^2C data line (open drain). Pull up to VDDIO with a 4.7 kΩ resistor
46	SCL	I	Digital	I^2C clock. Pull up to VDDIO with a 4.7 kΩ resistor
47	VDDIO	I	Analog	Supply for I^2C bus. Bypass with 0.1 μF ceramic capacitor. Connect to 1.7 V to 3.6 V supply. Ensure VDDIO is always lesser than or equal to VIN
48	PWRON	I	Digital	Power ON/OFF input from processor
-	EP	GND	GND	Expose pad. Functions as ground return for buck and boost regulators. Tie this pad to the inner and external ground planes through vias to allow effective thermal dissipation

Notes

3. Unused switching regulators should be connected as follows: Pins SWxLX and SWxFB should be unconnected and Pin SWxIN should be connected to VIN with a 0.1 μF bypass capacitor.

5 General product characteristics

5.1 Maximum ratings

Table 3. Maximum voltage ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause malfunction or permanent damage to the device. The detailed maximum voltage rating per pin can be found in the pin list section.

Symbol	Description	Value	Unit	Notes
Electrical ratings				
VPWR, ICTEST1, ICTEST2, LDOG	–	-0.3 to 7.5	V	(4)
VIN, VIN2, VLDO1IN, SW1IN, SW2IN, SW3IN, SW1LX, SW2LX, SW3LX	–	-0.3 to 4.8	V	
INTB, SD_VSEL, RESETBMCU, SW1FB, SW2FB, SW3FB, VLDO1, VLDO2IN, VLDO3, VLDO34IN, VLDO4, V33, VCC_SD, VSNVS, LICELL, VCORE, SDA, SCL, VDDIO, PWRON	–	-0.3 to 3.6	V	
VLDO2	VLDO2 linear regulator output	-0.3 to 2.5	V	
VCOREDIG	Digital core supply voltage output	-0.3 to 1.65	V	
VCOREREF	Bandgap reference voltage output	-0.3 to 1.5	V	
V_{ESD}	ESD ratings • Human body model • Charge device model	 ±2000 ±500	V	(5)

Notes

4. 7.5 V Maximum DC voltage rated.
5. ESD testing is performed in accordance with the Human body model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), and the Charge device model (CDM), Robotic (C_{ZAP} = 4.0 pF).

5.2 Thermal characteristics

Table 4. Thermal ratings

Symbol	Description (rating)	Min.	Max.	Unit	Notes
Thermal ratings					
T_A	Ambient operating temperature range • Industrial version • Consumer version	 -40 -40	 105 85	°C	
T_J	Operating junction temperature range	-40	125	°C	(6)
T_{ST}	Storage temperature range	-65	150	°C	
T_{PPRT}	Peak package reflow temperature	–	(8)	°C	(7) (8)
QFN48 thermal resistance and package dissipation ratingS					
$R_{\theta JA}$	Junction to ambient, natural convection • Four layer board (2s2p) • Eight layer board (2s6p)	 – –	 24 15	°C/W	(9) (10) (11)
$R_{\theta JB}$	Junction to Board	–	11	°C/W	(12)
$R_{\Theta JCBOTTOM}$	Junction to case bottom	–	1.4	°C/W	(13)
ΨJT	Junction to package top • Natural convection	–	1.3	°C/W	(14)

Notes

6. Do not operate beyond 125 °C for extended periods of time. Operation above 150 °C may cause permanent damage to the IC. See thermal protection thresholds for thermal protection features.
7. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.
8. NXP's package reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For peak package reflow temperature and moisture sensitivity levels (MSL), go to www.nxp.com, search by part number (remove prefixes/suffixes) and enter the core ID to view all orderable parts, and review parametrics.
9. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
10. The Board uses the JEDEC specifications for thermal testing (and simulation) JESD51-7 and JESD51-5.
11. Per JEDEC JESD51-6 with the board horizontal.
12. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
13. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
14. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters (Ψ) are not available, the thermal characterization parameter is written as Psi-JT.

5.3 Current consumption

The current consumption of the individual blocks is described in detail in the following table.

Table 5. Current consumption summary

T_A= -40 °C to 105 °C, V_{PWR}= 0 V (External pass FET is not populated), V_{IN} = 3.6 V, V_{DDIO} = 1.7 V to 3.6 V, L_{ICELL} = 1.8 V to 3.3 V, V_{SNVS} = 3.0 V, typical external component values, unless otherwise noted. Typical values are characterized at VIN = 3.6 V, V_{PWR} = 0 V, V_{DDIO} = 3.3 V, L_{ICELL} = 3.0 V, V_{SNVS} = 3.0 V and 25 °C, unless otherwise noted.

Mode	PF3001 conditions	System conditions	Typ.	Max.	Unit	Notes
Coin Cell	VSNVS from LICELL, All other blocks off, V_{IN} = 0.0 V	No load on VSNVS	4.0	7.0	µA	(15) (16)
Off	VSNVS from VIN or LICELL Wake-up from PWRON active 32 kHz RC on All other blocks off VIN ≥ UVDET	No load on VSNVS, PMIC able to wake-up	16	25	µA	(15) (16)
ON	VSNVS from VIN SW1 in APS SW2 in APS SW3 in APS Trimmed 16 MHz RC enabled Trimmed reference active, VLDO1-4 enabled V33 enabled VCC_SD enabled	No load on any of the regulators.	1.2		mA	

Notes

15. At 25 °C only.
16. When V_{IN} is below the UVDET threshold, in the range of 1.8 V ≤ V_{IN} < 2.65 V, the quiescent current increases by 50 µA, typically.

5.4 Electrical characteristics

Table 6. Electrical characteristics – front-end input LDO

All parameters are specified at T_A = -40 °C to 105 °C, V_{PWR} = 5.0 V, V_{IN} = 4.4 V, I_{VIN} = 300 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{PWR} = 5.0 V, V_{IN} = 4.4 V, I_{VIN} = 300 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Front end input LDO (VPWR LDO)						
V_{PWR}	Operating input voltage • In regulation • In dropout operation	 4.6 3.7	 – –	 5.5 4.6	V	(17)
V_{IN}	On mode output voltage, 4.6 V < V_{PWR} < 5.5 V, 0.0 mA < I_{VIN} < 3000 mA	4.3	4.4	4.55	V	
I_{VIN}	Operating load current at VIN, 3.7 V < V_{PWR} < 5.5 V	0.0	–	3.0	A	
I_{LDOGQ}	ON mode quiescent current, No load,	–	5.0	10	mA	
V_{IN}	Low power mode output voltage, 4.6 V < V_{PWR} < 5.5 V 0.0 mA < I_{VIN} < 1.0 mA	3.7		4.5	V	
$V_{PWROFFMODE}$	Off mode output voltage, (CL = 100 µF) 4.6 V < V_{PWR} < 5.5 V, 0.0 mA < I_{VIN} < 35 µA	3.2		4.8	V	
V_{PWRUV}	VPWR undervoltage threshold (upon undervoltage condition the external pass FET is turned off)	3.1	–	3.7	V	
V_{PWROV}	VPWR overvoltage threshold (upon overvoltage condition interrupt is asserted at INTB)	5.5	–	6.5	V	
$I_{VINUVILIMIT}$	VPWR LDO current limit under VIN short-circuit (V_{IN} < UVDET)	–	–	300	mA	
$I_{VINLEAKAGE}$	Reverse leakage current from VIN to VPWR, No external pass FET, VPWR is grounded, device is in OFF state	–	–	1.0	µA	
$I_{VPWROFF}$	VPWR LDO Off mode quiescent current	–	–	75	µA	(18)

Notes

17. While the front end LDO can handle spikes up to 7.5 V at VPWR for as long as 200 µs, the circuit is not expected to be continuously operated when VPWR is above 5.5 V.
18. This specification gives the leakage current in the VPWR LDO block. Total OFF mode current includes the quiescent current from the other blocks as specified in Table 5.

Table 7. Static electrical characteristics – SW1

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{SW1IN} = 3.6 V, V_{SW1} = 1.2 V, I_{SW1} = 100 mA, typical external component values, f_{SW1} = 2.0 MHz, unless otherwise noted. Typical values are characterized at V_{IN} = V_{SW1IN} = 3.6 V, V_{SW1} = 1.2 V, I_{SW1} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit	Notes
Switch mode supply SW1						
V_{SW1IN}	Operating input voltage	2.8	–	4.5	V	(19)
V_{SW1}	Nominal output voltage	–	Table 40	–	V	
V_{SW1ACC}	Output voltage accuracy • PWM, APS, 2.8 V < V_{SW1IN} < 4.5 V, 0 < I_{SW1} < 2.75 A 0.7 V ≤ V_{SW1} ≤ 1.2 V • PFM, APS, 2.8 V < V_{SW1IN} < 4.5 V, 0 < I_{SW1} < 2.75A 1.225 V < V_{SW1} < 1.425 V • PFM, steady state, 2.8 V < V_{SW1IN} < 4.5 V, 0 < I_{SW1} < 150 mA 1.8 V ≤ V_{SW1} ≤ 1.425 V • PWM, APS, 2.8 V < V_{SW1IN} < 4.5 V, 0 < I_{SW1} < 2.75A 1.8 V < V_{SW1} < 3.3 V • PFM, steady state, 2.8 V < V_{SW1IN} < 4.5 V, 0 < I_{SW1} < 150 mA 1.8 V ≤ V_{SW1} ≤ 3.3 V	-25 -25 -45 -6.0 -6.0	–	25 25 45 6.0 6.0	mV mV mV % %	
I_{SW1}	Rated output load current, • 2.8 V ≤ V_{SW1IN} ≤ 4.5 V, 0.7 V < V_{SW1} < 1.425 V, 1.8 V, 3.3 V	–	–	2750	mA	
I_{SW1Q}	Quiescent current • PFM mode • APS mode	– –	22 300	– –	µA	
I_{SW1LIM}	Current limiter peak current detection , current through inductor • SW1ILM = 0 (default) • SW1ILM = 1	3.5 2.6	5.5 4.0	7.5 5.4	A	
ΔV_{SW1}	Output ripple	–	5.0	–	mV	
R_{SW1DIS}	Discharge resistance	–	600	–	Ω	

Notes

19. The maximum operating input voltage is 4.55 V when VPWR LDO is used

Table 8. Dynamic electrical characteristics - SW1

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{SW1IN} = 3.6 V, V_{SW1} = 1.2 V, I_{SW1} = 100 mA, typical external component values, f_{SW1} = 2.0 MHz, unless otherwise noted. Typical values are characterized at V_{IN} = V_{SW1IN} = 3.6 V, V_{SW1} = 1.2 V, I_{SW1} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SW1 (single phase)						
V_{SW1OSH}	Start-up Overshoot, I_{SW1} = 0 mA, slew rate = 25 mV/4 µs, V_{IN} = V_{SW1IN} = 4.5 V, V_{SW1} = 1.425 V	–	–	66	mV	
t_{ONSW1}	Turn-on time, enable to 90% of end value, I_{SW1} = 0 mA, slew rate = 25 mV/4 µs, V_{IN} = V_{SW1IN} = 4.5 V, V_{SW1} = 1.425 V	–	–	500	µs	

Table 9. Static electrical characteristics – SW2

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{SW2IN} = 3.6 V, V_{SW2} = 3.15 V, I_{SW2} = 100 mA, typical external component values, f_{SW2} = 2.0 MHz, unless otherwise noted. Typical values are characterized at V_{IN} = V_{SW2IN} = 3.6 V, V_{SW2} = 3.15 V, I_{SW2} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SW2						
V_{SW2IN}	Operating Input Voltage	2.8	–	4.5	V	(20), (21)
V_{SW2}	Nominal output voltage	–	Table 42	–	V	
V_{SW2ACC}	Output voltage accuracy • PWM, APS, 2.8 V ≤ V_{SW2IN} ≤ 4.5 V, 0 ≤ I_{SW2} ≤ 1.25 A • 1.50 V ≤ V_{SW2} ≤ 1.85 V • 2.5 V ≤ V_{SW2} ≤ 3.3 V • PFM, 2.8 V ≤ V_{SW2IN} ≤ 4.5 V, 0 ≤ I_{SW2} ≤ 50 mA • 1.50 V ≤ V_{SW2} ≤ 1.85 V • 2.5 V ≤ V_{SW2} ≤ 3.3 V	 -3.0 -6.0 -6.0 -6.0	 – – – –	 3.0 6.0 6.0 6.0	%	
I_{SW2}	Rated output load current, 2.8 V < V_{SW2IN} < 4.5 V, 1.50 V < V_{SW2} < 1.85 V, 2.5 V < V_{SW2} < 3.3 V	–	–	1250	mA	(22)
I_{SW2Q}	Quiescent current • PFM mode • APS mode (low output voltage settings, CTL_SW2_HL = 0) • APS mode (high output voltage settings, CTL_SW2_HL = 1)	 – – –	 23 145 305	 – – –	µA	
I_{SW2LIM}	Current limiter peak current detection, current through inductor • SW2ILM = 0 (default) • SW2ILM = 1	 1.625 1.235	 2.5 1.9	 3.375 2.565	A	
ΔV_{SW2}	Output ripple	–	5.0	–	mV	
R_{ONSW2P}	SW2 P-MOSFET $R_{DS(on)}$ at V_{IN} = V_{SW2IN} = 3.3 V	–	215	245	mΩ	
R_{ONSW2N}	SW2 N-MOSFET $R_{DS(on)}$ at V_{SW2IN} = V_{SW2IN} = 3.3 V	–	258	326	mΩ	
I_{SW2PQ}	SW2 P-MOSFET leakage current, V_{IN} = V_{SW2IN} = 4.5 V	–	–	10.5	µA	
I_{SW2NQ}	SW2 N-MOSFET leakage current, V_{IN} = V_{SW2IN} = 4.5 V	–	–	3.0	µA	
R_{SW2DIS}	Discharge resistance during OFF mode	–	600	–	Ω	

Notes

20. The maximum operating input voltage is 4.55 V when VPWR LDO is used.
21. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any PF3001 regulator, or external system supply.
22. The higher output voltages available depend on the voltage drop in the conduction path as given by the following equation: (V_{SW2IN} - V_{SW2}) = I_{SW2}* (DCR of Inductor +R_{ONSW2P} + PCB trace resistance).

Table 10. Dynamic electrical characteristics - SW2

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{SW2IN} = 3.6 V, V_{SW2} = 3.15 V, ISW2 = 100 mA, typical external component values, f_{SW2} = 2.0 MHz, unless otherwise noted. Typical values are characterized at V_{IN} = V_{SW2IN} = 3.6 V, V_{SW2} = 3.15 V, I_{SW2} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch Mode Supply SW2						
V_{SW2OSH}	Start-up overshoot, I_{SW2} = 0.0 mA, slew rate = 25 mV/4 µs, V_{IN} = V_{SW2IN} = 4.5 V	–	–	66	mV	
t_{ONSW2}	Turn-on time, enable to 90% of end value, I_{SW2} = 0.0 mA, slew rate = 25 mV/4 µs, V_{IN} = V_{SW2IN} = 4.5 V	–	–	500	µs	

Table 11. Static electrical characteristics – SW3

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{SW3IN} = 3.6 V, V_{SW3} = 1.5 V, I_{SW3} = 100 mA, typical external component values, f_{SW3} = 2.0 MHz. Typical values are characterized at V_{IN} = V_{SW3IN} = 3.6 V, V_{SW3} = 1.5 V, I_{SW3} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SW3						
V_{SW3IN}	Operating input voltage	2.8	–	4.5	V	(23)
V_{SW3}	Nominal output voltage	–	Table 44	–	V	
V_{SW3ACC}	Output voltage accuracy • PWM, APS, 2.8 V < V_{SW3IN} < 4.5 V, 0 < I_{SW3} < 1.5 A, 0.9 V < V_{SW3} < 1.65 V • PFM, steady state (2.8 V < V_{SW3IN} < 4.5 V, 0 < I_{SW3} < 50 mA), 0.9 V < V_{SW3} < 1.65 V	-3.0 -6.0	– –	3.0 6.0	%	
I_{SW3}	Rated output load current, 2.8 V < V_{SW3IN} < 4.5 V, 0.9 V < V_{SW3} < 1.65 V, PWM, APS mode	–	–	1500	mA	(24)
I_{SW3Q}	Quiescent current • PFM mode • APS mode	– –	50 150	– –	µA	
I_{SW3LIM}	Current limiter peak current detection, current through inductor • SW3ILIM = 0 (default) • SW3ILIM = 1	1.95 1.45	3.0 2.25	4.05 3.05	A	
ΔV_{SW3}	Output ripple	–	5.0	–	mV	
R_{ONSW3P}	SW3 P-MOSFET $R_{DS(on)}$ at V_{IN} = V_{SW3IN} = 3.3 V	–	205	235	mΩ	
R_{ONSW3N}	SW3 N-MOSFET $R_{DS(on)}$ at V_{IN} = V_{SW3IN} = 3.3 V	–	250	315	mΩ	
I_{SW3PQ}	SW3 P-MOSFET leakage current, V_{IN} = V_{SW3IN} = 4.5 V	–	–	12	µA	
I_{SW3NQ}	SW3 N-MOSFET leakage current, V_{IN} = V_{SW3IN} = 4.5 V	–	–	4.0	µA	
R_{SW3DIS}	Discharge resistance during off mode	–	600	–	Ω	

Notes

23. The maximum operating input voltage is 4.55 V when VPWR LDO is used.
24. The higher output voltages available depend on the voltage drop in the conduction path as given by the following equation: (V_{SW3IN} - V_{SW3}) = I_{SW3}* (DCR of Inductor +R_{ONSW3P} + PCB trace resistance).

Table 12. Dynamic Electrical Characteristics - SW3

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = $V_{SW\ 3IN}$ = 3.6 V, V_{SW3} = 1.5 V, I_{SW3} = 100 mA, typical external component values, f_{SW3} = 2.0 MHz. Typical values are characterized at V_{IN} = V_{SW3IN} = 3.6 V, V_{SW3} = 1.5 V, I_{SW3} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V_{SW3OSH}	Start-up overshoot, I_{SW3} = 0.0 mA, slew rate = 25 mV/4 µs, V_{IN} = V_{SW3IN} = 4.5 V	–	–	66	mV	
t_{ONSW3}	Turn-on time, enable to 90% of end value, I_{SW3} = 0 mA, slew rate = 25 mV/4 µs, V_{IN} = V_{SW3IN} = 4.5 V	–	–	500	µs	

Table 13. Static electrical characteristics - VSNVS

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{SNVS} = 3.0 V, I_{SNVS} = 5.0 µA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{SNVS} = 3.0 V, I_{SNVS} = 5.0 µA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VSNVS						
V_{IN}	Operating input voltage • Valid coin cell range • Valid V_{IN}	 1.8 2.25	 – –	 3.3 4.5	V	(25)
I_{SNVS}	Operating load current, $V_{INMIN} < V_{IN} < V_{INMAX}$	1.0	–	1000	µA	
V_{SNVS}	Output voltage • 5.0 µA < I_{SNVS} < 1000 µA (OFF), 3.20 V < V_{IN} < 4.5 V • 5.0 µA < I_{SNVS} < 1000 µA (ON), 3.20 V < V_{IN} < 4.5 V • 5.0 µA < I_{SNVS} < 1000 µA (coin cell mode), 2.84 V < V_{COIN} < 3.3 V	 -5.0 -5.0 V_{COIN}-0.10	 3.0 3.0 –	 7.0 5.0 V_{COIN}	 % % V	
$V_{SNVSDROP}$	Dropout voltage, 2.85 V < V_{IN} < 2.9 V, 1.0 µA < I_{SNVS} < 1000 µA	–	–	110	mV	
$I_{SNVSLIM}$	Current limit, $V_{IN} > V_{TH1}$	1100	–	6750	µA	
VSNVS DC, switch						
V_{LICELL}	Operating input voltage, valid coin cell range	1.8	–	3.3	V	
I_{SNVS}	Operating load current	1.0	–	1000	µA	
$R_{DSONSNVS}$	Internal switch $R_{DS(on)}$, V_{COIN} = 2.6 V	–	–	100	Ω	

Notes

25. The maximum operating input voltage is 4.55 V when VPWR LDO is used

Table 14. Dynamic electrical characteristics - VSNVS

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{SNVS} = 3.0 V, I_{SNVS} = 5.0 µA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{SNVS} = 3.0 V, I_{SNVS} = 5.0 µA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VSNVS						
$V_{SNVSTON}$	Turn-on time (load capacitor, 0.47 µF), from $V_{IN} = V_{TH1}$ to 90% of V_{SNVS}, V_{COIN} = 0.0 V, I_{SNVS} = 5.0 µA	–	–	24	ms	(26),(27)
$V_{SNVSOSH}$	Start-up overshoot, I_{SNVS} = 5.0 µA	–	40	70	mV	
$V_{SNVSLOTR}$	Transient load response, 3.2 < $V_{IN} \leq$ 4.5 V, I_{SNVS} = 100 to 1000 µA	2.8	–	–	V	
V_{TL1}	V_{IN} falling threshold (V_{IN} powered to coin cell powered)	2.45	2.70	3.05	V	
V_{TH1}	V_{IN} rising threshold (coin cell powered to V_{IN} powered)	2.50	2.75	3.10	V	
V_{HYST1}	V_{IN} threshold hysteresis for V_{TH1}-V_{TL1}	5.0	–	–	mV	
$V_{SNVSCROSS}$	Output voltage during crossover, V_{COIN} > 2.9 V, switch to LDO: $V_{IN} > V_{TH1}$, I_{SNVS} = 100 µA, LDO to switch: $V_{IN} < V_{TL1}$, I_{SNVS} = 100 µA	2.45	–	–	V	

Notes

26. The start-up of V_{SNVS} is not monotonic. It first rises to 1.0 V and then settles to 3.0 V.
27. From coin cell insertion to V_{SNVS} = 1.0 V, the delay time is typically 400 ms.

Table 15. Static electrical characteristics - VLDO1

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{LDO1IN} = 3.6 V, V_{LDO1} = 3.3 V, I_{LDO1} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{LDO1IN} = 3.6 V, V_{LDO1} = 3.3 V, I_{LDO1} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO1 linear regulator						
V_{LDO1IN}	Operating input voltage • 1.8 V ≤ $V_{LDO1NOM}$ ≤ 2.5 V • 2.6 V ≤ $V_{LDO1NOM}$ ≤ 3.3 V	2.8 $V_{LDO1NOM}$ +0.250	– –	4.5 4.5	V	(28), (29)
$V_{LDO1NOM}$	Nominal output voltage	–	Table 47	–	V	
I_{LDO1}	Operating load current	0.0	–	100	mA	
$V_{LDO1TOL}$	Output voltage tolerance, $V_{LDO1INMIN}$ < V_{LDO1IN} < 4.5 V, 0.0 mA < I_{LDO1} < 100 mA, VLDO1 = 1.8 V to 3.3 V	-3.0	–	3.0	%	
I_{LDO1Q}	Quiescent current, no load, change in $I_{VIN,}$ when VLDO1 enabled	–	13	–	µA	
$I_{LDO1LIM}$	Current limit, I_{LDO1} when V_{LDO1} is forced to $V_{LDO1NOM}$/2	122	167	280	mA	

Notes

28. The maximum operating input voltage is 4.55 V when VPWR LDO is used.
29. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any PF3001 regulator, or external system supply.

Table 16. Dynamic electrical characteristics - VLDO1

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{LDO1IN} = 3.6 V, V_{LDO1} = 3.3 V, I_{LDO1} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{LDO1IN} = 3.6 V, V_{LDO1} = 3.3 V, I_{LDO1} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO1 linear regulator						
$PSRR_{VLDO1}$	PSRR, I_{LDO1} = 75 mA, 20 Hz to 20 kHz • VLDO1 = 1.8 V to 3.3 V, V_{LDO1IN} = $V_{LDO1INMIN}$ + 100 mV • VLDO1 = 1.8 V to 3.3 V, V_{LDO1IN} = $V_{LDO1NOM}$ + 1.0 V	35 52	40 60	– –	dB	
$NOISE_{VLDO1}$	Output noise density, V_{LDO1IN} = $V_{LDO1INMIN}$, I_{LDO1} = 75 mA • 100 Hz to <1.0 kHz • 1.0 kHz to <10 kHz • 10 kHz to 1.0 MHz	– – –	-114 -129 -135	-102 -123 -130	dBV/ √Hz	
t_{ONLDO1}	Turn-on time, enable to 90% of end value, V_{LDO1IN} = $V_{LDO1INMIN}$ to 4.5 V, I_{LDO1} = 0.0 mA, all output voltage settings	60	–	500	µs	
$t_{OFFLDO1}$	Turn-off time, disable to 10% of initial value, V_{LDO1IN} = $V_{LDO1INMIN}$, I_{LDO1} = 0.0 mA	–	–	10	ms	
$LDO1_{OSHT}$	Start-up overshoot, V_{LDO1IN} = $V_{LDO1INMIN}$ to 4.5 V, I_{LDO1} = 0.0 mA	–	1.0	2.0	%	

Table 17. Static electrical characteristics - VLDO2

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{LDO2IN} = 3.0 V, V_{LDO2} = 1.55 V, I_{LDO2} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{LDO2IN} = 3.0 V, V_{LDO2} = 1.55 V, I_{LDO2} = 10 mA and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO2 linear regulator						
V_{LDO2IN}	Operating input voltage	1.75	–	3.40	V	
$V_{LDO2NOM}$	Nominal output voltage	–	Table 47	–	V	
I_{LDO2}	Operating load current	0.0	–	250	mA	
$V_{LDO2TOL}$	Output voltage tolerance, 1.75 V < V_{LDOIN1} < 3.40 V, 0.0 mA < I_{LDO2} < 250 mA, VLDO2 = 0.8 V to 1.55 V	-3.0	–	3.0	%	
I_{LDO2Q}	Quiescent current, no load, change in I_{VIN} and $I_{VLDO2IN}$, When V_{LDO2} enabled	–	16	–	µA	
$I_{LDO2LIM}$	Current limit, I_{LDO2} when V_{LDO2} is forced to $V_{LDO2NOM}$/2	333	417	612	mA	

Table 18. Dynamic electrical characteristics - VLDO2

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{LDO2IN} = 3.0 V, V_{LDO2} = 1.55 V, I_{LDO2} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{LDO2IN} = 3.0 V, V_{LDO2} = 1.55 V, I_{LDO2} = 10 mA and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO2 linear regulator						
$PSRR_{VLDO2}$	PSRR, I_{LDO2} = 187.5 mA, 20 Hz to 20 kHz • VLDO2 = 0.8 V to 1.55 V • VLDO2 = 1.1 V to 1.55 V	 50 37	 60 45	 – –	dB	
$NOISE_{VLDO2}$	Output noise density, V_{LDO2IN} = 1.75 V, I_{LDO2} = 187.5 mA • 100 Hz to <1.0 kHz • 1.0 kHz to <10 kHz • 10 kHz to 1.0 MHz	 – – –	 -108 -118 -124	 -100 -108 -112	dBV/√Hz	
t_{ONLDO2}	Turn-on time, enable to 90% of end value, V_{LDO2IN} = 1.75 V to 3.4 V, I_{LDO2} = 0.0 mA	60	–	500	µs	
$t_{OFFLDO2}$	Turn-off time, disable to 10% of initial value, V_{LDO2IN} = 1.75 V, I_{LDO2} = 0.0 mA	–	–	10	ms	
$LDO2_{OSHT}$	Start-up overshoot, V_{LDO2IN} = 1.75 V to 3.4 V, I_{LDO2} = 0.0 mA	–	1.0	2.0	%	

Table 19. Static electrical characteristics – VCC_SD

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{CC_SD} = 1.85 V, I_{VCC_SD} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{CC_SD} = 1.85 V, I_{VCC_SD} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VCC_SD linear regulator						
V_{IN}	Operating input voltage	2.8	–	4.5	V	(30), (31), (32)
V_{CC_SDNOM}	Nominal output voltage	–	Table 50	–	V	
I_{VCC_SD}	Operating load current	0.0	–	100	mA	
V_{CC_SDTOL}	Output voltage accuracy, 2.8 V < V_{IN} < 4.5 V, 0.0 mA < I_{VCC_SD} < 100 mA, VCC_SD[1:0] = 00 to 11	-3.0	–	3.0	%	
I_{VCC_SDQ}	Quiescent current, no load, change in I_{VIN} and I_{VIN2}, when V_{CC_SD} enabled	–	13	–	µA	
I_{VCC_SDLIM}	Current limit, I_{VCC_SD} when V_{CC_SD} is forced to V_{CC_SDNOM}/2	122	167	280	mA	

Notes

30. When the LDO output voltage is set above 2.6 V, the minimum allowed input voltage needs to be at least the output voltage plus 0.25 V.
31. The maximum operating input voltage is 4.55 V when VPWR LDO is used.
32. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any PF3001 regulator, or external system supply.

Table 20. Dynamic electrical characteristics - VCC_SD

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{CC_SD} = 1.85 V, I_{VCC_SD} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{CC_SD} = 1.85 V, I_{VCC_SD} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VCC_SD linear regulator						
$PSRR_{VCC_SD}$	PSRR, I_{VCC_SD} = 75 mA, 20 Hz to 20 kHz • VCC_SD[1:0] = 00 - 10, V_{IN} = 2.8 V + 100 mV • VCC_SD[1:0] = 10 - 11, V_{IN} = V_{CC_SDNOM} + 1.0 V	 35 52	 40 60	 – –	dB	
$NOISE_{VCC_SD}$	Output noise density, V_{IN} = 2.8V, I_{VCC_SD} = 75 mA • 100 Hz to <1.0 kHz • 1.0 kHz to <10 kHz • 10 kHz to 1.0 MHz	 – – –	 -114 -129 -135	 -102 -123 -130	dBV/√Hz	
t_{ONVCC_SD}	Turn-on time, enable to 90% of end value, V_{IN} = 2.8 V to 4.5 V, I_{VCC_SD} = 0.0 mA	60	–	500	µs	
t_{OFFVCC_SD}	Turn-off time, disable to 10% of initial value, V_{IN} = 2.8 V, I_{VCC_SD} = 0.0 mA	–	–	10	ms	
VCC_SD_{OSHT}	Start-up overshoot, V_{IN} = 2.8 V to 4.5 V, I_{VCC_SD} = 0.0 mA	–	1.0	2.0	%	

Table 21. Static electrical characteristics – V33

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{33} = 3.3 V, I_{V33} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{33} = 3.3 V, I_{V33} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V33 linear regulator						
V_{IN}	Operating input voltage, 2.9 V ≤ V_{33NOM} ≤ 3.6 V	2.8	–	4.5	V	(33), (34), (35)
V_{33NOM}	Nominal output voltage	–	Table 49	–	V	
I_{V33}	Operating load current	0.0	–	350	mA	
V_{33TOL}	Output voltage tolerance, 2.8 V < V_{IN} < 4.5 V, 0.0 mA < I_{V33} < 350 mA, V_{33}[1:0] = 00 to 11	-3.0	–	3.0	%	
I_{V33Q}	Quiescent current, no load, change in I_{VIN}, when V_{33} enabled	–	13	–	µA	
I_{V33LIM}	Current limit, I_{V33} when V_{33} is forced to V_{33NOM}/2	435	584.5	950	mA	

Notes

33. When the LDO Output voltage is set above 2.6 V the minimum allowed input voltage need to be at least the output voltage plus 0.25 V for proper regulation due to the dropout voltage generated through the internal LDO transistor.
34. The maximum operating input voltage is 4.55 V when VPWR LDO is used.
35. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any PF3001 regulator, or external system supply.

Table 22. Dynamic electrical characteristics – V33

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{33} = 3.3 V, I_{V33} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{33} = 3.3 V, I_{V33} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V33 linear regulator						
$PSRR_{V33}$	PSRR, I_{V33} = 262.5 mA, 20 Hz to 20 kHz, V_{33}[1:0] = 00 - 11, V_{IN} = V_{33NOM} + 1.0 V	52	60	–	dB	(36)
$NOISE_{V33}$	Output noise density, V_{IN} = 2.8 V, I_{V33} = 262.5 mA • 100 Hz to <1.0 kHz • 1.0 kHz to <10 kHz • 10 kHz to 1.0 MHz	 – – –	 -114 -129 -135	 -102 -123 -130	dBV/√Hz	
t_{ONV33}	Turn-on time, enable to 90% of end value, V_{IN} = 2.8 V, to 4.5 V, I_{V33} = 0.0 mA	60	–	500	µs	
t_{OFFV33}	Turn-off time, disable to 10% of initial value, V_{IN} = 2.8 V, I_{V33} = 0.0 mA	–	–	10	ms	
V_{33OSHT}	Start-up overshoot, V_{IN} = 2.8 V to 4.5 V, I_{V33} = 0.0 mA	–	1.0	2.0	%	

Notes

36. When the LDO Output voltage is set above 2.6 V the minimum allowed input voltage need to be at least the output voltage plus 0.25 V for proper regulation due to the dropout voltage generated through the internal LDO transistor.

Table 23. Static electrical characteristics – VLDO3

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, $V_{LDO34IN}$ = 3.6 V, V_{LDO3} = 3.3 V, I_{LDO3} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, $V_{LDO34IN}$ = 3.6 V, V_{LDO3} = 3.3 V, I_{LDO3} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO3 linear regulator						
$V_{LDO34IN}$	Operating input voltage • 1.8 V ≤ $V_{LDO3NOM}$ ≤ 2.5 V • 2.6 V ≤ $V_{LDO3NOM}$ ≤ 3.3 V	2.8 $V_{LDO3NOM}$ +0.250	– –	3.6 3.6	V	(37)
$V_{LDO3NOM}$	Nominal output voltage	–	Table 48	–	V	
I_{LDO3}	Operating load current	0.0	–	100	mA	
$V_{LDO3TOL}$	Output voltage tolerance, $V_{LDO34INMIN}$ < $V_{LDO34IN}$ < 4.5 V, 0.0 mA < I_{LDO3} < 100 mA, VLDO3 = 1.8 V to 3.3 V	-3.0	–	3.0	%	
I_{LDO3Q}	Quiescent current, no load, change in I_{VIN} and $I_{VLDO34IN}$, When V_{LDO3} enabled	–	13	–	µA	
$I_{LDO3LIM}$	Current limit, I_{LDO3} when V_{LDO3} is forced to $V_{LDO3NOM}$/2	122	167	280	mA	

Notes

37. Beyond VLDO34IN rating, the ESD protection can be sensitive to voltage transients.

Table 24. Dynamic electrical characteristics – VLDO3

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, $V_{LDO34IN}$ = 3.6 V, V_{LDO3} = 3.3 V, I_{LDO3} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, $V_{LDO34IN}$ = 3.6 V, V_{LDO3} = 3.3 V, I_{LDO3} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO3 linear regulator						
$PSRR_{VLDO3}$	PSRR, I_{LDO3} = 75 mA, 20 Hz to 20 kHz • VLDO3 = 1.8 V to 3.3 V, $V_{LDO34IN}$ = $V_{LDO34INMIN}$ + 100 mV • VLDO3 = 1.8 V to 3.3 V, $V_{LDO34IN}$ = $V_{LDO3NOM}$ + 1.0 V	35 52	40 60	– –	dB	
$NOISE_{VLDO3}$	Output noise density, $V_{LDO34IN}$ = $V_{LDO34INMIN}$, I_{LDO3} = 75 mA • 100 Hz to <1.0 kHz • 1.0 kHz to <10 kHz • 10 kHz to 1.0 MHz	– – –	-114 -129 -135	-102 -123 -130	dBV/√Hz	
t_{ONLDO3}	Turn-on time, enable to 90% of end value, $V_{LDO34IN}$ = $V_{LDO34INMIN}$ to 4.5 V, I_{LDO3} = 0.0 mA	60	–	500	µs	
$t_{OFFLDO3}$	Turn-off time, disable to 10% of initial value, $V_{LDO34IN}$ = $V_{LDO34INMIN}$, I_{LDO3} = 0.0 mA	–	–	10	ms	
$LDO3_{OSHT}$	Start-up overshoot, $V_{LDO34IN}$ = $V_{LDO34IN2MIN}$ to 4.5 V, I_{LDO3} = 0.0 mA	–	1.0	2.0	%	

Table 25. Static electrical characteristics - VLDO4

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, $V_{LDO34IN}$ = 3.6 V, V_{LDO4} = 3.3 V, I_{LDO4} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, $V_{LDO34IN}$ = 3.6 V, V_{LDO4} = 3.3 V, I_{LDO4} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO4 linear regulator						
$V_{LDO34IN}$	Operating input voltage • 1.8 V ≤ $V_{LDO4NOM}$ ≤ 2.5 V • 2.6 V ≤ $V_{LDO4NOM}$ ≤ 3.3 V	2.8 $V_{LDO4NOM}$ +0.250	– –	3.6 3.6	V	(38)
$V_{LDO4NOM}$	Nominal output voltage	–	Table 48	–	V	
I_{LDO4}	Operating load current	0.0	–	350	mA	
$V_{LDO4TOL}$	Output voltage tolerance, $V_{LDO34INMIN}$ < $V_{LDO34IN}$ < 4.5 V, 0.0 mA < I_{LDO3} < 100 mA, VLDO4 = 1.9 V to 3.3 V	-3.0	–	3.0	%	
I_{LDO4Q}	Quiescent current, no load, change in I_{VIN} and $I_{VLDO34IN}$, When V_{LDO4} enabled	–	13	–	µA	
$I_{LDO4LIM}$	Current limit, I_{LDO4} when V_{LDO4} is forced to $V_{LDO4NOM}$/2	435	584.5	950	mA	
$PSRR_{VLDO4}$	PSRR, I_{LDO4} = 262.5 mA, 20 Hz to 20 kHz • VLDO4 = 1.9 V to 3.3 V, $V_{LDO34IN}$ = $V_{LDO34INMIN}$ + 100 mV • VLDO4 = 1.9 V to 3.3 V, $V_{LDO34IN}$ = $V_{LDO4NOM}$ + 1.0 V	35 52	40 60	– –	dB	

Notes

38. Beyond VLDO34IN rating, the ESD protection can be sensitive to voltage transients.

Table 26. Dynamic electrical characteristics - VLDO4

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, $V_{LDO34IN}$ = 3.6 V, V_{LDO4} = 3.3 V, I_{LDO4} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, $V_{LDO34IN}$ = 3.6 V, V_{LDO4} = 3.3 V, I_{LDO4} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO4 linear regulator						
$NOISE_{VLDO4}$	Output noise density, $V_{LDO34IN2}$ = $V_{LDO34INMIN}$, I_{LDO4} = 262.5 mA • 100 Hz to <1.0 kHz • 1.0 kHz to <10 kHz • 10 kHz to 1.0 MHz	– – –	-114 -129 -135	-102 -123 -130	dBV/√Hz	
t_{ONLDO4}	Turn-on time, enable to 90% of end value, $V_{LDO34IN}$ = $V_{LDO34INMIN}$, 4.5 V, I_{LDO4} = 0.0 mA	60	–	500	µs	
$t_{OFFLDO4}$	Turn-off time, disable to 10% of initial value, $V_{LDO34IN}$ = $V_{LDO34INMIN}$, I_{LDO4} = 0.0 mA	–	–	10	ms	
$LDO4_{OSHT}$	Start-up overshoot, $V_{LDO34IN}$ = $V_{LDO34INMIN}$, 4.5 V, I_{LDO4} = 0.0 mA	–	1.0	2.0	%	

Table 27. Static electrical characteristics - Coin Cell

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, typical external component values, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Coin cell						
$V_{COINACC}$	Charge voltage accuracy	-100	–	-100	mV	
$I_{COINACC}$	Charge current accuracy	-30	–	30	%	
I_{COIN}	Coin cell charge current • I_{COINHI} (in On mode) • I_{COINLO} (in On mode)	– –	60 10	– –	µA	

Table 28. Static electrical characteristics - Digital I/O

All parameters are specified at T_A = -40 °C to 105 °C, V_{DDIO} = 1.7 V to 3.6 V, V_{PWR} = 0 V (external FET not populated), and typical external component values and full load current range, unless otherwise noted.

Pin Name	Parameter	Load condition	Min.	Max.	Unit	Notes
PWRON	• V_L • V_H	– –	0.0 0.8 * V_{SNVS}	0.2 * V_{SNVS} 3.6	V	
RESETBMCU	• V_{OL} • V_{OH}	-2.0 mA Open Drain	0.0 0.7 * V_{DDIO}	0.4 * V_{DDIO} V_{DDIO}	V	
SCL	• V_L • V_H	– –	0.0 0.8 * V_{DDIO}	0.2 * V_{DDIO} 3.6	V	
SDA	• V_L • V_H • V_{OL} • V_{OH}	– – -2.0 mA Open Drain	0.0 0.8 * V_{DDIO} 0.0 0.7 * V_{DDIO}	0.2 * V_{DDIO} 3.6 0.4 * V_{DDIO} V_{DDIO}	V	
INTB	• V_{OL} • V_{OH}	-2.0 mA Open Drain	0.0 0.7 * V_{DDIO}	0.4 * V_{DDIO} V_{DDIO}	V	
SD_VSEL	• V_L • V_H	– –	0.0 0.8 * V_{DDIO}	0.2 * V_{DDIO} 3.6	V	

Table 29. Static electrical characteristics - Internal Supplies

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 2.8 V to 4.5 V, LICELL = 1.8 V to 3.3 V, and typical external component values. Typical values are characterized at V_{IN} = 3.6 V, LICELL = 3.0 V, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VCOREDIG (digital core supply)						
$V_{COREDIG}$	Output voltage • ON mode • Coin cell mode and OFF mode	– –	1.5 1.3	– –	V	(39)
VCORE (analog core supply)						
V_{CORE}	Output voltage • ON mode and charging • Coin cell mode and OFF mode	– –	2.775 0.0	– –	V	(39)
VCOREREF (bandgap regulator reference)						
$V_{COREREF}$	Output voltage at 25 °C	–	1.2	–	V	(39)
$V_{COREREFACC}$	Absolute trim accuracy	–	0.5	–	%	
$V_{COREREFTACC}$	Temperature drift	–	0.25	–	%	

Notes

39. 3.1 V < V_{IN} < 4.5 V, no external loading on VCOREDIG, VCORE, or VCOREREF.

Table 30. Static electrical characteristics - UVDET threshold

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 2.8 V to 4.5 V, LICELL = 1.8 V to 3.3 V, and typical external component values. Typical values are characterized at V_{IN} = 3.6 V, LICELL = 3.0 V, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V_{IN} UVDET threshold						
V_{UVDET}	• Rising • Falling	– 2.5	– –	3.1 –	V	

6 Functional description and application information

6.1 Introduction

The PF3001 is a highly integrated, low quiescent current power management IC featuring three buck regulators and seven LDO regulators. The PF3001 provides all the necessary rails to power a complete system including the application processor, memory, and peripherals. The PF3001 operates from an input voltage of up to 5.5 V. Output voltage, start-up sequence, and other functions are set in integrated one-time-programmable (OTP) memory.

6.2 Power generation

The buck regulators in the PF3001 provide supply to the processor cores and to other voltage domains, such as I/O and memory. Dynamic voltage scaling is provided to allow controlled supply rail adjustments for the processor cores and other circuitry.

The linear regulators in the PF3001 can be used as general purpose regulators to power peripherals and lower power processor rails. The VCC_SD LDO regulator supports the dual voltage requirement by high speed SD card readers. Depending on the system power path configuration, the LDO regulators can be directly supplied from the main input supply or from the switching regulators to power peripherals, such as audio, camera, Bluetooth, and Wireless LAN, etc.

The VSNVS block behaves as an LDO, or as a bypass switch to supply the SNVS/SRTC circuitry on the i.MX processors; V_{SNVS} may be powered from V_{IN}, or from a coin cell.

To accommodate applications powered by main supplies of voltages higher than 4.5 V and up to 5.5 V, the PF3001 incorporates a front-end LDO regulator using an external pass FET to keep the maximum regulator input voltage of the regulators at 4.5 V. Applications with an input voltage lower than 4.5 V can directly power the regulators without using the front-end LDO.

Table 31 shows a summary of the voltage regulators in the PF3001.

Table 31. PF3001 power tree

Supply	Output voltage (V)	Programming step size (mV)	Maximum load current (mA)
SW1	0.7 to 1.425 1.8 and 3.3	25 (N/A)	2750
SW2	1.5 to 1.85 2.5 to 3.3	50 variable	1250
SW3	0.9 to 1.65	50	1500
VLDO1	1.8 to 3.3	50	100
VLDO2	0.8 to 1.55	50	250
VCC_SD	2.85 to 3.3 1.8 to 1.85	150 50	100
V33	2.85 to 3.3	150	350
VLDO3	1.8 to 3.3	100	100
VLDO4	1.8 to 3.3	100	350
VSNVS	3.0	NA	1.0

Figure 5. PF3001 typical power map

Figure 5 shows a simplified power map with various recommended options to supply the different block within the PF3001, as well as the typical application voltage domain on the i.MX Series processors. Note that each application power tree is dependent upon the system's voltage and current requirements, therefore a proper input voltage should be selected for the regulators.

6.3 Functional description

6.3.1 Control logic and interface signals

The PF3001 is fully programmable via the I^2C interface. Additional communication is provided by direct logic interfacing including INTB, RESETBMCU, PWRON, and SD_VSEL. Refer to Table 28 for logic levels for these pins.

6.3.1.1 PWRON

PWRON is an input signal to the IC which generates a turn-on event. A turn-on event brings the PF3001 out of OFF mode and into the ON mode. Refer to Modes of operation for the various modes (states) of operation of the IC. If the PWRON signal is high and $V_{IN} > U_{VDET}$, the PMIC turns on; the interrupt and sense bits, PWRONI and PWRONS respectively, are set.

6.3.1.2 RESETBMCU

RESETBMCU is an open-drain, active low output. It is de-asserted 2.0 ms after the last regulator in the start-up sequence is enabled. This signal can be used to bring the processor out of reset (POR), or as an indicator which all supplies have been enabled; it is only asserted during a turn-off event. The RESETBMCU signal is internal timer based and does not monitor the regulators.

6.3.1.3 INTB

INTB is an open drain, active low output. It is asserted when any fault occurs, provided the fault interrupt is unmasked. INTB is de-asserted after the fault interrupt is cleared by software, which requires writing a “1” to the fault interrupt bit.

6.3.1.4 SD_VSEL

SD_VSEL is an input pin which sets the output voltage range of the VCC_SD regulator. When SD_VSEL = HIGH, the VCC_SD regulator operates in the lower output voltage range. When SD_VSEL = LOW, the VCC_SD regulator operates in the higher output voltage range. The SD_VSEL input buffer is powered by the VDDIO supply. When a valid VDDIO voltage is not present, the output of the SD_VSEL buffer defaults to a logic high thus keeping the VCC_SD regulator output in the lower voltage range.

6.3.2 Start-up

The PF3001 is available in a number of pre-programmed fixed start-up sequences to suit a wide variety of system configurations. Refer to Table 32 for programming details of the different values.

Table 32. Start-up configuration [40]

Registers	Pre-programmed OTP configuration						
	A1	A2	A3	A4	A5	A6	A7
Default I^2C Address	0x08	0x08	0x08	0x08	0x08	0x08	0x08
VSNVS_VOLT	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V
SW1_VOLT	1.10 V	1.10 V	1.375 V	1.375 V	1.375 V	1.4 V	1.4 V
SW1_SEQ	1	1	2	1	1	3	3
SW2_VOLT	1.8 V	1.8 V	3.3 V	3.3 V	3.15 V	3.3 V	3.3 V
SW2_SEQ	2	2	4	2	2	3	3
SW3_VOLT	1.35 V	1.2 V	1.35 V	1.5 V	1.2 V	1.2 V	1.35 V
SW3_SEQ	5	5	3	3	4	3	3
VLDO1_VOLT	1.8 V	1.8 V	3.3 V	1.8 V	1.8 V	3.3 V	3.3 V
VLDO1_SEQ	4	4	OFF	OFF	3	3	3
VLDO2_VOLT	1.5 V	1.5 V	1.5 V	1.2 V	1.5 V	1.5 V	1.5 V
VLDO2_SEQ	4	4	OFF	3	OFF	OFF	OFF
VLDO3_VOLT	3.3 V	3.3 V	2.5 V	1.8 V	3.1 V	1.8 V	1.8 V
VLDO3_SEQ	3	3	OFF	OFF	2	3	OFF
VLDO4_VOLT	3.3 V	3.3 V	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V
VLDO4_SEQ	3	3	4	3	3	3	3
V33_VOLT	3.3 V	3.3 V	3.0 V	3.3 V	2.85 V	3.3 V	3.3 V
V33_SEQ	3	3	1	2	OFF	2	2
VCC_SD_VOLT	3.3 V/1.85 V	3.3 V/1.85 V	3.3 V/1.85 V	3.0 V/1.80 V	3.15 V/1.80 V	3.3 V/1.85 V	3.3 V/1.85 V
VCC_SD_SEQ	4	4	5	3	2	3	3
PU CONFIG, SEQ_CLK_SPEED	2000 µs	2000 µs	500 µs	2000 µs	2000 µs	2000 µs	2000 µs
PU CONFIG, SWDVS_CLK	12.5 mV/µs	12.5 mV/µs	6.25 mV/µs	12.5 mV/µs	12.5 mV/µs	6.25 mV/µs	6.25 mV/µs
PU CONFIG, PWRON	Level sensitive	Level sensitive	Level sensitive	Level sensitive	Level sensitive	Level sensitive	Level sensitive
SW1_FREQ	2.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz
SW2_FREQ	2.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz
SW3_FREQ	2.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz

Notes

40. This table specifies the default output voltage of the LDOs and SWx after start-up and/or when the LDOs and SWx are enabled. The VCC_SD voltage depends on the state of the SD_VSEL pin.

6.3.3 Start-up timing diagram

Figure 6 shows the start-up timing of the regulators as determined by their OTP sequence. The trimmed 32 kHz clock controls all the start-up timing.

Figure 6. Start-up timing diagram

6.3.4 16 MHz and 32 kHz clocks

The PF3001 incorporates two clocks: a trimmed 16 MHz RC oscillator and an untrimmed 32 kHz RC oscillator. The 32 kHz untrimmed clock is only used in the following conditions:

- V_{IN} < UVDET
- All regulators are in PFM switching mode

A 32 kHz clock, derived from the 16 MHz trimmed clock, is used when accurate timing is needed under the following conditions:

- During start-up, V_{IN} > UVDET

When the 16 MHz is active in the ON mode, the debounce times are referenced to the 32 kHz derived from the 16 MHz clock. The exceptions are the LOWVINI and PWRONI interrupts, which are referenced to the 32 kHz untrimmed clock. Switching frequency of the switching regulators is derived from the trimmed 16 MHz clock.

The 16 MHz clock and hence the switching frequency of the regulators, can be adjusted to improve the noise integrity of the system. By changing the factory trim values of the 16 MHz clock, the user may add an offset as small as ±3.0% of the nominal frequency. Contact your NXP representative for detailed information on this feature.

6.3.5 Optional front-end input LDO regulator

6.3.5.1 LDO regulator description

This section describes the optional front-end LDO regulator provided by the PF3001 in order to facilitate the operation with supply voltages higher than 4.5 V and up to 5.5 V.

For non-battery operated applications, when the input supply voltage exceeds 4.5 V, the front-end LDO can be activated by populating the external PMOS pass FET MP1 in Figure 7 and connecting the VPWR pin to the main supply. Under this condition, the LDO control block self-starts with a local bandgap reference. When the VIN pin reaches UVDET rising threshold, the reference is switched to the main trimmed bandgap reference to maintain the required VIN accuracy. In applications using an input supply voltage of 4.5 V or lower, the PMOS pass FET should not be populated, the VPWR pin should be grounded externally, and the VIN pin should be used instead as the main supply input pin. The input pins of the switching regulators should always be connected to the VIN net.

The main components of the LDO regulator are an external power P-channel MOSFET and an internal differential error amplifier. One input of the amplifier monitors a fraction of the output voltage at VIN determined by the resistor ratio of R1 and R2 as shown in Figure 7. The second input to the differential amplifier is from a stable bandgap voltage reference. If the output voltage rises too high relative to the reference voltage, the gate voltage of the power FET is changed to maintain a constant output voltage.

Figure 7. Front-end LDO block diagram

6.3.5.2 Undervoltage/short-circuit and overvoltage detection

Short-circuit to GND at VIN is detected using an under voltage monitor at VIN which senses excessive droop on the VIN line and consequently turns off (disable) the external PMOS pass FET. Overvoltage at VPWR is detected if VPWR exceeds the V_{PWROV} threshold (typically 6.0 V). Upon the detection of an overvoltage event an interrupt is generated and bit 2 is set in INTSTAT3 register. The INTB pin is pulled low if the VPWROVM mask bit is cleared. The interrupt is filtered using a 122 µs debouncing circuit. The VPWROV interrupt is not asserted if the overvoltage event occurs during start up. The VPWROVS bit can be read using I^2C to detect an overvoltage condition.

6.3.5.3 External components

Table 33 lists the typical component values for the general purpose LDO regulators.

Table 33. Input LDO external components

Component	Value
Minimum output capacitor on VIN rail	100 µF [41]
MP1	Fairchild FDMA908PZ, Vishay SiA447DJ, or comparable

Notes

41. Use X5R/X7R ceramic capacitors with a voltage rating at least two times the nominal voltage. The 100 µF capacitance is the total capacitance on the VIN rail including the capacitance at the various regulator inputs. For example, 2 x 22 µF capacitors can be used along with 10 µF capacitors at all the SWx and LDOx inputs to achieve a total of 100 µF capacitance.

6.3.6 Internal core voltages

All regulators use the main bandgap as the reference. The main bandgap is bypassed with a capacitor at VCOREREF. VCOREDIG is a 1.5 V regulator powering all the digital logic in the PF3001. VCOREDIG is regulated at 1.28 V in off and coin cell modes. The VCORE supply is used to bias internal analog rails. No external DC loading is allowed on VCORE, VCOREDIG, or VCOREREF. VCOREDIG is kept powered as long as there is a valid supply and/or valid coin cell.

6.3.7 Buck regulators

The PF3001 integrates three independent buck regulators: SW1, SW2, and SW3. Each regulator has associated registers controlling its output voltage during on mode. After boot up, contents of the SWxVOLT[4:0] register can be set through I^2C to set the output voltage during on mode.

Figure 8. Generic SWx block diagram

Table 34. SWx regulators external components

Components	Description	Values
CINSWx	SWx input capacitor	10 µF
CINSWxHF	SWx decoupling input capacitor	0.1 µF
COSWx	SWx output capacitor	2 x 22 µF (10 V or higher voltage rated capacitors) or 3 x 22 µF (6.3 V rated capacitors)
LSWx	SWx inductor	1.5 µH

Use X5R or X7R capacitors with voltage rating at least two times the nominal voltage.

6.3.7.1 Switching modes

The buck regulators can operate in different switching modes. Changing between switching modes can occur by I^2C programming. Available switching modes for buck regulators are presented in Table 35.

Table 35. Switching mode description

Mode	Description
OFF	The regulator is switched off and the output voltage is discharged using an internal resistor
PFM	In this mode, the regulator operates in forced PFM mode. The main error amplifier is turned off and a hysteretic comparator is used to regulate output voltage. Use this mode for load currents less than 50 mA.
PWM	In this mode, the regulator operates in forced PWM mode.
APS	In this mode, the regulator operates in pulse skipping mode at light loads and switches over to PWM modes for heavier load conditions. This is the default mode in which the regulators power up during a turn-on event.

During soft-start of the buck regulators, the controller transitions through the PFM, APS, and PWM switching modes. 3.0 ms after the output voltage reaches regulation, the controller transitions to the selected switching mode. Depending on the particular switching mode selected, additional ripple may be observed on the output voltage rail as the controller transitions between switching modes. The operating mode of the regulator in on mode is controlled using the SWxMODE[3:0] bits associated with each regulator. Table 36 summarizes the Buck regulator programmability for normal mode.

Table 36. Regulator mode control

SWxMODE[3:0]	Normal mode
0000	Off
0001	PWM
0011	PFM
1000 (default)	APS

6.3.7.2 Dynamic voltage scaling

To reduce overall power consumption, processor core voltages can be varied depending on the mode or activity level of the processor.

Normal operation: The output voltage is selected by I^2C bits SW1[4:0] for SW1 and SW2[2:0] for SW2, and SW3[3:0] for SW3. A voltage transition initiated by I^2C is governed by the DVS stepping rate which is 25 mV per step each 4.0 µs.

The regulators have a strong sourcing and sinking capability in PWM mode, therefore the fastest rising and falling slopes are determined by the regulator in PWM mode. However, if the regulators are programmed in PFM or APS mode during a DVS transition, the falling slope can be influenced by the load. Additionally, as the current capability in PFM mode is reduced, controlled DVS transitions in PFM mode could be affected. Critically timed DVS transitions are best assured with PWM mode operation.

Figure 9 shows the general behavior for the regulators when initiated with I^2C programming. During the DVS period the overcurrent condition on the regulator should be masked.

Figure 9. Voltage stepping with fixed DVS

6.3.7.3 Regulator phase clock

The SWxPHASE[1:0] bits select the phase of the regulator clock as shown in Table 37. By default, each regulator is initialized at 90 ° out of phase with respect to each other. For example, SW1 is set to 0 °, SW2 is set to 90 °, and SW3 is set to 180 ° by default at power up.

Table 37. Regulator phase clock selection

SWxPHASE[1:0]	Phase of clock sent to regulator (degrees)
00	0
01	90
10	180
11	270

The SWxFREQ[1:0] register is used to set the desired switching frequency for each one of the buck regulators. Table 39 shows the selectable options for SWxFREQ[1:0]. For each frequency, all phases are available, this allows regulators operating at different frequencies to have different relative switching phases. However, not all combinations are practical. For example, 2.0 MHz, 90 ° and 4.0 MHz, 180 ° are the same in terms of phasing. Table 38 shows the optimum phasing when using more than one switching frequency.

Table 38. Optimum phasing

Frequencies	Optimum phasing
1.0 MHz 2.0 MHz	0 ° 180 °
1.0 MHz 4.0 MHz	0 ° 180 °
2.0 MHz 4.0 MHz	0 ° 180 °
1.0 MHz 2.0 MHz 4.0 MHz	0 ° 90 ° 90 °

Table 39. Regulator frequency configuration

SWxFREQ[1:0]	Frequency
00	1.0 MHz
01	2.0 MHz (default)
10	4.0 MHz
11	Reserved

6.3.7.4 SW1

SW1 is a 2.75 A buck regulator. The SW1 output voltage is programmable from 1.5 V to 3.3 V. In this configuration, the SW1LX pins are connected together to a single inductor, providing up to 2.75 A current capability for high current applications. The feedback and all other controls are accomplished using the SW1FB pin.

6.3.7.5 SW1 setup and control registers

SW1 output voltages are programmable from 0.7 V to 1.425 V in steps of 25 mV. They can additionally be programmed at 1.8 V or 3.3 V. The output voltage set point is independently programmed for Normal mode by setting the SW1[4:0] bits respectively. Table 40 shows the output voltage coding.

Table 40. SW1 output voltage configuration

Set Point	SW1[4:0]	SW1x output (V)	Set Point	SW1[4:0]	SW1x output (V)
0	00000	0.700	16	10000	1.100
1	00001	0.725	17	10001	1.125
2	00010	0.750	18	10010	1.150
3	00011	0.775	19	10011	1.175
4	00100	0.800	20	10100	1.200
5	00101	0.825	21	10101	1.225
6	00110	0.850	22	10110	1.250
7	00111	0.875	23	10111	1.275
8	01000	0.900	24	11000	1.300
9	01001	0.925	25	11001	1.325
10	01010	0.950	26	11010	1.350
11	01011	0.975	27	11011	1.375
12	01100	1.000	28	11100	1.400

Table 40. SW1 output voltage configuration (continued)

Set Point	SW1[4:0]	SW1x output (V)	Set Point	SW1[4:0]	SW1x output (V)
13	01101	1.025	29	11101	1.425
14	01110	1.050	30	11110	1.800
15	01111	1.075	31	11111	3.300

Table 41 provides a list of registers used to configure and operate the SW1 regulator.

Table 41. SW1 register summary

Register	Address	Output
SW1VOLT	0x20	SW1 output voltage set point in normal operation
SW1MODE	0x23	SW1 switching mode selector register
SW1CONF	0x24	SW1 phase and frequency configuration

6.3.7.6 SW2 setup and control registers

SW2 is a single phase, 1.25 A rated buck regulator. The SW2 output voltage is programmable from 1.5 V to 1.85 V in 50 mV steps if the CTL_SW2_HL bit is low or from 2.5 V to 3.3 V in 150 mV steps, if the bit CTL_SW2_HL is set high. This internal bit CTL_SW2_HL is decided by the SW2 start-up voltage in the start-up sequence. During normal operation, output voltage of the SW2 regulator can be changed through I^2C only within the range set by the CTL_SW2_HL bit. The output voltage set point is independently programmed for Normal mode by setting the SW2[2:0] bits, respectively. Table 42 shows the output voltage coding valid for SW2.

Table 42. SW2 output voltage configuration

Low output voltage range (CTL_SW2_HL= 0)		High output voltage range (CTL_SW2_HL=1)	
SW2[2:0]	SW2 output	SW2[2:0]	SW2 output
000	1.500	000	2.500
001	1.550	001	2.800
010	1.600	010	2.850
011	1.650	011	3.000
100	1.700	100	3.100
101	1.750	101	3.150
110	1.800	110	3.200
111	1.850	111	3.300

Setup and control of SW2 is done through the I^2C registers listed in Table 43.

Table 43. SW2 register summary

Register	Address	Description
SW2VOLT	0x35	SW2 output voltage set point on normal operation
SW2MODE	0x38	SW2 switching mode selector register
SW2CONF	0x39	SW2 phase, frequency, and ILIM configuration

6.3.7.7 SW3 setup and control registers

SW3 output voltage is programmable from 0.90 V to 1.65 V in 50 mV steps to support different types of DDR memory as listed in Table 44.

Table 44. SW3 output voltage configuration

SW3[3:0]	SW3 output (V)	SW3[3:0]	SW3 output (V)
0000	0.90	1000	1.30
0001	0.95	1001	1.35
0010	1.00	1010	1.40
0011	1.05	1011	1.45
0100	1.10	1100	1.50
0101	1.15	1101	1.55
0110	1.20	1110	1.60
0111	1.25	1111	1.65

Table 45 provides a list of registers used to configure and operate SW3.

Table 45. SW3 register summary

Register	Address	Output
SW3VOLT	0x3C	SW3 output voltage set point on normal operation
SW3MODE	0x3F	SW3 switching mode selector register
SW3CONF	0x40	SW3 phase, frequency, and ILIM configuration

6.3.8 LDO regulators description

This section describes the LDO regulators provided by the PF3001. All regulators use the main bandgap as reference. When a regulator is disabled, the output discharges through an internal pull-down resistor.

Figure 10. General LDO block diagram

6.3.8.1 External components

Table 46 lists the typical component values for the general purpose LDO regulators.

Table 46. LDO external components

Regulator	Output capacitor (µF)[42]
VLDO1	2.2
VLDO2	4.7
VLDO3	2.2
VLDO4	4.7
V33	4.7
VCC_SD	2.2

Notes
42. Use X5R/X7R ceramic capacitors.

6.3.8.2 Current limit protection

All the LDO regulators in the PF3001 have current limit protection. In the event of an overload condition, the regulators transitions from a voltage regulator to a current regulator which regulates output current per the current limit threshold.

Additionally, if the REGSCPEN bit in Table 107 is set, the LDO is turned off if the current limit event lasts for more than 8.0 ms. The LDO is disabled by resetting its VLDOxEN bit, while at the same time, an interrupt VLDOxFAULTI is generated to flag the fault to the system processor. The VLDOxFAULTI interrupt is maskable through the VLDOxFAULTM mask bit. By default, the REGSCPEN is not set; therefore, at start-up none of the regulators is disabled if an overloaded condition occurs. A fault interrupt, VLDOxFAULTI, is generated in an overload condition regardless of the state of the REGSCPEN bit.

6.3.8.3 LDO voltage control

Each LDO is fully controlled through its respective VLDOxCTL register. This register enables the user to set the LDO output voltage according toTable 47 for VLDO1 and VLDO2; and uses the voltage set point on Table 48 for VLDO3 and VLDO4. Table 49 lists the voltage set points for the V33 LDO and Table 50 provides the output voltage set points for the VCC_SD LDO, based on SD_VSEL control signal.

Table 47. VLDO1, VLDO2 output voltage configuration

VLDO1[3:0] VLDO2[3:0]	VLDO1 output (V)	VLDO2 output (V)
0000	1.80	0.80
0001	1.90	0.85
0010	2.00	0.90
0011	2.10	0.95
0100	2.20	1.00
0101	2.30	1.05
0110	2.40	1.10
0111	2.50	1.15
1000	2.60	1.20
1001	2.70	1.25
1010	2.80	1.30
1011	2.90	1.35
1100	3.00	1.40

Table 47. VLDO1, VLDO2 output voltage configuration (continued)

VLDO1[3:0] VLDO2[3:0]	VLDO1 output (V)	VLDO2 output (V)
1101	3.10	1.45
1110	3.20	1.50
1111	3.30	1.55

Table 48. VLDO3, VLDO4 output voltage configuration

VLDO3[3:0] VLDO4[3:0]	VLDO3 or VLDO4 output (V)
0000	1.80
0001	1.90
0010	2.00
0011	2.10
0100	2.20
0101	2.30
0110	2.40
0111	2.50
1000	2.60
1001	2.70
1010	2.80
1011	2.90
1100	3.00
1101	3.10
1110	3.20
1111	3.30

Table 49. V33 output voltage configuration

V33[1:0]	V33 output (V)
00	2.85
01	3.00
10	3.15
11	3.30

Table 50. VCC_SD output voltage configuration

VCC_SD[1:0]	VCC_SD output (V) VSD_VSEL= 0	VCC_SD output (V) VSD_VSEL= 1
00	2.85	1.80
01	3.00	1.80
10	3.15	1.80
11	3.30	1.85

Along with the output voltage configuration, the LDOs can be enabled or disabled at anytime during normal mode operation. Each regulator has associated I^2C bits for this. Table 51 presents a summary of all valid combinations of the control bits on VLDOxCTL register and the expected behavior of the LDO output.

Table 51. LDO control

VLDOxEN/ V33EN/ VCC_SDEN	VLDOxOUT/ V33OUT/ VCC_SDOUT
0	Off
1	On

6.3.9 VSNVS LDO/switch

VSNVS powers the low power, SNVS/RTC domain on the processor. It derives its power from either VIN, or coin cell, and cannot be disabled. When powered by both, V_{IN} takes precedence when above the appropriate comparator threshold. When powered by V_{IN}, VSNVS is an LDO capable of supplying 3.0 V. When powered by coin cell, the VSNVS output tracks the coin cell voltage by means of a switch, whose maximum resistance is 100 Ω. In this case, the V_{SNVS} voltage is simply the coin cell voltage minus the voltage drop across the switch, which is 100 mV at a rated maximum load current of 1000 μA.

When the coin cell is applied for the first time, VSNVS outputs 1.0 V. Only when V_{IN} is applied thereafter does V_{SNVS} transition to its default value, or programmed value if different. Upon subsequent removal of V_{IN}, with the coin cell attached, V_{SNVS} changes configuration from an LDO to a switch, provided certain conditions are met as described in Table 52.

Figure 11. VSNVS supply switch architecture

Table 52 provides a summary of the V_{SNVS} operation at different input voltage V_{IN} and with or without coin cell connected to the system.

Table 52. SNVS Modes of Operation

VSNVSVOLT[2:0]	VIN	MODE
110	> VTH1	VIN LDO 3.0 V
110	< VTL1	Coin cell switch

6.3.9.1 VSNVS control

The V_{SNVS} output level is configured through the VSNVSVOLT[2:0] bits on VSNVSCTL register as shown in table Table 53.

Table 53. Register VSNVSCTL - ADDR 0x6B

Name	Bit #	R/W	Default	Description
VSNVSVOLT	2:0	R/W	0b000	Configures VSNVS output voltage.[43] 000 = RSVD 001 = RSVD 010 = RSVD 011 = RSVD 100 = RSVD 101 = RSVD 110 = 3.0 V (default) 111 = RSVD
Unused	7:3	–	0b00000	Unused

Notes
43. Only valid when a valid input voltage is present.

6.3.9.2 VSNVS external components

Table 54. VSNVS external components

Capacitor	Value (µF)
VSNVS	0.47

6.3.9.3 Coin cell battery backup

The LICELL pin provides for a connection of a coin cell backup battery or a “super” capacitor. If the voltage at VIN goes below the V_{IN} threshold (VTL1), contact-bounced, or removed, the coin cell maintained logic is powered by the voltage applied to LICELL. The supply for internal logic and the VSNVS rail switches over to the LICELL pin when V_{IN} goes below VTL1, even in the absence of a voltage at the LICELL pin, resulting in clearing of memory and turning off VSNVS. Applications concerned about this behavior can tie the LICELL pin to any system voltage between 1.8 V and 3.0 V. A 0.47 µF capacitor should be placed from LICELL to ground under all circumstances.

6.3.9.4 Coin cell charger control

The coin cell charger circuit functions as a current-limited voltage source, resulting in the CC/CV taper characteristic typically used for rechargeable Lithium-Ion batteries. The coin cell charger is enabled via the COINCHEN bit while the coin cell voltage is programmable through the VCOIN[2:0] bits on register COINCTL on Table 55. The coin cell charger voltage is programmable. In the ON state, the charger current is fixed at ICOINHI. In the OFF state, coin cell charging is not available as the main battery could be depleted unnecessarily. The coin cell charging stops when V_{IN} is below UVDET.

Table 55. Coin cell charger voltage

VCOIN[2:0]	V_{COIN} (V) [44]
000	2.50
001	2.70
010	2.80
011	2.90
100	3.00
101	3.10

Table 55. Coin cell charger voltage (continued)

VCOIN[2:0]	V_{COIN} (V) [44]
110	3.20
111	3.30

Notes
44. Coin cell voltages selected based on the type of LICELL used on the system.

Table 56. Register COINCTL - ADDR 0x1A

Name	Bit #	R/W	Default	Description
VCOIN	2:0	R/W	0x00	Coin cell charger output voltage selection. See Table 55 for all options selectable through these bits.
COINCHEN	3	R/W	0x00	Enable or disable the coin cell charger
Unused	7:4	–	0x00	Unused

6.3.9.5 External components

Table 57. Coin cell charger external components

Component	Value	Units
LICELL bypass capacitor	100	nF

6.4 Power dissipation

During operation, the temperature of the die should not exceed the operating junction temperature noted in Table 4. To optimize the thermal management and to avoid overheating, the PF3001 provides thermal protection. An internal comparator monitors the die temperature. Interrupts THERM110, THERM120, THERM125, and THERM130 is generated when the respective thresholds specified in Table 58 are crossed in either direction. The temperature range can be determined by reading the THERMxxxS bits in register INTSENSE0.

In the event of excessive power dissipation, thermal protection circuitry shuts down the PF3001. This thermal protection acts above the thermal protection threshold listed in Table 58. To avoid any unwanted power downs resulting from internal noise, the protection is debounced for 8.0 ms. This protection should be considered as a fail-safe mechanism and therefore the system should be configured such that this protection is not tripped under normal conditions.

Table 58. Thermal protection thresholds

Parameter	Min.	Typ.	Max.	Units
Thermal 110 °C threshold (THERM110)	100	110	120	°C
Thermal 120 °C threshold (THERM120)	110	120	130	°C
Thermal 125 °C threshold (THERM125)	115	125	135	°C
Thermal 130 °C threshold (THERM130)	120	130	140	°C
Thermal warning hysteresis	2.0	–	4.0	°C
Thermal protection threshold	130	140	150	°C

6.5 Modes of operation

6.5.1 State diagram

The operation of the PF3001 can be reduced to three states, or modes: ON, OFF, and Coin cell. Figure 12 shows the state diagram of the PF3001, along with the conditions to enter and exit from each state.

Figure 12. State diagram

To complement the state diagram in Figure 12, a description of the states is provided in following sections. Note that V_{IN} must exceed the rising UVDET threshold to allow a power up. Refer to Table 30 for the UVDET thresholds. Additionally, I^2C control is not possible in the coin cell mode and the interrupt signal, INTB, is only active in the on state.

6.5.1.1 ON mode

The PF3001 enters the on mode after a turn-on event. RESETBMCU is de-asserted, and pulled high via an external pull-up resistor, in this mode of operation. To enter the on mode, VIN voltage must surpass the rising UVDET threshold and PWRON must be asserted. From the on mode, when the voltage at VIN drops below the undervoltage falling threshold, UVDET, the state machine transitions to the coin cell mode.

6.5.1.2 OFF mode

The PF3001 enters the Off mode after a turn-off event. Only VCOREDIG and VSNVS are powered in the mode of operation. To exit the off mode, a valid turn-on event is required. RESETBMCU is asserted, LOW, in this mode. Turn off events can be achieved using the PWRON pin, thermal protection, as described by the following.

6.5.1.3 PWRON pin

The PWRON pin is used to power off the PF3001. The PWRON pin powers off the PMIC under conditions where the PWRON pin is low.

6.5.1.4 Thermal protection

If the die temperature surpasses a given threshold, the thermal protection circuit powers off the PMIC to avoid damage. A turn-on event does not power on the PMIC while it is in thermal protection. The part remains in off mode until the die temperature decreases below a given threshold. See Power dissipation section for more detailed information.

6.5.1.5 Coin cell mode

In the coin cell state, the coin cell is the only valid power source to the PMIC. No turn-on event is accepted in the coin cell state. Transition to the off state requires V_{IN} surpasses the UVDET threshold. RESETBMCU is held low in this mode. If the coin cell is depleted, a complete system reset occurs. At the next application of power and the detection of a turn-on event, the system re-initializes with all I^2C bits including, those that reset on COINPORB are restored to their default states.

6.5.2 State machine flow summary

Table 59 provides a summary matrix of the PF3001 flow diagram to show the conditions needed to transition from one state to another.

Table 59. State machine flow summary

STATE		Next state		
		OFF	**Coin cell**	**ON**
Initial State	**OFF**	X	V_{IN} < UVDET	PWRON = 1 and V_{IN} > UVDET
	Coin cell	V_{IN} > UVDET	X	X
	ON	Thermal Shutdown	V_{IN} < UVDET	X
		PWRON = 0		

6.5.3 Performance characteristics curves

V_{IN} = 3.6 V, $SW1_{OUT}$ = 1.0 V, $SW2_{OUT}$ = 1.8 V, $SW3_{OUT}$ = 1.0 V, Switching frequency = 2.0 MHz, Mode = APS; $LDO1_{OUT}$ = 1.8 V, $LDO2_{OUT}$ = 1.0 V, $LDO3_{OUT}$ = 1.8 V, $LDO4_{OUT}$ = 1.8 V, $V33_{OUT}$ = 3.3 V, VCC_SD_{OUT} = 3.3 V, unless otherwise noted

Figure 13. Start-up sequence

Figure 14. Load transient response - LDO2

Figure 15. Load transient response - LDO1, LDO3 and VCC_SD

Figure 16. Load transient response - LDO4 and V33

Figure 17. Load transient response - buck regulators

Figure 18. Quiescent current - LDOs

Figure 19. Load regulation - LDOs

Figure 20. Dropout voltage - VLDO1, VLDO3, VCC_SD - V_{OUT} = 3.3 V

Figure 21. Dropout voltage - VLDO1, VLDO3, VCC_SD - V_{OUT} = 1.8 V

Figure 22. Dropout voltage - VLDO4, V33 - V_{OUT} = 3.3 V

Figure 23. Dropout voltage - VLDO4 - V_{OUT} = 1.8 V

6.6 Control interface I²C block description

The PF3001 contains an I²C interface port which allows access by a processor, or any I²C master, to the register set. Via these registers the resources of the IC can be controlled. The registers also provide status information about how the IC is operating.

6.6.1 I²C device ID

I²C interface protocol requires a device ID for addressing the target IC on a multi-device bus. The I²C address of the PF3001 is set to 0x08.

6.6.2 I²C operation

The I²C mode of the interface is implemented generally following the fast mode definition which supports up to 400 kbits/s operation (exceptions to the standard are noted to be 7-bit only addressing and no support for General Call addressing.) Timing diagrams, electrical specifications, and further details can be found in the I²C specification, which is available for download.

I²C read operations are also performed in byte increments separated by an ACK. Read operations also begin with the MSB and each byte is sent out unless a STOP command or NACK is received prior to completion.

The following examples show how to write and read data to and from the IC. The host initiates and terminates all communication. The host sends a master command packet after driving the start condition. The device responds to the host if the master command packet contains the corresponding slave address. In the following examples, the device is always shown responding with an ACK to transmissions from the host. If at any time a NACK is received, the host should terminate the current transaction and retry the transaction.

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Figure 24. I²C write example

Figure 25. I²C read example

6.6.3 Interrupt handling

The system is informed about important events based on interrupts. Unmasked interrupt events are signaled to the processor by driving the INTB pin low. Each interrupt is latched so even if the interrupt source becomes inactive, the interrupt remains set until cleared. Each interrupt can be cleared by writing a “1” to the appropriate bit in the Interrupt Status register; this causes the INTB pin to go high. If there are multiple interrupt bits set the INTB pin remains low until all are either masked or cleared. If a new interrupt occurs while the processor clears an existing interrupt bit, the INTB pin remains low.

Each interrupt can be masked by setting the corresponding mask bit to a 1. As a result, when a masked interrupt bit goes high, the INTB pin does not go low. A masked interrupt can still be read from the Interrupt Status register. This gives the processor the option of polling for status from the IC. The IC powers up with all interrupts masked, so the processor must initially poll the device to determine if any interrupts are active. Alternatively, the processor can unmask the interrupt bits of interest. If a masked interrupt bit was already high, the INTB pin goes low after unmasking.

The sense registers contain status and input sense bits so the system processor can poll the current state of interrupt sources. They are read only, and not latched or clearable. Interrupts generated by external events are debounced; therefore, the event needs to be stable throughout the debounce period before an interrupt is generated. Nominal debounce periods for each event are documented in the INT summary Table 60. Due to the asynchronous nature of the debounce timer, the effective debounce time can vary slightly.

6.6.4 Interrupt bit summary

Table 60 summarizes all interrupt, mask, and sense bits associated with INTB control. For more detailed behavioral descriptions, refer to the related chapters.

Table 60. Interrupt, Mask, and Sense Bits

Interrupt	Mask	Sense	Purpose	Trigger	Debounce time (ms)
LOWVINI	LOWVINM	LOWVINS	Low input voltage detect Sense is 1 if below 2.70 V threshold	H to L	3.9 [45]
PWRONI	PWRONM	PWRONS	Power on button event	H to L	31.25 [45]
			Sense is 1 if PWRON is high.	L to H	31.25
THERM110	THERM110M	THERM110S	Thermal 110 °C threshold Sense is 1 if above threshold	Dual	3.9
THERM120	THERM120M	THERM120S	Thermal 120 °C threshold Sense is 1 if above threshold	Dual	3.9
THERM125	THERM125M	THERM125S	Thermal 125 °C threshold Sense is 1 if above threshold	Dual	3.9
THERM130	THERM130M	THERM130S	Thermal 130 °C threshold Sense is 1 if above threshold	Dual	3.9
SW1FAULTI	SW1FAULTM	SW1FAULTS	Regulator 1 overcurrent limit Sense is 1 if above current limit	L to H	8.0
SW2FAULTI	SW2FAULTM	SW2FAULTS	Regulator 2 overcurrent limit Sense is 1 if above current limit	L to H	8.0
SW3FAULTI	SW3FAULTM	SW3FAULTS	Regulator 3 overcurrent limit Sense is 1 if above current limit	L to H	8.0
VLDO1FAULTI	VLDO1FAULTM	VLDO1FAULTS	VLDO1 overcurrent limit Sense is 1 if above current limit	L to H	8.0
VLDO2FAULTI	VLDO2FAULTM	VLDO2FAULTS	VLDO2 overcurrent limit Sense is 1 if above current limit	L to H	8.0
VCC_SDFAULTI	VCC_SDFAULTM	VCC_SDFAULTS	VCC_SD overcurrent limit Sense is 1 if above current limit	L to H	8.0
V33FAULTI	V33FAULTM	V33FAULTS	V33 overcurrent limit Sense is 1 if above current limit	L to H	8.0
VLDO3FAULTI	VLDO3FAULTM	VLDO1FAULTS	VLDO3 overcurrent limit Sense is 1 if above current limit	L to H	8.0

Table 60. Interrupt, Mask, and Sense Bits (continued)

Interrupt	Mask	Sense	Purpose	Trigger	Debounce time (ms)
VLDO4FAULTI	VLDO4FAULTM	VLDO4FAULTS	VLDO4 overcurrent limit Sense is 1 if above current limit	L to H	8.0
VPWROVI	VPWROVM	VPWROVS	VPWR pin overvoltage interrupt	L to H	0.122

Notes
45. Typical debounce timing for the falling edge can be extended with PWRONDBNC[1:0].

A full description of all interrupt, mask, and sense registers is provided in Table 61 to Table 72.

Table 61. Register INTSTAT0 - ADDR 0x05

Name	Bit #	R/W	Default	Description
PWRONI	0	R/W1C	0	Power on interrupt bit
LOWVINI	1	R/W1C	0	Low-voltage interrupt bit
THERM110I	2	R/W1C	0	110 °C thermal interrupt bit
THERM120I	3	R/W1C	0	120 °C thermal interrupt bit
THERM125I	4	R/W1C	0	125 °C thermal interrupt bit
THERM130I	5	R/W1C	0	130 °C thermal interrupt bit
Unused	7:6	–	0b00	Unused

Table 62. Register INTMASK0 - ADDR 0x06

Name	Bit #	R/W	Default	Description
PWRONM	0	R/W1C	1	Power on interrupt mask bit
LOWVINM	1	R/W1C	1	Low-voltage interrupt mask bit
THERM110M	2	R/W1C	1	110 °C thermal interrupt mask bit
THERM120M	3	R/W1C	1	120 °C thermal interrupt mask bit
THERM125M	4	R/W1C	1	125 °C thermal interrupt mask bit
THERM130M	5	R/W1C	1	130 °C thermal interrupt mask bit
Unused	7:6	–	0b00	Unused

Table 63. Register INTSENSE0 - ADDR 0x07

Name	Bit #	R/W	Default	Description
PWRONS	0	R	0	Power on sense bit 0 = PWRON low 1 = PWRON high
LOWVINS	1	R	0	Low-voltage sense bit 0 = VIN > 2.7 V 1 = VIN ≤ 2.7 V
THERM110S	2	R	0	110 °C thermal sense bit 0 = Below threshold 1 = Above threshold
THERM120S	3	R	0	120 °C thermal sense bit 0 = Below threshold 1 = Above threshold
THERM125S	4	R	0	125 °C thermal sense bit 0 = Below threshold 1 = Above threshold

Table 63. Register INTSENSE0 - ADDR 0x07 (continued)

Name	Bit #	R/W	Default	Description
THERM130S	5	R	0	130 °C thermal sense bit 0 = Below threshold 1 = Above threshold
ICTEST1S	6	R	0	0 = ICTEST1 pin is grounded 1 = ICTEST1 to VCOREDIG or greater
ICTEST2S	7	R	0	Additional ICTEST2 voltage sense pin 0 = ICTEST2 pin is grounded 1 = ICTEST2 to VCOREDIG or greater

Table 64. Register INTSTAT1 - ADDR 0x08

Name	Bit #	R/W	Default	Description
SW1FAULTI	0	R/W1C	0	SW1 overcurrent interrupt bit
Unused	1	R/W1C	0	Unused
Unused	2	R/W1C	0	Unused
SW2FAULTI	3	R/W1C	0	SW2 overcurrent interrupt bit
SW3FAULTI	4	R/W1C	0	SW3 overcurrent interrupt bit
Unused	5	R/W1C	0	Unused
Unused	6	R/W1C	0	Unused
Unused	7	–	0	Unused

Table 65. Register INTMASK1 - ADDR 0x09

Name	Bit #	R/W	Default	Description
SW1FAULTM	0	R/W	1	SW1 overcurrent interrupt mask bit
Unused	1	R/W	1	Unused
Unused	2	R/W	1	Unused
SW2FAULTM	3	R/W	1	SW2 overcurrent interrupt mask bit
SW3FAULTM	4	R/W	1	SW3 overcurrent interrupt mask bit
Unused	5	R/W	1	Unused
Unused	6	R/W	1	Unused
Unused	7	–	0	Unused

Table 66. Register INTSENSE1 - ADDR 0x0A

Name	Bit #	R/W	Default	Description
SW1FAULTS	0	R	0	SW1 overcurrent sense bit 0 = Normal operation 1 = Above current limit
Unused	1	R	0	Unused
Unused	2	R	0	Unused
SW2FAULTS	3	R	0	SW2 overcurrent sense bit 0 = Normal operation 1 = Above current limit
SW3FAULTS	4	R	0	SW3 overcurrent sense bit 0 = Normal operation 1 = Above current limit

Table 66. Register INTSENSE1 - ADDR 0x0A (continued)

Name	Bit #	R/W	Default	Description
Unused	5	R	0	Unused
Unused	6	R	0	Unused
Unused	7	–	0	Unused

Table 67. Register INTSTAT3 - ADDR 0x0E

Name	Bit #	R/W	Default	Description
Unused	0	R/W1C	0	Unused
Unused	1	–	0b0	Unused
VPWROVI	2	R/W1C	0b0	High when overvoltage event is detected in the front-end LDO circuit. This bit defaults to 0b1 when VPWR is grounded and the V_{IN} path is used to power the PF3001.
Unused	5:3	–	0b0	Unused
Unused	6	R/W1C	0b0	Unused
Unused	7	R/W1C	0	Unused

Table 68. Register INTMASK3 - ADDR 0x0F

Name	Bit #	R/W	Default	Description
Unused	0	R/W	1	Unused
Unused	1	–	0	Unused
VPWROVM	2	R/W	1	VPWR overvoltage interrupt mask bit
Unused	5:3	–	0b000	Unused
Unused	6	R/W	1	Unused
Unused	7	R/W	1	Unused

Table 69. Register INTSENSE3 - ADDR 0x10

Name	Bit #	R/W	Default	Description
Unused	0	R	0	Unused
Unused	1	–	0b0	Unused
VPWROVS	2	R	0	VPWR overvoltage interrupt sense bit
Unused	5:3	–	0b000	Unused
Unused	6	R	0	Unused
Unused	7	R	0	Unused

Table 70. Register INTSTAT4 - ADDR 0x11

Name	Bit #	R/W	Default	Description
VLDO1FAULTI	0	R/W1C	0	VLDO1 overcurrent interrupt bit
VLDO2FAULTI	1	R/W1C	0	VLDO2 overcurrent interrupt bit
VCC_SDFAULTI	2	R/W1C	0	VCC_SD overcurrent interrupt bit
V33FAULTI	3	R/W1C	0	V33 overcurrent interrupt bit
VLDO3FAULTI	4	R/W1C	0	VLDO3 overcurrent interrupt bit
VLDO4FAULTI	5	R/W1C	0	VLDO4 overcurrent interrupt bit
Unused	7:6	–	0b00	Unused

Table 71. Register INTMASK4 - ADDR 0x12

Name	Bit #	R/W	Default	Description
VLDO1FAULTM	0	R/W	1	VLDO1 overcurrent interrupt mask bit
VLDO2FAULTM	1	R/W	1	VLDO2 overcurrent interrupt mask bit
VCC_SDFAULTM	2	R/W	1	VCC_SD overcurrent interrupt mask bit
V33FAULTM	3	R/W	1	V33 overcurrent interrupt mask bit
VLDO3FAULTM	4	R/W	1	VLDO3 Overcurrent interrupt mask bit
VLDO4FAULTM	5	R/W	1	VLDO4 Overcurrent interrupt mask bit
Unused	7:6	–	0b00	Unused

Table 72. Register INTSENSE4 - ADDR 0x13

Name	Bit #	R/W	Default	Description
VLDO1FAULTS	0	R	0	VLDO1 overcurrent sense bit 0 = Normal operation 1 = Above current limit
VLDO2FAULTS	1	R	0	VLDO2 overcurrent sense bit 0 = Normal operation 1 = Above current limit
VCC_SDFAULTS	2	R	0	VCC_SD overcurrent sense bit 0 = Normal operation 1 = Above current limit
V33FAULTS	3	R	0	V33 overcurrent sense bit 0 = Normal operation 1 = Above current limit
VLDO3FAULTS	4	R	0	VLDO3 overcurrent sense bit 0 = Normal operation 1 = Above current limit
VLDO4FAULTS	5	R	0	VLDO4 overcurrent sense bit 0 = Normal operation 1 = Above current limit
Unused	7:6	–	0b00	Unused

6.6.5 Specific registers

6.6.5.1 IC and version identification

The IC and other version details can be read via identification bits. These are hard-wired on the chip and described in Table 73 to Table 75.

Table 73. Register DEVICEID - ADDR 0x00

Name	Bit #	R/W	Default	Description
DEVICEID	3:0	R	0x1	0001 = PF3001
Unused	7:4	–	0x3	Unused

Table 74. Register SILICON REV- ADDR 0x03

Name	Bit #	R/W	Default	Description
METAL_LAYER_REV	3:0	R	0x0	Represents the metal mask revision Pass 0.0 = 0000 … Pass 0.15 = 1111
FULL_LAYER_REV	7:4	R	0x1	Represents the full mask revision Pass 1.0 = 0001 … Pass 15.0 = 1111

Table 75. Register FABID - ADDR 0x04

Name	Bit #	R/W	Default	Description
FIN	1:0	R	0b00	Allows for characterizing different options within the same reticule
FAB	3:2	R	0b00	Represents the wafer manufacturing facility
Unused	7:4	R	0b0000	Unused

6.6.5.2 Embedded memory

There are four register banks of general purpose embedded memory to store critical data. The data written to MEMA[7:0], MEMB[7:0], MEMC[7:0], and MEMD[7:0] is maintained by the coin cell when the main battery is deeply discharged, removed, or contact-bounced. The contents of the embedded memory are reset by COINPORB. The banks can be used for any system need for bit retention with coin cell backup.

Table 76. Register MEMA ADDR 0x1C

Name	Bit #	R/W	Default	Description
MEMA	7:0	R/W	0x00	Memory bank A

Table 77. Register MEMB ADDR 0x1D

Name	Bit #	R/W	Default	Description
MEMB	7:0	R/W	0x00	Memory bank B

Table 78. Register MEMC ADDR 0x1E

Name	Bit #	R/W	Default	Description
MEMC	7:0	R/W	0x00	Memory bank C

Table 79. Register MEMD ADDR 0x1F

Name	Bit #	R/W	Default	Description
MEMD	7:0	R/W	0x00	Memory bank D

6.6.5.3 Register descriptions

This section describes all the PF3001 registers and their individual bits. Address order is as listed in Register map.

6.6.5.3.1 Interrupt status register 0 (INTSTAT0)

INSTAT0 is one of the four status interrupt registers. This register contains six status flags. Write a logic 1 to clear a flag.

Table 80. Status interrupt register 0 (INTSTAT0)

Address: 0x05 functional page **Access: User read/write [46]**

	7	6	5	4	3	2	1	0
R W			THERM130I	THERM125I	THERM120I	THERM110I	LOWVINI	PWRONI
Default	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Notes
46. Read: Anytime
Write: Anytime

Table 81. INTSTAT0 field descriptions

Field	Description
5 THERM130I	**130 °C thermal interrupt bit** — THERM130I is set to 1 when the THERM130 threshold specified in is crossed in either direction (bi-directional). This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Die temperature has not crossed THERM130 threshold. 1 Die temperature has crossed THERM130 threshold.
4 THERM125I	**125 °C thermal interrupt bit** — THERM125I is set to 1 when the THERM125 threshold specified in is crossed in either direction (bi-directional). This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Die temperature has not crossed THERM125 threshold. 1 Die temperature has crossed THERM125 threshold.
3 THERM120I	**120 °C thermal interrupt bit** — THERM120I is set to 1 when the THERM120 threshold specified in is crossed in either direction (bi-directional). This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Die temperature has not crossed THERM120 threshold. 1 Die temperature has crossed THERM120 threshold.
2 THERM110I	**110 °C thermal interrupt bit** — THERM110I is set to 1 when the THERM110 threshold specified in is crossed in either direction (bi-directional). This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Die temperature has not crossed THERM110 threshold. 1 Die temperature has crossed THERM110 threshold.
1 LOWVINI	**Low-voltage interrupt bit** — LOWVINI is set to 1 when a low-voltage event occurs on VIN. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 V_{IN} > 2.7 V (typical) 1 V_{IN} < 2.7 V (typical)
0 PWRONI	**Power on interrupt bit** —PWRONI is set to 1 when the turn on event occurs. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Power on has not occurred. 1 Power on has occurred.

6.6.5.3.2 Interrupt status mask register 0 (INTMASK0)

INTMASK0 is the mask register for the status interrupt register INTSTAT0. Write a logic 0 to a bit to unmask the corresponding interrupt. When unmasked, the corresponding interrupt state is reflected on the INTB pin.

Table 82. Interrupt status mask register 0 (INTMASK0)

Address: 0x06 functional page **Access: User read/write** [47]

	7	6	5	4	3	2	1	0
R W			THERM130M	THERM125M	THERM120M	THERM110M	LOWVINM	PWRONM
Default	0	0	1	1	1	1	1	1

= Unimplemented or Reserved

Notes
47. Read: Anytime
Write: Anytime

Table 83. INTMASK0 field descriptions

Field	Description
5 THERM130M	**130 °C thermal interrupt mask bit** 0 THERM130I Unmasked 1 THERM130I Masked
4 THERM125M	**125 °C thermal interrupt mask bit** 0 THERM125I Unmasked 1 THERM125I Masked
3 THERM120M	**120 °C thermal interrupt mask bit** 0 THERM120I Unmasked 1 THERM120I Masked
2 THERM110M	**110 °C thermal interrupt mask bit** 0 THERM110I Unmasked 1 THERM110I Masked
1 LOWVINM	**Low-voltage interrupt mask bit** 0 LOWVINI Unmasked 1 LOWVINI Masked
0 PWRONM	**Power on interrupt mask bit** 0 PWRONI Unmasked 1 PWRONI Masked

6.6.5.3.3 Interrupt sense register 0 (INTSENSE0)

This register has seven read-only sense bits. These sense bits reflects the actual state of the corresponding function.

Table 84. Interrupt sense register 0 (INTSENSE0)

Address: 0x07 functional page **Access: User read-only [48]**

	7	6	5	4	3	2	1	0
R	ICTEST2S		THERM130S	THERM125S	THERM120S	THERM110S	LOWVINS	PWRONS
W								
Default	X [52]	0	X [51]	X [51]	X [51]	X [51]	X [50]	X [49]

= Unimplemented or Reserved

Notes
48. Read: Anytime
49. Default value depends on the initial PWRON pin state.
50. Default value depends on the initial VIN voltage.
51. Default value depends on the initial temperature of the die.
52. Default value depends on the initial ICTEST2 pin state.

Table 85. INTSENSE0 field descriptions

Field	Description
7 ICTEST2S	**VDDOTP voltage sense bit** 0 ICTEST2 grounded. 1 ICTEST2 to VCOREDIG or greater.
5 THERM130S	**130 °C thermal interrupt sense bit** 0 Die temperature below THERM130 threshold. 1 Die temperature above THERM130 threshold.
4 THERM125S	**125 °C thermal interrupt sense bit** 0 Die temperature below THERM125 threshold. 1 Die temperature has crossed THERM125 threshold.
3 THERM120S	**120 °C thermal interrupt sense bit** 0 Die temperature below THERM120 threshold. 1 Die temperature has crossed THERM120 threshold.
2 THERM110S	**110 °C thermal interrupt sense bit** 0 Die temperature below THERM110 threshold. 1 Die temperature has crossed THERM110 threshold.
1 LOWVINS	**Low-voltage interrupt sense bit** 0 $V_{IN} > 2.7$ V (typical) 1 $V_{IN} < 2.7$ V (typical)
0 PWRONS	**Power on interrupt sense bit** 0 PWRON low. 1 PWRON high.

6.6.5.3.4 Interrupt status register 1 (INTSTAT1)

INSTAT1 is one of the three status interrupt registers. This register contains three status flags. Write a logic 1 to clear a flag.

Table 86. Status interrupt register 1 (INTSTAT1)

Address: 0x08 functional page **Access: User read/write** [53]

	7	6	5	4	3	2	1	0
R W				SW3FAULTI	SW2FAULTI			SW1FAULTI
Default	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Notes
53. Read: Anytime
Write: Anytime

Table 87. INTSTAT1 field descriptions

Field	Description
4 SW3FAULTI	**SW3 overcurrent interrupt bit** — SW3FAULTI is set to 1 when the SW3 regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 SW3 in normal operation 1 SW3 above current limit
3 SW2FAULTI	**SW2 overcurrent interrupt bit** — SW2FAULTI is set to 1 when the SW2 regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 SW2 in normal operation 1 SW2 above current limit
0 SW1FAULTI	**SW1 overcurrent interrupt bit** — SW1FAULTI is set to 1 when the SW1 regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 SW1 in normal operation 1 SW1 above current limit

6.6.5.3.5 Interrupt status mask register 1 (INTMASK1)

INTMASK1 is the mask register for the status interrupt register INTSTAT1. Write a logic 0 to a bit to unmask the corresponding interrupt. When unmasked, the corresponding interrupt state is reflected on the INTB pin.

Table 88. Interrupt status mask register 1 (INTMASK1)

Address: 0x09 functional page **Access: User read/write** [54]

	7	6	5	4	3	2	1	0
R W				SW3FAULTM	SW2FAULTM			SW1FAULTM
Default	0	0	0	1	1	0	1	0

= Unimplemented or Reserved

Notes
54. Read: Anytime
Write: Anytime

Table 89. INTMASK1 field descriptions

Field	Description
4 SW3FAULTM	**SW3 overcurrent interrupt mask bit** 0 SW3FAULTI Unmasked 1 SW3FAULTI Masked
3 SW2FAULTM	**SW2 overcurrent interrupt mask bit** 0 SW2FAULTI Unmasked 1 SW2FAULTI Masked
0 SW1FAULTM	**SW1 overcurrent interrupt mask bit** 0 SW1FAULTI Unmasked 1 SW1FAULTI Masked

6.6.5.3.6 Interrupt sense register 1 (INTSENSE1)

This register has three read-only sense bits. These sense bits reflect the actual state of the corresponding function.

Table 90. Interrupt sense register 1 (INTSENSE1)

Address: 0x0A functional page **Access: User read-only [55]**

	7	6	5	4	3	2	1	0
R				SW3FAULTS	SW2FAULTS			SW1FAULTS
W								
Default	0	0	0	X[56]	X[56]	0	X[56]	X[56]

= Unimplemented or Reserved

Notes
55. Read: Anytime
56. Default value depends on the regulator initial state

Table 91. INTSENSE1 field descriptions

Field	Description
4 SW3FAULTS	**SW3 overcurrent sense bit** 0 SW3 in normal operation 1 SW3 above current limit
3 SW2FAULTS	**SW2 overcurrent sense bit** 0 SW2 in normal operation 1 SW2 above current limit
0 SW1FAULTS	**SW1 overcurrent sense bit** 0 SW1 in normal operation 1 SW1 above current limit

6.6.5.3.7 Interrupt status register 3 (INTSTAT3)

INSTAT3 is one of the status interrupt registers. This register contains a status flag. Write a logic 1 to clear a flag.

Table 92. Status interrupt register 3 (INTSTAT3)

Address: 0x0E Functional Page **Access: User read/write [57]**

	7	6	5	4	3	2	1	0
R W						VPWROVI		
Default	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Notes
57. Read: Anytime
Write: Anytime

Table 93. INTSTAT3 field descriptions

Field	Description
2 VPWROVI	**VPWR overvoltage interrupt bit** — High when overvoltage event is detected in the front-end LDO circuit. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 VPWR in normal operation range. 1 VPWR in overvoltage range.

6.6.5.3.8 Interrupt status mask register 3 (INTMASK3)

INTMASK3 is the mask register for the status interrupt register INTSTAT3. Write a logic 0 to a bit to unmask the corresponding interrupt. When unmasked, the corresponding interrupt state is reflected on the INTB pin.

Table 94. Interrupt status mask register 3 (INTMASK3)

Address: 0x0F functional page **Access: User read/write [58]**

	7	6	5	4	3	2	1	0
R W						VPWROVM		
Default	1	1	0	0	0	1	0	1

= Unimplemented or Reserved

Notes
58. Read: Anytime
Write: Anytime

Table 95. INTMASK3 field descriptions

Field	Description
2 VPWROVM	**VPWR overvoltage interrupt mask bit** 0 VPWROVI Unmasked 1 VPWROVI Masked

6.6.5.3.9 Interrupt sense register 3 (INTSENSE3)

This register has a read-only sense bit. This sense bit reflects the actual state of the corresponding function.

Table 96. Interrupt sense register 3 (INTSENSE3)

Address: 0x10 functional page **Access: User read-only** [59]

	7	6	5	4	3	2	1	0
R						VPWROVS		
W								
Default	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Notes
59. Read: Anytime

Table 97. INTSENSE3 field descriptions

Field	Description
2 VPWROVS	**VPWR overvoltage interrupt sense bit** 0 VPWR in normal operation range. 1 VPWR in overvoltage range.

6.6.5.3.10 Interrupt status register 4 (INTSTAT4)

INSTAT4 is one of the status interrupt registers. This register contains six status flags. Write a logic 1 to clear a flag.

Table 98. Status interrupt register 4 (INTSTAT4)

Address: 0x11 functional page **Access: User read/write** [60]

	7	6	5	4	3	2	1	0
R W			VLDO4FAULTI	VLDO3FAULTI	V33FAULTI	VCC_SDFAULTI	VLDO2FAULTI	VLDO1FAULTI
Default	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Notes
60. Read: Anytime
Write: Anytime

Table 99. INTSTAT4 field descriptions

Field	Description
5 VLDO4FAULTI	**VLDO4 overcurrent interrupt bit** — VLDO4FAULTI is set to 1 when the VLDO4 regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 VLDO4 in normal operation 1 VLDO4 above current limit
4 VLDO3FAULTI	**VLDO3 overcurrent interrupt bit** — VLDO3FAULTI is set to 1 when the VLDO3 regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 VLDO3 in normal operation 1 VLDO3 above current limit
3 V33FAULTI	**V33 overcurrent interrupt bit** — V33FAULTI is set to 1 when the V33 regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 V33 in normal operation 1 V33 above current limit
2 VCC_SDFAULTI	**VCC_SD overcurrent interrupt bit** — VCC_SDFAULTI is set to 1 when the VCC_SD regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 VCC_SD in normal operation 1 VCC_SD above current limit
1 VLDO2FAULTI	**VLDO2 overcurrent interrupt bit** — VLDO2FAULTI is set to 1 when the VLDO2 regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 VLDO2 in normal operation range. 1 VLDO2 above current limit
0 VLDO1FAULTI	**VLDO1 overcurrent interrupt bit** — VLDO1FAULTI is set to 1 when the VLDO1 regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 VLDO1 in normal operation range. 1 VLDO1 above current limit

6.6.5.3.11 Interrupt status mask register 4 (INTMASK4)

INTMASK4 is the mask register for the status interrupt register INTSTAT4. Write a logic 0 to a bit to unmask the corresponding interrupt. When unmasked, the corresponding interrupt state is reflected on the INTB pin.

Table 100. Interrupt status mask register 4 (INTMASK4)

Address: 0x12 functional page — **Access: User read/write** [61]

	7	6	5	4	3	2	1	0
R W			VLDO4FAULTM	VLDO3FAULTM	V33FAULTM	VCC_SDFAULTM	VLDO2FAULTM	VLDO1FAULTM
Default	0	0	1	1	1	1	1	1

= Unimplemented or Reserved

Notes
61. Read: Anytime
Write: Anytime

Table 101. INTMASK4 field descriptions

Field	Description
5 VLDO4FAULTM	**VLDO4 overcurrent interrupt mask bit** 0 VLDO4FAULTI Unmasked 1 VLDO4FAULTI Masked
4 VLDO3FAULTM	**VLDO3 overcurrent interrupt mask bit** 0 VLDO3FAULTI Unmasked 1 VLDO3FAULTI Masked
3 V33FAULTM	**V33 overcurrent interrupt mask bit** 0 V33FAULTI Unmasked 1 V33FAULTI Masked
2 VCC_SDFAULTM	**VCC_SD overcurrent interrupt mask bit** 0 VCC_SDFAULTI Unmasked 1 VCC_SDFAULTI Masked
1 VLDO2FAULTM	**VLDO2 overcurrent interrupt mask bit** 0 VLDO2FAULTI Unmasked 1 VLDO2FAULTI Masked
0 VLDO1FAULTM	**VLDO1 overcurrent interrupt mask bit** 0 VLDO1FAULTI Unmasked 1 VLDO1FAULTI Masked

6.6.5.3.12 Interrupt sense register 4 (INTSENSE4)

This register has read-only sense bits. These sense bits reflect the actual state of the corresponding function.

Table 102. Interrupt sense register 4 (INTSENSE4)

Address: 0x13 functional page **Access: User read-only [62]**

	7	6	5	4	3	2	1	0
R			VLDO4FAULTS	VLDO3FAULTS	V33FAULTS	VCC_SDFAULTS	VLDO2FAULTS	VLDO1FAULTS
W								
Default	0	0	X [63]	X [63]	X [63]	X [63]	X [63]	X [63]

= Unimplemented or Reserved

Notes
62. Read: Anytime
63. Default value depends on the regulator initial state

Table 103. INTSENSE4 field descriptions

Field	Description
5 VLDO4FAULTS	**VLDO4 overcurrent sense bit** 0 VLDO4 in normal operation 1 VLDO4 above current limit
4 VLDO3FAULTS	**VLDO3 overcurrent sense bit** 0 VLDO3 in normal operation 1 VLDO3 above current limit
3 V33FAULTS	**V33 overcurrent sense bit** 0 V33 in normal operation 1 V33 above current limit
2 VCC_SDFAULTS	**VCC_SD overcurrent sense bit** 0 VCC_SD in normal operation 1 VCC_SD above current limit
1 VLDO2FAULTS	**VLDO2 overcurrent sense bit** 0 VLDO2 in normal operation 1 VLDO2 above current limit
0 VLDO1FAULTS	**VLDO1 overcurrent sense bit** 0 VLDO1 in normal operation 1 VLDO1 above current limit

6.6.5.3.13 Coin cell control register (COINCTL)

This register is used to control the coin cell charger.

Table 104. Coin cell control register (COINCTL)

Address: 0x1A functional page **Access: User read/write [64]**

	7	6	5	4	3	2	1	0
R W					COINCHEN	VCOIN		
Default	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Notes
64. Read: Anytime
Write: Anytime

Table 105. COINCTL field descriptions

Field	Description
3 COINCHEN	**Coin cell charger enable bit** 0 Coin Cell charger disabled. 1 Coin Cell charger enabled.
2:0 VCOIN	**Coin cell charger output voltage selection** — This field is used to set the coin cell charging voltage from 2.50 V to 3.30 V. See Table 55 for all options selectable through these bits.

6.6.5.3.14 Power control register (PWRCTL)

Table 106. Power control register (PWRCTL)

Address: 0x1B functional page **Access: User read/write [65]**

	7	6	5	4	3	2	1	0
R W	REGSCPEN						PWRONRSTEN	RESTARTEN
Default	0	0	0	1	0	0	0	0

= Unimplemented or Reserved

Notes
65. Read: Anytime
Write: Anytime

Table 107. PWRCTL field descriptions

Field	Description
7 REGSCPEN	**Short-circuit protection enable bit** — When REGSCPEN is set to 1, whenever a current limit event occurs on a LDO regulator, this regulator is shutdown. 0 Short-circuit protection disabled 1 Short-circuit protection enabled
1 PWRONRSTEN	**PWRON reset enable bit** — When set to 1, the PF3001 can enter OFF mode when the PWRON pin is held low for 4 seconds or longer. See PWRON Pin section for details. 0 Disallow OFF mode after PWRON held low 1 Allow OFF mode after PWRON held low
0 RESTARTEN	**Restart enable bit** — When set to 1, the PF3001 restarts automatically after a power off event generated by the PWRON (held low for 4 seconds or longer) when PWR_CFG bit = 1. 0 Automatic restart disabled. 1 Automatic restart enabled.

6.6.5.3.15 Embedded memory register A (MEMA)

Table 108. Embedded memory register A (MEMA)

Address: 0x1C functional page **Access: User read/write [66]**

	7	6	5	4	3	2	1	0
R W	MEMA							
Default	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Notes
66. Read: Anytime
Write: Anytime

Table 109. MEMA field descriptions

Field	Description
7:0 MEMA	**Memory bank A** — This register is maintained in case of a main battery loss as long as the coin cell is present. The contents of the embedded memory are reset by COINPORB.

6.6.5.3.16 Embedded memory register B (MEMB)

Table 110. Embedded memory register B (MEMB)

Address: 0x1D functional page **Access: User read/write** [67]

	7	6	5	4	3	2	1	0
R W	MEMB							
Default	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Notes
67. Read: Anytime
Write: Anytime

Table 111. MEMB field descriptions

Field	Description
7:0 MEMB	**Memory bank B** — This register is maintained in case of a main battery loss as long as the coin cell is present. The contents of the embedded memory are reset by COINPORB.

6.6.5.3.17 Embedded memory register C (MEMC)

Table 112. Embedded memory register C (MEMC)

Address: 0x1E Functional Page **Access: User read/write** [68]

	7	6	5	4	3	2	1	0
R W	MEMC							
Default	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Notes
68. Read: Anytime
Write: Anytime

Table 113. MEMC field descriptions

Field	Description
7:0 MEMC	**Memory bank C** — This register is maintained in case of a main battery loss as long as the coin cell is present. The contents of the embedded memory are reset by COINPORB.

6.6.5.3.18 Embedded memory register D (MEMD)

Table 114. Embedded memory register D (MEMD)

Address: 0x1F functional page **Access: User read/write [69]**

	7	6	5	4	3	2	1	0
R W	MEMD							
Default	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Notes
69. Read: Anytime
Write: Anytime

Table 115. MEMD field descriptions

Field	Description
7:0 MEMD	**Memory bank D** — This register is maintained in case of a main battery loss as long as the coin cell is present. The contents of the embedded memory are reset by COINPORB.

6.6.5.3.19 SW1 voltage control register (SW1VOLT)

This register is used to set the output voltage of the SW1 regulator in normal operation.

Table 116. SW1 voltage control register (SW1VOLT)

Address: 0x20 functional page **Access: User read/write [70]**

	7	6	5	4	3	2	1	0
R W				SW1				
Default	0	0	0	X [71]	X [71]	X [71]	X [71]	X [71]

= Unimplemented or Reserved

Notes
70. Read: Anytime
Write: Anytime
71. Default value depends on OTP content.

Table 117. SW1VOLT field descriptions

Field	Description
4:0 SW1	**SW1 output voltage** — Refer to Table 40

6.6.5.3.20 SW1 switching mode selector register (SW1MODE)

This register is used to set the switching mode of the SW1 regulator.

Table 118. SW1 switching mode selector register (SW1MODE)

Address: 0x23 functional page					Access: User read/write [72]			
	7	6	5	4	3	2	1	0
R W					SW1MODE			
Default	0	0	0	0	X [73]	X [73]	X [73]	X [73]

= Unimplemented or Reserved

Notes
72. Read: Anytime
Write: Anytime
73. Default value depends on start-up sequence.

Table 119. SW1MODE field descriptions

Field	Description
3:0 SW1MODE	**SW1 switching mode selector** — Refer to Table 36

6.6.5.3.21 SW1 configuration register (SW1CONF)

This register is used to configure DVS, switching frequency, phase and current limit settings of the SW1 regulator.

Table 120. SW1 configuration register (SW1CONF)

Address: 0x24 functional page					Access: User read/write [74]			
	7	6	5	4	3	2	1	0
R W			SW1PHASE		SW1FREQ			SW1ILIM
Default	0	0	0	0	X [75]	X [75]	0	0

= Unimplemented or Reserved

Notes
74. Read: Anytime
Write: Anytime
75. Default value depends on OTP content.

Table 121. SW1CONF field descriptions

Field	Description
5:4 SW1PHASE	**SW1 phase clock bit**— SW1PHASE is used to set the phase clock for SW1. Refer to Table 37.
3:2 SW1FREQ	**SW1 switching frequency**— SW1PHASE is used to set the desired switching frequency for SW1. Refer to Table 39.
0 SW1ILIM	**SW1 current limiter bit**— This bit configures the current limit for SW1. 0 2.75 A (typ). 1 2.0 A (typ).

6.6.5.3.22 SW2 voltage control register (SW2VOLT)

This register is used to set the output voltage of the SW2 regulator in normal operation.

Table 122. SW2 voltage control register (SW2VOLT)

Address: 0x35 functional page **Access: User read/write [76]**

	7	6	5	4	3	2	1	0
R W				SW2				
Default	0	0	0	X [77]	X [77]	X [77]	X [77]	X [77]

= Unimplemented or Reserved

Notes
76. Read: Anytime
Write: Anytime
77. Default value depends on start-up sequence.

Table 123. SW2VOLT field descriptions

Field	Description
4:0 SW2	**SW2 output voltage** — Refer to Table 42.

6.6.5.3.23 SW2 switching mode selector register (SW2MODE)

This register is used to set the switching mode of the SW2 regulator.

Table 124. SW2 switching mode selector register (SW2MODE)

Address: 0x38 functional page **Access: User read/write [78]**

	7	6	5	4	3	2	1	0
R W					SW2MODE			
Default	0	0	0	0	X [79]	X [79]	X [79]	X [79]

= Unimplemented or Reserved

Notes
78. Read: Anytime
Write: Anytime
79. Default value depends on start-up sequence.

Table 125. SW2MODE field descriptions

Field	Description
3:0 SW2MODE	**SW2 switching mode selector** — Refer to Table 36.

6.6.5.3.24 SW2 configuration register (SW2CONF)

This register is used to configure DVS, switching frequency, phase and current limit settings of the SW2 regulator.

Table 126. SW2 configuration register (SW2CONF)

Address: 0x39 functional page **Access: User read/write [80]**

	7	6	5	4	3	2	1	0
R W			SW2PHASE		SW2FREQ			SW2ILIM
Default	0	0	0	0	X [81]	X [81]	0	0

= Unimplemented or Reserved

Notes
80. Read: Anytime
Write: Anytime
81. Default value depends on OTP content.

Table 127. SW2CONF field descriptions

Field	Description
5:4 SW2PHASE	**SW2 phase clock bit**— SW2PHASE is used to set the phase clock for SW2. Refer to Table 37.
3:2 SW2FREQ	**SW2 switching frequency**— SW2PHASE is used to set the desired switching frequency for SW2. Refer to Table 39.
0 SW2ILIM	**SW2 current limiter bit**— This bit configures the current limit for SW2. 0 2.75 A (typ). 1 2.0 A (typ).

6.6.5.3.25 SW3 voltage control register (SW3VOLT)

This register is used to set the output voltage of the SW3 regulator in normal operation.

Table 128. SW3 voltage control register (SW3VOLT)

Address: 0x3C functional page **Access: User read/write [82]**

	7	6	5	4	3	2	1	0
R W				SW3				
Default	0	0	0	X [83]	X [83]	X [83]	X [83]	X [83]

= Unimplemented or Reserved

Notes
82. Read: Anytime
Write: Anytime
83. Default value depends on start-up sequence.

Table 129. SW3VOLT field descriptions

Field	Description
4:0 SW3	**SW3 output voltage** — Refer to Table 44.

6.6.5.3.26 SW3 switching mode selector register (SW3MODE)

This register is used to set the switching mode of the SW3 regulator.

Table 130. SW3 switching mode selector register (SW3MODE)

Address: 0x3F functional page					Access: User read/write [84]			
	7	6	5	4	3	2	1	0
R W					SW3MODE			
Default	0	0	0	0	X [85]	X [85]	X [85]	X [85]

= Unimplemented or Reserved

Notes
84. Read: Anytime
Write: Anytime
85. Default value depends on start-up sequence.

Table 131. SW3MODE field descriptions

Field	Description
3:0 SW3MODE	**SW3 switching mode selector** — Refer to Table 36.

6.6.5.3.27 SW3 configuration register (SW3CONF)

This register is used to configure DVS, switching frequency, phase and current limit settings of the SW3 regulator.

Table 132. SW3 configuration register (SW3CONF)

Address: 0x40 functional page					Access: User read/write [86]			
	7	6	5	4	3	2	1	0
R W			SW3PHASE		SW3FREQ			SW3ILIM
Default	0	0	1	0	X [87]	X [87]	0	0

= Unimplemented or Reserved

Notes
86. Read: Anytime
Write: Anytime
87. Default value depends on OTP content.

Table 133. SW3CONF field descriptions

Field	Description
5:4 SW3PHASE	**SW3 phase clock bit**— SW3PHASE is used to set the phase clock for SW3. Refer to Table 37.
3:2 SW3FREQ	**SW3 switching frequency**— SW3PHASE is used to set the desired switching frequency for SW3. Refer to Table 39.
0 SW3ILIM	**SW3 current limiter bit**— This bit configures the current limit for SW3. 0 3.0 A (typ). 1 2.25 A (typ).

6.6.5.3.28 VSNVS control register (VSNVSCTL)

This register is used to control the VSNVS supply operation.

Table 134. VSNVS control register (VSNVSCTL)

Address: 0x6B functional page					Access: User read/write [88]			
	7	6	5	4	3	2	1	0
R W						VSNVSVOLT		
Default	0	0	0	0	0	X [89]	X [89]	X [89]

= Unimplemented or Reserved

Notes
88. Read: Anytime
Write: Anytime
89. Default value depends on start-up sequence.

Table 135. VSNVSCTL field descriptions

Field	Description
2:0 VSNVSVOLT	**VSNVS output voltage configuration**— VSNVSVOLT is used to configure the VSNVS output voltage. Values below are typical voltages. 000 = RSVD 001 = RSVD 010 = RSVD 011 = RSVD 100 = RSVD 101 = RSVD 110 = 3.0 V (default) 111 = RSVD

6.6.5.3.29 VLDO1 control register (VLDO1CTL)

This register is used to configure output voltage, normal mode operation of the VLDO1 regulator.

Table 136. VLDO1 control register (VLDO1CTL)

Address: 0x6C functional page					Access: User read/write [90]			
	7	6	5	4	3	2	1	0
R W				VLDO1EN	VLDO1			
Default	0	0	0	X [91]	X [91]	X [91]	X [91]	X [91]

= Unimplemented or Reserved

Notes
90. Read: Anytime
Write: Anytime
91. Default value depends on start-up sequence.

Table 137. VLDO1CTL field descriptions

Field	Description
4 VLDO1EN	**VLDO1 enable bit** — VLDO1EN is used to enable or disable the VLDO1 regulator. 0 VLDO1 disabled 1 VLDO1 enabled
3:0 VLDO1	**VLDO1 output voltage configuration**— Refer to Table 47.

6.6.5.3.30 VLDO2 control register (VLDO2CTL)

This register is used to configure output voltage, normal mode operation of the VLDO2 regulator.

Table 138. VLDO2 control register (VLDO2CTL)

Address: 0x6D functional page **Access: User read/write [92]**

	7	6	5	4	3	2	1	0
R W				VLDO2EN	VLDO2			
Default	0	0	0	X [93]	X [93]	X [93]	X [93]	X [93]

= Unimplemented or Reserved

Notes
92. Read: Anytime
Write: Anytime
93. Default value depends on start-up sequence.

Table 139. VLDO2CTL field descriptions

Field	Description
4 VLDO2EN	**VLDO2 enable bit** — VLDO2EN is used to enable or disable the VLDO2 regulator. 0 VLDO2 Disabled 1 VLDO2 Enabled
3:0 VLDO2	**VLDO2 output voltage configuration**— Refer to Table 47.

6.6.5.3.31 VCC_SD control register (VCC_SDCTL)

This register is used to configure output voltage, Normal mode operation of the VCC_SD regulator.

Table 140. CC_SD control register (VCC_SDCTL)

Address: 0x6E functional page					Access: User read/write [94]			
	7	6	5	4	3	2	1	0
R W				VCC_SDEN			VCC_SD	
Default	0	0	0	X [95]	0	0	X [95]	X [95]

= Unimplemented or Reserved

Notes
94. Read: Anytime
Write: Anytime
95. Default value depends on start-up sequence.

Table 141. VCC_SDCTL field descriptions

Field	Description
4 VCC_SDEN	**VCC_SD enable bit** — VCC_SDEN is used to enable or disable the VCC_SD regulator. 0 VCC_SD Disabled 1 VCC_SD Enabled
1:0 VCC_SD	**VCC_SD output voltage configuration**— Refer to Table 50.

6.6.5.3.32 V33 control register (V33CTL)

This register is used to configure output voltage, normal mode operation of the V33 regulator.

Table 142. V33 control register (V33CTL)

Address: 0x6F functional page					Access: User read/write [96]			
	7	6	5	4	3	2	1	0
R W				V33EN			V33	
Default	0	0	0	X [97]	0	0	X [97]	X [97]

= Unimplemented or Reserved

Notes
96. Read: Anytime
Write: Anytime
97. Default value depends on start-up sequence.

Table 143. V33CTL field descriptions

Field	Description
4 V33EN	**V33 enable bit** — V33EN is used to enable or disable the VLDO2 regulator. 0 V33 Disabled 1 V33 Enabled
1:0 V33	**V33 output voltage configuration**— Refer to Table 49.

6.6.5.3.33 VLDO3 control register (VLDO3CTL)

This register is used to configure output voltage, normal mode operation of the VLDO3 regulator.

Table 144. VLDO3 control register (VLDO3CTL)

Address: 0x70 functional page **Access: User read/write [98]**

	7	6	5	4	3	2	1	0
R W				VLDO3EN	VLDO3			
Default	0	0	0	X [99]	X [99]	X [99]	X [99]	X [99]

= Unimplemented or Reserved

Notes
98. Read: Anytime
Write: Anytime
99. Default value depends on start-up sequence.

Table 145. VLDO3CTL field descriptions

Field	Description
4 VLDO3EN	**VLDO3 enable bit** — VLDO3EN is used to enable or disable the VLDO3 regulator. 0 VLDO3 Disabled 1 VLDO3 Enabled
3:0 VLDO3	**VLDO3 output voltage configuration**— Refer to Table 48.

6.6.5.3.34 VLDO4 control register (VLDO4CTL)

This register is used to configure output voltage, normal mode operation of the VLDO4 regulator.

Table 146. VLDO4 control register (VLDO4CTL)

Address: 0x71 functional page **Access: User read/write [100]**

	7	6	5	4	3	2	1	0
R W				VLDO4EN	VLDO4			
Default	0	0	0	X [101]	X [101]	X [101]	X [101]	X [101]

= Unimplemented or Reserved

Notes
100. Read: Anytime
Write: Anytime
101. Default value depends on start-up sequence.

Table 147. VLDO4CTL field descriptions

Field	Description
4 VLDO4EN	**VLDO4 enable bit** — VLDO4EN is used to enable or disable the VLDO4 regulator. 0 VLDO4 Disabled 1 VLDO4 Enabled
3:0 VLDO4	**VLDO4 output voltage configuration**— Refer to Table 48.

6.6.5.3.35 Page selection register

This register is used to access the extended register pages.

Table 148. Page selection register

Address: 0x7F functional page **Access: User read/write** [102]

	7	6	5	4	3	2	1	0
R W					PAGE			
Default	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Notes
102. Read: Anytime
Write: Anytime

Table 149. Page register field descriptions

Field	Description
3:0 PAGE	**Register page selection** — The PAGE field is used to select the register pages. 0000 Functional page selected

6.6.6 Register map

The register map is only one page and its addresses and data fields are each eight bits wide. This page registers 0x00 to 0x7F are referred to as “functional”.

Registers missing in the sequence are reserved; reading from them returns a value 0x00, and writing to them has no effect. The contents of all registers are given in the tables defined in this chapter; each table is structure as follows:

Name: Name of the bit

Bit #: The bit location in the register (7-0)

R/W: Read/Write access and control

- R is read-only access
- R/W is read and write access
- RW1C is read and write access with write 1 to clear

Reset: Reset signals are color coded based on the following legend.

Bits reset by SC and VCOREDIG_PORB
Bits reset by PWRON or loaded default
Bits reset by DIGRESETB
Bits reset by PORB or RESETBMCU
Bits reset by VCOREDIG_PORB
Bits reset by POR or OFFB

Default: The value after reset, as noted in the default column of the memory map.

- Fixed defaults are explicitly declared as 0 or 1.
- “X” corresponds to Read/Write bits initialized at start-up. Bits are subsequently I^2C modifiable, when their reset has been released. “X”, may also refer to bits which may have other dependencies. For example, some bits may depend on the version of the IC, or a value from an analog block, for instance the sense bits for the interrupts.

6.6.6.1 Register map

Table 150. Functional page

				BITS[7:0]							
Add	**Register Name**	**R/W**	**Default**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00	DeviceID	R	8'b0011_0000	–	–	–	–	DEVICE ID [3:0]			
				0	0	1	1	0	0	0	1
03	SILICONREVID	R	8'b0001_0000	FULL_LAYER_REV[3:0]				METAL_LAYER_REV[3:0]			
				0	0	0	1	0	0	0	0
04	FABID	R	8'b0000_0000	–	–	–	–	FAB[1:0]		FIN[1:0]	
				0	0	0	0	0	0	0	0
05	INTSTAT0	RW1C	8'b0000_0000	–	–	THERM130I	THERM125I	THERM120I	THERM110I	LOWVINI	PWRONI
				0	0	0	0	0	0	0	0
06	INTMASK0	R/W	8'b0011_1111	–	–	THERM130M	THERM125M	THERM120M	THERM110M	LOWVINM	PWRONM
				0	0	1	1	1	1	1	1
07	INTSENSE0	R	8'b00xx_xxxx	ICTEST2S	ICTESTS	THERM130S	THERM125S	THERM120S	THERM110S	LOWVINS	PWRONS
				0	0	x	x	x	x	x	x
08	INTSTAT1	RW1C	8'b0000_0000	–	–	–	SW3FAULTI	SW2FAULTI	–	–	SW1FAULTI
				0	0	0	0	0	x	0	0

Table 150. Functional page (continued)

				BITS[7:0]							
Add	**Register Name**	**R/W**	**Default**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
09	INTMASK1	R/W	8'b0111_1111	–	–	–	SW3FAULTM	SW2FAULTM	–	–	SW1FAULTM
				0	1	1	1	1	1	1	1
0A	INTSENSE1	R	8'b0xxx_xxxx	–	–	–	SW3FAULTS	SW2FAULTS	–	–	SW1FAULTS
				0	x	x	x	x	x	x	x
0E	INTSTAT3	RW1C	8'b0000_0000	–	–	–	–	–	VPWROVI	–	–
				0	0	0	0	0	0	0	0
0F	INTMASK3	R/W	8'b1100_0101	–	–	–	–	–	VPWROVI	–	–
				1	1	0	0	0	1	0	1
10	INTSENSE3	R	8'b0000_000x	–	–	–	–	–	VPWROVS	–	–
				0	0	0	0	0	0	0	x
11	INTSTAT4	RW1C	8'b0000_0000	–	–	VLDO4FAULTI	VLDO3FAULTI	V33FAULTI	VCC_SDFAULTI	VLDO2FAULTI	VLDO1FAULTI
				0	0	0	0	0	0	0	0
12	INTMASK4	R/W	8'b0011_1111	–	–	VLDO4 FAULTM	VLDO3 FAULTM	V33 FAULTM	VCC_SDFAULTM	VLDO2FAULTM	VLDO1FAULTM
				0	0	1	1	1	1	1	1
13	INTSENSE4	R	8'b00xx_xxxx	–	–	VLDO4 FAULTS	VLDO3 FAULTS	V33 FAULTS	VCC_SD FAULTS	VLDO2 FAULTS	VLDO1 FAULTS
				0	0	x	x	x	x	x	x
1A	COINCTL	R/W	8'b0000_0000	–	–	–	–	COINCHEN	VCOIN[2:0]		
				0	0	0	0	0	0	0	0
1B	PWRCTL	R/W	8'b0001_0000	REGSCPEN	–	–		PWRONBDBNC[1:0]		PWRONRSTEN	RESTARTEN
				0	0	0	1	0	0	0	0
1C	MEMA	R/W	8'b0000_0000	MEMA[7:0]							
				0	0	0	0	0	0	0	0
1D	MEMB	R/W	8'b0000_0000	MEMB[7:0]							
				0	0	0	0	0	0	0	0
1E	MEMC	R/W	8'b0000_0000	MEMC[7:0]							
				0	0	0	0	0	0	0	0
1F	MEMD	R/W	8'b0000_0000	MEMD[7:0]							
				0	0	0	0	0	0	0	0
20	SW1VOLT	R/W	8'b000x_xxxx	–	–	–	SW1[4:0]				
				0	0	0	–	–	–	–	–
21	SW1STBY	R/W	8'b000x_xxxx	–	–	–	–	–	–	–	–
				0	0	0	–	–	–	–	–
22	SW1OFF	R/W	8'b000x_xxxx	–	–	–	–	–	–	–	–
				0	0	0	–	–	–	–	–
23	SW1MODE	R/W	8'b0000_xxxx	–	–	–	–	SW1MODE[3:0]			
				0	0	0	x	–	–	–	–

Table 150. Functional page (continued)

				BITS[7:0]							
Add	**Register Name**	**R/W**	**Default**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
24	SW1CONF	R/W	8'bxx00_xxx0	–	–	SW1PHASE[1:0]		SW1FREQ[1:0]		–	SW1ILIM
				x	x	0	0	x	x	x	0
2E	RSVD	R/W	8'b0000_0000	–	–	–	–				
				x	x	x	x	x	x	x	x
2F	RSVD	R/W	8'b0000_0000	–	–	–	–				
				x	x	x	x	x	x	x	x
30	RSVD	R/W	8'b0000_0000	–	–	–	–				
				x	x	x	x	x	x	x	x
31	RSVD	R/W	8'b0001_0000	–	–	–	–	–			
				x	x	0	–	–	–	–	–
32	RSVD	R/W	8'bx100_0000	–	–	–		–		–	–
				x	–	x	x	–	–	x	x
35	SW2VOLT	R/W	8'b0xxx_0110	–	–	–	–	SW2_HL	SW2[2:0]		
				0	x	x	x	–	–	–	—
36	SW2STBY	R/W	8'b0xxx_xxxx	–	–	–	–	–	–	–	–
				0	x	x	x	x	x	x	x
37	SW2OFF	R/W	8'b0xxx_xxxx	–	–	–	–	–	–	–	–
				0	x	x	x	x	x	x	x
38	SW2MODE	R/W	8'b0010_1000	–	–	–	–	SW2MODE[3:0]			
				0	0	0	0	1	0	0	0
39	SW2CONF	R/W	8'bxx01_xxx0	–	–	SW2PHASE[1:0]		SW2FREQ[1:0]		–	SW2ILIM
				x	x	0	1	x	x	x	0
3C	SW3VOLT	R/W	8'b0xxx_1100	–	–	–	–	SW3[3:0]			
				0	x	x	x	–	–	–	–
3D	RSVD	R/W	8'b0xxx_1100	–	–	–	–	–	–	–	–
				0	x	x	x	–	–	–	–
3E	RSVD	R/W	8'b0xxx_1100	–	–	–	–	–	–	–	–
				0	x	–	x	–	–	–	–
3F	SW3MODE	R/W	8'b0011_1000	–	–	0	–	SW3MODE[3:0]			
				0	0	1	1	1	0	0	0
40	SW3CONF	R/W	8'bxx10_xxx0	–	–	SW3PHASE[1:0]		SW3FREQ[1:0]		–	SW3ILIM
				x	–	1	0	–	–	0	0
66	RSVD	R/W	8'b0xx0_0000	–	–		–	–		–	
				0	x	x	0	x	x	x	x
69	RSVD	R/W	8'b0xxx_xxx0	–	–	–	–	–	–	–	–
				0	x	x	x	x	x	x	x
6A	RSVD	R/W	8'b000x_0000	–	–	–	–	–	–	–	–
				x	x	x	–	x	x	x	x

Table 150. Functional page (continued)

				BITS[7:0]							
Add	**Register Name**	**R/W**	**Default**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
6B	VSNVSCTL	R/W	8'b0000_0110	–	–	–	–	–	VSNVSVOLT[2:0]		
				0	0	0	0	0	1	1	0
6C	VLDO1CTL	R/W	8'b010x_1110	–	–	–	VLDO1EN	VLDO1[3:0]			
				0	0	0	–	–	–	–	—
6D	VLDO2CTL	R/W	8'b000x_1000	–	–	–	VLDO2EN	VLDO2[3:0]			
				0	0	0	–	–	–	–	—
6E	VCC_SDCTL	R/W	8'b000x_xx10	–	–	–	VCC_SDEN	–	–	VCC_SD[1:0]	
				0	0	0	–	x	x	–	–
6F	V33CTL	R/W	8'b000x_xx10	–	–	–	V33EN	–	–	V33[1:0]	
				0	0	0	–	x	x	–	–
70	VLDO3CTL	R/W	8'b010x_0000	–	–	–	VLDO3EN	VLDO3[3:0]			
				0	0	0	–	–	–	–	–
71	VLDO4CTL	R/W	8'b000x_xxxx	–	–	–	VLDO4EN	VLDO4[3:0]			
				0	0	0	–	–	–	–	–
7F	RSVD	R/W	8'b0000_0000	–	–	–	–				
				0	0	0	0	0	0	0	0

7 Typical applications

7.1 Application diagram

Figure 26. Typical application schematic

8 Bill of materials

The following table provides a complete list of the recommended components on a full featured system using the PF3001 Critical components are provided with a recommended part number; but equivalent components may be used.

Table 151. Bill of materials for -40 °C to 85 °C applications [(103)]

Value	Qty	Description	Part#	Manufacturer	Component/pin
PMIC					
N/A	1	Power management IC	PF3001	NXP	IC
Buck regulators					
1.5 µH	3	IND PWR 1.5 µH at 1.0 MHz 2.9A 20% 2016	DFE252012P-1R5M	Toko Inc.	SW1, SW2, SW3 inductors
		IND PWR 1.5 µH at 1.0 MHz 2.2A 20% 1210	BRL3225T1R5M	Taiyo Yuden	Alternate for low power applications
4.7 µF	3	CAP CER 4.7 µF 10 V 20% X5R 0402	GRM155R61A475MEAA	Murata	SW1, SW2, SW3 input capacitors
0.1 µF	3	CAP CER 0.1 µF 10 V 20% X5R 0603	GRM033R61A104ME84	Murata	SW1, SW2, SW3 input capacitors (optional)
22 µF	6	CAP CER 22 µF 10 V 20% X5R 0201	GRM188R61A226ME15	Murata	SW1, SW2, SW3 output capacitors
Linear regulators					
1.0 µF	3	CAP CER 1.0 µF 10 V 20% X5R 0201	GRM033R61A105ME44	Murata	VLDO1, VLDO2, VLDO3, and VLDO4 input capacitors
2.2 µF	3	CAP CER 2.2 µF 10V 20% X5R 0201	GRM033R61A225ME47	Murata	VLDO1, VLDO3, VCC_SD output capacitors
10 µF	1	CAP CER 10 µF 10 V 20% X7R 0402	GRM155R61A106ME11	Murata	V33 and VCC_SD input capacitor
4.7 µF	3	CAP CER 4.7 µF 10V 20% X5R 0402	GRM155R61A475MEAA	Murata	VLDO2, VLDO4, V33 output capacitors
Miscellaneous					
1.0 µF	4	CAP CER 1.0 µF 10V 20% X5R 0201	GRM033R61A105ME44	Murata	VCORE, VCOREDIG, capacitors
0.22 µF	2	CAP CER 0.22 µF 10V 20% X5R 0201	GRM033R61A224ME90	Murata	VCOREREF and coin cell output capacitors
47 µF	4	CAP CER 47 µF 10V 20% X5R 0805	GRM21BR61A476ME15	Murata	Front-end LDO capacitors for VIN and VPWR
2.2 µF	1	CAP CER 2.2 µF 10V 20% X5R 0201	GRM033R61A225ME47	Murata	VIN Input Capacitor when not using front-end LDO
0.1 µF	4	CAP CER 0.1 µF 10V 10% X5R 0201	GRM033R61A104KE84	Murata	VPWR, VIN Input capacitors (optional)
N/A	1	TRAN PMOS 11. A 12 V 12 SOT-1220	PMPB15XP	NXP	External MOSFET
100 k	2	RES MF 100K 1/16W 1% 0402	RC0402FR-07100KL	Yageo America	Pull-up resistor
4.7 k	2	RES MF 4.70K 1/20W 1% 0201	RC0201FR-074K7L	Yageo America	Pull-up resistor

Notes

103. NXP does not assume liability, endorse, or warrant components from external manufacturers are referenced in circuit drawings or tables. While NXP offers component recommendations in this configuration, it is the customer's responsibility to validate their application.

Table 152. Bill of materials for -40 °C to 105 °C applications [104]

Value	Qty	Description	Part#	Manufacturer	Component/pin
PMIC					
N/A	1	Power management IC	PF3000	NXP	IC
Buck regulators					
1.5 µH	3	IND PWR 1.5µH@1MHz 2.9A 20% 2016	DFE201610E-1R5M	TOKO INC.	SW1, SW2, SW3 inductors
		IND PWR 1.5µH@1MHz 2.2A 20% 1210	BRL3225T1R5M	Taiyo Yuden	Alternate for low power applications
4.7 µF	3	CAP CER 4.7µF 10V 10% X7S 0603	GRM188C71A475KE11	Murata	SW1, SW2, SW3 input capacitors
0.1 µF	3	CAP CER 0.1µF 10V 10% X7S 0201	GRM033C71A104KE14	Murata	SW1, SW2, SW3 input capacitors (optional)
22 µF	6	CAP CER 22µF 10V 20% X7T 0805	GRM21BD71A226ME44	Murata	SW1, SW2, SW3 output capacitors
Linear regulators					
1.0 µF	3	CAP CER 1.0µF 10V 10% X7S 0402	GRM155C71A105KE11	Murata	VLDO1, VLDO2, VLDO3 and VLDO4 input capacitors
2.2 µF	3	CAP CER 2.2µF 10V 10% X7S 0402	GRM155C71A225KE11	Murata	VLDO1, VLDO3, VCC_SD output capacitors
10 µF	1	CAP CER 10µF 10V 20% X7T 0603	GRM188D71A106MA73	Murata	V33 and VCC_SD input capacitor
4.7 µF	3	CAP CER 4.7µF 10V 10% X7S 0603	GRM188C71A475KE11	Murata	VLDO2, VLDO4, V33 output capacitors
1.0 µF	4	CAP CER 1.0µF 10V 10% X7R 0402	GRM155C71A105KE11	Murata	VCORE, VCOREDIG capacitors
0.22 µF	2	CAP CER 0.22µF 10V 10% X7R 0402	GRM155R71A224KE01	Murata	VCOREREF and coin cell output capacitors
47 µF	4	CAP CER 47µF 10V 20% X7R 1210	GRM32ER71A476ME15	Murata	Front-end LDO capacitors for VIN and VPWR.
2.2 µF	1	CAP CER 2.2µF 10V 10% X7S 0402	GRM155C71A225KE11	Murata	VIN Input Capacitor when not using front-end LDO
0.1 µF	4	CAP CER 0.1µF 10V 10% X7S 0201	GRM033C71A104KE14	Murata	VPWR, VIN input capacitors (optional)
N/A	1	TRAN PMOS 11. A 12 V 12 SOT-1220	PMPB15XP	NXP	External MOSFET
100 k	2	RES MF 100K 1/16W 1% 0402	RC0402FR-07100KL	YAGEO AMERICA	Pull-up resistors
4.7 k	2	RES MF 4.70K 1/20W 1% 0201	RC0201FR-074K7L	YAGEO AMERICA	I²C pull-up resistors

Notes

104. NXP does not assume liability, endorse, or warrant components from external manufacturers are referenced in circuit drawings or tables. While NXP offers component recommendations in this configuration, it is the customer's responsibility to validate their application.

9 Thermal information

9.1 Rating data

The thermal rating data of the packages has been simulated with the results listed in Thermal ratings. Junction to ambient thermal resistance nomenclature: the JEDEC specification reserves the symbol $R_{\theta JA}$ or θJA (Theta-JA) strictly for junction-to-ambient thermal resistance on a 1s test board in natural convection environment. $R_{\theta JMA}$ or θJMA (Theta-JMA) is used for both junction-to-ambient on a 2s2p test board in natural convection and for junction-to-ambient with forced convection on both 1s and 2s2p test boards. It is anticipated the generic name, Theta-JA, continues to be commonly used. The JEDEC standards can be consulted at http://www.jedec.org.

9.2 Estimation of junction temperature

An estimation of the chip junction temperature T_J can be obtained from the equation:

$T_J = T_A + (R_{\theta JA} \times P_D)$

with:

T_A = Ambient temperature for the package in °C

$R_{\theta JA}$ = Junction to ambient thermal resistance in °C/W

P_D = Power dissipation in the package in W

The junction to ambient thermal resistance is an industry standard value providing a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board $R_{\theta JA}$ and the value obtained on a four layer board $R_{\theta JMA}$. Actual application PCBs show a performance close to the simulated four layer board value although this may be somewhat degraded in case of significant power dissipated by other components placed close to the device.

At a known board temperature, the junction temperature T_J is estimated using the following equation

$T_J = T_B + (R_{\theta JB} \times P_D)$ with

T_B = Board temperature at the package perimeter in °C

$R_{\theta JB}$ = Junction to board thermal resistance in °C/W

P_D = Power dissipation in the package in W

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made.

10 Packaging

10.1 Packaging dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number. See the Thermal characteristics section for specific thermal characteristics for each package.

Table 153. Package drawing information

Package	Suffix	Package outline drawing number
48-pin QFN 7X7 mm - 0.5mm pitch	EP	98ASA00719D
48 QFN 7.0 mm x 7.0 mm WF-type (wettable flank)	EP	98ASA00933D

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: QFN, THERMALLY ENHANCED, 7 X 7 X 0.85, 0.5 PITCH, 48 TERMINAL	DOCUMENT NO: 98ASA00719D	REV: B
	STANDARD: NON-JEDEC	
		27 JUN 2014

PF3001

DETAIL G
VIEW ROTATED 90°CW

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	STANDARD: NON-JEDEC	
		27 JUN 2014

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THIS IS A NON–JEDEC REGISTERED PACKAGE.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.
5. DIMENSION APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.3 MM FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

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TITLE: QFN, THERMALLY ENHANCED, 7 X 7 X 0.85, 0.5 PITCH, 48 TERMINAL	DOCUMENT NO: 98ASA00719D	REV: B
	STANDARD: NON–JEDEC	
		27 JUN 2014

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TITLE: QFN, THERMALLY ENHANCED, 7 X 7 X 0.85, 0.5 PITCH, 48 TERMINAL	DOCUMENT NO: 98ASA00933D	REV: O
	STANDARD: NON-JEDEC	
		23 SEP 2015

DETAIL G
VIEW ROTATED 90°CW

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TITLE: QFN, THERMALLY ENHANCED, 7 X 7 X 0.85, 0.5 PITCH, 48 TERMINAL	DOCUMENT NO: 98ASA00933D	REV: O
	STANDARD: NON-JEDEC	
		23 SEP 2015

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THIS IS A NON–JEDEC REGISTERED PACKAGE.
4. COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.
5. MIN METAL GAP SHOULD BE 0.2 MM.

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TITLE: QFN, THERMALLY ENHANCED, 7 X 7 X 0.85, 0.5 PITCH, 48 TERMINAL	DOCUMENT NO: 98ASA00933D	REV: O
	STANDARD: NON–JEDEC	
		23 SEP 2015

11 Revision history

Revision	Date	Description of Changes
1.0	8/2015	• Initial release
	9/2015	• Corrected package image on page 1
2.0	3/2016	• Added 98ASA00933D and the page 1 package image for wettable flank • Changed Table 2, pins 7, 10, 18, and 28, from Bypass with at least a 10 µF to Bypass with at least a 4.7 µF • Added PC33PF3001A6ES and PC33PF3001A7ES to Table 1
	8/2016	• Changed PC33PF3001A6ES and PC33PF3001A7ES to MC parts in Table 1
3.0	4/2017	• Corrected typo in Figure 1 • Updated Table 62 (changed default value to 1)
4.0	8/2017	• Updated notes (37) and (38) as per CIN 201707041I

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