# MC74LCX540

# Low-Voltage CMOS Octal Buffer Flow Through Pinout

## With 5 V−Tolerant Inputs and Outputs (3−State, Inverting)

The MC74LCX540 is a high performance, inverting octal buffer operating from a 2.3 to 3.6 V supply. This device is similar in function to the MC74LCX240, while providing flow through architecture. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A $V_I$ specification of 5.5 V allows MC74LCX540 inputs to be safely driven from 5 V devices. The MC74LCX540 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

Current drive capability is 24 mA at the outputs. The Output Enable ($\overline{OE1}$, $\overline{OE2}$) inputs, when HIGH, disables the outputs by placing them in a HIGH Z condition.

### Features

- Designed for 2.3 to 3.6 V $V_{CC}$ Operation
- 5 V Tolerant − Interface Capability With 5 V TTL Logic
- Supports Live Insertion and Withdrawal
- $I_{OFF}$ Specification Guarantees High Impedance When $V_{CC}$ = 0 V
- LVTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10 μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500 mA
- ESD Performance:
  - Human Body Model >2000 V
  - Machine Model >200 V
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

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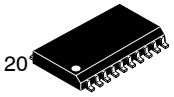
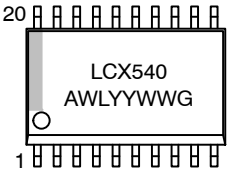
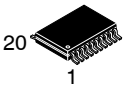
**MARKING DIAGRAMS**

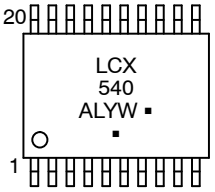



**SOIC−20 WB**
**DW SUFFIX**
**CASE 751D**




**TSSOP−20**
**DT SUFFIX**
**CASE 948E**




| | | |
|---|---|---|
| A | = | Assembly Location |
| L, WL | = | Wafer Lot |
| Y, YY | = | Year |
| W, WW | = | Work Week |
| G or ▪ | = | Pb−Free Package |

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

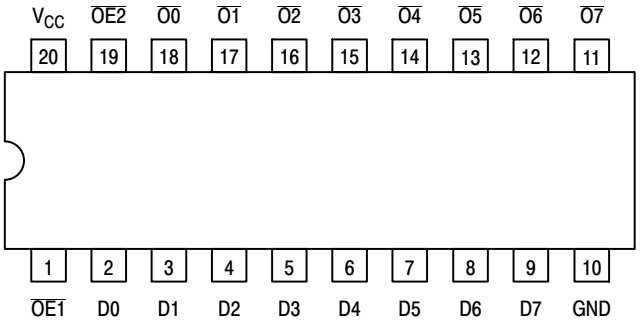



**Figure 1. Pinout: 20−Lead** (Top View)

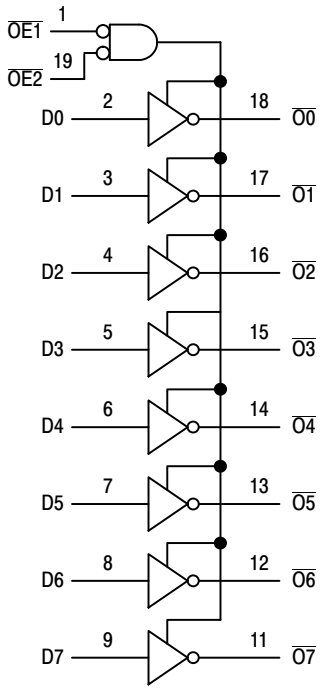



**Figure 2. Logic Diagram**

**PIN NAMES**

| Pins | Function |
|---|---|
| $\overline{OEn}$ | Output Enable Inputs |
| Dn | Data Inputs |
| $\overline{On}$ | 3−State Outputs |

**TRUTH TABLE**

| Inputs | | | Outputs |
|---|---|---|---|
| $\overline{OE1}$ | $\overline{OE2}$ | Dn | $\overline{On}$ |
| L | L | L | H |
| L | L | H | L |
| X | H | X | Z |
| H | X | X | Z |

H = High Voltage Level
L = Low Voltage Level
Z = High Impedance State
X = High or Low Voltage Level and Transitions are Acceptable
For $I_{CC}$ reasons, DO NOT FLOAT Inputs

## MAXIMUM RATINGS

| Symbol | Parameter | Condition | Value | Units |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | | −0.5 to +7.0 | V |
| $V_I$ | DC Input Voltage | | $-0.5 \le V_I \le +7.0$ | V |
| $V_O$ | DC Output Voltage | Output in 3−State | $-0.5 \le V_O \le +7.0$ | V |
| | | (Note 1) | $-0.5 \le V_O \le V_{CC} + 0.5$ | V |
| $I_{IK}$ | DC Input Diode Current | $V_I$ < GND | −50 | mA |
| $I_{OK}$ | DC Output Diode Current | $V_O$ < GND | −50 | mA |
| | | $V_O > V_{CC}$ | +50 | mA |
| $I_O$ | DC Output Source/Sink Current | | ±50 | mA |
| $I_{CC}$ | DC Supply Current Per Supply Pin | | ±100 | mA |
| $I_{GND}$ | DC Ground Current Per Ground Pin | | ±100 | mA |
| $T_{STG}$ | Storage Temperature Range | | −65 to +150 | °C |
| MSL | Moisture Sensitivity | | Level 1 | |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Output in HIGH or LOW State. $I_O$ absolute maximum rating must be observed.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage<br>Operating<br>Data Retention Only | <br>2.0<br>1.5 | <br>3.3<br>3.3 | <br>3.6<br>3.6 | V |
| $V_I$ | Input Voltage | 0 | | 5.5 | V |
| $V_O$ | Output Voltage<br>(HIGH or LOW State)<br>(3−State) | <br>0<br>0 | | <br>$V_{CC}$<br>5.5 | V |
| $I_{OH}$ | HIGH Level Output Current, $V_{CC}$ = 3.0 V − 3.6 V | | | −24 | mA |
| $I_{OL}$ | LOW Level Output Current, $V_{CC}$ = 3.0 V − 3.6 V | | | 24 | mA |
| $I_{OH}$ | HIGH Level Output Current, $V_{CC}$ = 2.7 V − 3.0 V | | | −12 | mA |
| $I_{OL}$ | LOW Level Output Current, $V_{CC}$ = 2.7 V − 3.0 V | | | 12 | mA |
| $T_A$ | Operating Free−Air Temperature | −40 | | +85 | °C |
| $\Delta t/\Delta V$ | Input Transition Rise or Fall Rate, $V_{IN}$ from 0.8 V to 2.0 V, $V_{CC}$ = 3.0 V | 0 | | 10 | ns/V |

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MC74LCX540DWR2G | SOIC−20 WB<br>(Pb−Free) | 1000 Tape & Reel |
| MC74LCX540DTG | TSSOP−20<br>(Pb−Free) | 75 Units / Rail |
| MC74LCX540DTR2G | TSSOP−20<br>(Pb−Free) | 2000 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## DC ELECTRICAL CHARACTERISTICS

| Symbol | Characteristic | Condition | $T_A$ = −40°C to +85°C | | Units |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $V_{IH}$ | HIGH Level Input Voltage (Note 2) | 2.7 V ≤ $V_{CC}$ ≤ 3.6 V | 2.0 | | V |
| $V_{IL}$ | LOW Level Input Voltage (Note 2) | 2.7 V ≤ $V_{CC}$ ≤ 3.6 V | | 0.8 | V |
| $V_{OH}$ | HIGH Level Output Voltage | 2.7 V ≤ $V_{CC}$ ≤ 3.6 V; $I_{OH}$ = −100 μA | $V_{CC}$ − 0.2 | | V |
| | | $V_{CC}$ = 2.7 V; $I_{OH}$ = −12 mA | 2.2 | | |
| | | $V_{CC}$ = 3.0 V; $I_{OH}$ = −18 mA | 2.4 | | |
| | | $V_{CC}$ = 3.0 V; $I_{OH}$ = −24 mA | 2.2 | | |
| $V_{OL}$ | LOW Level Output Voltage | 2.7 V ≤ $V_{CC}$ ≤ 3.6 V; $I_{OL}$ = 100 μA | | 0.2 | V |
| | | $V_{CC}$ = 2.7 V; $I_{OL}$ = 12 mA | | 0.4 | |
| | | $V_{CC}$ = 3.0 V; $I_{OL}$ = 16 mA | | 0.4 | |
| | | $V_{CC}$ = 3.0 V; $I_{OL}$ = 24 mA | | 0.55 | |
| $I_{OZ}$ | 3−State Output Current | $V_{CC}$ = 3.6 V, $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $V_{OUT}$ = 0 to 5.5 V | | ±5 | μA |
| $I_{OFF}$ | Power Off Leakage Current | $V_{CC}$ = 0, $V_{IN}$ = 5.5 V or $V_{OUT}$ = 5.5 V | | 10 | μA |
| $I_{IN}$ | Input Leakage Current | $V_{CC}$ = 3.6 V, $V_{IN}$ = 5.5 V or GND | | ±5 | μA |
| $I_{CC}$ | Quiescent Supply Current | $V_{CC}$ = 3.6 V, $V_{IN}$ = 5.5 V or GND | | 10 | μA |
| $\Delta I_{CC}$ | Increase in $I_{CC}$ per Input | 2.3 ≤ $V_{CC}$ ≤ 3.6 V; $V_{IH}$ = $V_{CC}$ − 0.6 V | | 500 | μA |

2. These values of $V_I$ are used to test DC electrical characteristics only.

## AC CHARACTERISTICS ($t_R$ = $t_F$ = 2.5 ns; $C_L$ = 50 pF; $R_L$ = 500 Ω)

| Symbol | Parameter | Waveform | Limits | | | Units |
|---|---|---|---|---|---|---|
| | | | $T_A$ = −40°C to +85°C | | | |
| | | | $V_{CC}$ = 3.0 V to 3.6 V | | $V_{CC}$ = 2.7 V | |
| | | | Min | Max | Max | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>Input to Output | 1 | 1.5<br>1.5 | 6.5<br>6.5 | 7.5<br>7.5 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output Enable Time to<br>High and Low Level | 2 | 1.5<br>1.5 | 8.5<br>8.5 | 9.5<br>9.5 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output Disable Time From<br>High and Low Level | 2 | 1.5<br>1.5 | 7.5<br>7.5 | 8.5<br>8.5 | ns |
| $t_{OSHL}$<br>$t_{OSLH}$ | Output−to−Output Skew (Note 3) | | | 1.0<br>1.0 | | ns |

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH−to−LOW ($t_{OSHL}$) or LOW−to−HIGH ($t_{OSLH}$); parameter guaranteed by design.

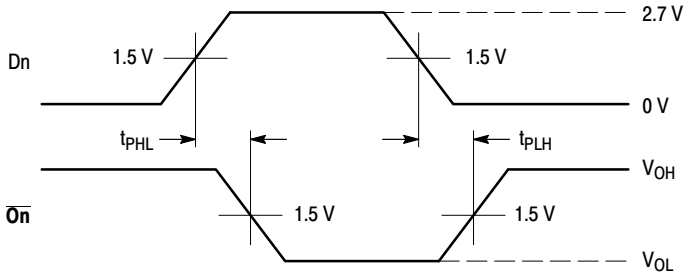
## DYNAMIC SWITCHING CHARACTERISTICS

| Symbol | Characteristic | Condition | $T_A$ = +25°C | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{OLP}$ | Dynamic LOW Peak Voltage (Note 4) | $V_{CC}$ = 3.3 V, $C_L$ = 50 pF, $V_{IH}$ = 3.3 V, $V_{IL}$ = 0 V | | 0.8 | | V |
| $V_{OLV}$ | Dynamic LOW Valley Voltage (Note 4) | $V_{CC}$ = 3.3 V, $C_L$ = 50 pF, $V_{IH}$ = 3.3 V, $V_{IL}$ = 0 V | | 0.8 | | V |

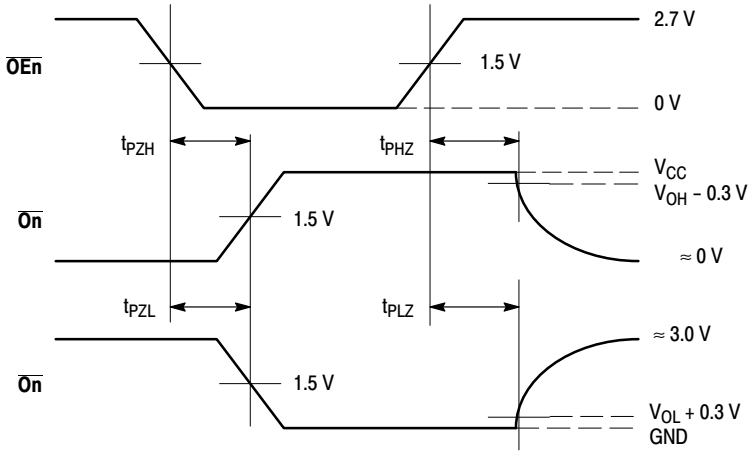
4. Number of outputs defined as “n”. Measured with “n−1” outputs switching from HIGH−to−LOW or LOW−to−HIGH. The remaining output is measured in the LOW state.

## CAPACITIVE CHARACTERISTICS

| Symbol | Parameter | Condition | Typical | Units |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{CC}$ = 3.3 V, $V_I$ = 0 V or $V_{CC}$ | 7 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{CC}$ = 3.3 V, $V_I$ = 0 V or $V_{CC}$ | 8 | pF |
| $C_{PD}$ | Power Dissipation Capacitance | 10 MHz, $V_{CC}$ = 3.3V, $V_I$ = 0 V or $V_{CC}$ | 25 | pF |

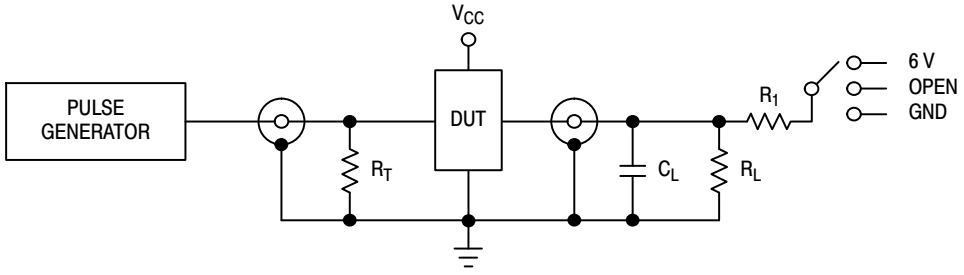



**WAVEFORM 1 – PROPAGATION DELAYS**
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1 MHz; $t_W$ = 500 ns




**WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES**
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1 MHz; $t_W$ = 500 ns

**Figure 3. AC Waveforms**



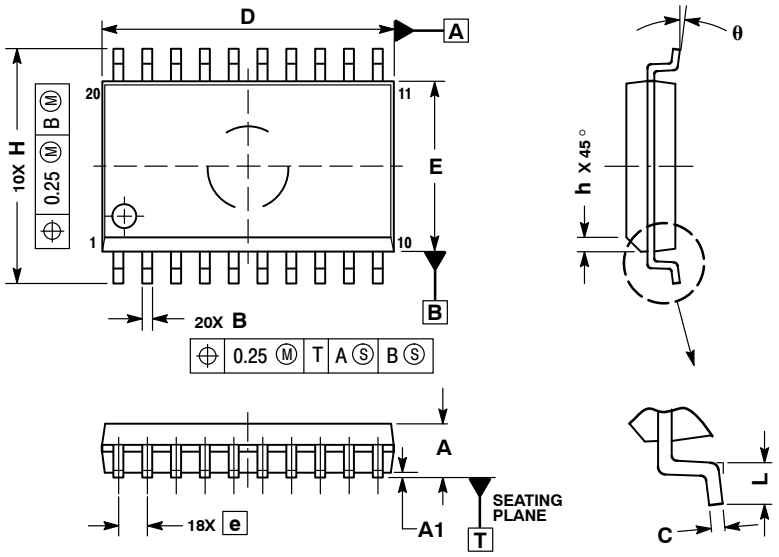

| Test | Switch |
|---|---|
| $t_{PLH}$, $t_{PHL}$ | Open |
| $t_{PZL}$, $t_{PLZ}$ | 6 V |
| Open Collector/Drain $t_{PLH}$ and $t_{PHL}$ | 6 V |
| $t_{PZH}$, $t_{PHZ}$ | GND |

$C_L$ = 50 pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1$ = 500 Ω or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50 Ω)

**Figure 4. Test Circuit**

## PACKAGE DIMENSIONS

**SOIC−20 WB**
CASE 751D−05
ISSUE G

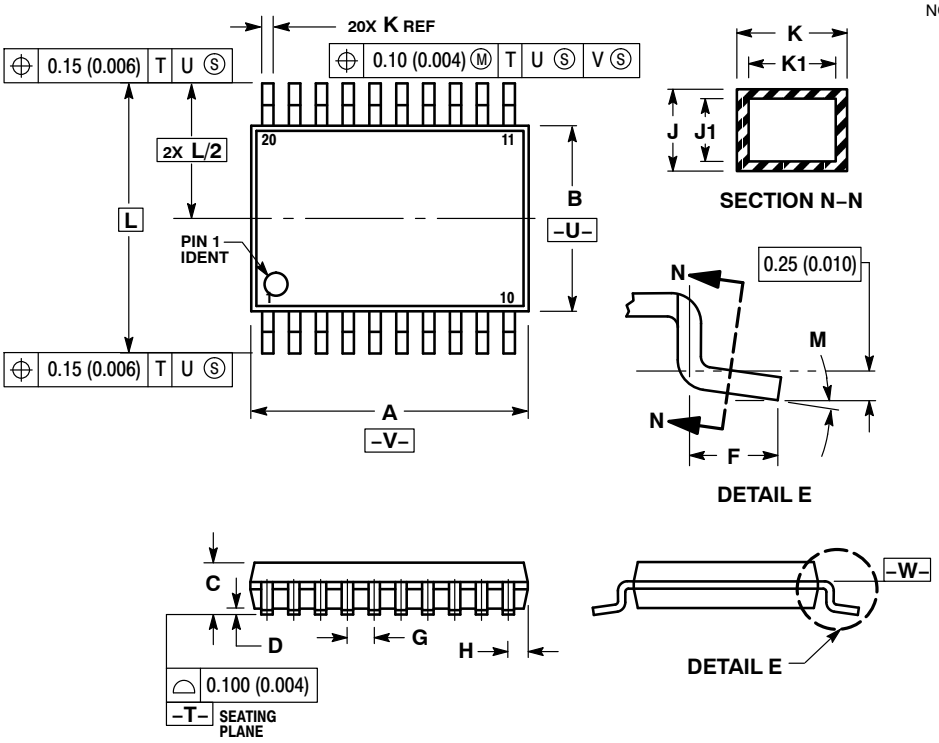



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

## PACKAGE DIMENSIONS

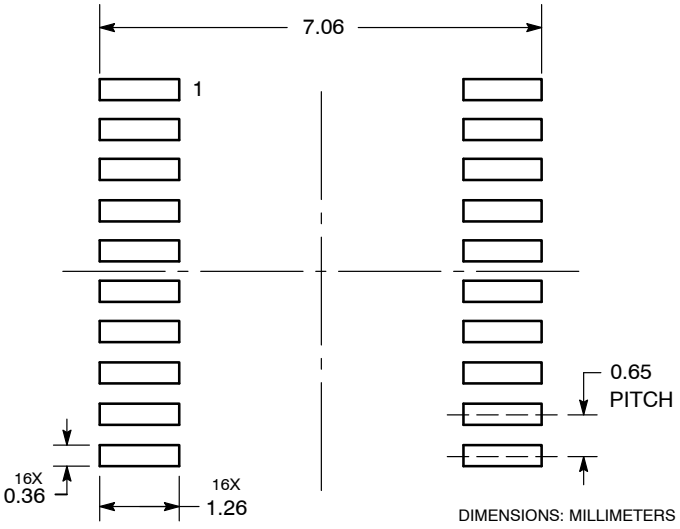
**TSSOP−20**
CASE 948E−02
ISSUE C




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

### SOLDERING FOOTPRINT




DIMENSIONS: MILLIMETERS

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**MC74LCX540/D**

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- Консультации по применению компонента;
- Поставка образцов и прототипов;
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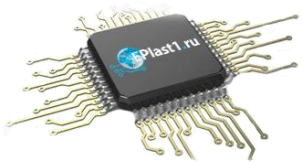
- Защита от снятия компонента с производства.

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