ACT8600

Rev 3, 15-Nov-12

Advanced PMU for Ingenic JZ4760/60B/70 Processors

FEATURES

- Optimized for Ingenic JZ4760, JZ4760B, and JZ4770 Processors
- Three Step-Down DC/DC Converters
- One Step-Up DC/DC Converter
- USB OTG Switch with 600mA Current Limit
- Four Low-Noise LDOs
- Two Low IQ Keep-Alive LDOs
- Backup Battery Charger
- Single-Cell Li+*ActivePath*™ Battery Charger
- I²C™ Serial Interface
- Interrupt Controller
- Power On Reset Interface and Sequencing Controller
- Minimum External Components
- 5×5mm TQFN55-40 Package
  - 0.75mm Package Height
  - Pb-Free and RoHS Compliant

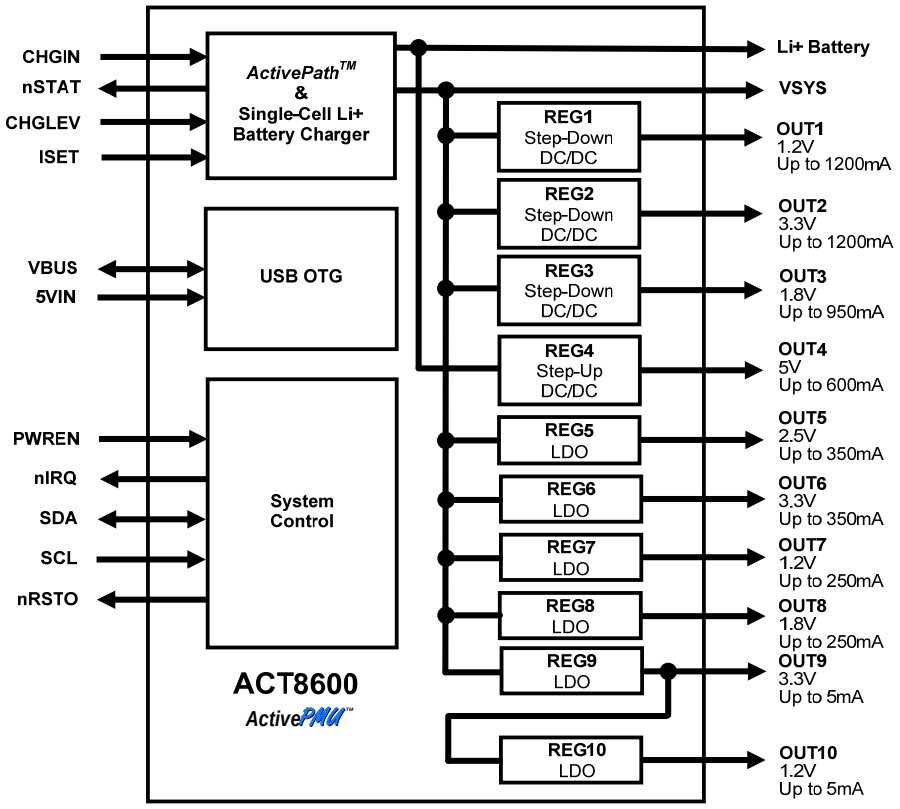
GENERAL DESCRIPTION

The ACT8600 is a complete, cost effective, highly-efficient *ActivePMU*™ power management solution, optimized for the unique power, voltage-sequencing, and control requirements of the Ingenic JZ4760, JZ4760B and JZ4770 processors.

This device features three highly efficient step-down DC/DC converters, one step-up DC/DC converter, four low-noise, low-dropout linear regulators, and two Low IQ always on Keep-Alive linear regulators, a current limit switch for USB OTG, along with a complete battery charging solution featuring the advanced *ActivePath*™ system-power selection function.

The ACT8600 is available in a compact, Pb-Free and RoHS-compliant TQFN55-40 package.

SYSTEM BLOCK DIAGRAM



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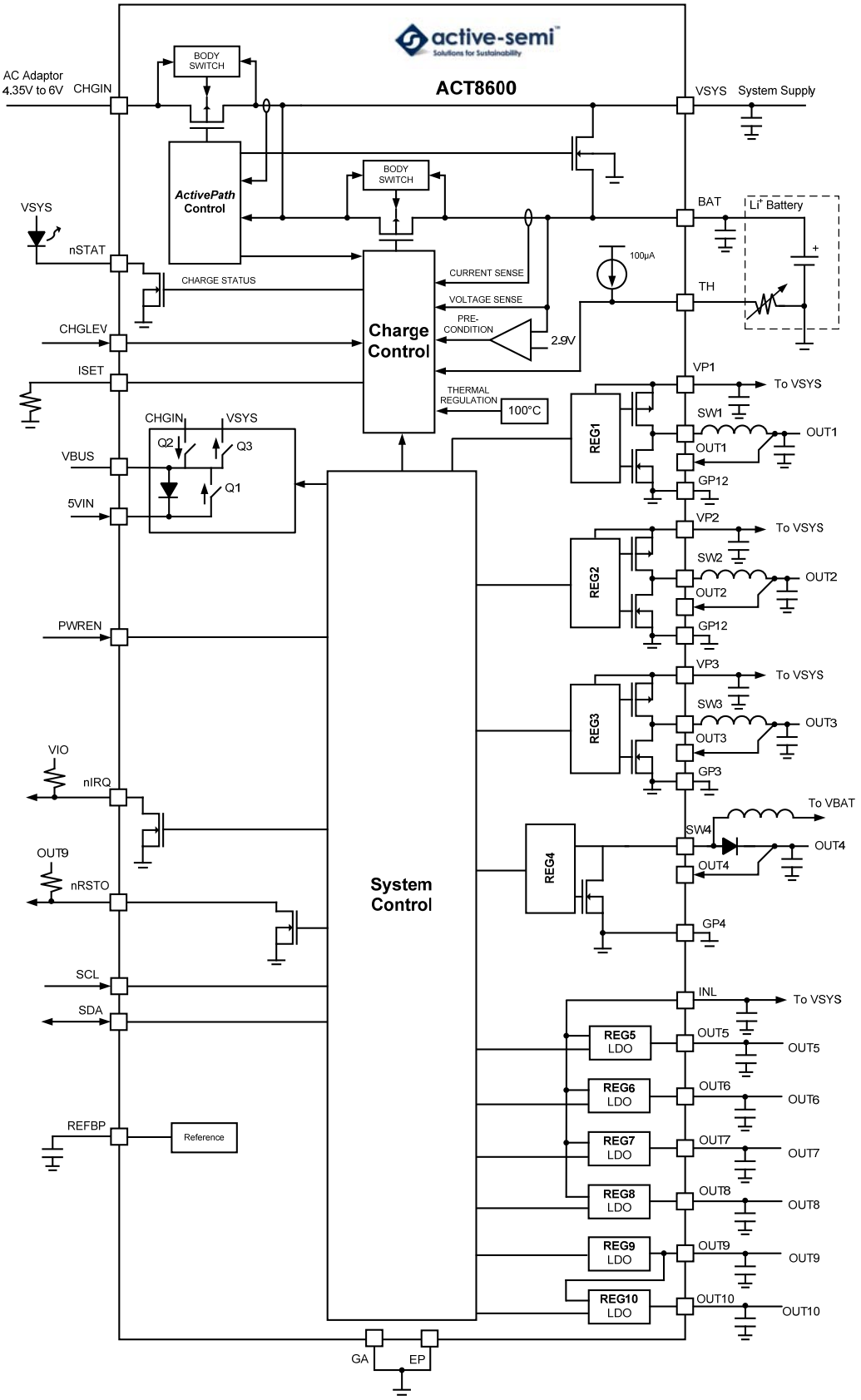
FUNCTIONAL BLOCK DIAGRAM

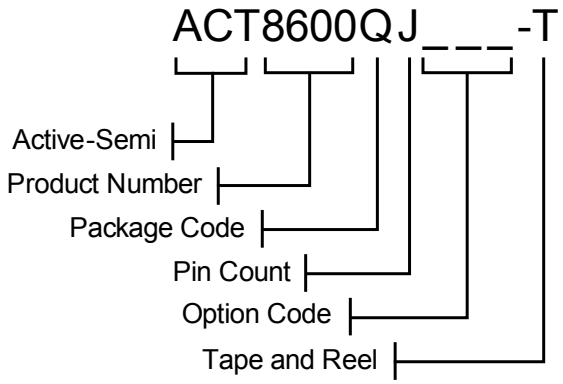


ORDERING INFORMATION①

PART NUMBER	V_{OUT1}	V_{OUT2}	V_{OUT3}	V_{OUT4}	V_{OUT5}	V_{OUT6}	V_{OUT7}	V_{OUT8}	V_{OUT9}	V_{OUT10}	PACKAGE	PINS	TEMPERATURE RANGE
ACT8600QJ162-T	1.2V	3.3V	1.8V	5V	2.5V	3.3V	1.2V	1.8V	3.3V	1.2V	TQFN55-40	40	-40°C to +85°C

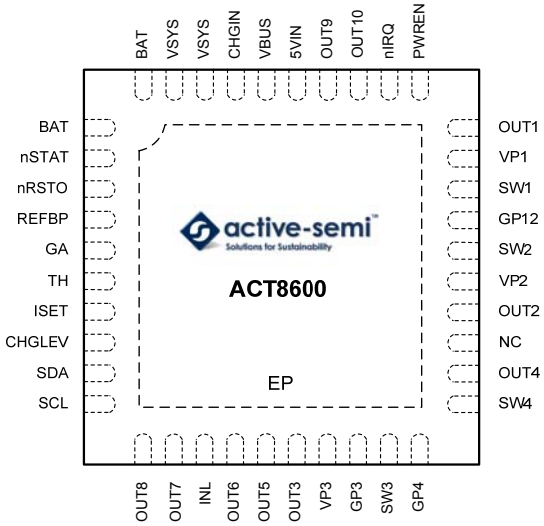
①: All Active-Semi components are RoHS Compliant and with Pb-free plating unless specified differently. The term Pb-free means semiconductor products that are in compliance with current RoHS (Restriction of Hazardous Substances) standards.

②: Standard product options are identified in this table. Contact factory for custom options. Minimum order quantity is 12,000 units.



PIN CONFIGURATION

TOP VIEW



Thin - QFN (TQFN55-40)

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1, 40	BAT	Battery charger output. Connect this pin directly to the battery anode (+ terminal).
2	nSTAT	Active-Low Open-Drain Charger Status Output. nSTAT has a 8mA (typ.) current limit, allowing it to directly drive an indicator LED without additional external components.
3	nRSTO	Active low open-drain Reset Output.
4	REFBP	Reference Bypass. Connect a 0.047µF ceramic capacitor from REFBP to GA.
5	GA	Ground.
6	TH	Temperature Sensing Input.
7	ISET	Charge Current Set. Program the maximum charge current by connecting a resistor (R_{ISET}) between ISET and GA.
8	CHGLEV	Charge Current Selection Input.
9	SDA	Data Input for I^2C Serial Interface. Data is read on the rising edge of SCL.
10	SCL	Clock Input for I^2C Serial Interface.
11	OUT8	REG8 Output. Bypass it to ground with a 2.2µF capacitor.
12	OUT7	REG7 Output. Bypass it to ground with a 2.2µF capacitor.
13	INL	Power Input for the LDOs. Bypass to GA with a high quality ceramic capacitor placed as close to the IC as possible.
14	OUT6	REG6 Output. Bypass it to ground with a 2.2µF capacitor.
15	OUT5	REG5 Output. Bypass it to ground with a 2.2µF capacitor.
16	OUT3	Output voltage sense for REG3.
17	VP3	Power input for REG3. Bypass to GP3 with a high quality ceramic capacitor placed as close to the IC as possible.
18	GP3	Power Ground for REG3. Connect GA, GP12, GP3 and GP4 together at a single point as close to the IC as possible.
19	SW3	Switch Node for REG3.
20	GP4	Power Ground for REG4. Connect GA, GP12 and GP3 together at a single point as close to the IC as possible.

PIN DESCRIPTIONS CONT'D

PIN	NAME	DESCRIPTION
21	SW4	Switch Node for REG4.
22	OUT4	REG4 Output.
23	NC	No Connect.
24	OUT2	Output Voltage Sense for REG2.
25	VP2	Power Input for REG2. Bypass to GP12 with a high quality ceramic capacitor placed to the IC as close as possible.
26	SW2	Switch Node for REG2.
27	GP12	Power Ground for REG1 and REG2. Connect GA, GP12 and GP3 together at a single point as close to the IC as possible.
28	SW1	Switch Node for REG1.
29	VP1	Power Input for REG1. Bypass to GP12 with a high quality ceramic capacitor placed to the IC as close as possible.
30	OUT1	Output Voltage Sense for REG1.
31	PWREN	Master enable pin.
32	nIRQ	Open-Drain Interrupt Output.
33	OUT10	REG10 Output. Bypass it to GA with a 0.47µF capacitor.
34	OUT9	REG9 Output. Bypass it to GA with a 1µF capacitor.
35	5VIN	5V Input pin for OTG switch (optionally from OUT4 or external 5V source).
36	VBUS	USB VBUS.
37	CHGIN	Power Input for the Battery Charger. Bypass CHGIN to GA with a capacitor placed as close to the IC as possible. The battery charger is automatically enabled when a valid voltage is present on CHGIN .
38, 39	VSYS	System Output Pins. Bypass to GA with a 10µF or larger ceramic capacitor.
EP	EP	Exposed Pad. Must be soldered to ground on PCB.

ABSOLUTE MAXIMUM RATINGS①

PARAMETER	VALUE	UNIT
VP1, VP2 to GP12 VP3 to GP3	-0.3 to + 6	V
BAT, VSYS, INL, VBUS, 5VIN to GA	-0.3 to + 6	V
CHGIN to GA	-0.3 to + 14	V
SW1, OUT1 to GP12	-0.3 to (V_{VP1} + 0.3)	V
SW2, OUT2 to GP12	-0.3 to (V_{VP2} + 0.3)	V
SW3, OUT3 to GP3	-0.3 to (V_{VP3} + 0.3)	V
SW4, OUT4 to GP4	-0.3 to + 42	V
nIRQ, nRSTO, nSTAT to GA	-0.3 to + 6	V
PWREN, SCL, SDA, CHGLEV, TH, ISET, REFBP to GA	-0.3 to (V_{VSYS} + 0.3)	V
OUT5, OUT6, OUT7, OUT8, OUT9, OUT10 to GA	-0.3 to (V_{INL} + 0.3)	V
GP12, GP3, GP4 to GA	-0.3 to + 0.3	V
Operating Ambient Temperature	-40 to 85	°C
Maximum Junction Temperature	125	°C
Maximum Power Dissipation TQFN55-40 (Thermal Resistance=30°C/W)	3.2	W
Storage Temperature	-65 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C

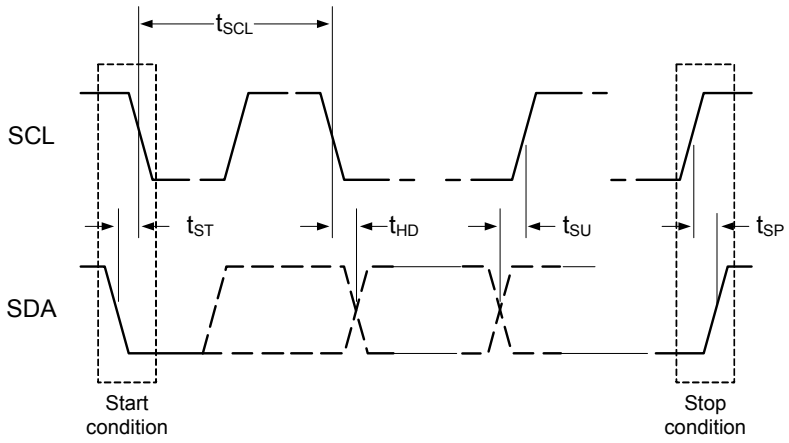
①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

I²C INTERFACE ELECTRICAL CHARACTERISTICS

(V_{VSYS} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL, SDA Input Low	V_{VSYS} = 3.1V to 5.5V, T_A = -40ºC to 85ºC			0.35	V
SCL, SDA Input High	V_{VSYS} = 3.1V to 5.5V, T_A = -40ºC to 85ºC	1.55			V
SDA Leakage Current			0	1	µA
SCL Leakage Current			0	1	µA
SDA Output Low	I_{OL} = 5mA			0.35	V
SCL Clock Period, t_{SCL}		1.5			µs
SDA Data Setup Time, t_{SU}		100			ns
SDA Data Hold Time, t_{HD}		300			ns
Start Setup Time, t_{ST}	For Start Condition	100			ns
Stop Setup Time, t_{SP}	For Stop Condition	100			ns

Figure 1:
I²C Compatible Serial Bus Timing



GLOBAL REGISTER MAP

OUTPUT	ADDRESS		BITS							
			D7	D6	D5	D4	D3	D2	D1	D0
SYS	0x00	NAME	nSYSLEVMSK	nSYSSTAT	VSYSDAT	*Reserved*	SYSLEV[3]	SYSLEV[2]	SYSLEV[1]	SYSLEV[0]
		DEFAULT①	0	R	R	0	0	0	0	0
SYS	0x01	NAME	nTMSK	TSTAT	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*
		DEFAULT①	0	R	0	0	0	0	0	0
REG1	0x10	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	0	0	1	1	0	0	0
REG1	0x12	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	PHASE	nFLTMSK	OK
		DEFAULT①	1	0	0	0	0	0	0	R
REG2	0x20	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	0	1	1	1	0	0	1
REG2	0x22	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	PHASE	nFLTMSK	OK
		DEFAULT①	1	0	0	0	0	1	0	R
REG3	0x30	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	0	1	0	0	1	0	0
REG3	0x32	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	PHASE	nFLTMSK	OK
		DEFAULT①	1	0	0	0	0	0	0	R
REG4	0x40	NAME	VSET[7]	VSET[6]	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	1	0	1	0	1	0	0
REG4	0x41	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	OK
		DEFAULT①	0	0	0	0	0	0	0	R
REG5	0x50	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	1	1	1	0	0	0	1
REG5	0x51	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	DIS	nFLTMSK	OK
		DEFAULT①	1	0	0	0	0	1	0	R
REG6	0x60	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	0	1	1	1	0	0	1
REG6	0x61	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	DIS	nFLTMSK	OK
		DEFAULT①	0	0	0	0	0	1	0	R
REG7	0x70	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	0	0	1	1	0	0	0
REG7	0x71	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	DIS	nFLTMSK	OK
		DEFAULT①	0	0	0	0	0	1	0	R
REG8	0x80	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	0	1	0	0	1	0	0
REG8	0x81	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	DIS	nFLTMSK	OK
		DEFAULT①	0	0	0	0	0	1	0	R
REG910	0x91	NAME	ON9	ON10	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*
		DEFAULT①	1	0	0	0	0	0	0	0
APCH	0xA1	NAME	SUSCHG	*Reserved*	TOTTIMO[1]	TOTTIMO[0]	PRETIMO[1]	PRETIMO[0]	CHGLEV	OVPSET[0]
		DEFAULT①	0	0	1	0	1	0	0	0
APCH	0xA8	NAME	TIMRSTAT	TEMPSTAT	INSTAT	CHGSTAT	TIMRDAT	TEMPDAT	INDAT	CHGDAT
		DEFAULT①	R	R	R	R	R	R	R	R
APCH	0xA9	NAME	TIMRTOT	TEMPIN	INCON	CHGEOCIN	TIMRPRE	TEMPOUT	INDIS	CHGEOCOUT
		DEFAULT①	0	0	0	0	0	0	0	0
APCH	0xAA	NAME	CHG_ACIN	CHG_USB	CSTATE[0]	CSTATE[1]	*Reserved*	*Reserved*	*Reserved*	CHGLEVSTAT
		DEFAULT①	R	R	R	R	R	R	R	R
OTG	0xB0	NAME	ONQ1	ONQ2	ONQ3	Q1OK	Q2OK	VBUSSTAT	DBILIMQ3	VBUSDAT
		DEFAULT①	0	0	1	R	R	R	0	R
OTG	0xB2	NAME	INVBUSR	INVBUSF	*Reserved*	*Reserved*	nFLTMSKQ1	nFLTMSKQ2	*nVBUSMSK*	*Reserved*
		DEFAULT	0	0	0	0	0	0	0	0
INT	0xC1	NAME	INTADR7	INTADR6	INTADR5	INTADR4	INTADR3	INTADR2	INTADR1	INTADR0
		DEFAULT	R	R	R	R	R	R	R	R

①: Default values of ACT8600QJ162-T.

Note: Every Reserved bit should be kept as Default Value

REGISTER AND BIT DESCRIPTIONS

OUTPUT	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
SYS	0x00	[7]	nSYSLEVMSK	R/W	VSYS Voltage Level Interrupt Mask. Set this bit to 1 to unmask the interrupt. See the *Programmable System Voltage Monitor* section for more information
SYS	0x00	[6]	nSYSSTAT	R	System Voltage Status. Value is 1 when SYSLEV interrupt is generated, value is 0 otherwise.
SYS	0x00	[5]	VSYSDAT	R	VSYS Voltage Monitor real time status. Value is 1 when V_{VSYS} < SYSLEV, value is 0 otherwise.
SYS	0x00	[4]	-	R	Reserved.
SYS	0x00	[3:0]	SYSLEV	R/W	System Voltage Detect Threshold. Defines the SYSLEV voltage threshold. See the *Programmable System Voltage Monitor* section for more information.
SYS	0x01	[7]	nTMSK	R/W	Thermal Interrupt Mask. Set this bit to 1 to unmask the interrupt.
SYS	0x01	[6]	TSTAT	R	Thermal Interrupt Status. Value is 1 when a thermal interrupt is generated, value is 0 otherwise.
SYS	0x01	[5:0]	-	R	Reserved.
REG1	0x10	[7:6]	-	R	Reserved.
REG1	0x10	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG1	0x12	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG1	0x12	[6:3]	-	R	Reserved.
REG1	0x12	[2]	PHASE	R/W	Regulator Phase Control. Set bit to 1 for the regulator to operate 180° out of phase with the oscillator, clear bit to 0 for the regulator to operate in phase with the oscillator.
REG1	0x12	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG1	0x12	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG2	0x20	[7:6]	-	R	Reserved.
REG2	0x20	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG2	0x22	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG2	0x22	[6:3]	-	R	Reserved.
REG2	0x22	[2]	PHASE	R/W	Regulator Phase Control. Set bit to 1 for the regulator to operate 180° out of phase with the oscillator, clear bit to 0 for the regulator to operate in phase with the oscillator.
REG2	0x22	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG2	0x22	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.

REGISTER AND BIT DESCRIPTIONS CONT'D

OUTPUT	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
REG3	0x30	[7:6]	-	R	Reserved.
REG3	0x30	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG3	0x32	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG3	0x32	[6:3]	-	R	Reserved.
REG3	0x32	[2]	PHASE	R/W	Regulator Phase Control. Set bit to 1 for the regulator to operate 180° out of phase with the oscillator, clear bit to 0 for the regulator to operate in phase with the oscillator.
REG3	0x32	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG3	0x32	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG4	0x40	[7:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG4	0x41	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG4	0x41	[6:1]	-	R	Reserved.
REG4	0x41	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG5	0x50	[7:6]	-	R	Reserved.
REG5	0x50	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG5	0x51	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG5	0x51	[6:3]	-	R	Reserved.
REG5	0x51	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG5	0x51	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG5	0x51	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG6	0x60	[7:6]	-	R	Reserved.
REG6	0x60	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG6	0x61	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG6	0x61	[6:3]	-	R	Reserved.
REG6	0x61	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG6	0x61	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG6	0x61	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.

REGISTER AND BIT DESCRIPTIONS CONT'D

OUTPUT	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
REG7	0x70	[7:6]	-	R	Reserved.
REG7	0x70	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG7	0x71	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG7	0x71	[6:3]	-	R	Reserved.
REG7	0x71	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG7	0x71	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG7	0x71	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG8	0x80	[7:6]	-	R	Reserved.
REG8	0x80	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG8	0x81	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG8	0x81	[6:3]	-	R	Reserved.
REG8	0x81	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG8	0x81	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG8	0x81	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG910	0x91	[7]	ON9	R/W	REG9 Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG910	0x91	[6]	ON10	R/W	REG10 Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG910	0x91	[5:0]	-	R	Reserved.
APCH	0xA1	[7]	SUSCHG	R/W	Charge Suspend Control Input. Set bit to 1 to suspend charging, clear bit to 0 to allow charging to resume.
APCH	0xA1	[6]	-	R	Reserved.
APCH	0xA1	[5:4]	TOTTIMO	R/W	Total Charge Time-out Selection. See the *Charge Safety Timers* section for more information.
APCH	0xA1	[3:2]	PRETIMO	R/W	Precondition Charge Time-out Selection. See the *Charge Safety Timers* section for more information.
APCH	0xA1	[1]	CHGLEV	R/W	Charge Current Selection Input. See *Charge Current Programming* Section.
APCH	0xA1	[0]	OVPSET	R/W	Input Over-Voltage Protection Threshold Selection. See the *Input Over-Voltage Protection* section for more information.
APCH	0xA8	[7]	TIMRSTAT①	R/W	Charge Time-out Interrupt Status. Set this bit with TIMRPRE[ ] and/or TIMRTOT[ ] to 1 to generate an interrupt when charge safety timers expire, read this bit to get charge time-out interrupt status. See the *Charge Safety Timers* section for more information.

①: Valid only when CHGIN UVLO Threshold<V_{CHGIN}<CHGIN OVP Threshold.

REGISTER AND BIT DESCRIPTIONS CONT'D

OUTPUT	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
APCH	0xA8	[6]	TEMPSTAT①	R/W	Battery Temperature Interrupt Status. Set this bit with TEMPIN[ ] and/or TEMPOUT[ ] to 1 to generate an interrupt when a battery temperature event occurs, read this bit to get the battery temperature interrupt status. See the *Battery Temperature Monitoring* section for more information.
APCH	0xA8	[5]	INSTAT	R/W	Input Voltage Interrupt Status. Set this bit with INCON[ ] and/or INDIS[ ] to generate an interrupt when UVLO or OVP condition occurs, read this bit to get the input voltage interrupt status. See the *Charge Current Programming* section for more information.
APCH	0xA8	[4]	CHGSTAT①	R/W	Charge State Interrupt Status. Set this bit with CHGEOCIN[ ] and/or CHGEOCOUT[ ] to 1 to generate an interrupt when the state machine gets in or out of EOC state, read this bit to get the charger state interrupt status. See the *State Machine Interrupts* section for more information.
APCH	0xA8	[3]	TIMRDAT①	R	Charge Timer Status. Value is 1 when precondition time-out or total charge time-out occurs. Value is 0 in other case.
APCH	0xA8	[2]	TEMPDAT①	R	Temperature Status. Value is 0 when battery temperature is outside of valid range. Value is 1 when battery temperature is inside of valid range.
APCH	0xA8	[1]	INDAT	R	Input Voltage Status. Value is 1 when a valid input at CHGIN is present. Value is 0 when a valid input at CHGIN is not present.
APCH	0xA8	[0]	CHGDAT①	R	Charge State Machine Status. Value is 1 indicates the charger state machine is in EOC state, value is 0 indicates the charger state machine is in other states.
APCH	0xA9	[7]	TIMRTOT	R/W	Total Charge Time-out Interrupt Control. Set both this bit and TIMRSTAT[ ] to 1 to generate an interrupt when a total charge time-out occurs. See the *Charge Safety Timers* section for more information.
APCH	0xA9	[6]	TEMPIN	R/W	Battery Temperature Interrupt Control. Set both this bit and TEMPSTAT[ ] to 1 to generate an interrupt when the battery temperature goes into the valid range. See the *Battery Temperature Monitoring* section for more information.
APCH	0xA9	[5]	INCON	R/W	Input Voltage Interrupt Control. Set both this bit and INSTAT[ ] to 1 to generate an interrupt when CHGIN input voltage goes into the valid range. See the *Charge Current Programming* section for more information.
APCH	0xA9	[4]	CHGEOCIN	R/W	Charge State Interrupt Control. Set both this bit and CHGSTAT[ ] to 1 to generate an interrupt when the state machine goes into the EOC state. See the *State Machine Interrupts* section for more information.
APCH	0xA9	[3]	TIMRPRE	R/W	PRECHARGE Time-out Interrupt Control. Set both this bit and TIMRSTAT[ ] to 1 to generate an interrupt when a PRECHARGE time-out occurs. See the *Charge Safety Timers* section for more information.
APCH	0xA9	[2]	TEMPOUT	R/W	Battery Temperature Interrupt Control. Set both this bit and TEMPSTAT[ ] to 1 to generate an interrupt when the battery temperature goes out of the valid range. See the *Battery Temperature Monitoring* section for more information.

①: Valid only when CHGIN UVLO Threshold<V_{CHGIN}<CHGIN OVP Threshold.

REGISTER AND BIT DESCRIPTIONS CONT'D

OUTPUT	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
APCH	0xA9	[1]	INDIS	R/W	Input Voltage Interrupt Control. Set both this bit and INSTAT[ ] to 1 to generate an interrupt when CHGIN input voltage goes out of the valid range. See the *Charge Current Programming* section for more information.
APCH	0xA9	[0]	CHGEOCOUT	R/W	Charge State Interrupt Control. Set both this bit and CHGSTAT[ ] to 1 to generate an interrupt when the state machines jumps out of the EOC state. See the *State Machine Interrupts* section for more information.
APCH	0xAA	[7]	CHG_ACIN	R	Charge source indicator. Value is 1 when charging from AC source and value is 0 when charging from other source.
APCH	0xAA	[6]	CHG_USB	R	Charge source indicator. Value is 1 when charging from USB source and value is 0 when charging from other source.
APCH	0xAA	[5:4]	CSTATE	R	Charge State. Values indicate the current charging state. See the *State Machine Interrupts* section for more information.
APCH	0xAA	[3:1]	-	R	Reserved.
APCH	0xAA	[0]	CHGLEVSTAT	R	CHGLEV pin status. Value is 0 if CHGLEVSTAT is logic low; value is 1 otherwise.
OTG	0xB0	[7]	ONQ1	R/W	OTG Q1 Enable Bit. Set bit to 1 to turn on Q1; clear bit to 0 to turn off Q1.
OTG	0xB0	[6]	ONQ2	R/W	OTG Q2 Enable Bit. Set bit to 1 to turn on Q2; clear bit to 0 to turn off Q2.
OTG	0xB0	[5]	ONQ3	R/W	OTG Q3 Enable Bit. Set bit to 1 to turn on Q3; clear bit to 0 to turn off Q3.
OTG	0xB0	[4]	Q1OK	R	OTG Q1 Status. Value is 0 if Q1 can not start up successfully, or in current limit status.
OTG	0xB0	[3]	Q2OK	R	OTG Q2 Status. Value is 0 if Q2 can not start up successfully, or in current limit status.
OTG	0xB0	[2]	VBUSSTAT	R	VBUS Interrupt Status. Value is 1 if an interrupt is generated by either INVBUSR or INVBUSF.
OTG	0xB0	[1]	DBILIMQ3	R/W	Set to 1 to double the current limit of Q3.
OTG	0xB0	[0]	VBUSDAT	R	VBUS status. Value is 1 if a valid charging source is present at VBUS. Value is 0 otherwise.
OTG	0xB2	[7]	INVBUSR	R/W	VBUS Interrupt control. Set this bit to 1 to generate an interrupt when connecting a charger to VBUS (rising edge of VBUS).
OTG	0xB2	[6]	INVBUSF	R/W	VBUS Interrupt control. Set this bit to 1 to generate an interrupt when disconnecting a charger to VBUS (falling edge of VBUS).
OTG	0xB2	[5:4]	-	R	Reserved.
OTG	0xB2	[3]	nFLTMSKQ1	R/W	Q1 Interrupt Mask. Set this bit to 1 to generate an interrupt when the over-current threshold for Q1 is triggered.
OTG	0xB2	[2]	nFLTMSKQ2	R/W	Q2 Interrupt Mask. Set this bit to 1 to generate an interrupt when the over-current threshold for Q2 is triggered.
OTG	0xB2	[1]	nVBUSMSK	R/W	VBUS Interrupt Mask. Set this bit to 1 unmask to VBUS connection and/or disconnection interrupt.
OTG	0xB2	[0]	-	R	Reserved.
INT	0xC1	[7:0]	INTADR	R	Global Interrupt Address. See the *Interrupt Service Routine Section* for more information.

①: Valid only when CHGIN UVLO Threshold<V_{CHGIN}<CHGIN OVP Threshold.

SYSTEM CONTROL ELECTRICAL CHARACTERISTICS

(V_{VSYS} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range		2.3		5.5	V
UVLO Threshold Voltage	V_{VSYS} Rising		3.45		V
UVLO Hysteresis	V_{VSYS} Falling		200		mV
Supply Current	All Regulators Enabled		420		µA
Shutdown Supply Current	All Regulators Disabled except REG9, V_{VSYS} =3.6V		30		µA
Oscillator Frequency		2.060	2.220	2.380	MHz
Logic High Input Voltage		1.4			V
Logic Low Input Voltage				0.4	V
nRSTO Delay			40		ms
Thermal Shutdown Temperature	Temperature rising		160		°C
Thermal Shutdown Hysteresis			20		°C

STEP-DOWN DC/DC ELECTRICAL CHARACTERISTICS

(V_{VP1} = V_{VP2} = V_{VP3} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.7		5.5	V
UVLO_VP Threshold	Input Voltage Rising	2.5	2.6	2.7	V
UVLO_VP Hysteresis	Input Voltage Falling		100		mV
Standby Supply Current	Regulator Enabled, V_{VSYS} = 3.6V		68	95	µA
Shutdown Current	V_{VP} = 5.5V, Regulator Disabled		0	1	µA
Output Voltage Accuracy	V_{OUT} ≥ 1.2V, I_{OUT} = 10mA	-1.5%	V_{NOM}①	1.5%	V
Line Regulation	V_{VP} = Max (V_{NOM}① + 1, 3.2V) to 5.5V		0.15		%/V
Load Regulation	I_{OUT} = 10mA to IMAX②		0.0017		%/mA
Power Good Threshold	V_{OUT} Rising		93		%V_{NOM}
Power Good Hysteresis	V_{OUT} Falling		2.5		%V_{NOM}
Switching Frequency	V_{OUT} ≥ 20% of V_{NOM}	2.06	2.22	2.38	MHz
	V_{OUT} = 0V		520		kHz
Soft-Start Period	V_{OUT} = 3.3V		500		µs
Minimum On-Time			75	90	ns
REG1					
Maximum Output Current		1.2			A
Current Limit		1.70	2.00	2.75	A
PMOS On-Resistance	I_{SW1} = -100mA, V_{VSYS} = 3.6V		0.150		Ω
NMOS On-Resistance	I_{SW1} = 100mA, V_{VSYS} = 3.6V		0.120		Ω
SW1 Leakage Current	V_{VP1} = 5.5V, V_{SW1} = 0 or 5.5V		0	1	µA
REG2					
Maximum Output Current		1.2			A
Current Limit		1.70	2.00	2.75	A
PMOS On-Resistance	I_{SW2} = -100mA, V_{VSYS} = 3.6V		0.150		Ω
NMOS On-Resistance	I_{SW2} = 100mA, V_{VSYS} = 3.6V		0.120		Ω
SW2 Leakage Current	V_{VP2} = 5.5V, V_{SW2} = 0 or 5.5V		0	1	µA
REG3					
Maximum Output Current		0.95			A
Current Limit		1.10	1.45	1.85	A
PMOS On-Resistance	I_{SW3} = -100mA		0.150		Ω
NMOS On-Resistance	I_{SW3} = 100mA		0.120		Ω
SW3 Leakage Current	V_{VP3} = 5.5V, V_{SW3} = 0 or 5.5V		0	1	µA

①: V_{NOM} refers to the nominal output voltage level for V_{OUT} as defined by the *Ordering Information* section.

②: IMAX Maximum Output Current.

STEP-UP DC/DC ELECTRICAL CHARACTERISTICS

(V_{VP1} = V_{VP2} = V_{VP3} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.7		6	V
Operating Supply Current			0.8	1.7	mA
Standby Supply Current	No switching		80	150	µA
Shutdown Current	V_{VP} = 5.5V, Regulator Disabled		0.1	1	µA
Output Voltage Accuracy	V_{OUT} = 5V, I_{OUT} = 10mA	-3%	V_{NOM}①	3%	V
Line Regulation			0.019		%/V
Load Regulation			0.17		%/mA
Power Good Threshold	V_{OUT} Rising		93		$\%V_{NOM}$
Power Good Hysteresis	V_{OUT} Falling		7.5		$\%V_{NOM}$
Switching Frequency		1.032	1.110	1.188	MHz
Minimum On-Time			80		ns
Minimum Off-Time			40		ns
Maximum Output Current	V_{OUT} = 5V	0.6			A
Current Limit			1.35		A
Switch On-Resistance	I_{SW4} = 100mA		0.48		Ω
SW4 Leakage Current	V_{BAT} = 3.6V, V_{SW4} = 5V, REG4 disabled			10	µA

①: V_{NOM} refers to the nominal output voltage level for V_{OUT} as defined by the *Ordering Information* section.

LOW-NOISE LDO ELECTRICAL CHARACTERISTICS

(V_{INL} = 3.6V, C_{OUT5} = C_{OUT6} = C_{OUT7} = C_{OUT8} = 2.2μF, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.4		5.5	V
Output Voltage Accuracy	V_{OUT} ≥ 1.2V, T_A = 25°C, I_{OUT} = 10mA	-1.5%	V_{NOM}①	1.5%	V
Line Regulation	V_{INL} = Max (V_{OUT} + 0.5V, 3.6V) to 5.5V, LOWIQ[ ] = [0]		0.5		mV/V
Load Regulation	I_{OUT} = 1mA to IMAX②		0.08		V/A
Power Supply Rejection Ratio	f = 1kHz, I_{OUT} = 20mA, V_{OUT} =1.2V		80		dB
	f = 10kHz, I_{OUT} = 20mA, V_{OUT} =1.2V		70		
Supply Current per Output	Regulator Enabled		24	60	μA
	Regulator Disabled		0		
Soft-Start Period	V_{OUT} = 3.0V		100		μs
Power Good Threshold	V_{OUT} Rising		92		%
Power Good Hysteresis	V_{OUT} Falling		4		%
Output Noise	I_{OUT} = 20mA, f = 10Hz to 100kHz, V_{OUT} = 1.2V		30		$μV_{RMS}$
Discharge Resistance	LDO Disabled, DIS[ ] = 1		1.5		kΩ
REG5					
Dropout Voltage③	I_{OUT} = 160mA, V_{OUT} > 3.1V		130	200	mV
Maximum Output Current			350		mA
Current Limit④	V_{OUT} = 95% of regulation voltage	385	550		mA
Stable C_{OUT5} Range		2.2		20	μF
REG6					
Dropout Voltage③	I_{OUT} = 160mA, V_{OUT} > 3.1V		130	200	mV
Maximum Output Current			350		mA
Current Limit④	V_{OUT} = 95% of regulation voltage	385	550		mA
Stable C_{OUT6} Range		2.2		20	μF
REG7					
Dropout Voltage③	I_{OUT} = 160mA, V_{OUT} > 3.1V		160	300	mV
Maximum Output Current			250		mA
Current Limit④	V_{OUT} = 95% of regulation voltage	275	400		mA
Stable C_{OUT7} Range		2.2		20	μF
REG8					
Dropout Voltage③	I_{OUT} = 160mA, V_{OUT} > 3.1V		160	300	mV
Maximum Output Current			250		mA
Current Limit④	V_{OUT} = 95% of regulation voltage	275	400		mA
Stable C_{OUT8} Range		2.2		20	μF

①: V_{NOM} refers to the nominal output voltage level for V_{OUT} as defined by the *Ordering Information* section.

②: IMAX Maximum Output Current.

③: Dropout Voltage is defined as the differential voltage between input and output when the output voltage drops 100mV below the regulation voltage (for 3.1V output voltage or higher).

④: LDO current limit is defined as the output current at which the output voltage drops to 95% of the respective regulation voltage. Under heavy overload conditions the output current limit folds back by 50% (typ)

LOW-IQ LDO ELECTRICAL CHARACTERISTICS

(V_{VSYS} = 3.6V, C_{OUT9} = C_{OUT10} = 1µF, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
REG9 (VDDRTC18) — V_{NOM} = 3.3V					
Operating Voltage Range	V_{OUT} =1.8V	2.5		5.5	V
Output Voltage Accuracy	I_{OUT} = 1mA	-2.5	V_{NOM} ①	3.5	%
Line Regulation	V_{VSYS} = V_{OUT} + 1.2V to V_{VSYS} = 5.5V		0.2		%/V
Supply Current from VSYS	V_{VSYS} = V_{OUT} + 1.2V		2		µA
	V_{VSYS} < V_{OUT} + 0.7V		10		
Maximum Output current		5			mA
Stable C_{OUT} Range		0.47			µF
REG10 (VDDRTC12) — V_{NOM} = 1.2V					
Operating Voltage Range		1.7		5.5	V
Output Voltage Accuracy	I_{OUT} = 1mA	-3.5	V_{NOM} ①	2.5	%
Line Regulation	V_{IN} = V_{OUT} + 0.5V to V_{IN} = 5.5V		0.2		%/V
Supply Current from V_{OUT9}			2		µA
Maximum Output current		5			mA
Stable C_{OUT} Range		0.22			µF

OTG SUBSYSTEM ELECTRICAL CHARACTERISTICS

(V_{INL} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
5VIN to VBUS (Q1)					
Switch on resistance	5VIN = 5V, I_{LOAD} = 100mA		0.23		Ω
Current Limit Threshold		500	700		mA
Current Limit Delay			256		ms
CHGIN to VBUS (Q2)					
Switch on resistance	CHGIN = 5V, I_{LOAD} = 100mA		0.34		Ω
Current Limit Threshold		500	700		mA
Current Limit Delay			256		ms

①: V_{NOM} refers to the nominal output voltage level for V_{OUT} as defined by the *Ordering Information* section.

ActivePath™ CHARGER ELECTRICAL CHARACTERISTICS

(V_{CHGIN} = 5.0V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ActivePath					
CHGIN Operating Voltage Range		4.35		6.0	V
CHGIN UVLO Threshold	CHGIN Voltage Rising	3.1	3.5	3.9	V
CHGIN UVLO Hysteresis	CHGIN Voltage Falling		0.5		V
CHGIN OVP Threshold	CHGIN Voltage Rising	6.0	6.6	7.2	V
CHGIN OVP Hysteresis	CHGIN Voltage Falling		0.4		V
VBUS_UVLO Threshold	VBUS Voltage Rising	3.3	4.0	4.8	V
VBUS_UVLO Hysteresis	VBUS Voltage Falling		400		mV
CHGIN Supply Current	V_{CHGIN} < V_{UVLO}		35	70	µA
	V_{CHGIN} < V_{BAT} + 50mV, V_{CHGIN} > V_{UVLO}		100	200	µA
	V_{CHGIN} > V_{BAT} + 150mV, V_{CHGIN} > V_{UVLO} Charger disabled, I_{VSYS} = 0mA		1.2	2.0	mA
CHGIN to VSYS On-Resistance	I_{VSYS} = 100mA		0.25		Ω
CHGIN to VSYS Current Limit		1.5	2.25		A
VBUS Input Current Limit	CHGLEV = GA, V_{VSYS} =3.6V		75	110	mA
	CHGLEV = V_{VSYS}, DBILIMQ3[ ] = 0, V_{VSYS} =3.6V	400	450	500	
	CHGLEV = V_{VSYS}, DBILIMQ3[ ] = 1.		900		
VSYS REGULATION					
CHGIN to VSYS Regulated Voltage	I_{VSYS} = 10mA	4.45	4.6	4.8	V
nSTAT OUTPUT					
nSTAT Sink current	V_{nSTAT} = 2V	4	8	12	mA
nSTAT Leakage Current	V_{nSTAT} = 4.2V			1	µA
CHGLEV INPUTS					
CHGLEV Logic High Input Voltage		1.4			V
CHGLEV Logic Low Input Voltage				0.4	V
CHGLEV Leakage Current	V_{CHGLEV} = 4.2V			1	µA
TH INPUT					
TH Pull-Up Current	V_{CHGIN} > V_{BAT} + 100mV, Hysteresis = 50mV	91	100	109	µA
V_{TH} Upper Temperature Voltage Threshold (V_{THH})	Hot Detect NTC Thermistor	2.45	2.50	2.54	V
V_{TH} Lower Temperature Voltage Threshold (V_{THL})	Cold Detect NTC Thermistor	0.482	0.50	0.518	V
V_{TH} Hysteresis	Upper and Lower Thresholds		40		mV

ActivePath™ CHARGER ELECTRICAL CHARACTERISTICS CONT'D

(V_{CHGIN} = 5.0V, T_A = 25°C, unless otherwise specified.)

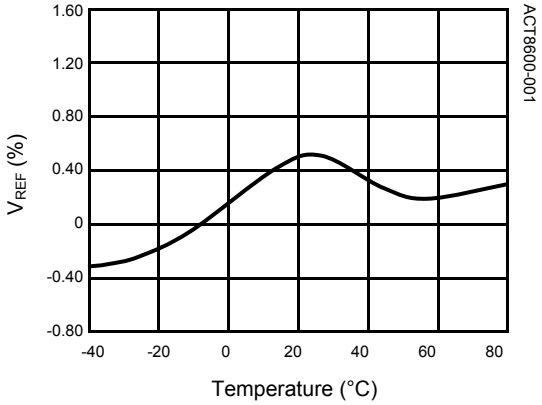
PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
CHARGER						
BAT Reverse Leakage Current	V_{CHGIN} = 0V, V_{BAT} = 4.2V, I_{VSYS} = 0mA, All REGs are OFF.			15		µA
BAT to VSYS On-Resistance				70		mΩ
ISET Pin Voltage	Fast Charge			1.2		V
	Precondition			0.13		
Charge Termination Voltage	T_A = -20°C to 70°C		4.179	4.200	4.221	V
	T_A = -40°C to 85°C		4.170	4.200	4.230	
Charge Current	V_{BAT} = 3.8V	AC-Mode	-10%	I_{CHG} ①	+10%	mA
		USB-Mode, CHGLEV = GA		Min (75mA, I_{CHG})		
		USB-Mode, CHGLEV = V_{VSYS}, DBILIMQ3[ ] = 0.		Min (450mA, I_{CHG})		
		USB-Mode, CHGLEV = V_{VSYS}, DBILIMQ3[ ] = 1.		Min (900mA, I_{CHG})		
Precondition Charge Current	V_{BAT} = 2.7V	AC-Mode		10% I_{CHG}		mA
		USB-Mode, CHGLEV = GA		Min (75mA, 10% × I_{CHG})		
		USB-Mode, CHGLEV = V_{VSYS}, DBILIMQ3[ ] = 0.		10% I_{CHG}		
		USB-Mode, CHGLEV = V_{VSYS}, DBILIMQ3[ ] = 1.		10% I_{CHG}		
Precondition Threshold Voltage	V_{BAT} Voltage Rising		2.7	2.9	3.1	V
Precondition Threshold Hysteresis	V_{BAT} Voltage Falling			150		mV
END-OF-CHARGE Current Threshold	V_{BAT} = 4.15V	AC-Mode, CHGLEV = V_{VSYS}		10% I_{CHG}		mA
		AC-Mode, CHGLEV = GA		10% I_{CHG}		
		USB-Mode, CHGLEV = V_{VSYS}		45		
		USB-Mode, CHGLEV = GA		45		
Charge Restart Threshold	V_{VSYS} - V_{BAT}, V_{BAT} Falling		170	200	230	mV
Precondition Safety Timer	PRETIMO[ ] = 10			80		min
Total Safety Timer	TOTTIMO[ ] = 10			6.5		hr
Thermal Regulation Threshold				100		°C

①: R_{ISET} (kΩ) = 2336 × (1V/I_{CHG} (mA)) - 0.205

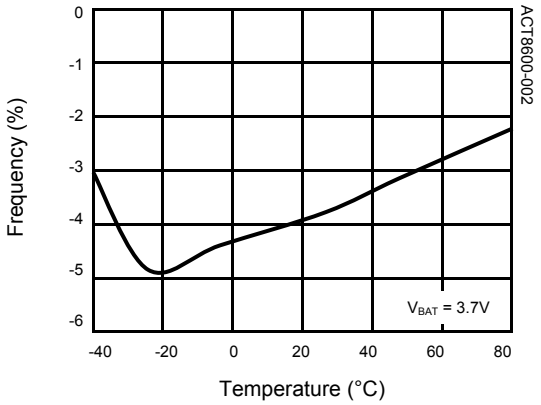
TYPICAL PERFORMANCE CHARACTERISTICS

(V_{VSYS} = 3.6V, T_A = 25°C, unless otherwise specified.)

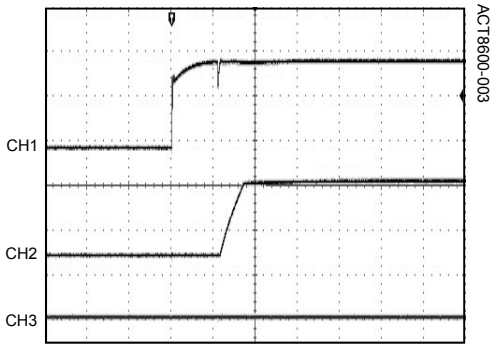
V_{REF} vs. Temperature



Frequency vs. Temperature

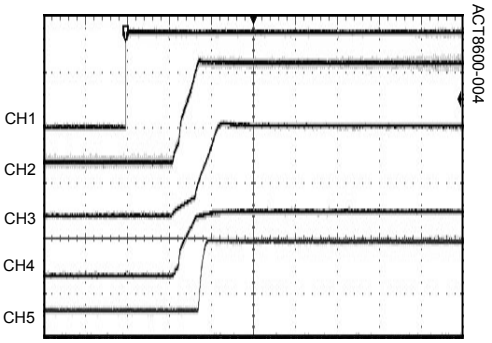


VBAT Connect



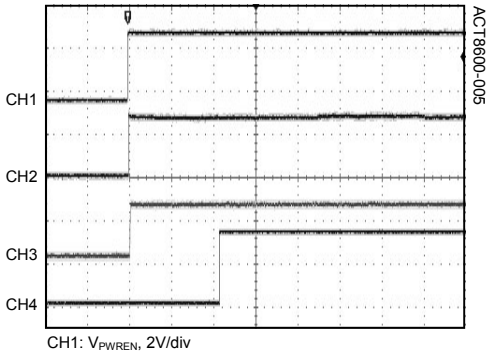
CH1: V_{BAT}, 2V/div
CH2: V_{OUT9}, 2V/div
CH3: V_{OUT10}, 1V/div
TIME: 400µs/div

PWREN Sequence



CH1: V_{PWREN}, 2V/div
CH2: V_{OUT3}, 1V/div
CH3: V_{OUT2}, 2V/div
CH4: V_{OUT1}, 1V/div
CH5: V_{OUT5}, 2V/div
TIME: 400µs/div

nRSTO Startup Sequence

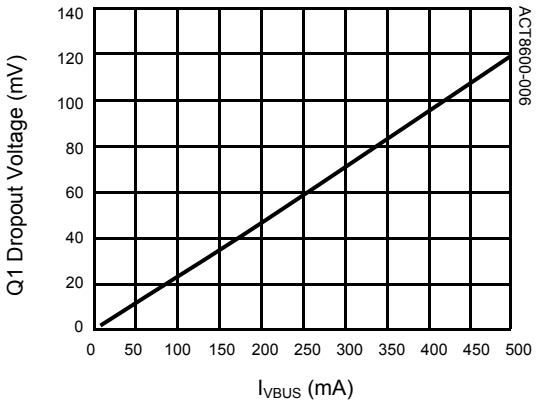


CH1: V_{PWREN}, 2V/div
CH2: V_{OUT3}, 1V/div
CH3: V_{OUT1}, 1V/div
CH4: V_{nRSTO}, 2V/div
TIME: 20ms/div

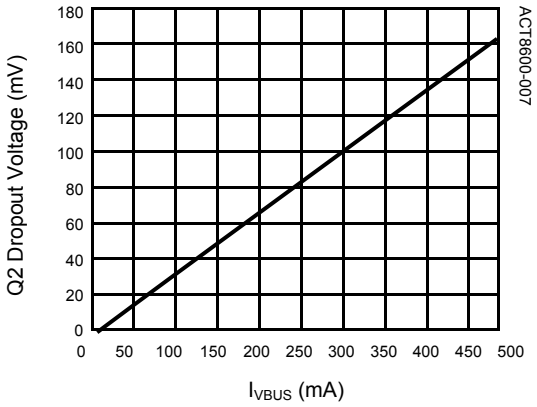
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(T_A = 25°C, unless otherwise specified.)

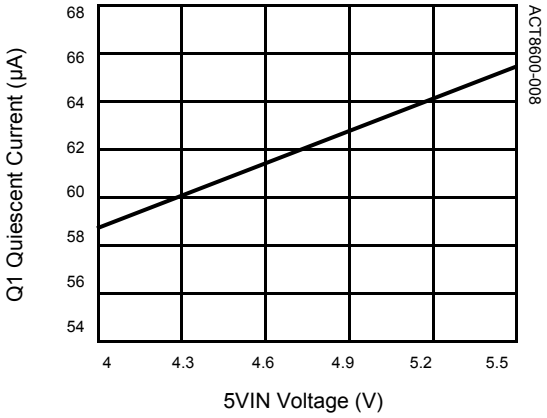
Q1 Dropout Voltage vs. I_{VBUS}



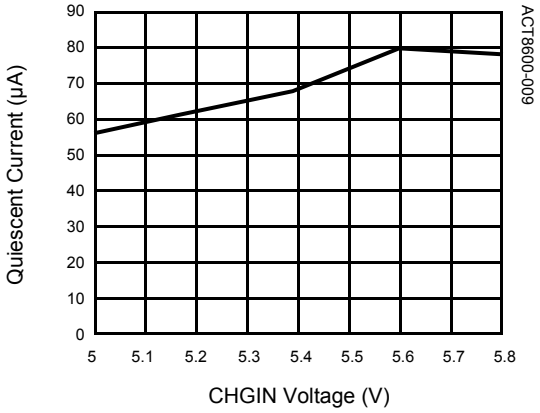
Q2 Dropout Voltage vs. I_{VBUS}



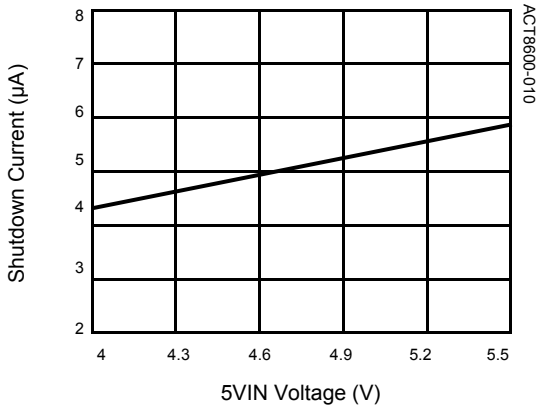
Q1 Quiescent Current vs. 5VIN Voltage



Q2 Quiescent Current vs. CHGIN Voltage



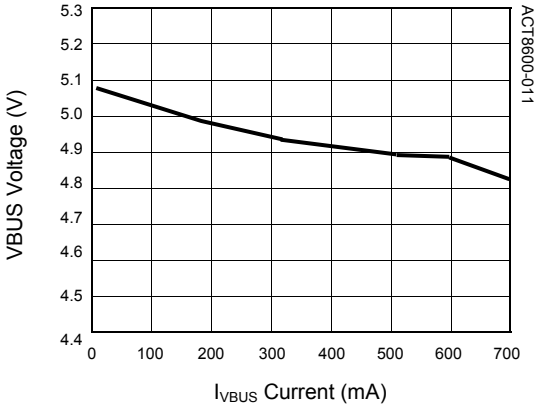
Q1 Shutdown Current vs. 5VIN Voltage



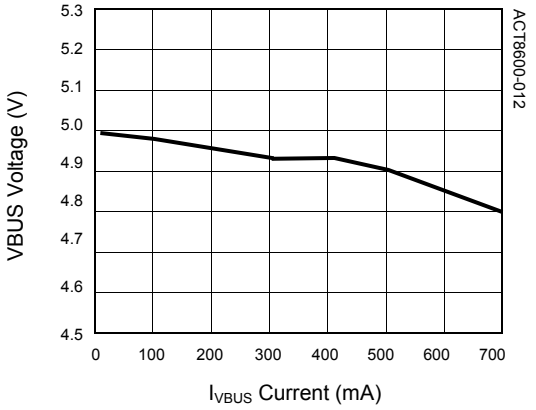
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(T_A = 25°C, unless otherwise specified.)

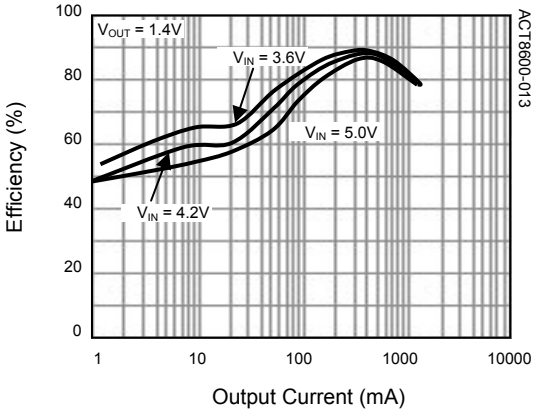
VBUS Voltage vs. I_{VBUS} Current (Supplied from 5VIN)



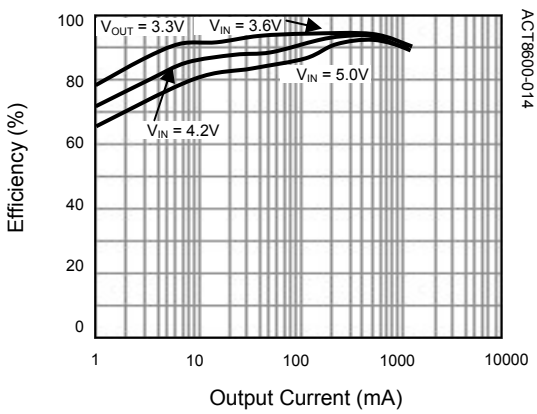
VBUS Voltage vs. I_{VBUS} (CHGIN Supply)



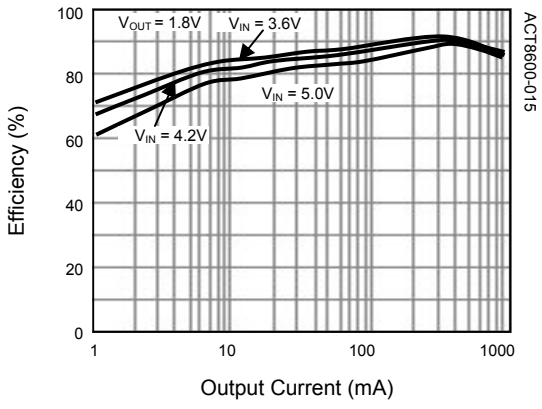
REG1 Efficiency vs. Output Current



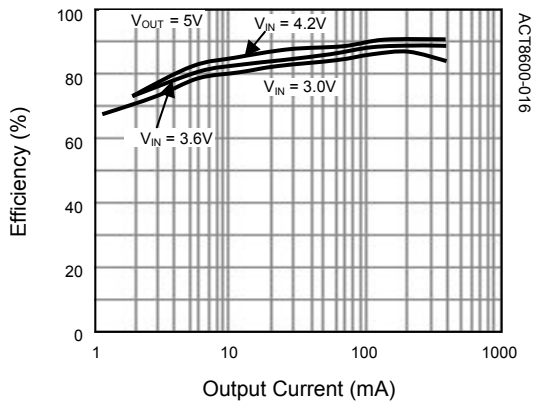
REG2 Efficiency vs. Output Current



REG3 Efficiency vs. Output Current



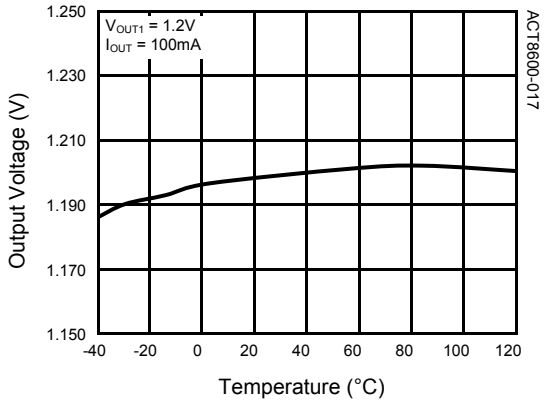
REG4 Efficiency vs. Output Current



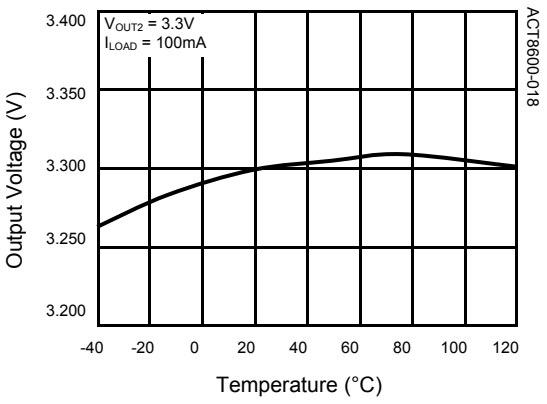
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(T_A = 25°C, unless otherwise specified.)

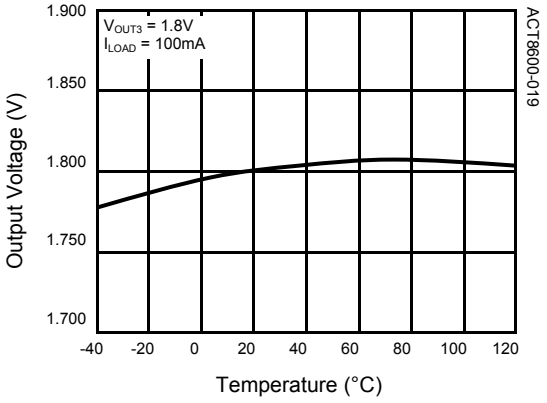
REG1 Output Voltage vs. Temperature



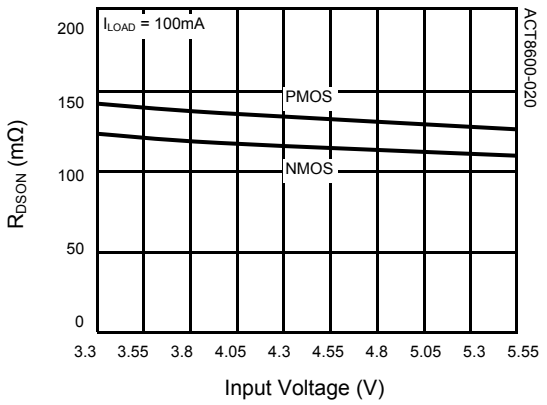
REG2 Output Voltage vs. Temperature



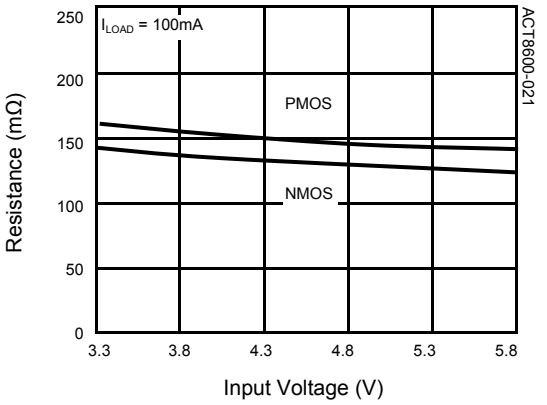
REG3 Output Voltage vs. Temperature



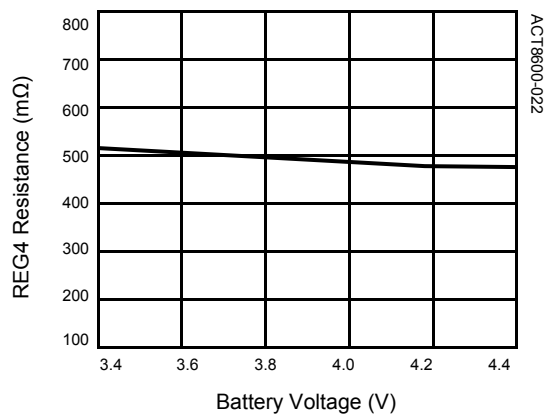
REG1, 2 MOSFET Resistance



REG3 MOSFET Resistance



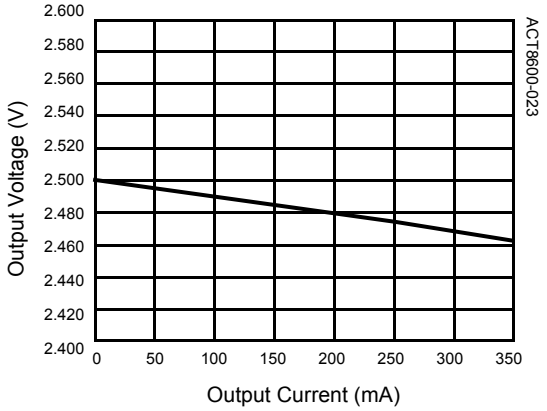
REG4 Resistance vs. Battery Voltage



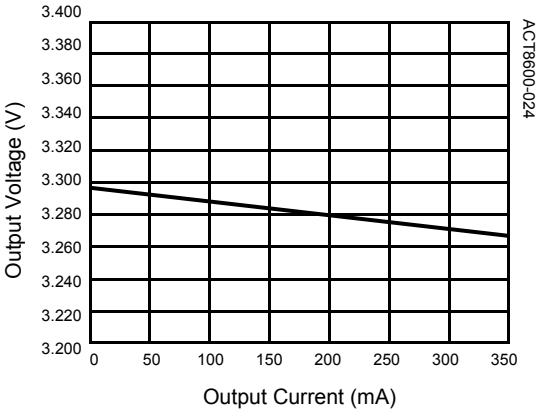
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(T_A = 25°C, unless otherwise specified.)

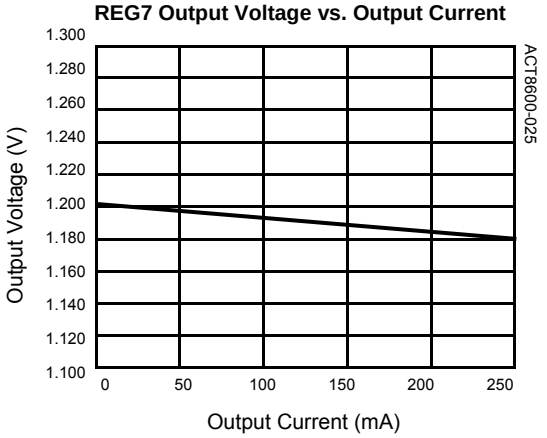
REG5 Output Voltage vs. Output Current



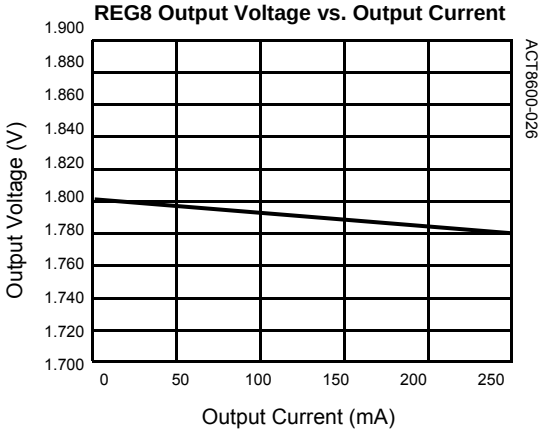
REG6 Output Voltage vs. Output Current



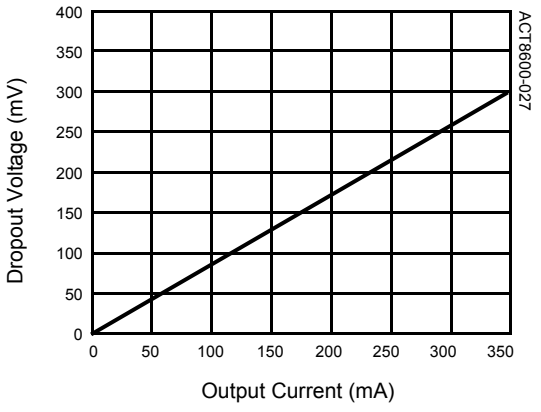
REG7 Output Voltage vs. Output Current



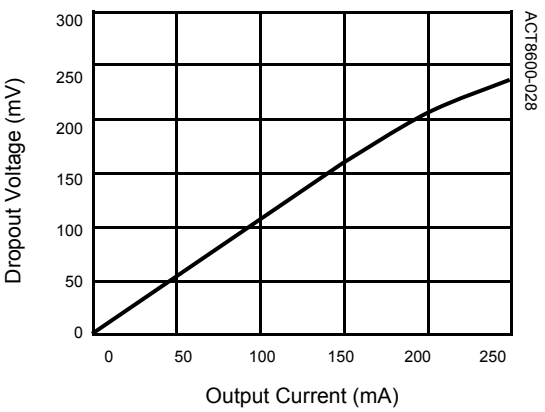
REG8 Output Voltage vs. Output Current



REG5/6 Dropout Voltage vs. Output Current



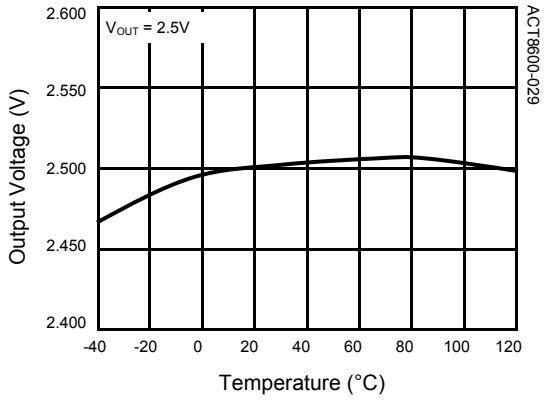
REG7/8 Dropout Voltage vs. Output Current



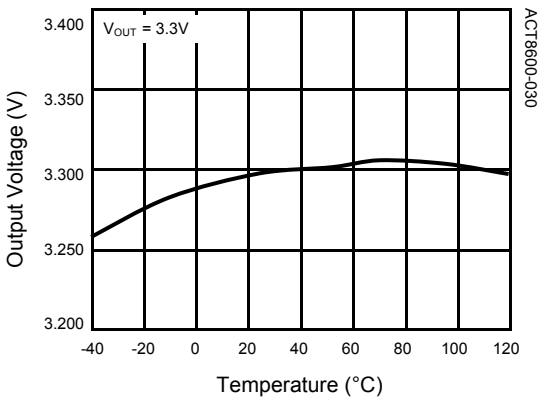
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(T_A = 25°C, unless otherwise specified.)

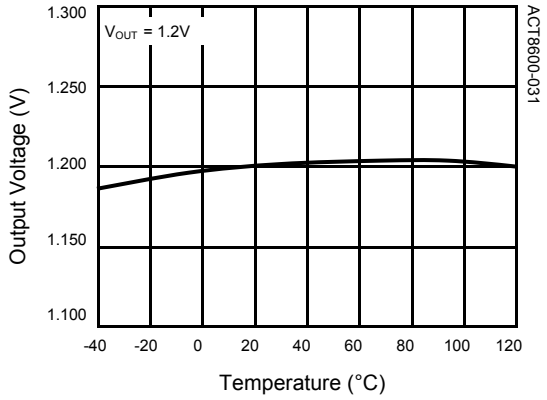
REG5 Output Voltage vs. Temperature



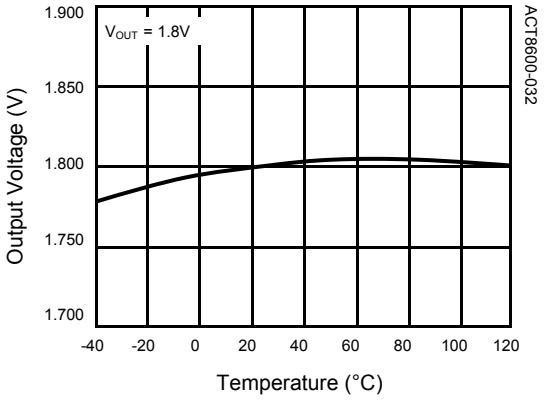
REG6 Output Voltage vs. Temperature



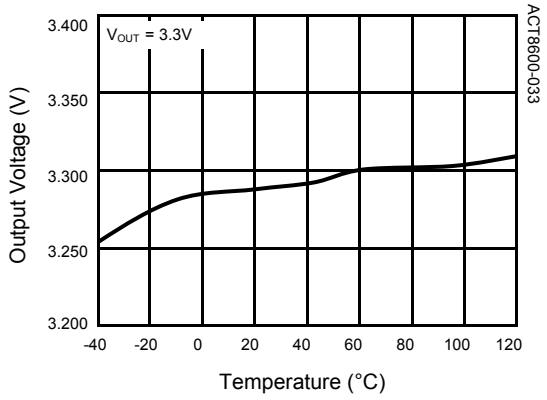
REG7 Output Voltage vs. Temperature



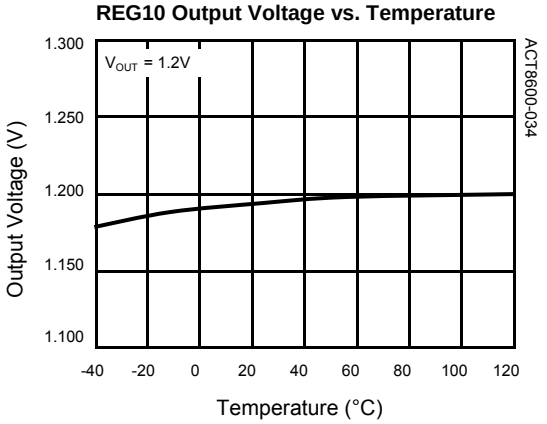
REG8 Output Voltage vs. Temperature



REG9 Output Voltage vs. Temperature

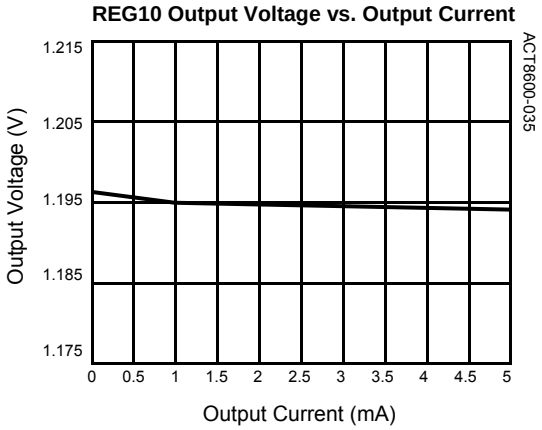


REG10 Output Voltage vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

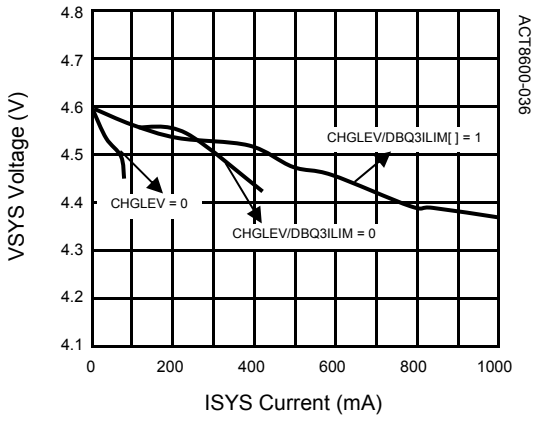
(T_A = 25°C, unless otherwise specified.)



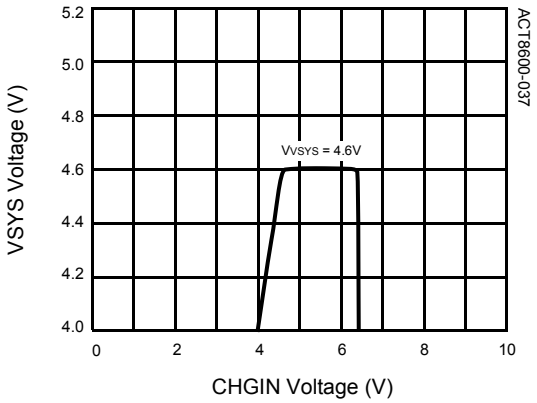
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(T_A = 25°C, unless otherwise specified.)

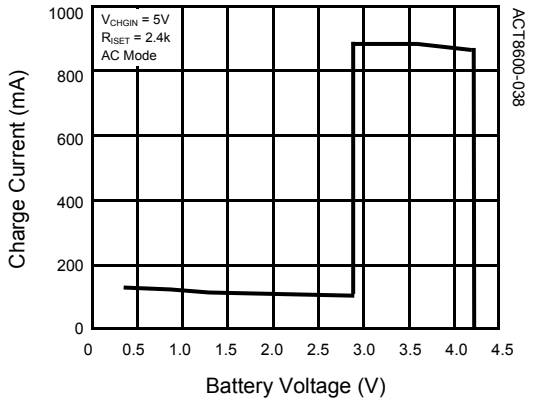
VSYS Voltage vs. VSYS Current (USB Mode)



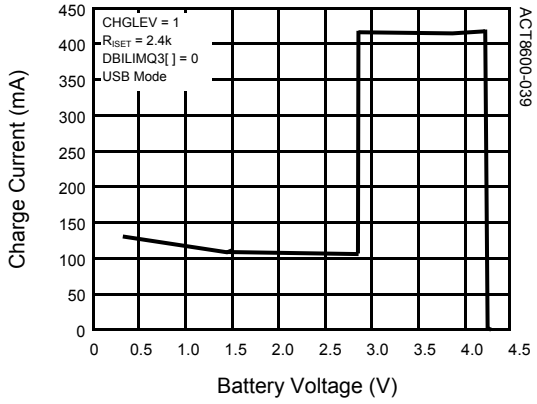
VSYS Voltage vs. CHGIN Voltage



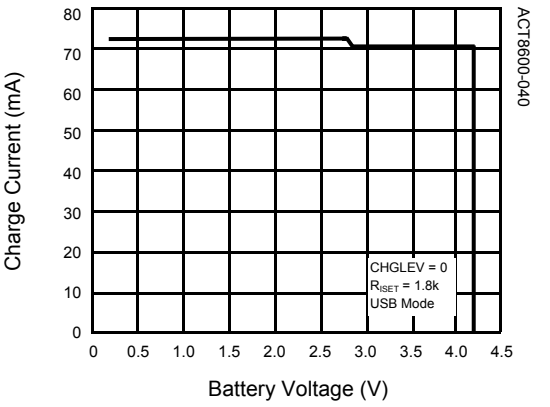
Charge Current vs. Battery Voltage



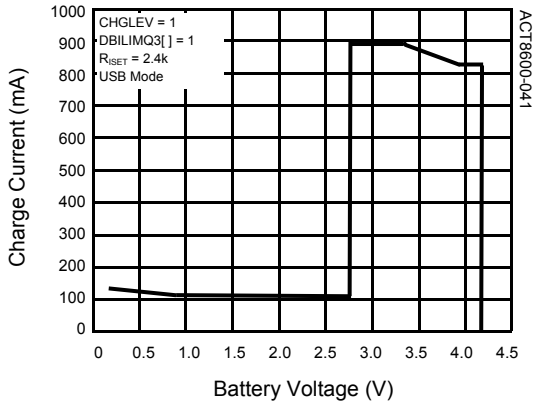
Charge Current vs. Battery Voltage



Charge Current vs. Battery Voltage



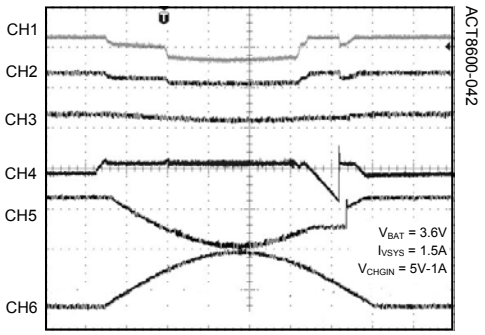
Charge Current vs. Battery Voltage



TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(T_A = 25°C, unless otherwise specified.)

DCCC and Battery Supplement Modes

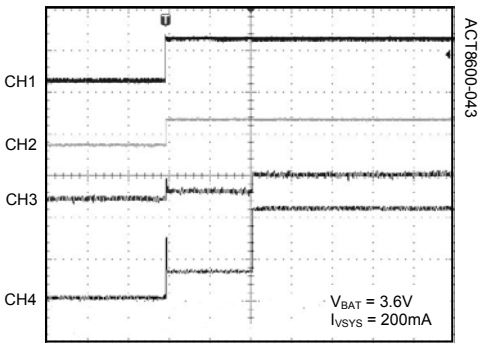


CH1: V_{VSYS}, 2V/div
CH2: V_{CHGIN}, 5V/div
CH3: V_{BAT}, 2V/div
CH4: I_{CHGIN}, 500mA/div
CH5: I_{BAT}, 1A/div
CH6: I_{VSYS}, 1A/div
TIME: 40ms/div

TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

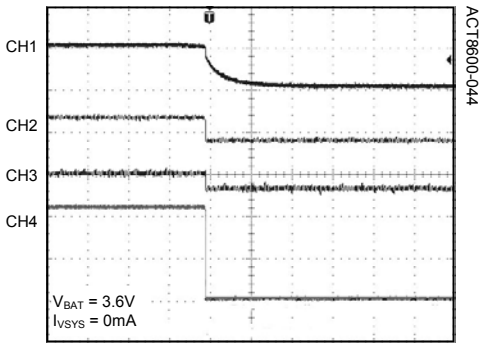
(T_A = 25°C, unless otherwise specified.)

CHGIN Applied



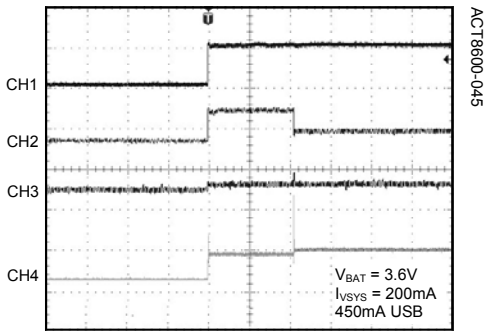
CH1: V_{CHGIN}, 5V/div
CH2: V_{VSYS}, 2V/div
CH3: V_{BAT}, 1V/div
CH4: I_{BAT}, 500mA/div
TIME: 20ms/div

CHGIN Removed



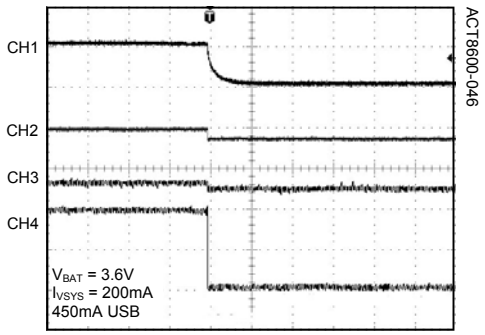
CH1: V_{CHGIN}, 5V/div
CH2: V_{VSYS}, 2V/div
CH3: V_{BAT}, 1V/div
CH4: I_{BAT}, 500mA/div
TIME: 20ms/div

VBUS Applied



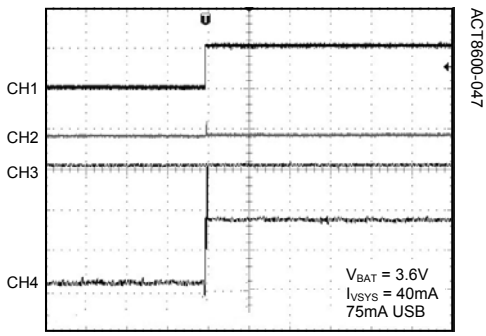
CH1: V_{VBUS}, 5V/div
CH2: V_{VSYS}, 2V/div
CH3: V_{BAT}, 1V/div
CH4: I_{BAT}, 500mA/div
TIME: 20ms/div

VBUS Removed



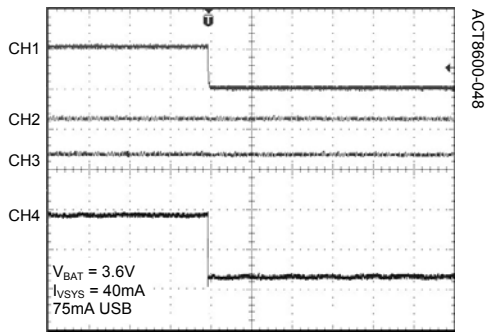
CH1: V_{VBUS}, 5V/div
CH2: V_{VSYS}, 2V/div
CH3: V_{BAT}, 1V/div
CH4: I_{BAT}, 200mA/div
TIME: 20ms/div

VBUS Applied



CH1: V_{VBUS}, 5V/div
CH2: V_{VSYS}, 2V/div
CH3: V_{BAT}, 2V/div
CH4: I_{BAT}, 50mA/div
TIME: 20ms/div

VBUS Removed

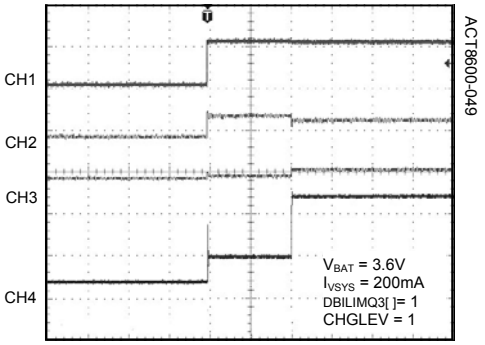


CH1: V_{VBUS}, 5V/div
CH2: V_{VSYS}, 2V/div
CH3: V_{BAT}, 2V/div
CH4: I_{BAT}, 50mA/div
TIME: 20ms/div

TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

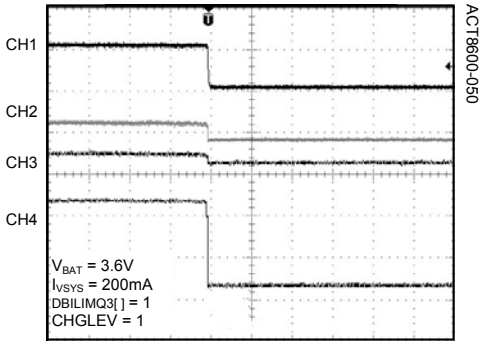
(T_A = 25°C, unless otherwise specified.)

VBUS Applied



CH1: V_{VBUS}, 5V/div
CH2: V_{VSYS}, 2V/div
CH3: V_{BAT}, 2V/div
CH4: I_{BAT}, 500mA/div
TIME: 20ms/div

VBUS Removed



CH1: V_{VBUS}, 5V/div
CH2: V_{VSYS}, 2V/div
CH3: V_{BAT}, 2V/div
CH4: I_{BAT}, 500mA/div
TIME: 20ms/div

SYSTEM CONTROL INFORMATION

Interfacing with the Ingenic JZ4770 Processor

The ACT8600 is optimized for use in applications using the Ingenic JZ4770 processor, supporting both the power domains as well as the signal interface for these processors.

The following paragraphs describe how to design ACT8600 with JZ4770 processor.

While the ACT8600 supports many possible configurations for powering these processors, one of the most common configurations is detailed in this datasheet.

Control Signals

Master Enable (PWREN) Input

PWREN is a logic input which turns ON REG1, REG2, REG3, and REG5 when asserted. All regulators except the RTC LDOs (REG9) will be turned OFF when PWREN is de-asserted.

nRSTO Output

The power on reset pin, nRSTO is an open-drain output. Connect a 10kΩ or greater pull-up resistor from nRSTO to REG9.

- The nRSTO output pin is asserted low only when the REG9 voltage is below 1.67V

- If REG1 is above its power-OK threshold when the reset timer (40ms) expires, nRSTO is de-asserted.

nIRQ Output

nIRQ is an open-drain output that asserts low any time an interrupt is generated. Connect a 10kΩ or greater pull-up resistor from nIRQ to the I/O rail. nIRQ is typically used to drive the interrupt input of the system processor.

Many of the ACT8600's functions support interrupt-generation as a result of various conditions. These are typically masked by default, but may be unmasked via the I^2C interface. For more information about the available fault conditions, refer to the appropriate sections of this datasheet.

Power Control Sequences

When the V_{VSYS} rises above the UVLO, or REG9 rises above 93% of its default value (in the case when a charged backup battery is installed), nRSTO is asserted low immediately and REG9 is enabled. REG1, REG2 and REG3 will be enabled when PWREN = 1 and V_{VSYS} is above 3.45V. When REG1 reaches 93% of the default value, REG5 will be enabled, and nRSTO is de-asserted after a 40ms delay.

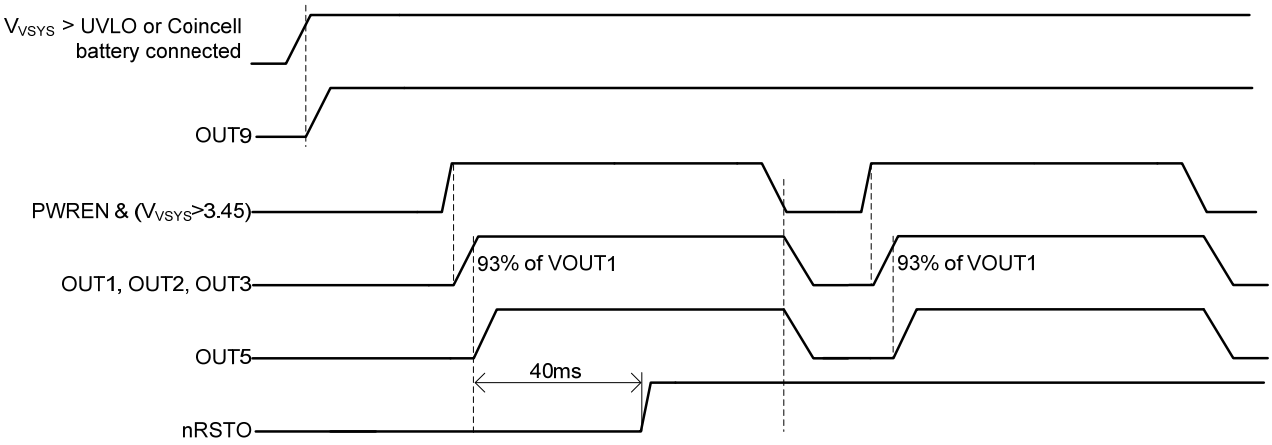
Once the system is turned ON, the processor may shut down the system by pulling down PWREN. In that case, all of the regulators, except REG9 will be turned off (REG9 is the always ON LDO). When PWREN is pulled high again, OUT1/2/3/5 will be turned ON again but nRSTO remains de-asserted as long as REG9 is within regulation.

Table 1:

ACT8600 and Ingenic JZ4770 Power Domains

POWER DOMAIN	ACT8600 CHANNEL	TYPE	DEFAULT VOLTAGE	CURRENT CAPABILITY
CPU Core	REG1	Step-Down DC/DC	1.2V	1200mA
IO / AVDAUD	REG2	Step-Down DC/DC	3.3V	1200mA
MEM	REG3	Step-Down DC/DC	1.8V	950mA
USB OTG	REG4	Step-Up DC/DC	5V	600mA
AVD	REG5	LDO	2.5V	350mA
General Purpose	REG6	LDO	1.8V	350mA
General Purpose	REG7	LDO	1.8V	250mA
General Purpose	REG8	LDO	1.8V	250mA
VDDRTC	REG9	LDO	3.3V	5mA
VDDRTC12	REG10	LDO	1.2V	5mA

Figure 2:
ACT8600 Power Sequence



FUNCTIONAL DESCRIPTION

I²C Interface

The ACT8600 features an I²C interface that allows advanced programming capability to enhance overall system performance. To ensure compatibility with a wide range of system processors, the I²C interface supports clock speeds of up to 400kHz ("Fast-Mode" operation) and uses standard I²C commands. I²C write-byte commands are used to program the ACT8600, and I²C read-byte commands are used to read the ACT8600's internal registers. The ACT8600 always operates as a slave device, and is addressed using a 7-bit slave address followed by an eighth bit, which indicates whether the transaction is a read-operation or a write-operation, [1011010x].

SDA is a bi-directional data line and SCL is a clock input. The master device initiates a transaction by issuing a START condition, defined by SDA transitioning from high to low while SCL is high. Data is transferred in 8-bit packets, beginning with the MSB, and is clocked-in on the rising edge of SCL. Each packet of data is followed by an "Acknowledge" (ACK) bit, used to confirm that the data was transmitted successfully.

For more information regarding the I²C 2-wire serial interface, go to the NXP website: http://www.nxp.com.

Interrupt Service Routine

The ACT8600 has number of interrupt trigger sources to simplify the customer interrupt service routine, the ACT8600 features a Interrupt Service Routine function as follow: Once the nIRQ asserts low, the CPU can read the 0xC1 byte to determine the source that asserts the interrupt. The CPU then reads the interrupt –related bit(s) within the source located at generated the interrupt then serve it. If there are multiple interrupts and pending, the cycle repeats until all the interrupts are served. The Global Interrupt Address is shown as Table 2.

Table 2:

Global Interrupt Address

0xC1 Value	Interrupt Source	Interrupt Address
0x00	SYSTEM	0x00
0x10	REG1	0x12
0x20	REG2	0x22
0x30	REG3	0x32
0x50	REG5	0x51
0x60	REG6	0x61
0x70	REG7	0x71
0x80	REG8	0x81
0xA0	APCH	0xA8, 0xA9
0xB0	OTG	0xB0, 0xB2

Housekeeping Functions

Programmable System Voltage Monitor

The ACT8600 features a programmable system-voltage monitor, which monitors the voltage at VSYS and compares it to a programmable threshold voltage. The VSYSMON comparator is designed to be immune to VSYS noise resulting from switching, load transients, etc. The VSYSMON comparator is disable by default; to enable it, set the SYSLEV[3:0] register to one of the value in Table 3. Note that there is a 200mV hysteresis between the rising and falling threshold for the comparator. The VSYSDAT [ ] bit reflects the output of the VSYSMON comparator. The value of VSYSDAT[ ] is 1 when V_{VSYS} < SYSLEV; value is 0 otherwise.

The VSYSMON comparator can generate an interrupt when V_{VSYS} is lower than SYSLEV[ ] voltage. The interrupt is masked by default by can be unmasked by setting nSYSLEVMSK[ ] = 1.

FUNCTIONAL DESCRIPTION CONT'D

Table 3:

SYSLEV Falling Threshold

SYSLEV[3:0]	SYSLEV Falling Threshold
1000	3.3
1001	3.4
1010	3.5
1011	3.6
1100	3.7
1101	3.8
1110	3.9
1111	4.0

Thermal Protection

The ACT8600 integrates thermal shutdown protection circuitry to prevent damage resulting from excessive thermal stress, as may be encountered under fault conditions.

Thermal Interrupt

If the thermal interrupt is unmasked (by setting nTMSK[ ] to 1), ACT8600 can generate an interrupt when the die temperature reaches 120°C (typ).

Thermal Protection

If the ACT8600 die temperature exceeds 160°C, the thermal protection circuitry disables all regulators and prevents the regulators from being enabled until the IC temperature drops by 20°C (typ).

STEP-DOWN DC/DC REGULATORS

General Description

REG1, REG2 and REG3 are fixed-frequency, current-mode, synchronous PWM step-down converters that achieves peak efficiencies of up to 97%. These regulators operate with a fixed frequency of 2.22MHz, minimizing noise in sensitive applications and allowing the use of small external components. Additionally, REG1, REG2 and REG3 are available with a variety of standard and custom output voltages, and may be software-controlled via the I^2C interface for systems that require advanced power management functions.

Output Current Capability

REG1, REG2, and REG3 are capable of supplying 1200mA, 1200mA and 950mA output current, respectively.

100% Duty Cycle Operation

REG1, REG2 and REG3 are capable of operating at up to 100% duty cycle. During 100% duty cycle operation, the high-side power MOSFETs are held on continuously, providing a direct connection from the input to the output (through the inductor), ensuring the lowest possible dropout voltage in battery powered applications.

Operating Mode

By default, REG1, REG2, and REG3 operate in fixed-frequency PWM mode at medium to heavy loads, then transition to a proprietary power-saving mode at light loads in order to save power.

Synchronous Rectification

REG1, REG2, and REG3 each feature integrated synchronous rectifiers, maximizing efficiency and minimizing the total solution size and cost by eliminating the need for external rectifiers.

Soft-Start

REG1, REG2 and REG3 include internal 500 us soft-start ramps which limit the rate of change of the output voltage, minimizing input inrush current and ensuring that the output powers up in a monotonic manner that is independent of loading on the outputs. This circuitry is effective any time the regulator is enabled, as well as after responding to a short-circuit or other fault condition.

Compensation

REG1, REG2 and REG3 utilize current-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. No compensation design is required; simply follow a few simple guide lines described below when choosing external components.

Input Capacitor Selection

The input capacitor reduces peak currents and noise induced upon the voltage source. A 4.7µF ceramic capacitor is recommended for each regulator in most applications.

Output Capacitor Selection

REG1, REG2 and REG3 were designed to take advantage of the benefits of ceramic capacitors, namely small size and very-low ESR. REG1, REG2 and REG3 are designed to operate with 22uF output capacitor over most of their output voltage ranges, although more capacitance may be desired depending on the duty cycle and load step requirements.

Inductor Selection

REG1, REG2, and REG3 utilize current-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. These devices were optimized for operation with 3.3µH inductors, although inductors in the 2.2µH to 4.7µH range can be used.

Configuration Options

Output Voltage Programming

By default, REG1, REG2 and REG3 power up and regulate to their default output voltages. Once the system is enabled, the output voltages may be modified through either the I^2C interface by writing to the VSET[ ] register. Using I^2C, the output voltage may be programmed to any voltage as shown in Table 4.

Interrupts

REG1, REG2 and REG3 may optionally interrupt the processor if their output voltages fall out regulation. Enable interrupts by setting a regulator's nFLTMSK[ ] bit.

CONFIGURABLE STEP-UP DC/DC

General Description

The step-up DC/DC is a highly efficient step-up DC/DC converter that employs a fixed frequency, current-mode, PWM architecture. This regulator is optimized for 5V applications as well as white-LED bias applications consisting of up to ten white-LEDs.

5V Applications

The boost converter is configured by default to provide a fixed 5V output voltage, without requiring external feedback resistors. Contact the factory for other voltage options.

In order to provide improved operation under very low duty-cycle conditions, such as when operating from a fully-charged Li+ cell to 5V, the boost converter may optionally be configured to operate at half of the frequency of the buck regulators.

Compensation and Stability

The boost regulator utilizes current-mode control and an internal compensation network to optimize transient performance, ease compensation, and improve stability over a wide range of operating conditions.

Inductor Selection

REG4 is optimized for operation with inductors in the 4.7uH to 10uH range, although larger inductor values of up to 22uH can be used to achieve the highest possible efficiency.

Input and Output Capacitor Selection

For 5V operation, a 10uF ceramic capacitor should be connected to the input and output of OUT4 respectively. A larger output capacitor may be used to minimize output voltage ripple if needed.

Rectifier Selection

The boost regulator requires a Schottky diode to rectify the inductor current. Select a low forward voltage drop Schottky diode with a forward current rating that is sufficient to support the maximum switch current of 900mA (typ) and a sufficient peak repetitive reverse voltage (VRRM) to support the output voltage.

Configuration Options

Output Voltage Programming

By default, the boost regulator powers up and regulates to its default output voltages. Once the system is enabled, the output voltages may be modified through either the I^2C interface by writing to the VSET[ ] register. Using I^2C, the output voltage may be programmed to any voltage as shown in Table 6.

Enabling the Boost Regulator

The boost regulator feature independent enable/disable control via the I^2C serial interface. Independently enable or disable the boost by writing to the ON[ ] bit for REG4.

Power-OK

The boost regulator features a power-OK status bit (OK[ ]) that can be read by the system microprocessor via the I^2C interface. If an output voltage is lower than the power-OK threshold, typically 6% below the programmed regulation voltage, this bit clears to 0.

LOW-DROPOUT LINEAR REGULATORS

General Description

The REG5, REG6, REG7 and REG8 are low-noise, low-dropout linear regulators (LDOs) that are optimized for low noise and high-PSRR operation.

LDO Output Voltage Programming

The REG5, REG6, REG7 and REG8 feature independently-programmable output voltages that are set via the I^2C serial interface, increasing flexibility while reducing total solution and size and cost. Set the output voltage by writing to the LDO's VSET[ ] register. Each LDO's VSET[ ] register provides the following output voltage options as shown in Table 5.

In order to ensure safe operation under over-load conditions, each LDO features current-limit circuitry with current fold-back. The current-limit the current that can be drawn from the output, providing protection in overload conditions. For additional protection under extreme over current conditions, current-fold-back protection reduces the current-limit by approximately 50% under extreme overload conditions.

Enabling and Disabling the LDOs

All LDOs feature independent enable/disable control via the I^2C serial interface. Independently enable or disable each output by writing to the appropriate ON[ ] bit.

Power-OK

The REG5, REG6, REG7 and REG8 feature a power-OK status bit (OK[ ]) that can be read by the system microprocessor via the I^2C interface. If an output voltage is lower than the power-OK threshold, typically 11% below the programmed regulation voltage, this bit clears to 0.

Interrupts

Each LDO may optionally interrupt the processor if its output voltage falls out of regulation. Enable interrupts by setting a regulator's nFLTMSK[ ] bit.

Optional LDO Output Discharge

The REG5, REG6, REG7 and REG8 feature optional output voltage discharge. When this feature is enabled, the LDO output is discharged to ground through a 1.5kΩ resistance when the LDO is shutdown. This feature may be enabled or disabled via the I^2C interface by writing to an LDO's DIS[ ] bit.

Output Capacitor Selection

The REG5, REG6, REG7 and REG8 require just a small 2.2uF ceramic capacitor for stability. For best performance, each output capacitor should be connected directly between each output and ground, with a short and direct connection. High quality ceramic capacitors such as X7R and X5R dielectric types are strongly recommended.

Backup Battery Charger

REG9 is always-on and REG10 is low-dropout linear regulators (LDO). They both feature low-quiescent supply current, and current-limit protection, and are ideally suited for always-on power supply applications, such as for a real-time clock, or as a backup-battery or super-cap charger.

REG9 features internal circuitry that limits the reverse supply current to less than 1uA when the input voltage falls below the output voltage, as can be encountered in backup-battery charging applications. REG9 internal circuitry monitors the input and the output, and disconnects internal circuitry and parasitic diodes when the input voltage falls below the output voltage, greatly minimizing backup battery discharge. The always-ON LDOs also feature a constant current-limit, which protects the IC under output short-circuit conditions as well as provides a constant charge current. When operating as a backup battery charger.

Figure 3:

Always ON LDO

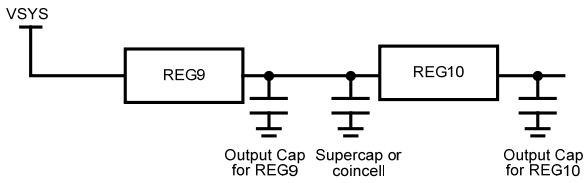


Table 4:

VSET[ ] Output Voltage Setting of DC/DC Step-Down Regulators (REG1—REG3)

REGx/VSET[2:0]	REGx/VSET[5:3]							
	000	001	010	011	100	101	110	111
000	0.600	0.800	1.000	1.200	1.600	2.000	2.400	3.200
001	0.625	0.825	1.025	1.250	1.650	2.050	2.500	3.300
010	0.650	0.850	1.050	1.300	1.700	2.100	2.600	3.400
011	0.675	0.875	1.075	1.350	1.750	2.150	2.700	3.500
100	0.700	0.900	1.100	1.400	1.800	2.200	2.800	3.600
101	0.725	0.925	1.125	1.450	1.850	2.250	2.900	3.700
110	0.750	0.950	1.150	1.500	1.900	2.300	3.000	3.800
111	0.775	0.975	1.175	1.550	1.950	2.350	3.100	3.900

Table 5:

VSET[ ] Output Voltage Setting of Low-Noise LDO Regulators (REG5—REG8)

REGx/VSET[2:0]	REGx/VSET[5:3]							
	000	001	010	011	100	101	110	111
000	0.600	0.800	1.000	1.200	1.600	2.000	2.400	3.200
001	0.625	0.825	1.025	1.250	1.650	2.050	2.500	3.300
010	0.650	0.850	1.050	1.300	1.700	2.100	2.600	3.400
011	0.675	0.875	1.075	1.350	1.750	2.150	2.700	3.500
100	0.700	0.900	1.100	1.400	1.800	2.200	2.800	3.600
101	0.725	0.925	1.125	1.450	1.850	2.250	2.900	3.700
110	0.750	0.950	1.150	1.500	1.900	2.300	3.000	3.800
111	0.775	0.975	1.175	1.550	1.950	2.350	3.100	3.900

Table 6:
VSET[ ] Output Voltage Setting of DC/DC Step-Up Regulator

REGx/VSET[4:0]	REGx/VSET[7:5]							
	000	001	010	011	100	101	110	111
00000	3.000	3.000	3.000	6.200	9.400	12.600	19.000	31.800
00001	3.000	3.000	3.100	6.300	9.500	12.800	19.400	32.200
00010	3.000	3.000	3.200	6.400	9.600	13.000	19.800	32.600
00011	3.000	3.000	3.300	6.500	9.700	13.200	20.200	33.000
00100	3.000	3.000	3.400	6.600	9.800	13.400	20.600	33.400
00101	3.000	3.000	3.500	6.700	9.900	13.600	21.000	33.800
00110	3.000	3.000	3.600	6.800	10.000	13.800	21.400	34.200
00111	3.000	3.000	3.700	6.900	10.100	14.000	21.800	34.600
01000	3.000	3.000	3.800	7.000	10.200	14.200	22.200	35.000
01001	3.000	3.000	3.900	7.100	10.300	14.400	22.600	35.400
01010	3.000	3.000	4.000	7.200	10.400	14.600	23.000	35.800
01011	3.000	3.000	4.100	7.300	10.500	14.800	23.400	36.200
01100	3.000	3.000	4.200	7.400	10.600	15.000	23.800	36.600
01101	3.000	3.000	4.300	7.500	10.700	15.200	24.200	37.000
01110	3.000	3.000	4.400	7.600	10.800	15.400	24.600	37.400
01111	3.000	3.000	4.500	7.700	10.900	15.600	25.000	37.800
10000	3.000	3.000	4.600	7.800	11.000	15.800	25.400	38.200
10001	3.000	3.000	4.700	7.900	11.100	16.000	25.800	38.600
10010	3.000	3.000	4.800	8.000	11.200	16.200	26.200	39.000
10011	3.000	3.000	4.900	8.100	11.300	16.400	26.600	39.400
10100	3.000	3.000	5.000	8.200	11.400	16.600	27.000	39.800
10101	3.000	3.000	5.100	8.300	11.500	16.800	27.400	40.200
10110	3.000	3.000	5.200	8.400	11.600	17.000	27.800	40.600
10111	3.000	3.000	5.300	8.500	11.700	17.200	28.200	41.000
11000	3.000	3.000	5.400	8.600	11.800	17.400	28.600	41.400
11001	3.000	3.000	5.500	8.700	11.900	17.600	29.000	41.400
11010	3.000	3.000	5.600	8.800	12.000	17.800	29.400	41.400
11011	3.000	3.000	5.700	8.900	12.100	18.000	29.800	41.400
11100	3.000	3.000	5.800	9.000	12.200	18.200	30.200	41.400
11101	3.000	3.000	5.900	9.100	12.300	18.400	30.600	41.400
11110	3.000	3.000	6.000	9.200	12.400	18.600	31.000	41.400
11111	3.000	3.000	6.100	9.300	12.500	18.800	31.400	41.400

USB OTG

General Description

When the system is acting as a USB OTG A-device, the OTG subsystem can provide power to VBUS from either 5VIN via Q1 or CHGIN via Q2 as shown in the figure. If VBUS is connected to a charger (either a charging port, a USB host or Hub, or a PC), the battery will be charged via Q3 (see Single-Cell Li+ ActivePath™ Charger section).

5VIN to VBUS (Q1)

Q1 is a PMOS switch that can provide 5V supply to VBUS from 5VIN pin which is typically connected to the output of the Boost regulator (REG4). Q1 is controlled by ONQ1[ ].

The current for Q1 is limited at 700mA to protect the Boost regulator or external source connected at 5VIN from overloaded. If the current across Q1 is over the limitation for more than 256ms, the switch is turned off automatically. A 0 to 1 transition on ONQ1[ ] is needed to turned Q1 on again after a over-current condition.

Q1 may optionally interrupt the processor when there is a over-current condition. Enable interrupts by setting the nFLTMSKQ1[ ] bit.

CHGIN to VBUS (Q2)

Q2 is a NMOS switch that can power VBUS from CHGIN. If Q2 is controlled by ONQ2[ ] and can only be turned on if Q1 is turned off.

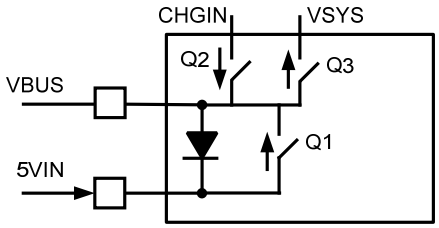
The current for Q2 is limited at 700mA prevent the external source connected at CHGIN from overloaded. If the current across Q2 is over the limitation for more than 256ms, the switch is turned off automatically. A 0 to 1 transition on ONQ2[ ] is needed to turned Q2 on again after a over-current condition.

Q2 also features an over voltage protection function. When the voltage at CHGIN is above 6V, Q2 is turned off automatically to avoid an over-voltage condition at VBUS.

Q2 may optionally interrupt the processor when there is a over-current condition. Enable interrupts by setting the nFLTMSKQ2[ ] bit.

Figure 4:

USB OTG subsystem



Single-Cell Li+ *ActivePath™* Charger

General Description

The charger features an advanced battery charger that incorporates the patent-pending *ActivePath™* architecture for system power selection. This combination of circuits provides a complete, advanced battery-management system that automatically selects the best available input supply, manages charge current to ensure system power availability, and provides a complete, high-accuracy (±0.5%), thermally regulated, full-featured single-cell linear Li+ Charger that can withstand input voltages of up to 12V at CHGIN.

ActivePath™ Architecture

The *ActivePath™* architecture performs three important functions:

1) System Configuration Optimization
2) Input Protection
3) Battery-Management

System Configuration Optimization

The *ActivePath* circuitry monitors the state of the input supply, the battery, and the system, and automatically reconfigures itself to optimize the power system. If a valid input supply at either CHGIN or VBUS is present, *ActivePath* powers the system from the input while charging the battery in parallel. Of the two possible charging sources, CHGIN is the preferred one over VBUS to allow the battery to charge as quickly as possible, while supplying the system. If a valid input supply is not present, *ActivePath* powers the system from the battery. If the input is present and the system current requirement exceeds the capability of the input supply, *ActivePath* allows system power to be drawn from both the battery and the input supply. Note that the battery will not be charged from VBUS pin when VBUS is supplied by the 5VIN pin (through Q1).

Input Protection for CHGIN

Input Over-Voltage Protection

The *ActivePath™* circuitry features input over-voltage protection circuitry for CHGIN. This circuitry disables charging when the input voltage exceeds the voltage set by OVPSET[ ], but stands off the input voltage in order to protect the system. Note that the adjustable OVP threshold is intended to provide the charge cycle with adjustable immunity against upward voltage transients on the input, and is not intended to allow continuous charging with input voltages above the charger's normal operating voltage range. Independent of the OVPSET[ ] setting, the charge cycle is not allowed to continue until the input voltage falls back into the charger's normal operating voltage range (i.e. below 6.0V).

In an input over-voltage condition this circuit limits V_{VSYS} to 4.6V, protecting any circuitry connected to V_{VSYS} from the over-voltage condition, which may exceed this circuitry's voltage capability. This circuit is capable of withstanding input voltages of up to 12V.

Table 7:
Input Over-Voltage Protection Setting

OVPSET[0]	OVP THRESHOLD
0	6.6V
1	7.0V

Input Supply Overload Protection

The *ActivePath™* circuitry monitors and limits the total current drawn from the input supply to a value set by the CHGIN/VBUS configuration and CHGLEV inputs, as well as the resistor connected to ISET. When charging from VBUS pin, the input current is limited to either 75mA, when CHGLEV is driven to a logic-low, or 450mA, when CHGLEV is driven to a logic-high. When charging from CHGIN, the input current is limited to 2.25A, typically.

Input Under Voltage Lockout

If the input voltage applied to CHGIN falls below 3.5V (typ), an input under-voltage condition is detected and the charger is disabled. Once an input under-voltage condition is detected, a new charge cycle will initiate when the input exceeds the under-voltage threshold by at least 500mV.

Battery Management

The ACT8600 features a full-featured, intelligent charger for Lithium-based cells, and was designed specifically to provide a complete charging solution with minimum system design effort.

The core of the charger is a CC/CV (Constant-Current/Constant-Voltage), linear-mode charge controller. This controller incorporates current and voltage sense circuitry, an internal 70mΩ power MOSFET, thermal-regulation circuitry, a full-featured state-machine that implements charge control and safety features, and circuitry that eliminates the reverse blocking diode required by conventional charger designs.

The charge termination voltage is highly accurate (±0.5%), and features a selection of charge safety timeout periods that protect the system from operation with damaged cells. Other features include pin-programmable fast-charge current and one current-limited nSTAT output that can directly drive LED indicator or provide a logic-level status signal to the host microprocessor.

Dynamic Charge Current Control (DCCC)

The ACT8600's *ActivePath™* charger features dynamic charge current control (DCCC) circuitry, which acts to ensure that the system remains powered while operating within the maximum output capability of the power adapter. The DCCC circuitry continuously monitors VSYS, and if the voltage at VSYS drops by more than 200mV, the DCCC circuitry automatically reduces charge current in order to prevent VSYS from continuing to drop.

Charge Current Programming

The ACT8600's *ActivePath™* charger features a flexible charge current-programming scheme that combines the convenience of internal charge current programming with the flexibility of resistor based charge current programming. Current limits and charge current programming are managed as a function of the CHGIN/VBUS configuration and CHGLEV pins, in combination with R_{ISET}, the resistance connected to the ISET pin.

When charging from CHGIN, the charger operates in “AC-mode' with a charge current programmed by R_{ISET}, and charge current is given by:

R_{ISET} (kΩ) = 2336 × (1V/I_{CHG}(mA)) - 0.205

When charging from VBUS, the charger operates in “USB-Mode”, with a maximum charge current defined by the CHGLEV input, and Q3DBILIM[ ] settings as summarized in Table 8.

Note that the actual charge current may be limited to a current lower than the programmed fast charge current due to the ACT8600’s internal thermal regulation loop. See the *Thermal Regulation* section for more information.

Charger Input Interrupts

In order to ease input supply detection and eliminate the size and cost of external detection circuitry, the charger has the ability to generate interrupts based upon the status of the input supply. This function is capable of generating an interrupt when the input is connected, disconnected, or both.

CHGIN Detection

An interrupt is generated any time the input supply is connected to CHGIN when INSTAT[ ] bit is set to 1 and the INCON[ ] bit is set to 1, and an interrupt is generated any time the input supply is disconnected when INSTAT[ ] bit is set to 1 and the INDIS[ ] bit is set to 1.

The status of the input may be read at any time by reading the INDAT[ ] bit, where a value of 1 indicates that the valid input (V_{CHGIN} UVLO<V_{CHGIN}<V_{OVP}) is present, and a value of 0 indicates that a valid input is not present. Reading the INSTAT[ ] bit indicates when the input has generated an interrupt; this bit will normally return a value of 0, but will return value of 1 when an input interrupt has been generated then the interrupt is automatically cleared to 0 upon reading.

VBUS Detection

When a valid input supply is connected to VBUS, an interrupt is generated when INVBUSR[ ] and nVBUSMSK[] is set. Similarly, an interrupt is generated when the input supply is disconnected from VBUS when INVBUSF[ ] and nVBUSMSK[ ] is set. The value of VBUSSTAT[ ], which indicate the status of VBUS interrupts, is 1 if an interrupt is generated by either INVBUSR[ ] or INVBUSF[ ]. VBUSDAT[ ] provides the real time status of VBUS and its value is 1 when a valid charging source is present at VBUS.

Table 8:

Charge Current Programming

CHARGING SOURCE	CHGLEV	Q3DBILIM	CHARGE CURRENT (mA)	PRECONDITION CHARGE CURRENT (mA)
VBUS	0	-	Min (75mA, I_{CHG})	Min (75mA, 10% × I_{CHG})
VBUS	1	0	Min (450mA, I_{CHG})	10% × I_{CHG}
VBUS	1	1	Min (900mA, I_{CHG})	10% × I_{CHG}
CHGIN	-	-	I_{CHG}	10% × I_{CHG}

Charge-Control State Machine

PRECONDITION State

A new charging cycle begins with the PRECONDITION state, and operation continues in this state until V_{BAT} exceeds the Precondition Threshold Voltage. When operating in PRECONDITION state, the cell is charged at 10% of the programmed maximum fast-charge constant current, I_{CHG}.

Once V_{BAT} reaches the Precondition Threshold Voltage, the state machine jumps to the FAST-CHARGE state. If V_{BAT} does not reach the Precondition Threshold Voltage before the Precondition Timeout period expires, then the state machine jumps to the TIMEOUT-FAULT state in order to prevent charging a damaged cell. See the *Charge Safety Timers* section for more information.

FAST-CHARGE State

In the FAST-CHARGE state, the charger operates in constant-current (CC) mode and regulates the charge current to the current set by R_{ISET}. Charging continues in CC mode until V_{BAT} reaches the charge termination voltage (V_{TERM}), at which point the state-machine jumps to the TOP-OFF state. If V_{BAT} does not reach V_{TERM} before the total time out period expires then the state-machine will jump to the "EOC" state and will re-initiate a new charge cycle after 32ms "relax". See the *Current Limits* and *Charge Current Programming* sections for more information about setting the maximum charge current.

TOP-OFF State

In the TOP-OFF state, the cell charges in constant-voltage (CV) mode. In CV mode operation, the charger regulates its output voltage to the 4.20V charge termination voltage, and the charge current is naturally reduced as the cell approaches full charge. Charging continues until the charge current drops to END-OF-CHARGE current threshold, at which point the state machine jumps to the END-OF-CHARGE (EOC) state.

If the state-machine does not jump out of the TOP-OFF state before the Total-Charge Timeout period expires, the state machine jumps to the EOC state and will re-initiate a new charge cycle if V_{BAT} falls below termination voltage 205mV (typ). For more information about the charge safety timers, see the *Charging Safety Times* section.

END-OF-CHARGE (EOC) State

In the END-OF-CHARGE (EOC) state, the charger presents a high-impedance to the battery, minimizing battery current drain and allowing the cell to "relax". The charger continues to monitor the cell voltage, and re-initiates a charging sequence if the cell voltage drops to 205mV (typ) below the charge termination voltage.

SUSPEND State

The state-machine jumps to the SUSPEND state any time the battery is removed, and any time the input voltage falls below either the UVLO threshold or exceeds the OVP threshold. Once none of these conditions are present, a new charge cycle initiates.

A charging cycle may also be suspended manually by setting the SUSPEND[ ] bit. In this case, initiate a new charging sequence by clearing SUSPEND[ ] to 0.

State Machine Status

The charger features the ability to generate interrupts when the charger state machine transitions. Set CHGEOCIN[ ] bit to 1 and CHGSTAT[ ] bit to 1 to generate an interruption when the charger state machine goes into the END-OF-CHARGE (EOC) state. Set CHGEOCOUT[ ] bit to 1 and CHGSTAT[ ] bit to 1 to generate an interruption when the charger state machine exists the EOC state.

The status of the charge state machine may be read at any time by reading the CHGDAT[ ] bit, where a value of 1 indicates State Machine is in EOC state, and value is 0 when State Machine is in other states. Reading the CHGSTAT[ ] bit indicates when a state machine transition has generated an interrupt; this bit will normally return a value of 0, but will return value of 1 when a state transition occurs then automatically clear to 0 upon reading.

For additional information about the charge cycle, CSTATE[0:1] may be read at any time via I^2C to determine the current charging state.

Figure 5:
Typical Li+ charge profile and ACT8600 charge states

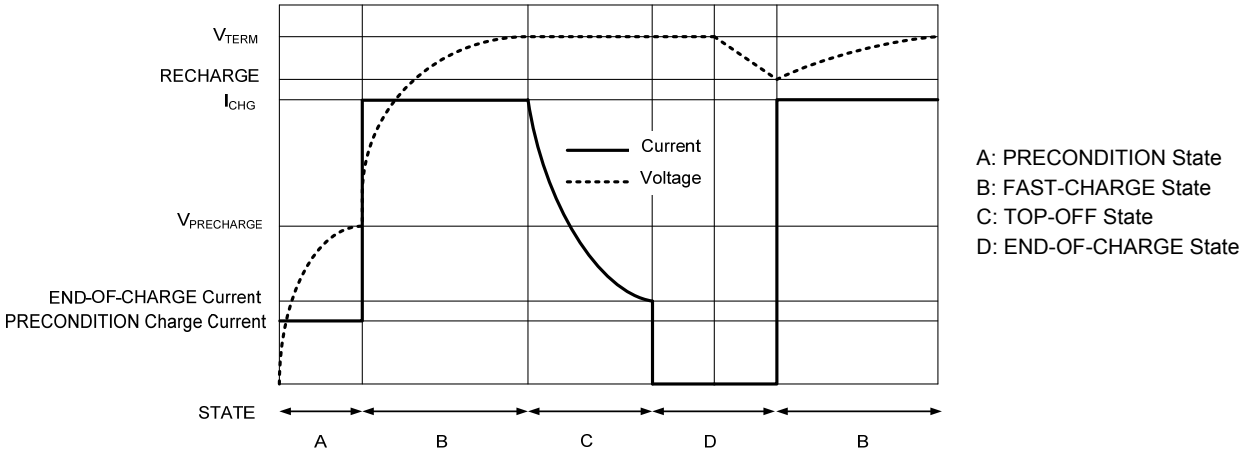


Figure 6:
Charger State Diagram

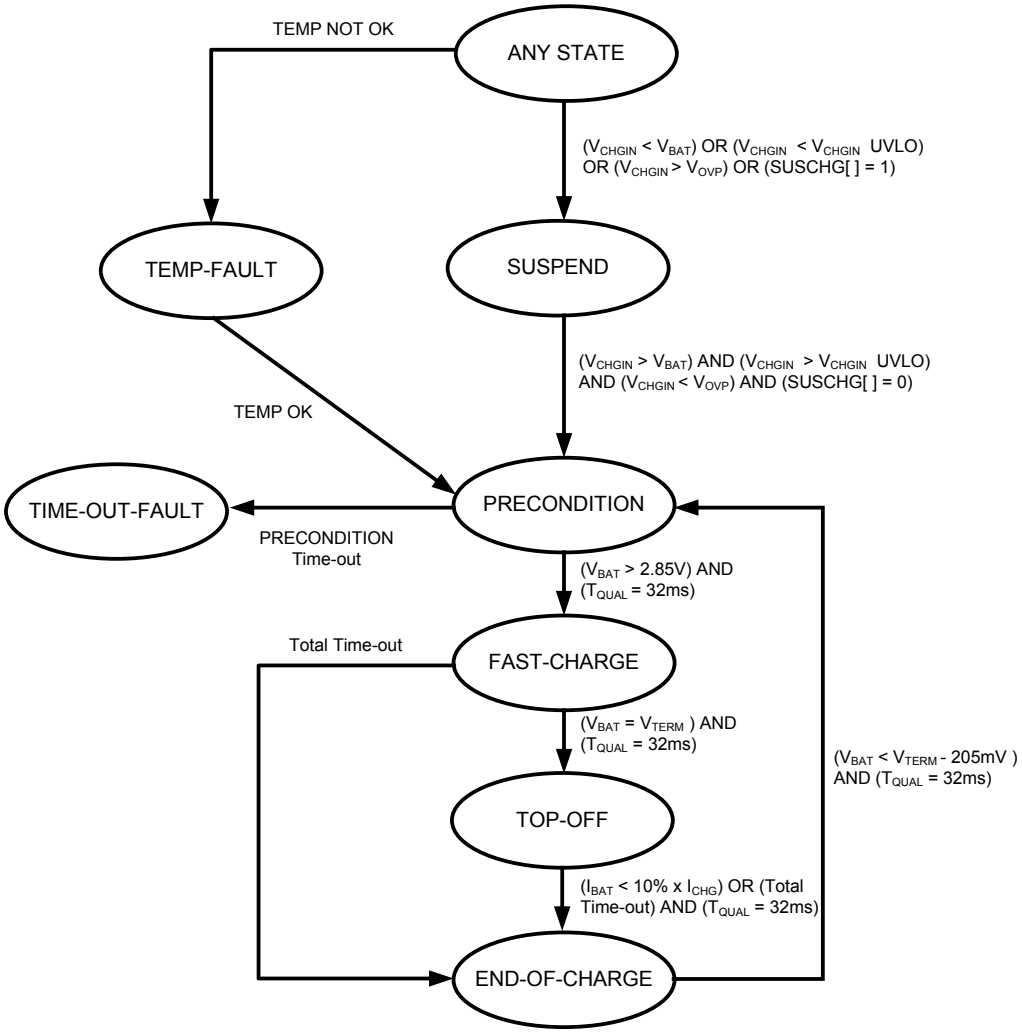


Table 9:
Charging Status Indication

CSTATE[0]	CSTATE[1]	STATE MACHINE STATUS
1	1	PRECONDITION
1	0	FAST-CHARGE/TOP-OFF
0	1	END-OF-CHARGE
0	0	SUSPEND/DISABLE/FAULT

Thermal Regulation

The charger features an internal thermal regulation loop that monitors die temperature and reduces charging current as needed to ensure that the die temperature does not exceed the thermal regulation threshold of 100°C. This feature protects against excessive junction temperature and makes the device more accommodating to aggressive thermal designs. Note, however, that attention to good thermal designs is required to achieve the fastest possible charge time by maximizing charge current.

Charge Safety Timers

The charger features programmable charge safety timers which help ensure a safe charge by detecting potentially damaged cells. These timers are programmable via the PRETIMO[1:0] and TOTTIMO[1:0] bits, as shown in Table 10 and Table 11. Note that in order to account for reduced charge current resulting from DCCC operation, the charge timeout periods are extended proportionally to the reduction in charge current. As a result, the actual safety period may exceed the nominal timer period.

The status of the charge timers may be read at any time by reading the TIMRDAT[ ] bit, where a value of 0 indicates that neither charge timer has expired, and a value of 1 indicates that one of the charge timers has expired.

Table 10:
PRECONDITION Safety Timer Setting

PRETIMO[1]	PRETIMO[0]	PRECONDITION TIMEOUT PERIOD
0	0	40 mins
0	1	60 mins
1	0	80 mins
1	1	Disabled

Table 11:
Total Safety Timer Setting

TOTTIMO[1]	TOTTIMO[0]	TOTAL TIMEOUT PERIOD
0	0	4 hrs
0	1	5 hrs
1	0	6.5 hrs
1	1	Disabled

Charge Status Indicator

The charger provides a charge-status indicator output, nSTAT. nSTAT is an open-drain output which sinks current when the charger is in an active-charging state, and is high-Z otherwise. nSTAT features an internal 8mA current limit, and is capable of directly driving a LED without the need of a current-limiting resistor or other external circuitry. To drive an LED, simply connect the LED between nSTAT pin and an appropriate supply, such as VSYS. For a logic-level charge status indication, simply connect a resistor from nSTAT to an appropriate voltage supply.

Table 12:
Charging Status Indication

STATE	nSTAT
PRECONDITION	Active
FAST-CHARGE	Active
TOP-OFF	Active
END-OF-CHARGE	High-Z
SUSPEND	High-Z
TEMPERATURE FAULT	High-Z
TIME-OUT FAULT	High-Z

Reverse-Current Protection

The charger includes internal reverse-current protection circuitry that eliminates the need for blocking diodes, reducing solution size and cost as well as dropout voltage relative to conventional battery chargers. When the voltage at CHGIN falls below V_{BAT}, the charger automatically reconfigures its power switch to minimize current drawn from the battery.

Battery Temperature Monitoring

In a typical application, the TH pin is connected to the battery pack's thermistor input, as shown in Figure 7. The charger continuously monitors the

temperature of the battery pack by injecting a 100µA (typ) current into the thermistor (via the TH pin) and sensing the voltage at TH. The voltage at TH is continuously monitored, and charging is suspended if the voltage at TH exceeds either of the internal V_{THH} and V_{THL} thresholds of 0.5V and 2.5V, respectively.

The net resistance (from TH to GA) required to cross the thresholds are given by:

100µA × RNOM × kHOT = 0.5V → RNOM × kHOT ≈ 5kΩ

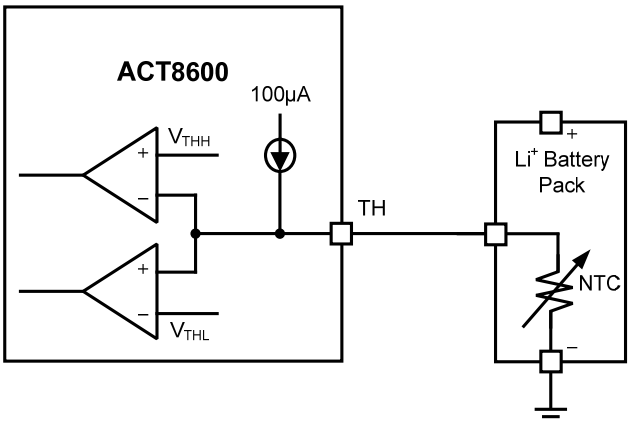
100µA × RNOM × kCOLD = 2.5V → RNOM × kCOLD ≈ 25kΩ

where RNOM is the nominal thermistor resistance at room temperature, and kHOT and kCOLD represent the ratios of the thermistor's resistance at the desired hot and cold thresholds, respectively, to the resistance at 25°C.

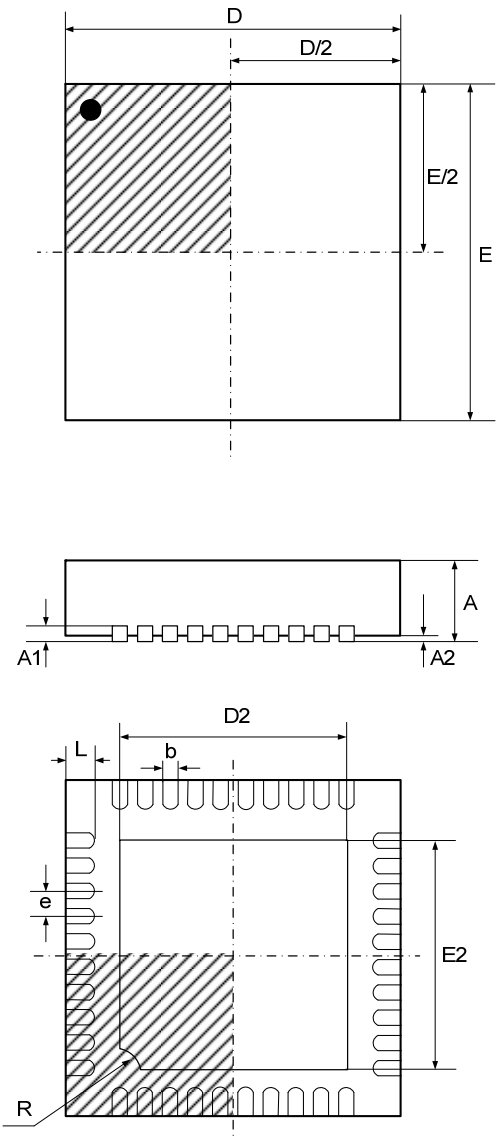
The status of the battery temperature pin may be read at any time by reading the TEMPDAT[ ] bit, where a value of 1 indicates that battery temperature is within the valid range, and a value of 0 indicates that battery temperature has exceeded either of the thresholds.

Figure 7:

Simple Configuration



TQFN55-40 PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILLIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.200 REF		0.008 REF	
A2	0.000	0.050	0.000	0.002
b	0.150	0.250	0.006	0.010
D	4.900	5.100	0.193	0.201
E	4.900	5.100	0.193	0.201
D2	3.450	3.750	0.136	0.148
E2	3.450	3.750	0.136	0.148
e	0.400 BSC		0.016 BSC	
L	0.300	0.500	0.012	0.020
R	0.300		0.012	

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- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
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- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

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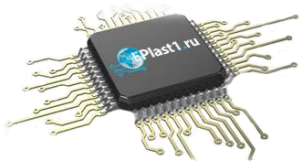
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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