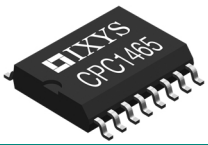
IXYS
INTEGRATED CIRCUITS DIVISION



CPC1465
SHDSL/ISDN DC Termination IC

Features
- Meets wetting (sealing) current requirements per ITU-T G.991.2
- Integrated bridge rectifier for polarity correction
- Uses inexpensive opto-coupler for DC signalling
- Electronic inductor, breakover, and latch circuits
- Current limiting and excess power protection circuits
- ANSI SHDSL and ISDN compatible
- MLT and SARTS compatible
- Compatible with portable test sets
- Excellent linearity
- Compatible with GlobespanVirata and Conexant SHDSL transceiver chip set families
- Small SOIC or DFN Package
- DFN package 60 percent smaller than SOIC
- SOIC is pin compatible with Agere LH1465AAE

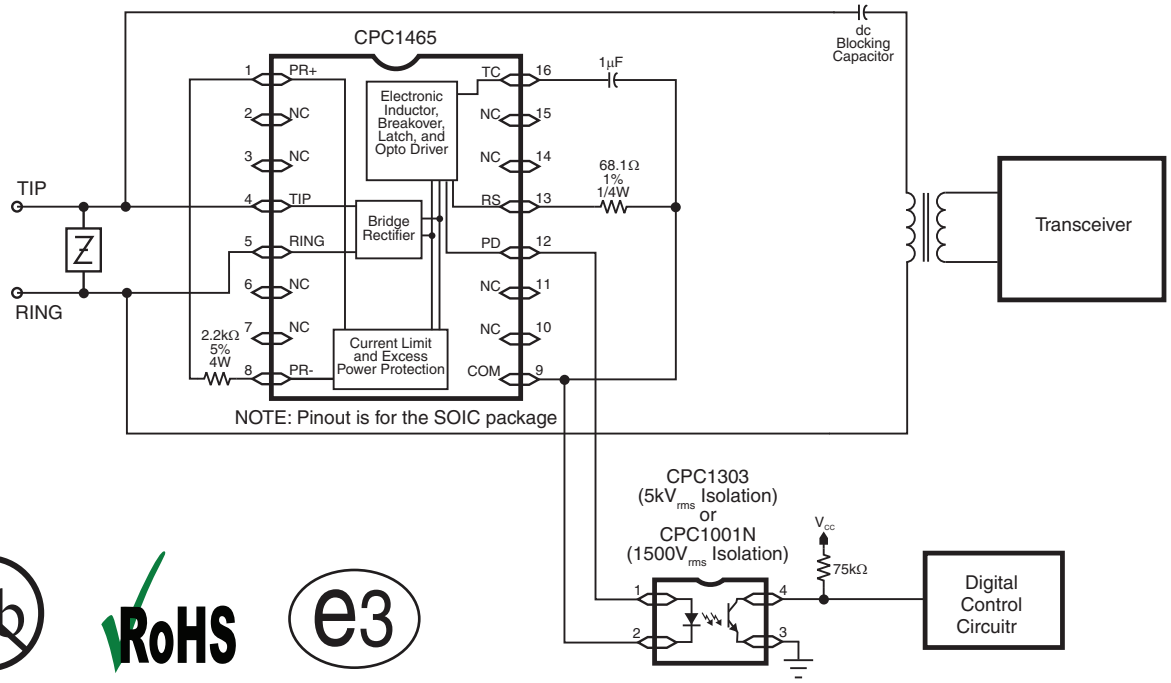
Applications
- Router and bridge customer premises equipment
- Leased line equipment
- T1/E1 network line cards and repeaters
- Network Termination 1 (NT1) equipment
- Mechanized Loop Test (MLT) networks
- Switched Access Remote Test System (SARTS) networks

Description
The CPC1465 is a DC termination IC used in Single-pair High-speed Digital Subscriber Line (SHDSL) and Integrated Services Digital Network subscriber line (ISDN) equipment. It provides a polarity insensitive DSL loop sealing current DC termination with a recognizable device signature for MLT systems. The CPC1465 passes low frequency ISDN network signalling information via an inexpensive optocoupler to the NT1's internal control logic.

Ordering Information

Part Number	Description
CPC1465D	DC Termination IC, 16-pin SOIC in tubes, 47/tube
CPC1465DTR	DC Termination IC, 16-pin SOIC tape and reel, 1000/reel
CPC1465M	DC Termination IC, 16-pin DFN in tubes, 52/tube
CPC1465MTR	DC Termination IC, 16-pin DFN tape and reel, 1000/reel

Figure 1. CPC1465 Typical 2-Wire DC Termination Application





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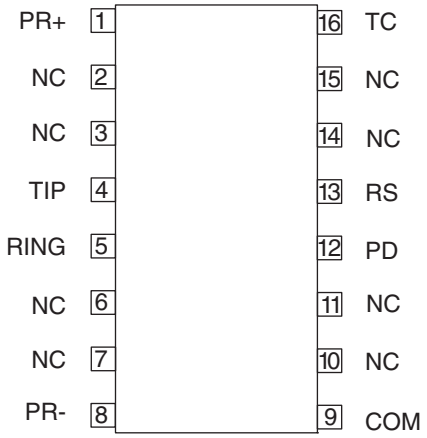
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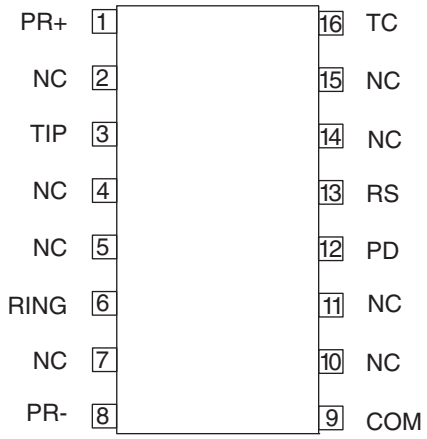
1. Specifications

1.1 Package Pinout

CPC1465D



CPC1465M



1.2 Pin Description

SOIC Pin	DFN Pin	Name	Description
1	1	PR+	Protection resistor positive side
2	2	NC	No connection
3		NC	No connection
4	3	TIP	Tip lead
	4	NC	No connection
	5	NC	No connection
5	6	RING	Ring lead
6		NC	No connection
7	7	NC	No connection
8	8	PR-	Protection resistor negative side
9	9	COM	Common
10	10	NC	No connection
11	11	NC	No connection
12	12	PD	Photo-diode (LED input current)
13	13	RS	Current limiting resistor
14	14	NC	No connection
15	15	NC	No connection
16	16	TC	Timing capacitor

1.3 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Maximum Voltage (T to R, R to T)*	-	300	V
Power dissipation	-	1	W
Operating temperature	-40	+85	°C
Operating relative humidity	5	95	%
Storage temperature	-40	+125	°C

**IXYS Integrated Circuits Division recommends the use of room-temperature-vulcanizing silicone RTV sealant on the SOIC package tip and ring pins (pins 4 and 5) to guard against the possibility of arcing.*

Electrical absolute maximum ratings are at 25°C.

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.4 Electrical Characteristics

Unless otherwise specified, minimum and maximum values are guaranteed by production testing requirements. Typical values are characteristic of the device and are the result of engineering evaluations. In addition, typical values are provided for informational purposes only and are not part of the testing requirements.

All electrical specifications are provided for T_A=25°C

1.4.1 DC Characteristics, Normal Operation

For operational templates: (see Figure 2 on page 5) and (see Figure 3 on page 5).

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Activate/Non-activate Voltage	Off State	V_{AN}	30.0	35.0	39.0	V
Breakover current	-	I_{BO}	-	0.5	1	mA
DC Voltage drop	Active State, 1 mA ≤ I_{SL} ≤ 20 mA	V_{ON}	-	12.5	15	V
DC leakage current	V_{OFF} = 20 V	I_{LKG}	-	1.5	5	µA
Hold/Release current	Active State	$I_{H/R}$	0.1	0.5	1.0	mA
Minimum on current	V_{ON} < 54 V	I_{MIN1}	20	38	-	mA
Minimum on current	54 V ≤ V_{ON} ≤ 100 V for 2 seconds, source resistance 200 Ω to 4 kΩ	I_{MIN2}	9.0	45	-	mA
Minimum on current	V_{ON} > 100 V	I_{MIN3}	0	0.1	-	mA
Maximum on current	V_{ON} ≤ 70 V	I_{MAX1}	-	38.4	70	mA
Maximum on current	V_{ON} > 70 V	I_{MAX2}	-	-	$\frac{V_{ON}}{1k\Omega}$	mA
Photodiode drive current	Active State	I_{PD}	0.2	0.3	10	mA

1.4.2 AC Characteristics, Normal Operation

For test conditions: (see Figure 4 on page 6) and (see Figure 5 on page 6).

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
ac impedance	200 Hz to 50 kHz	Z_{MT}	10	38	-	kΩ
Linearity distortion	f = 200 Hz to 40 kHz, I_{SL} = 1 mA to 20 mA, V_{APP} ≤ 10.5 V_{PP}	D1	75	78	-	dB
Linearity distortion	f = 200 Hz to 40 kHz, I_{SL} = 1 mA to 20 mA, V_{APP} ≤ 12 V_{PP}	D2	50	70	-	dB

1.4.3 Transition Characteristics, Normal Operation

For activation/deactivation test conditions: (see Figure 6 on page 7).

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Activate time	(see Figure 7 on page 7)	t1	3.0	13	50	ms
Deactivate time	(see Figure 8 on page 7)	t2	3.0	-	100	ms

Figure 2. I-V Requirements Template, 0 V to 50 V

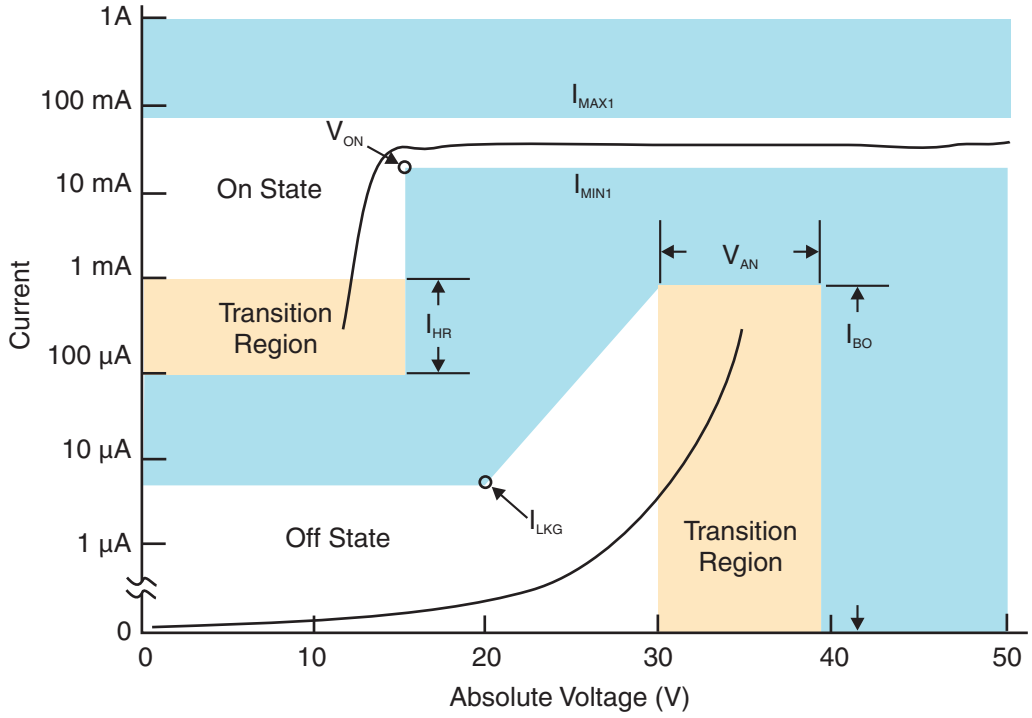


Figure 3. I-V Requirements Template, 0 V to 250 V

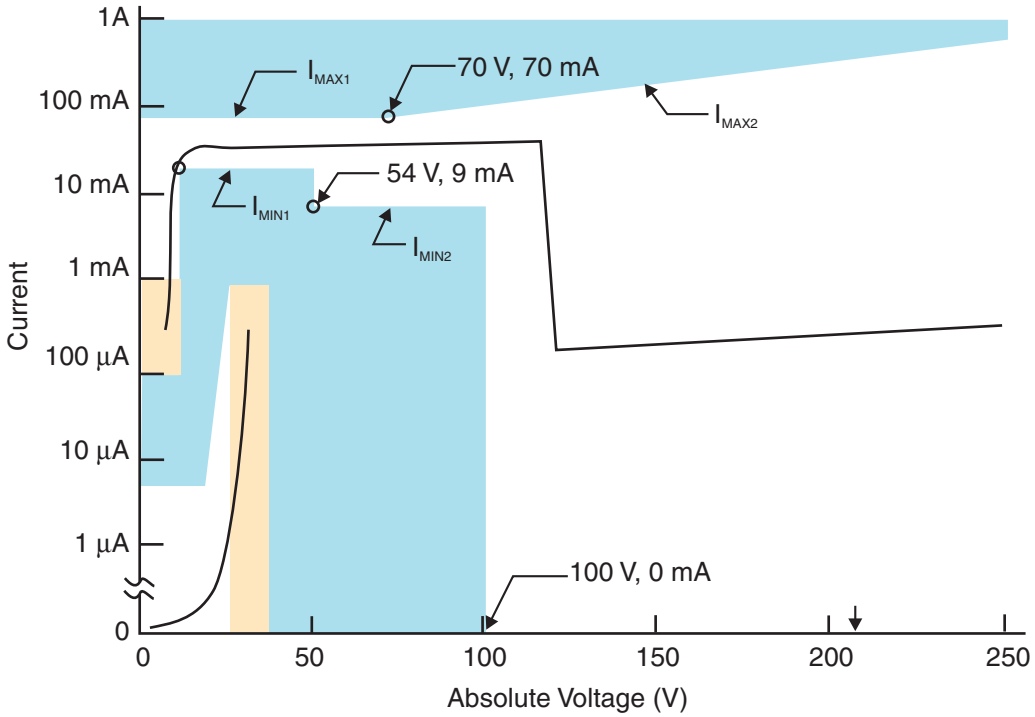
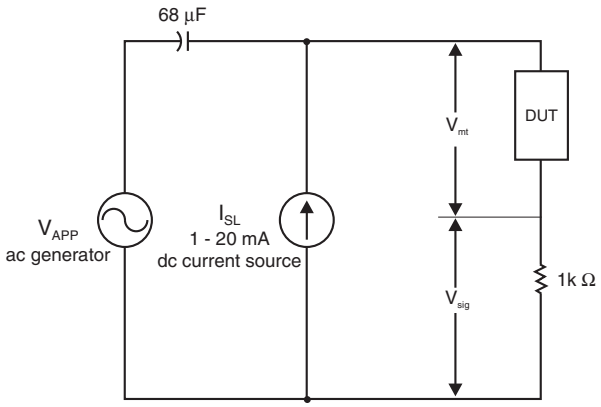


Figure 4. Test Circuit for ac Impedance and Linearity



$$Z_{mt} = \frac{1000 \times V_{mt}}{V_{sig}}$$

$$\text{Linearity} = 20\log\left[\frac{V_{mt}}{V_{sig2ndHarmonic}}\right] + 20\log\left[\frac{1000}{67.5}\right]$$

Figure 5. Linearity Requirement Template

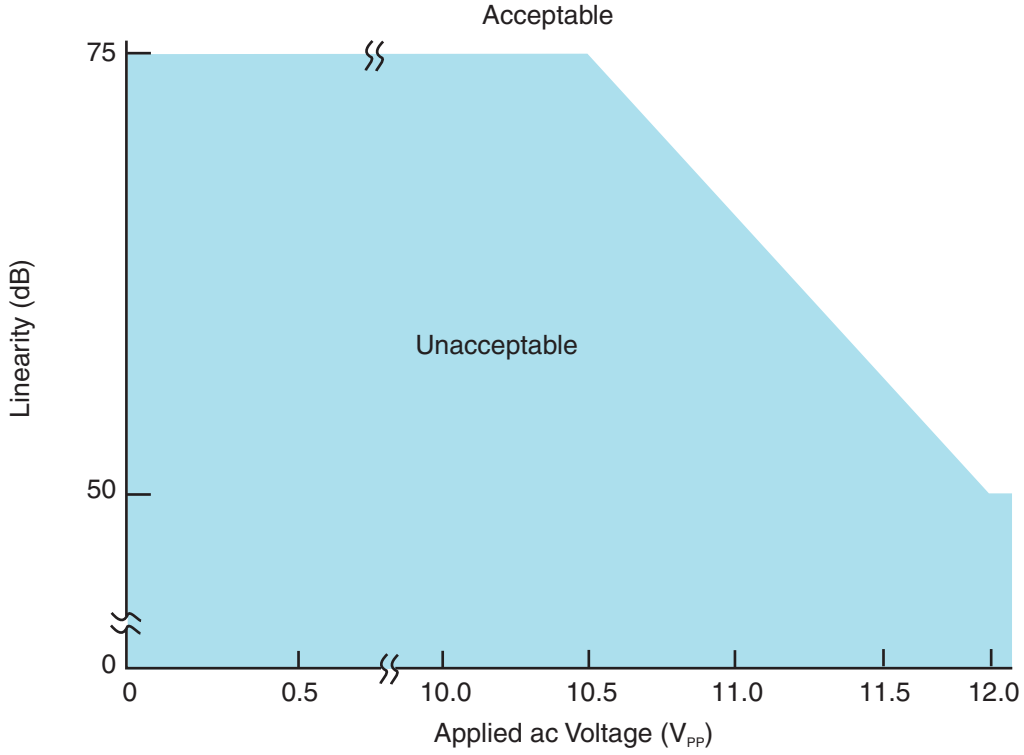


Figure 6. Test Circuit for Activate and Deactivate Times

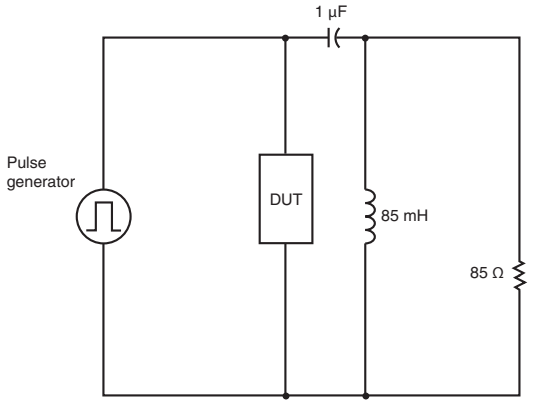


Figure 7. Applied Waveform for Activation Test

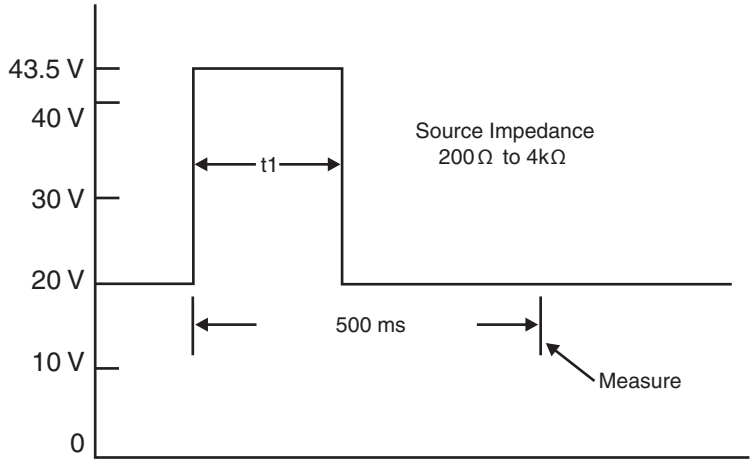
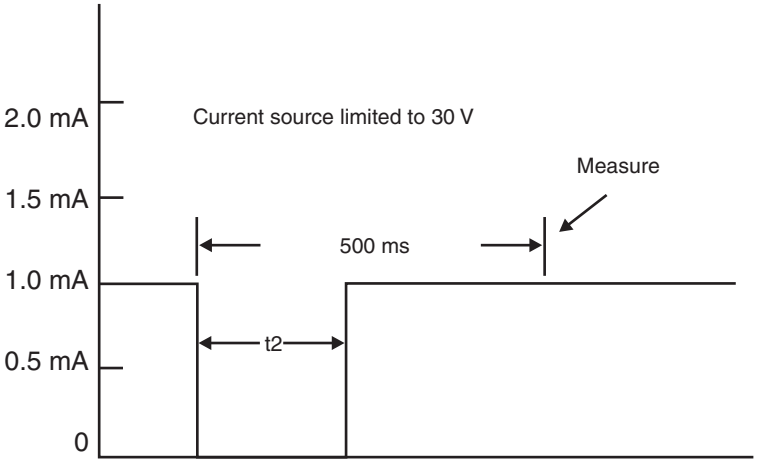


Figure 8. Applied Waveform for Deactivation Test



1.5 Application Signalling Characteristics

These tests assume crowbar protection across the CPC1465 limiting peak potentials to 250 V.

1.5.1 LED Trigger Characteristics During MLT Signalling

For test conditions: (see Figure 9 on page 9).

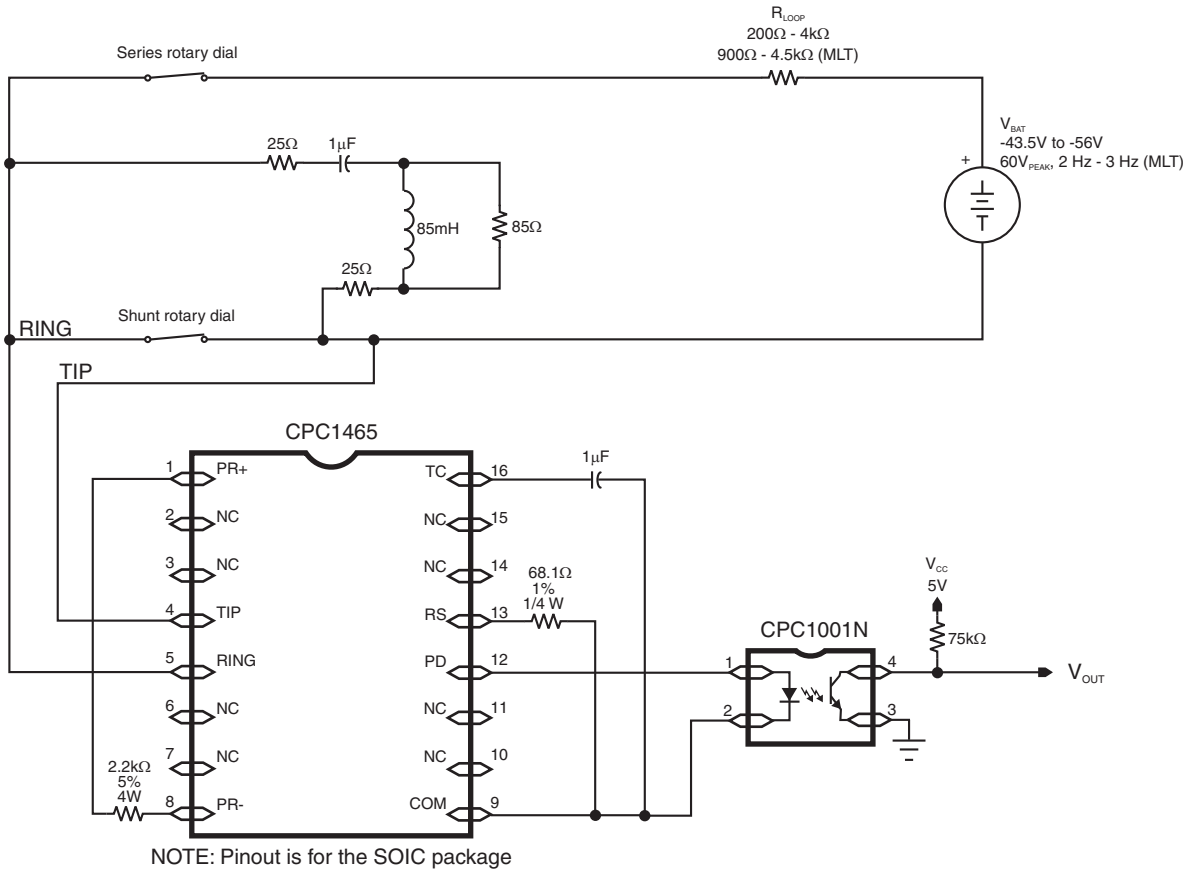
Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Applied ac Voltage	-	-	60	-	62	V_{PEAK}
Applied ac frequency	-	-	2	-	3	Hz
Number of half-cycles applied	-	-	6	-	10	-
Total loop resistance	-	-	900	-	4500	Ω
Required opto-coupler response						
Number of pulses per half-cycle applied	-	-	-	1	-	-
Pulse width (opto on)	(see Figure 9 on page 9)	T_{ON}	10	-	-	ms
Pulse width (opto off)	(see Figure 9 on page 9)	T_{OFF}	10	-	-	ms

1.5.2 LED Trigger Characteristics During Dial Test Set Signalling

For test conditions: (see Figure 9 on page 9).

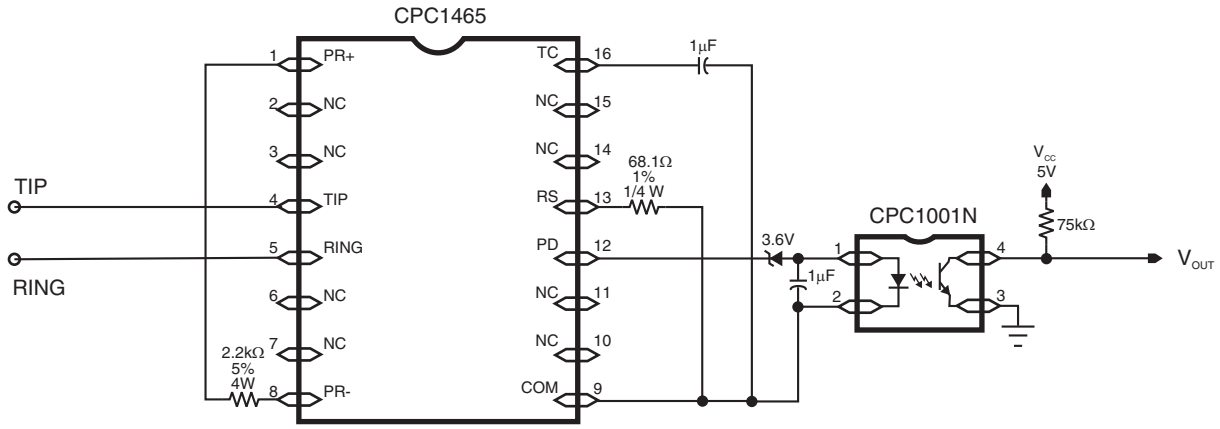
Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Applied dc battery Voltage	-	-	-43.5	-	-56	V_{DC}
Frequency (pulses per second)	-	-	4	-	8	-
Percent break	-	-	40	-	60	%
Number of pulses	-	-	6	-	10	-
Total Loop Resistance	-	-	200	-	4000	Ω
Required opto-coupler response						
Number of pulses per make/break applied	-	-	-	1	-	-
Pulse width (opto on)	(see Figure 9 on page 9)	T_{ON}	10	-	-	ms
Pulse width (opto off)	(see Figure 9 on page 9)	T_{OFF}	10	-	-	ms

Figure 9. Test Circuit for LED Operation



NOTE: Pinout is for the SOIC package

Figure 10. Typical ISDN NT1 Application Diagram



NOTE: Pinout is for the SOIC package

2. Functional Description

2.1 Introduction

The CPC1465 can be used for a number of designs requiring a dc hold circuit such as SHDSL modem and ISDN NT1 terminal applications. Typical SHDSL applications will use a circuit design similar to the one shown in Figure 10, “Typical ISDN NT1 Application Diagram” on page 9 while the typical ISDN NT1 circuit design will be similar to the one shown in Figure 10, “Typical ISDN NT1 Application Diagram” on page 9.

The DC Termination IC performs two functions in an ISDN NT1 terminal; as an electronic inductor providing a low impedance dc termination with a high impedance ac termination, and second as part of the dc signalling system for automated line testing capability. The CPC1465 meets or exceeds the requirements for an NT1 dc termination as described in ANSI T1.601-1991.

Whereas the SHDSL modem application does not have a signalling requirement, the signaling function provides an excellent method to monitor for the loss of sealing current. Generally, loss of sealing current in an SHDSL application indicates loop loss.

As can be seen in the application circuit in Figure 1 on page 1, CPC1465 designs require few external components. For the most basic design, all that is needed is a circuit protector, two resistors and a capacitor.

2.2 Surge Protection

Although the CPC1465 is current limited, it is not an over-voltage surge protector. To protect the CPC1465 against destructive over-voltage transients, IXYS Integrated Circuits Division recommends the use of a crowbar-type surge protector that limits the surge voltage seen by the CPC1465 to 250 V. The protection device must be able to withstand the surge requirements specified by the appropriate governing agency in regions where the product will be deployed. Teccor, Inc. and Bourns, Inc. make suitable surge protectors for most applications. Devices such as Teccor’s P1800SC or P2000SC Sidactors and Bourns’ TISP4220H3 or TISP4240H3 thyristors should provide suitable protection.

2.3 Bridge Rectifier

The bridge rectifier in the CPC1465 ensures that the device is polarity insensitive and provides consistent operational characteristics if the tip and ring leads are reversed.

2.4 State Transitions

The dc tip to ring voltage-current characteristics of the CPC1465 are shown in Figure 2, “I-V Requirements Template, 0 V to 50 V”, and in Figure 3, “I-V Requirements Template, 0 V to 250 V” on page 5.

Transition timings are illustrated in Figure 7, “Applied Waveform for Activation Test”, and in Figure 8, “Applied Waveform for Deactivation Test”. The test configuration for these timings is given in Figure 6, “Test Circuit for Activate and Deactivate Times”. All timing figures are located on page 7.

State transition timings are set by the 1 μF capacitor connected between the TC and COM pins.

2.4.1 Activation - On-State

Application of battery voltage to the loop causes the CPC1465 to conduct whenever the voltage exceeds approximately 35 V. With application of sufficient voltage applied across the tip and ring terminals, the CPC1465 will initially conduct a nominal 150 μA of sealing current for approximately 20 ms prior to activation. Once activated, the CPC1465 will remain in the on state for as long as the loop current exceeds a nominal 0.5 mA.

The CPC1465 turn-on timing circuit assures device activation will occur within 50 ms of an applied voltage greater than 43.5 V but not within the first 3 ms.

2.4.2 Deactivation - Off-State

While the CPC1465 activation protocol is based on an initial minimum voltage level, deactivation is based on a diminished sealing current level. Deactivation occurs when the nominal sealing current level drops below 0.5 mA with guaranteed deactivation occurring for sealing current levels less than 0.1 mA

The turn-off timing circuit deactivates the sealing current hold circuit when 1 mA of sealing current has been removed for 100 ms but ignores periods of loss up to 3 ms.

2.5 Photo-Diode (PD) Output Behavior

Output from the PD pin provides a minimum of 0.2 mA of photo-diode drive current for the opto-coupler LED anytime sealing current exceeds 1 mA.

Because LED current is interrupted whenever loop current is interrupted, the opto-coupler provides an excellent means of indicating loop availability for designs with a sealing current requirement.

2.6 On-State Behavior

2.6.1 Typical Conditions

On-state sealing current levels are determined by the network's power feed circuit and the loop's dc impedance. To compensate for low loop resistance or very high loop voltage, the CPC1465 limits the maximum sealing current to 70 mA.

The CPC1465 manages package power dissipation by shunting excess sealing current through the 2.2 kΩ 4W power resistor located between the PR+ and PR- pins.

2.6.2 Over-Voltage Conditions

Potentials in excess of 100 V applied to the tip and ring interface will cause the CPC1465 to disable the sealing current hold circuit and enter a standby state with very little current draw. Once the over-voltage condition is removed, the CPC1465 automatically resumes normal operation.

3. Manufacturing Information

3.1 Moisture Sensitivity



All plastic encapsulated semiconductor packages are susceptible to moisture ingression. IXYS Integrated Circuits Division classified all of its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL) rating** as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Rating
CPC1465D	MSL 1
CPC1465M	MSL 3

3.2 ESD Sensitivity



This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

3.3 Reflow Profile

This product has a maximum body temperature and time rating as shown below. All other guidelines of **J-STD-020** must be observed.

Device	Maximum Temperature x Time
CPC1465D / CPC1465M	260°C for 30 seconds

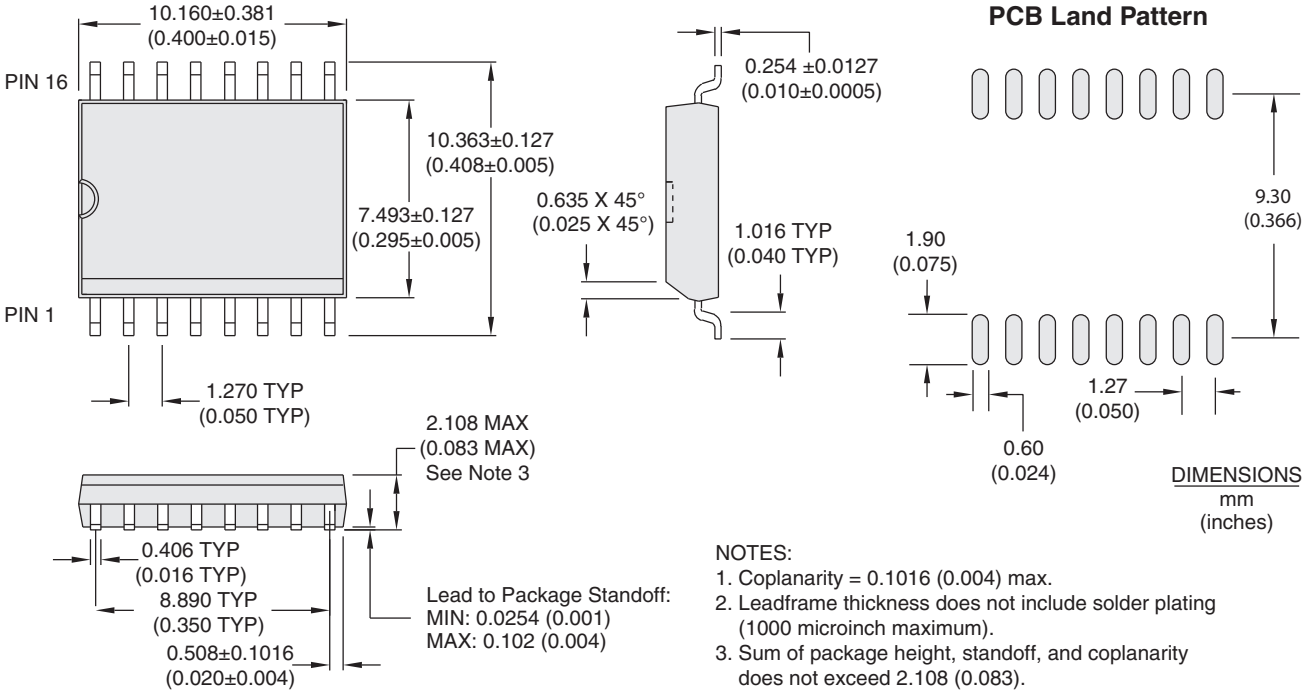
3.4 Board Wash

IXYS Integrated Circuits Division recommends the use of no-clean flux formulations. However, board washing to remove flux residue is acceptable, and the use of a short drying bake may be necessary. Chlorine-based or Fluorine-based solvents or fluxes should not be used. Cleaning methods that employ ultrasonic energy should not be used.



3.5 Mechanical Dimensions

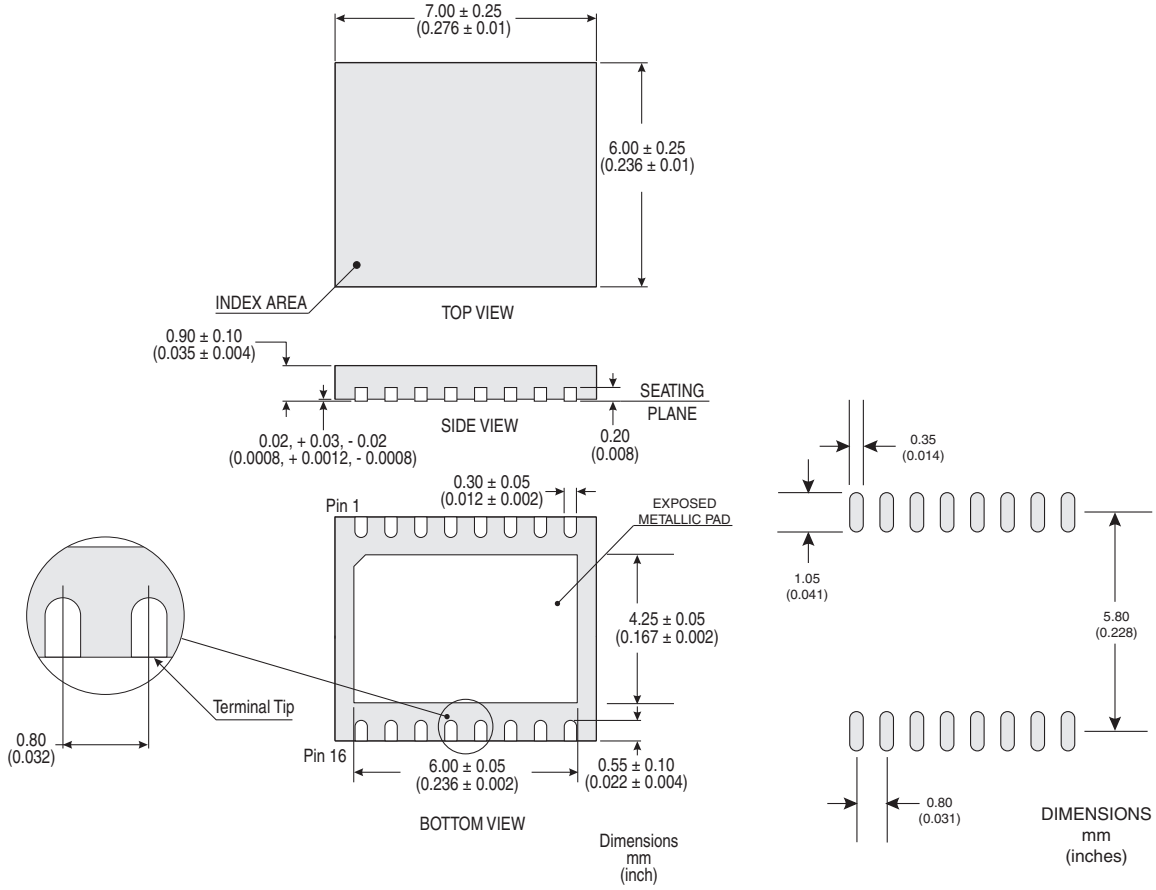
3.5.1 CPC1465D 16-Pin SOIC Package



NOTES:
1. Coplanarity = 0.1016 (0.004) max.
2. Leadframe thickness does not include solder plating (1000 microinch maximum).
3. Sum of package height, standoff, and coplanarity does not exceed 2.108 (0.083).

NOTE: The CPC1465 uses a slightly different package than the LH1465AAE. Some adjustment to the printed-circuit-board pad layout may be needed for existing applications.

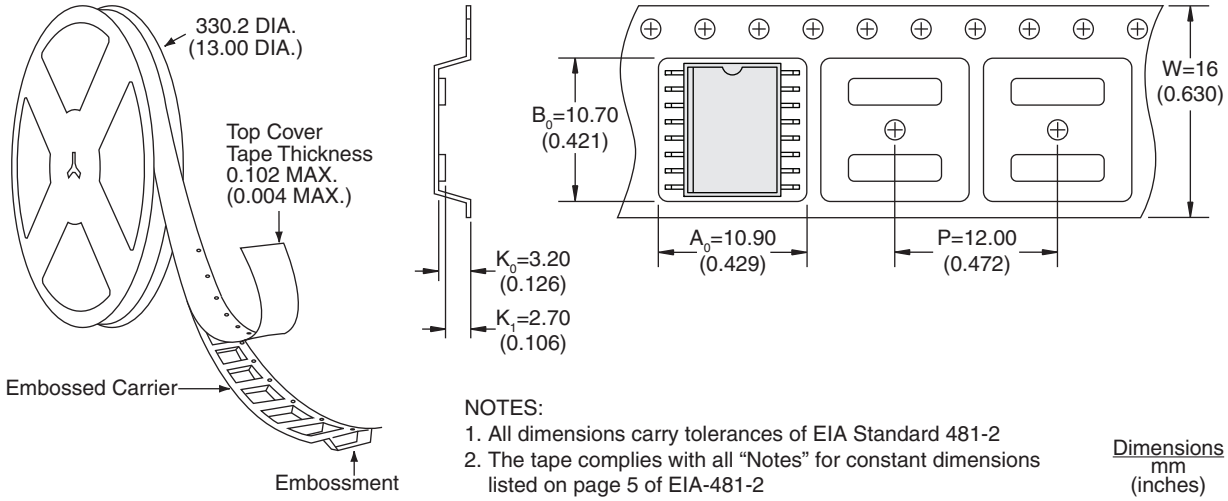
3.5.2 CPC1465M 16-Pin DFN Package



NOTE: As the metallic pad on the bottom of the DFN package is connected to the substrate of the die, IXYS Integrated Circuits Division recommends that no printed circuit board traces or vias be placed under this area.

3.6 Tape and Reel Packaging

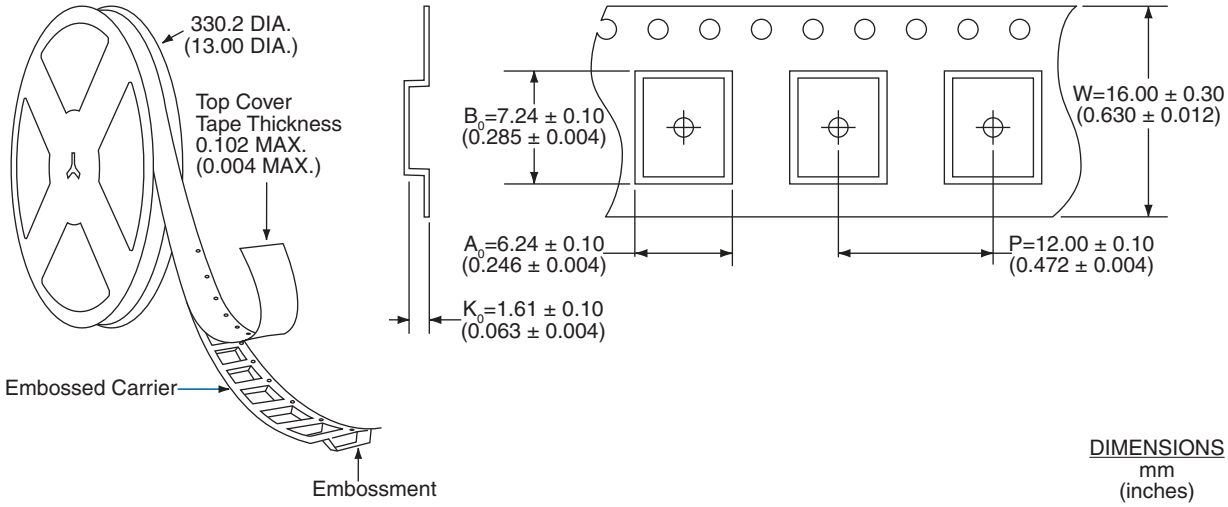
3.6.1 CPC1465DTR 16-Pin SOIC Tape & Reel



NOTES:
1. All dimensions carry tolerances of EIA Standard 481-2
2. The tape complies with all "Notes" for constant dimensions listed on page 5 of EIA-481-2

Dimensions
mm
(inches)

3.6.2 CPC1465MTR 16-Pin DFN Tape & Reel



DIMENSIONS
mm
(inches)

For additional information please visit our website at: www.ixysic.com

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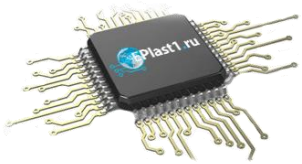
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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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