

CSD88539ND, Dual 60 V N-Channel NexFET™ Power MOSFETs

1 Features

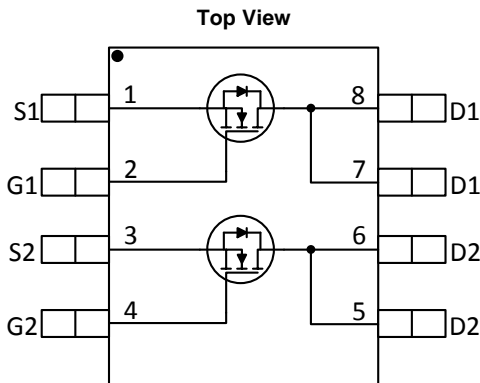
- Ultra-Low Q_g and Q_{gd}
- Avalanche Rated
- Pb Free
- RoHS Compliant
- Halogen Free

2 Applications

- Half Bridge for Motor Control
- Synchronous Buck Converter

3 Description

This dual SO-8, 60 V, 23 mΩ NexFET™ power MOSFET is designed to serve as a half bridge in low-current motor control applications.



Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	60		V
Q_g	Gate Charge Total (10 V)	7.2		nC
Q_{gd}	Gate Charge Gate to Drain	1.1		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 6\text{ V}$	27	mΩ
		$V_{GS} = 10\text{ V}$	23	mΩ
$V_{GS(th)}$	Threshold Voltage	3.0		V

Ordering Information

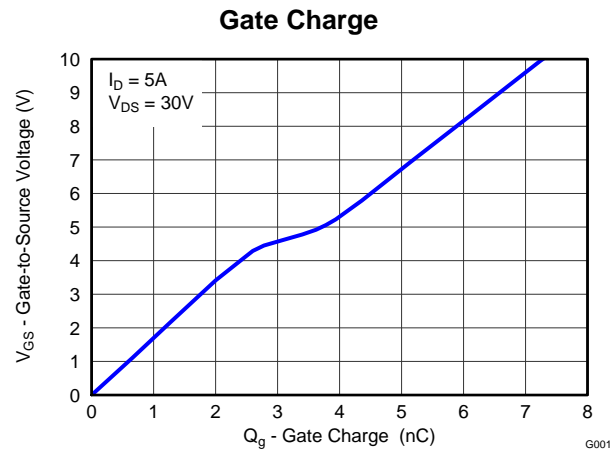
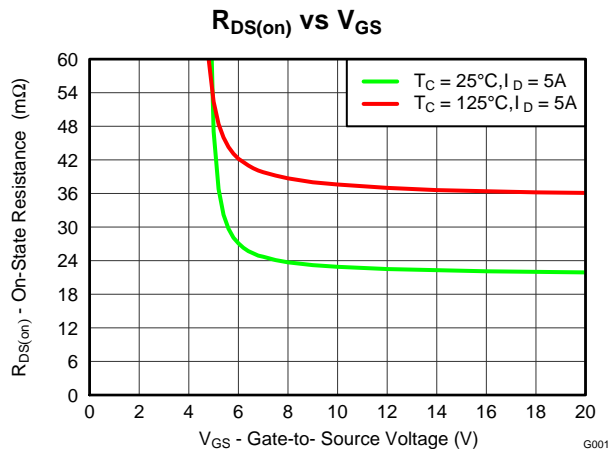
Device	Qty	Media	Package	Ship
CSD88539ND	2500	13-Inch Reel	SO-8 Plastic Package	Tape and Reel
CSD88539NDT	250	7-Inch Reel		

Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	60	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Continuous Drain Current (Package limited)	15	A
	Continuous Drain Current (Silicon limited), $T_C = 25^\circ\text{C}$	11.7	
	Continuous Drain Current ⁽¹⁾	6.3	
I_{DM}	Pulsed Drain Current ⁽²⁾	46	A
P_D	Power Dissipation ⁽¹⁾	2.1	W
T_J , T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
E_{AS}	Avalanche Energy, single pulse $I_D = 22\text{ A}$, $L = 0.1\text{ mH}$, $R_G = 25\text{ }\Omega$	24	mJ

(1) Typical $R_{\theta JA} = 60^\circ\text{C/W}$ on a 1-inch², 2-oz. Cu pad on a 0.06-inch thick FR4 PCB

(2) Pulse duration $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$



4 Specifications

4.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV _{DSS}	Drain-to-Source Voltage	V _{GS} = 0 V, I _D = 250 μA	60			V
I _{DSS}	Drain-to-Source Leakage Current	V _{GS} = 0 V, V _{DS} = 48 V			1	μA
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0 V, V _{GS} = 20 V			100	nA
V _{GS(th)}	Gate-to-Source Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	2.6	3.0	3.6	V
R _{DS(on)}	Drain-to-Source On Resistance	V _{GS} = 6 V, I _D = 5 A		27	34	mΩ
		V _{GS} = 10 V, I _D = 5 A		23	28	mΩ
g _{fs}	Transconductance	V _{DS} = 30 V, I _D = 5 A		19		S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{GS} = 0 V, V _{DS} = 30 V, f = 1 MHz		570	741	pF
C _{oss}	Output Capacitance			70	91	pF
C _{rss}	Reverse Transfer Capacitance			2.0	2.6	pF
R _G	Series Gate Resistance			6.6	13.2	Ω
Q _g	Gate Charge Total (10 V)	V _{DS} = 30 V, I _D = 5 A		7.2	9.4	nC
Q _{gd}	Gate Charge Gate to Drain			1.1		nC
Q _{gs}	Gate Charge Gate to Source			2.7		nC
Q _{g(th)}	Gate Charge at V _{th}			1.8		nC
Q _{oss}	Output Charge	V _{DS} = 30 V, V _{GS} = 0 V		9.6		nC
t _{d(on)}	Turn On Delay Time	V _{DS} = 30 V, V _{GS} = 10 V, I _{DS} = 5 A, R _G = 0 Ω		5		ns
t _r	Rise Time			9		ns
t _{d(off)}	Turn Off Delay Time			14		ns
t _f	Fall Time			4		ns
Diode Characteristics						
V _{SD}	Diode Forward Voltage	I _{SD} = 5 A, V _{GS} = 0 V		0.8	1	V
Q _{rr}	Reverse Recovery Charge	V _{DS} = 30 V, I _F = 5A, di/dt = 300A/μs		37		nC
t _{rr}	Reverse Recovery Time			21		ns

4.2 Thermal Characteristics

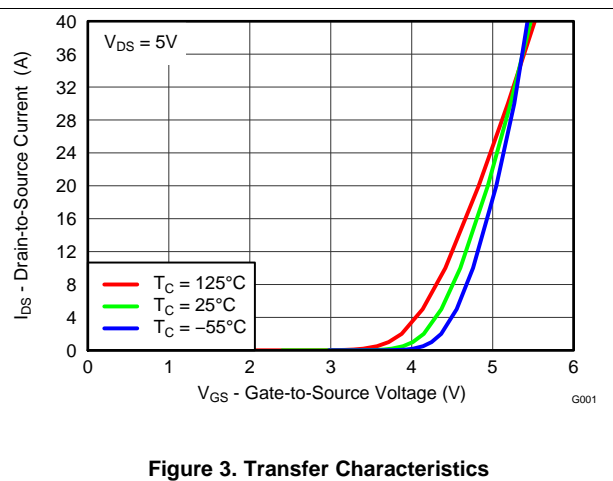
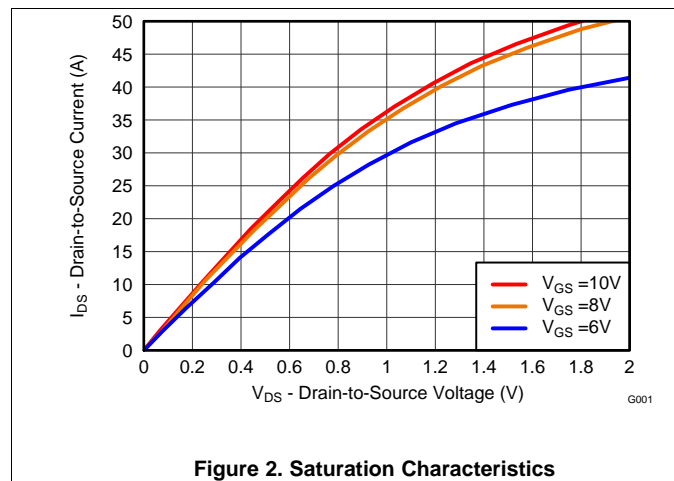
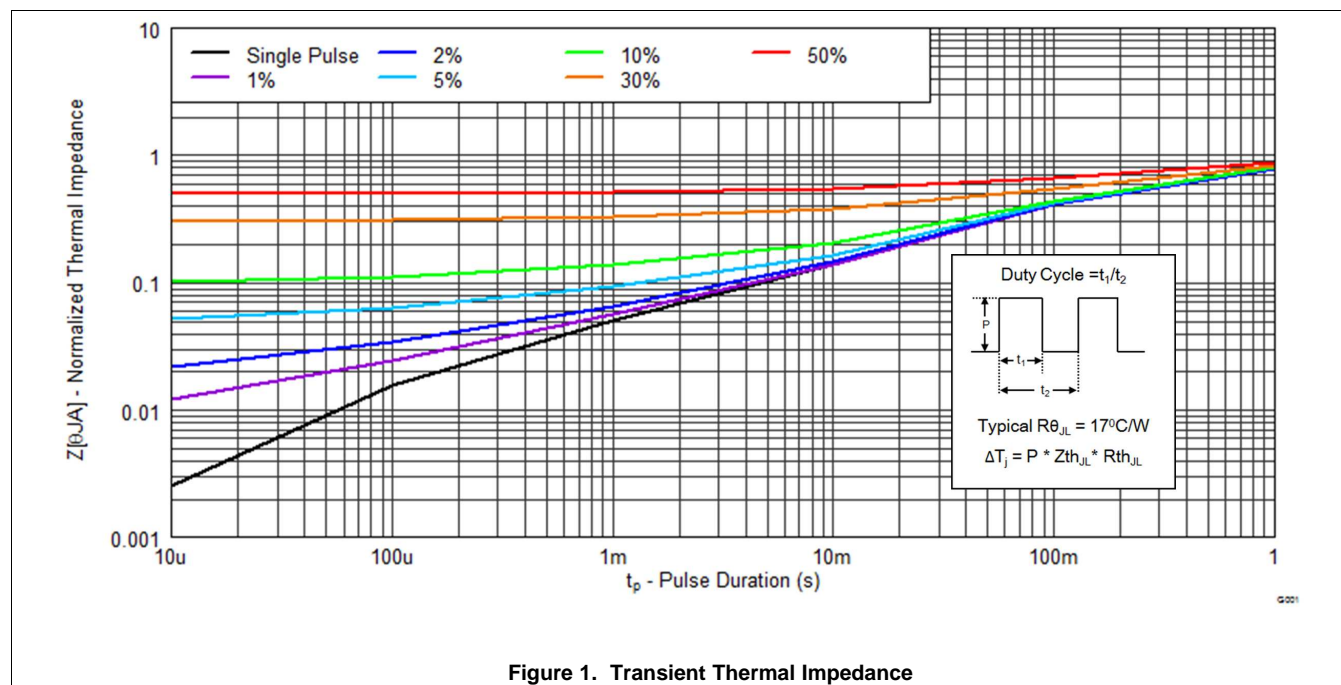
(T_A = 25°C unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
R _{θJL}	Junction-to-Lead Thermal Resistance ⁽¹⁾			20	°C/W
R _{θJA}	Junction-to-Ambient Thermal Resistance ⁽¹⁾⁽²⁾			75	°C/W

- (1) R_{θJC} is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. R_{θJC} is specified by design, whereas R_{θJA} is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.

4.3 Typical MOSFET Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)



Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

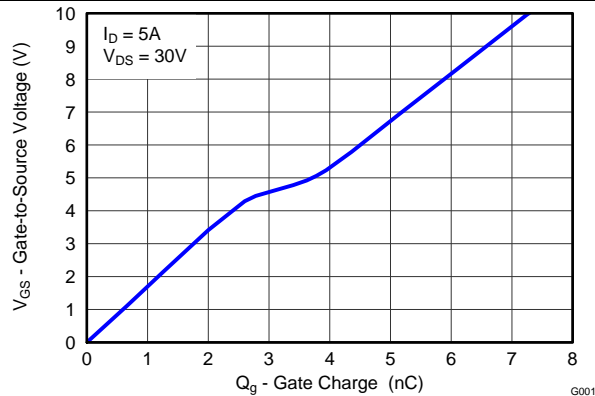


Figure 4. Gate Charge

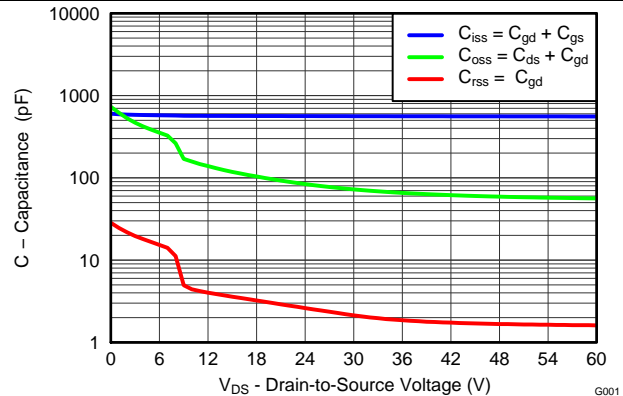


Figure 5. Capacitance

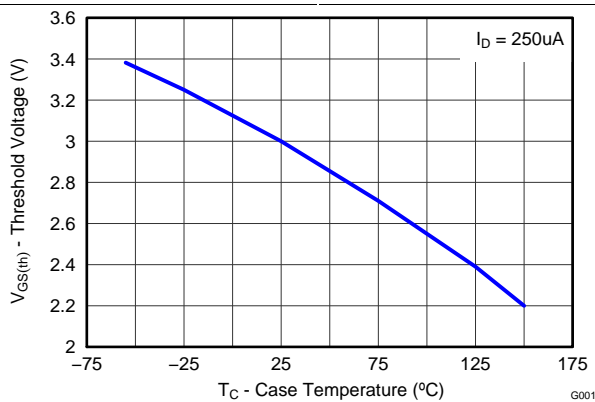


Figure 6. Threshold Voltage vs Temperature

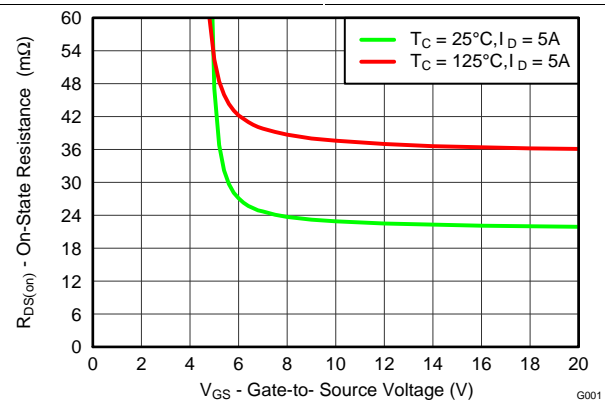


Figure 7. On-State Resistance vs Gate-to-Source Voltage

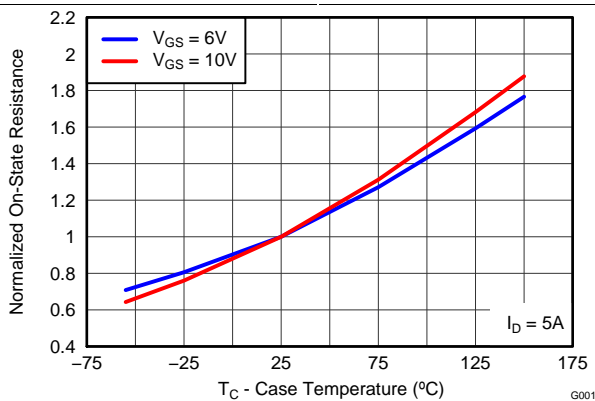


Figure 8. Normalized On-State Resistance vs Temperature

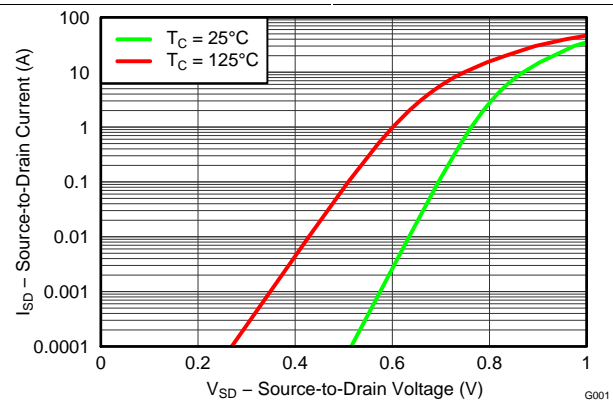


Figure 9. Typical Diode Forward Voltage

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

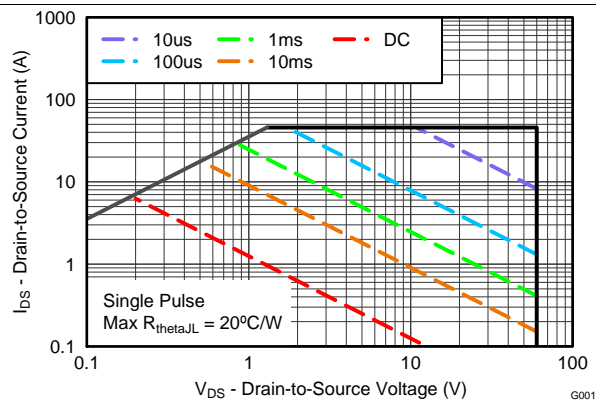


Figure 10. Maximum Safe Operating Area

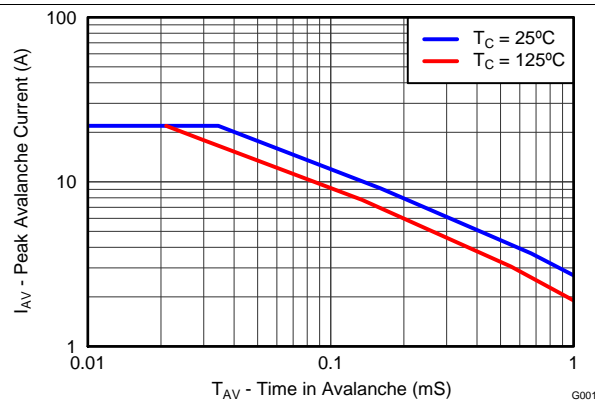


Figure 11. Single Pulse Unclamped Inductive Switching

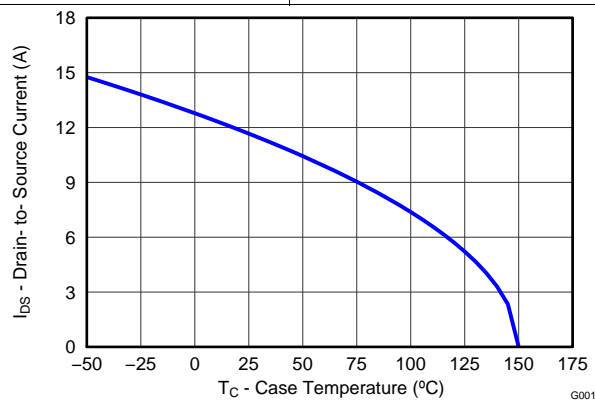
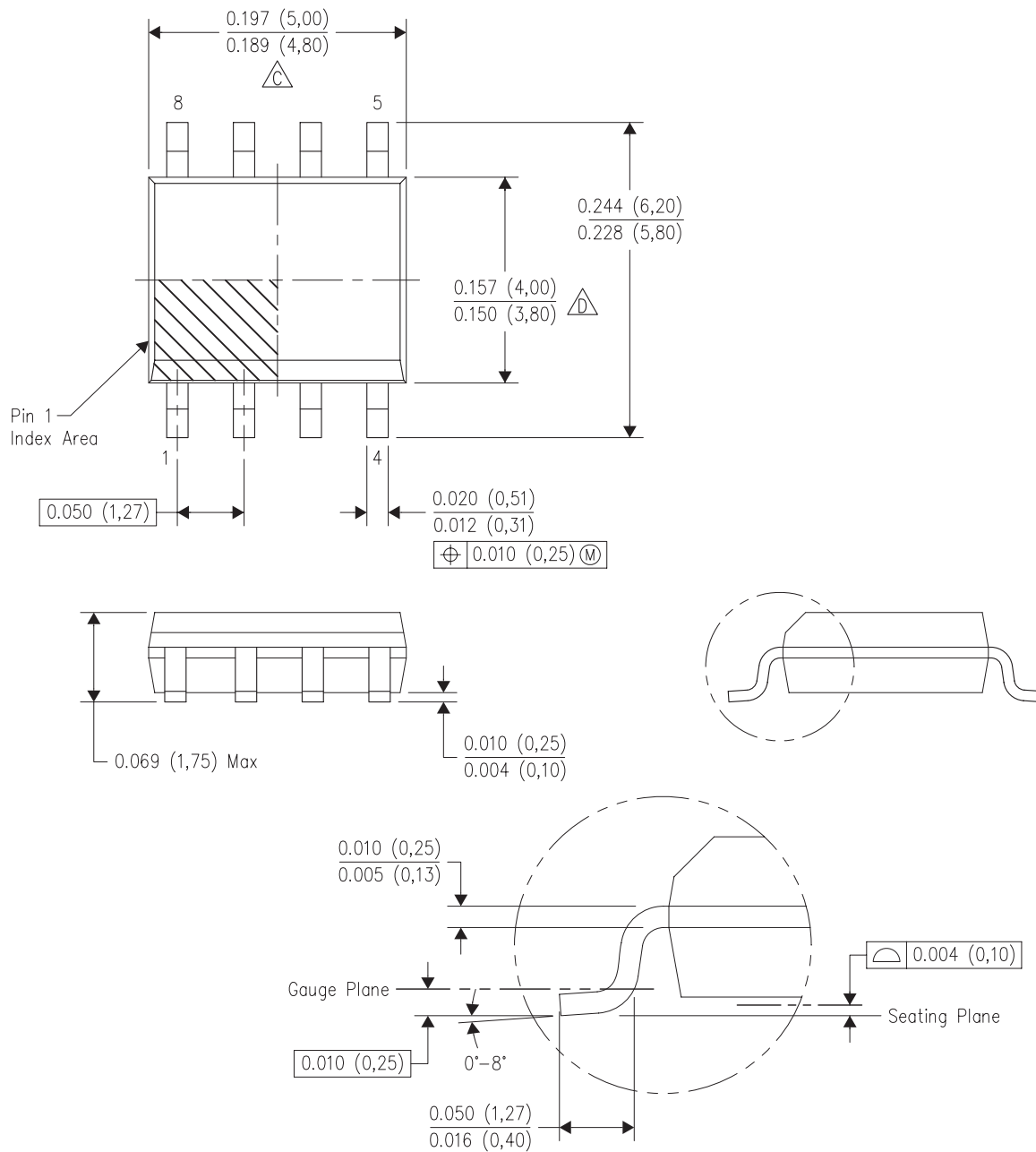


Figure 12. Maximum Drain Current vs Temperature

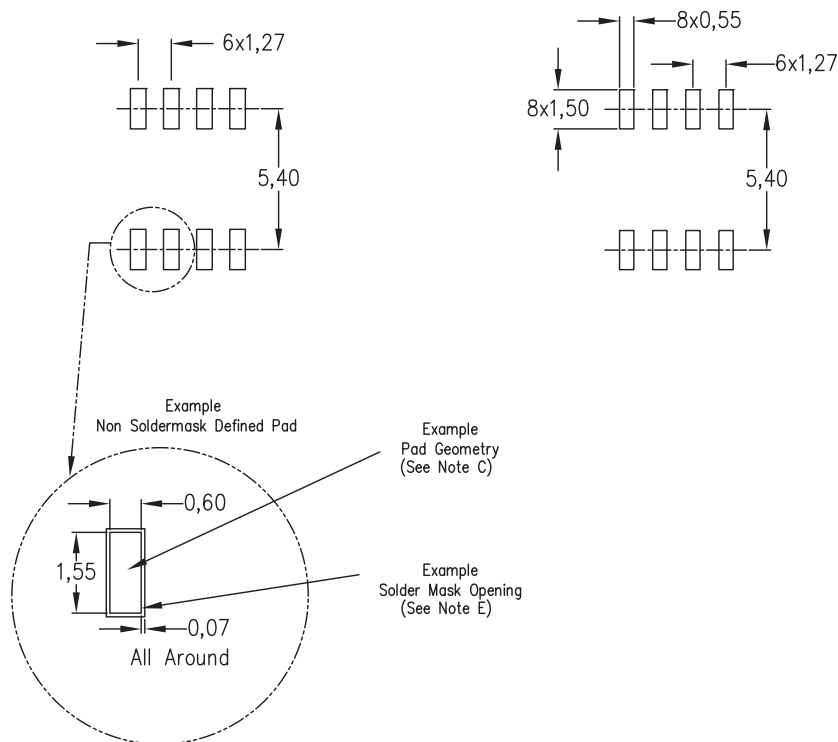
5 Mechanical Data

5.1 SO-8 Package Dimensions



1. All linear dimensions are in inches (millimeters).
2. This drawing is subject to change without notice.
3. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
4. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
5. Reference JEDEC MS-012 variation AA.

5.2 Recommended PCB Pattern and Stencil Opening



1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Publication IPC-7351 is recommended for alternate designs.
4. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
5. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

6 Device and Documentation Support

6.1 Trademarks

NexFET is a trademark of Texas Instruments.

6.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD88539ND	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-55 to 150	88539N	Samples
CSD88539NDT	ACTIVE	SOIC	D	8	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-55 to 150	88539N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
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- Подбор аналогов;
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- Техническая поддержка проекта;
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