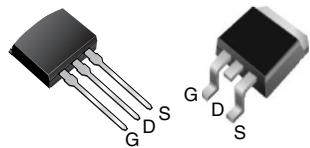
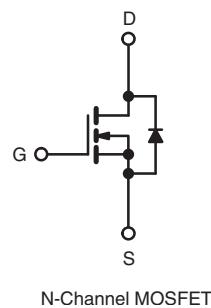


Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	400	
$R_{DS(on)}$ (Max.) (Ω)	$V_{GS} = 10$ V	1.0
Q_g (Max.) (nC)	22	
Q_{gs} (nC)	5.8	
Q_{gd} (nC)	9.3	
Configuration	Single	

I²PAK (TO-262)

D²PAK (TO-263)


FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Low Gate Charge Q_g Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective C_{oss} Specified
- Compliant to RoHS Directive 2002/95/EC



RoHS*
COMPLIANT
HALOGEN FREE
Available

APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching

TYPICAL SMPS TOPOLOGIES

- Single Transistor Flyback Xfmr. Reset
- Single Transistor Forward Xfmr. Reset (Both US Line Input Only)

ORDERING INFORMATION

Package	D ² PAK (TO-263)	D ² PAK (TO-263)	D ² PAK (TO-263)	I ² PAK (TO-262)
Lead (Pb)-free and Halogen-free	SiHF730AS-GE3	SiHF730ASTRL-GE3 ^a	SiHF730ASTRR-GE3 ^a	SiHF730AL-GE3
Lead (Pb)-free	IRF730ASPbF	IRF730ASTRLPbF ^a	IRF730ASTRRPbF ^a	IRF730ALPbF
	SiHF730AS-E3	SiHF730ASTL-E3 ^a	SiHF730ASTR-E3 ^a	SiHF730AL-E3

Note

- a. See device orientation.

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	400	V
Gate-Source Voltage	V_{GS}	± 30	
Continuous Drain Current	I_D	5.5	A
		3.5	
Pulsed Drain Current ^{a, e}	I_{DM}	22	
Linear Derating Factor		0.6	W/°C
Single Pulse Avalanche Energy ^{b, e}	E_{AS}	290	mJ
Avalanche Current ^a	I_{AR}	5.5	A
Repetitive Avalanche Energy ^a	E_{AR}	7.4	mJ
Maximum Power Dissipation	P_D	74	W
Peak Diode Recovery dV/dt ^{c, e}	dV/dt	4.6	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	°C

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Starting $T_J = 25$ °C, $L = 19$ mH, $R_g = 25$ Ω, $I_{AS} = 5.5$ A (see fig. 12).
c. $I_{SD} \leq 5.5$ A, $dI/dt \leq 90$ A/μs, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C.
d. 1.6 mm from case.
e. Uses IRF730A, SiHF730A data and test conditions.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mounted, steady-state) ^a	R _{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	-	1.7	

Note

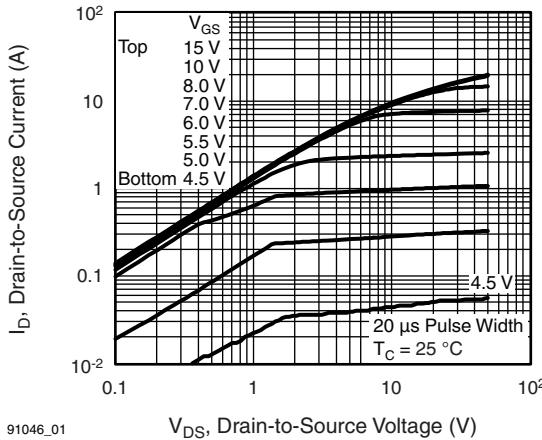
a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)

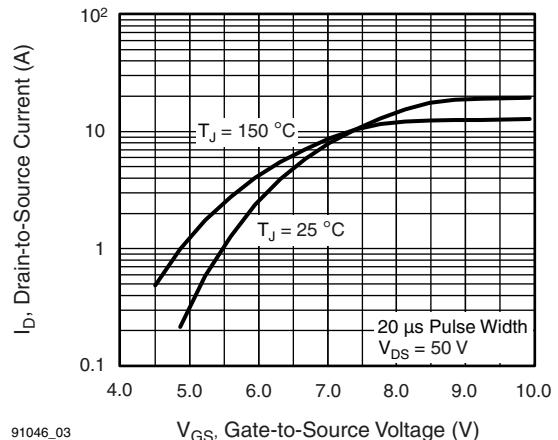
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0, I _D = 250 μA		400	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA ^d		-	0.5	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.5	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 30 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 400 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 320 V, V _{GS} = 0 V, T _J = 125 °C		-	-	250	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 3.3 A ^b	-	-	1.0	Ω
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 3.3 A ^d		3.1	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5 ^d		-	600	-	pF
Output Capacitance	C _{oss}			-	103	-	
Reverse Transfer Capacitance	C _{rss}			-	4.0	-	
Output Capacitance	C _{oss}	V _{GS} = 0 V	V _{DS} = 1.0 V, f = 1.0 MHz	-	890	-	nC
			V _{DS} = 320 V, f = 1.0 MHz	-	30	-	
Effective Output Capacitance	C _{oss eff.}		V _{DS} = 0 V to 320 V ^{c, d}	-	45	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 3.5 A, V _{DS} = 320 V, see fig. 6 and 13 ^{b, d}	-	-	22	ns
Gate-Source Charge	Q _{gs}			-	-	5.8	
Gate-Drain Charge	Q _{gd}			-	-	9.3	
Turn-On Delay Time	t _{d(on)}			-	10	-	
Rise Time	t _r	V _{DD} = 200 V, I _D = 3.5 A, R _g = 12 Ω, R _D = 57 Ω, see fig. 10 ^{b, d}	-	22	-	ns	
Turn-Off Delay Time	t _{d(off)}		-	20	-		
Fall Time	t _f		-	16	-		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	5.5	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	22	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 5.5 A, V _{GS} = 0 V ^b		-	-	1.6	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 3.5 A, dI/dt = 100 A/μs ^{b, d}		-	370	550	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	1.6	2.4	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

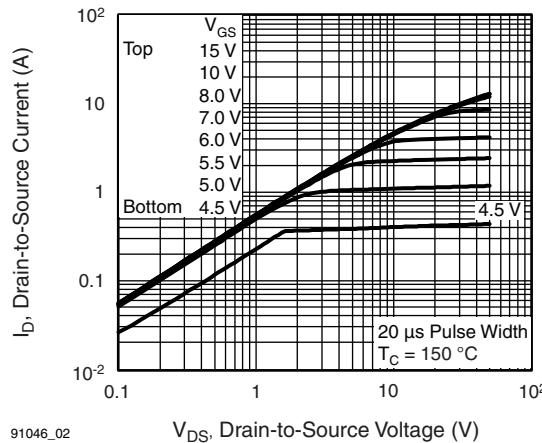
- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.
- c. C_{oss eff.} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}.
- d. Uses IRF730A, SiHF730A data and test conditions.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


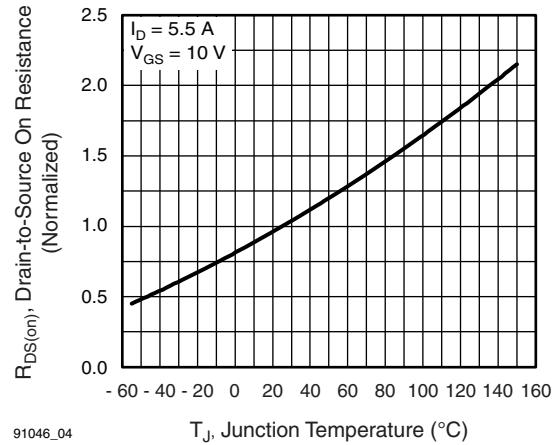
91046_01

Fig. 1 - Typical Output Characteristics

91046_03

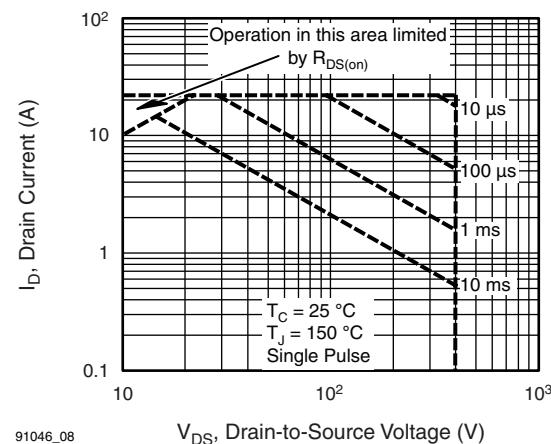
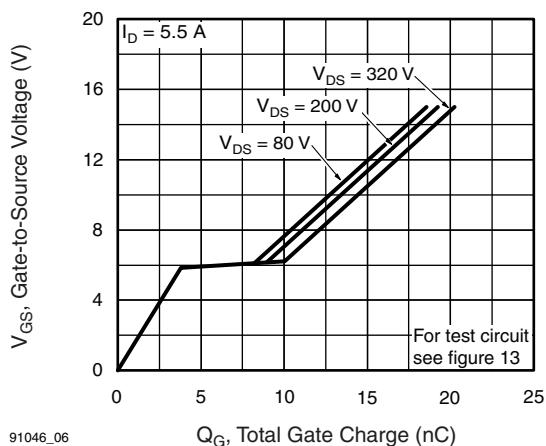
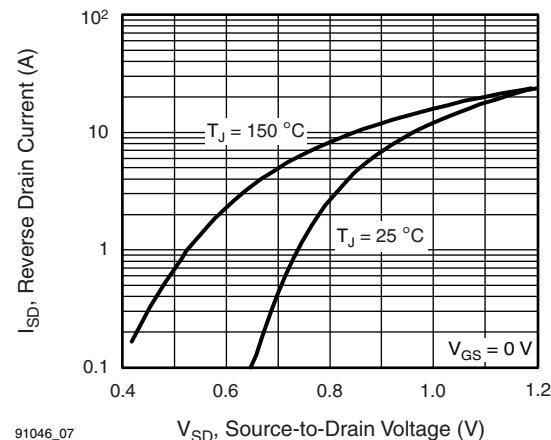
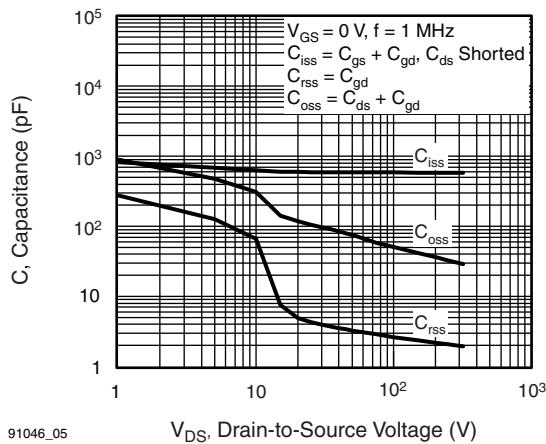
Fig. 3 - Typical Transfer Characteristics

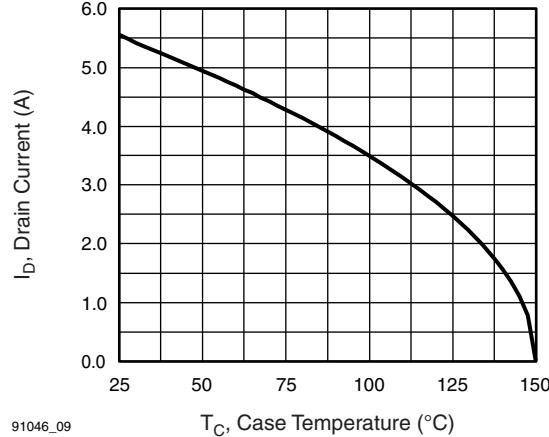
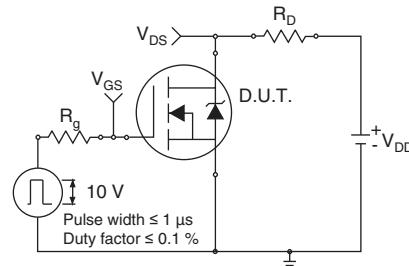
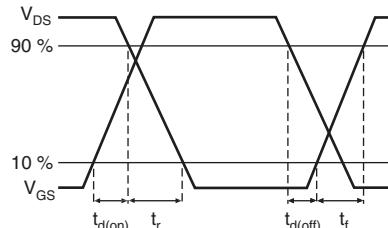
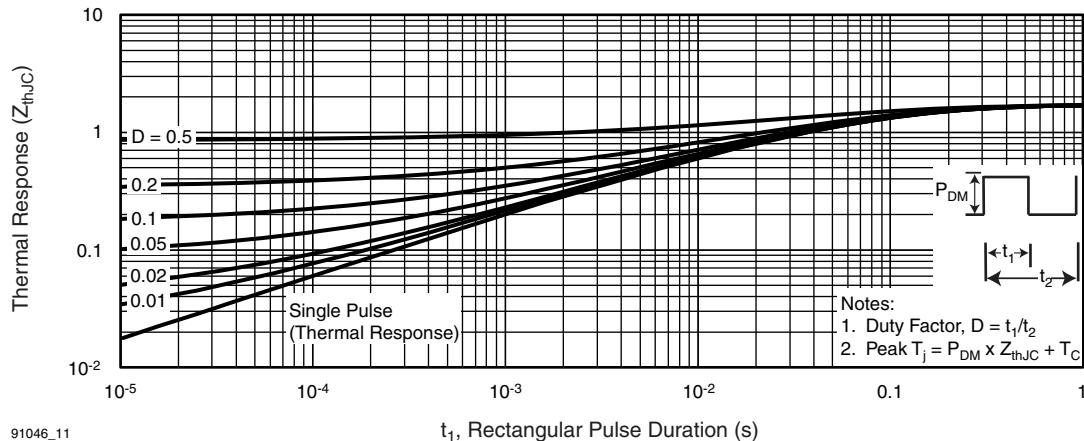
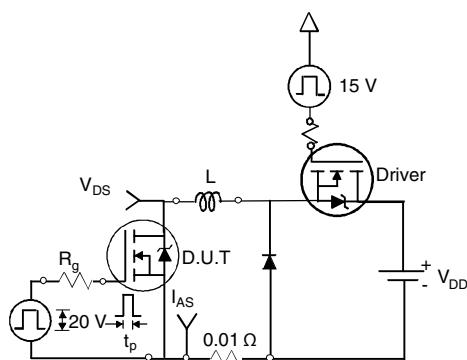
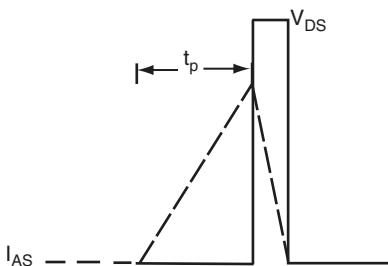
91046_02

Fig. 2 - Typical Output Characteristics

91046_04

Fig. 4 - Normalized On-Resistance vs. Temperature




Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 10a - Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig. 12a - Unclamped Inductive Test Circuit

Fig. 12b - Unclamped Inductive Waveforms

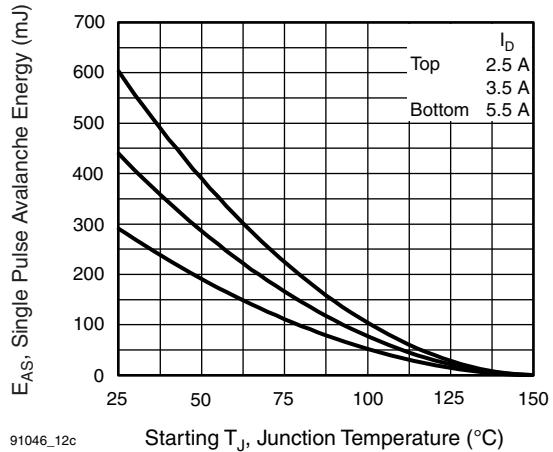


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

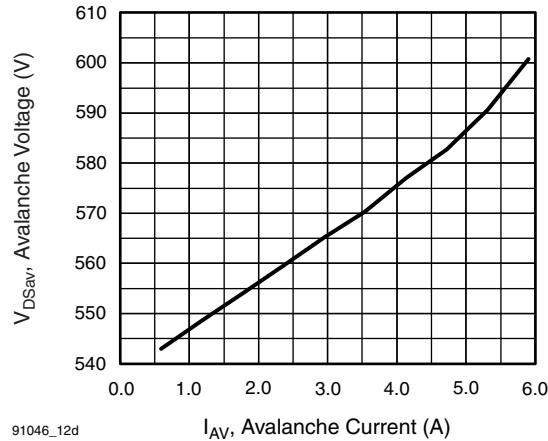


Fig. 12d - Typical Drain-to-Source Voltage vs. Avalanche Current

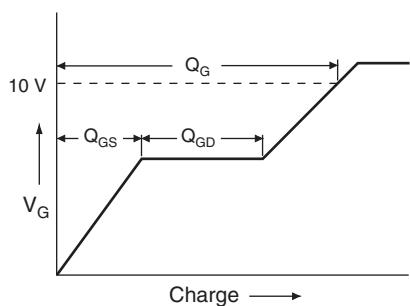


Fig. 13a - Maximum Avalanche Energy vs. Drain Current

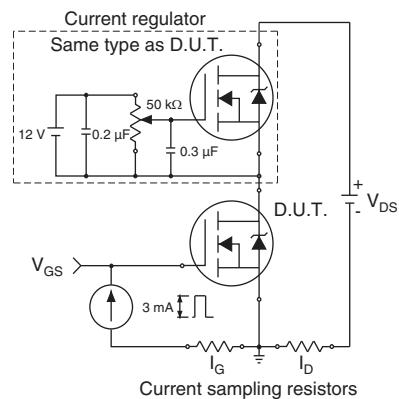


Fig. 13b - Gate Charge Test Circuit

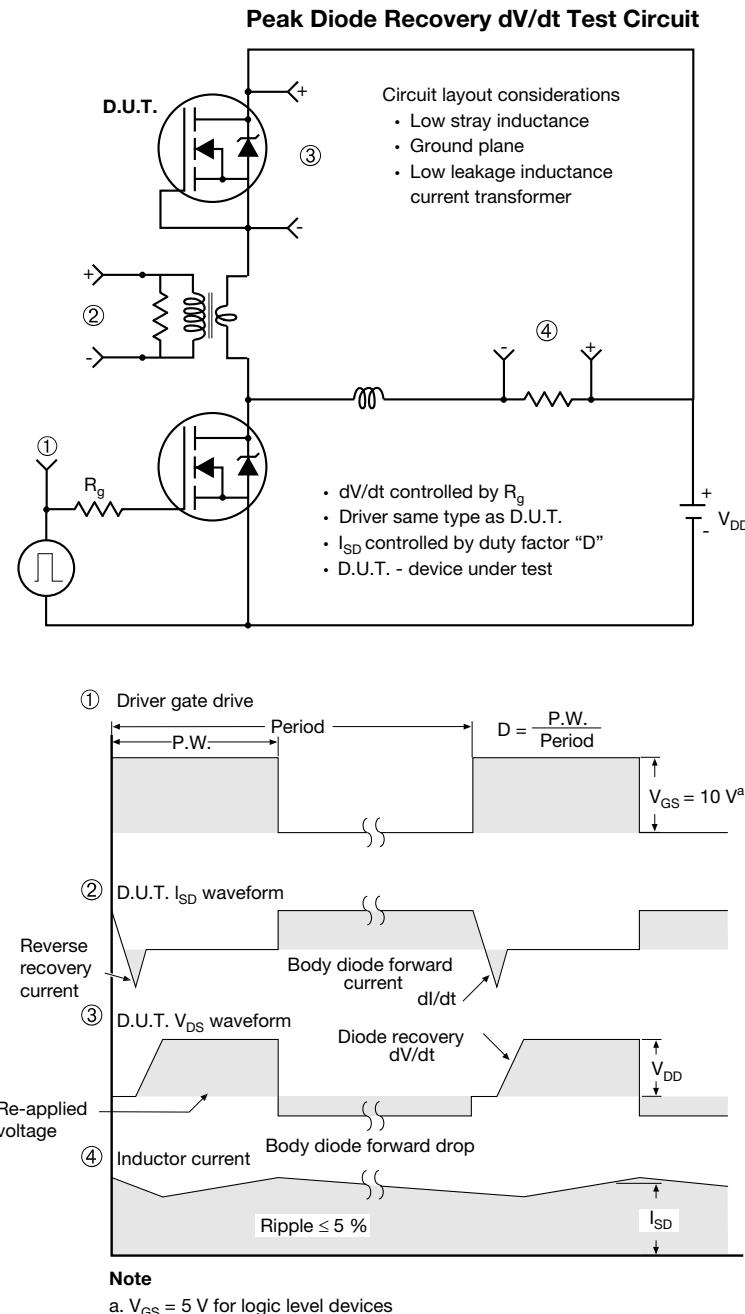
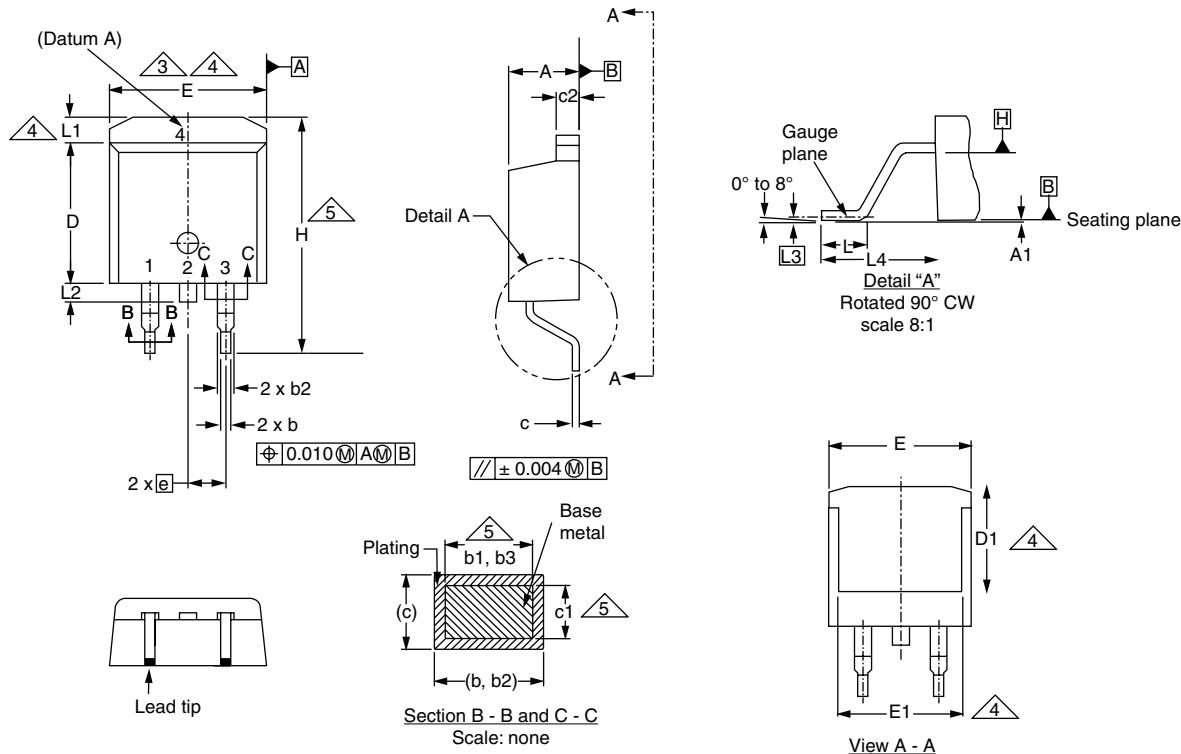


Fig. 14 - For N-Channel

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TO-263AB (HIGH VOLTAGE)

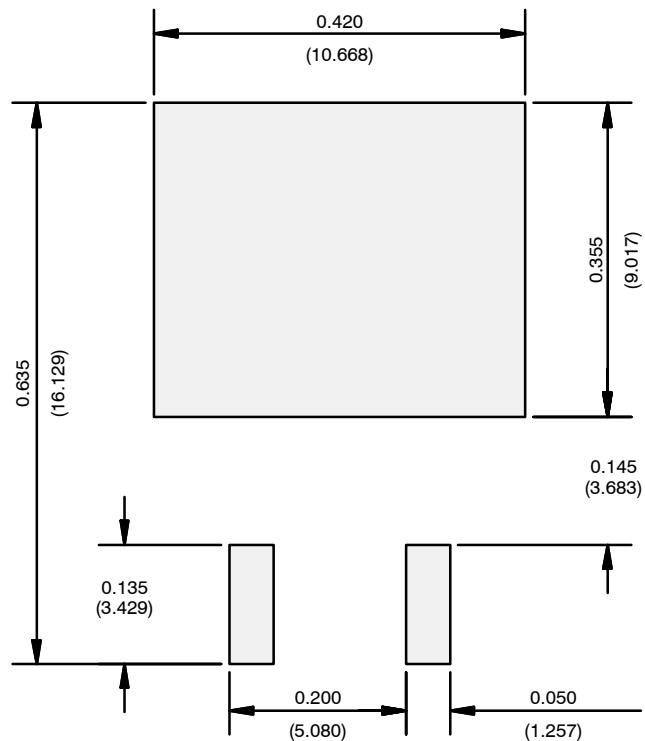


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994.
- Dimensions are shown in millimeters (inches).
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
- Thermal PAD contour optional within dimension E, L1, D1 and E1.
- Dimension b1 and c1 apply to base metal only.
- Datum A and B to be determined at datum plane H.
- Outline conforms to JEDEC outline to TO-263AB.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead

Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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- Поставка сложных, дефицитных, либо снятых с производства позиций;
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- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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