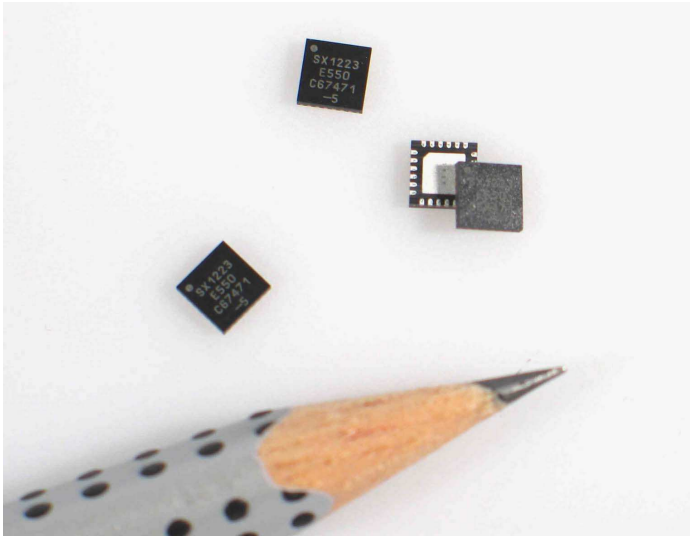

SX1223

425 – 475 MHz / 850 – 950 MHz

Integrated UHF Transmitter

GENERAL DESCRIPTION

The SX1223 is a single chip transmitter operating in UHF frequency bands including the 434, 869 and 915 MHz license-free ISM (Industrial Scientific and Medical) bands. Its highly integrated architecture allows for minimum external components while maintaining design flexibility. All major RF communication parameters are programmable and most of them can be set dynamically. The SX1223 offers the advantage of high data rate communication at rates of up to 153.6 kbit/s. The SX1223 is optimized for low cost applications while offering high RF output power. The device is suitable for applications which have to satisfy either the European (ETSI-300-220) or the North American (FCC part 15) regulatory standards.

APPLICATIONS

- Automated Meter Reading (AMR)
- Home Automation and Access Control
- High-Quality Speech, Music and Data over RF

KEY PRODUCT FEATURES

- RF output power: up to +10 dBm
- Low power consumption:
  T_X = 25.8 mA @ 10 dBm (typical)
- Supply voltage down to 2.0 V
- Data rate from 1.2 to 153.6 kbit/s
- On-chip frequency synthesizer
- Continuous phase 2-level FSK modulation
- Very small RoHS green package (TQFN24, 4mm x 4mm)

ORDERING INFORMATION

Part number	Temperature range	Package
SX1223I073TRT[(1)]	-40 ℃ to +85 ℃	TQFN24

(1) TR refers to tape & reel.
T refers to Lead Free package.
This device is WEEE and RoHS compliant.

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The SX1223 is a single chip transmitter operating in the 433, 868 and 915MHz license free ISM (Industrial Scientific and Medical) frequency bands; the frequency range is selectable between 425-475 MHz and 850-950 MHz. The modulation scheme is 2-FSK. The circuit has 4 functional modes: sleep mode, where all the blocks are switched off, standby mode, where only the crystal oscillator is on, synthesizer mode, where the frequency synthesizer is running, and transmission mode, where all the blocks are on, including the power amplifier. It complies with European (ETSI EN 300-220-1) and North American (FCC part 15) regulations.

There are three different methods of modulation:
- (mw1) pulling the VCO in closed loop: all the specified bit rates can be implemented, but a DC-free coding scheme is needed (e.g. Manchester), which means that the real information rate is half the bit rate,
- (mw2) pulling the VCO in open loop: all the specified bit rates can be implemented, and NRZ coding is allowed; but, since the control voltage of the VCO will drift due to leakage currents, the duration of the transmission is limited,
- (mw3) switching between two frequency divider ratios in closed loop; bit rates from 1.2 to 19.2 kbit/s are achievable with this method.

The circuit works on two selectable supply voltage ranges:
- (sv1) the high range (2.2 V to 3.6 V), where the on-chip regulators are activated,
- (sv2) the low range (2.0 V to 2.5 V), where the on-chip regulators are off.

A 3-wire bi-directional bus is used to communicate with SX1223 and gives access to the configuration register. An output clock of 1 MHz is user selectable for driving an external micro-controller.
SX1223 comes in a RoHS green TQFN-24 package (body size: 4 mm x 4 mm).

1 FUNCTIONAL BLOCK DIAGRAM

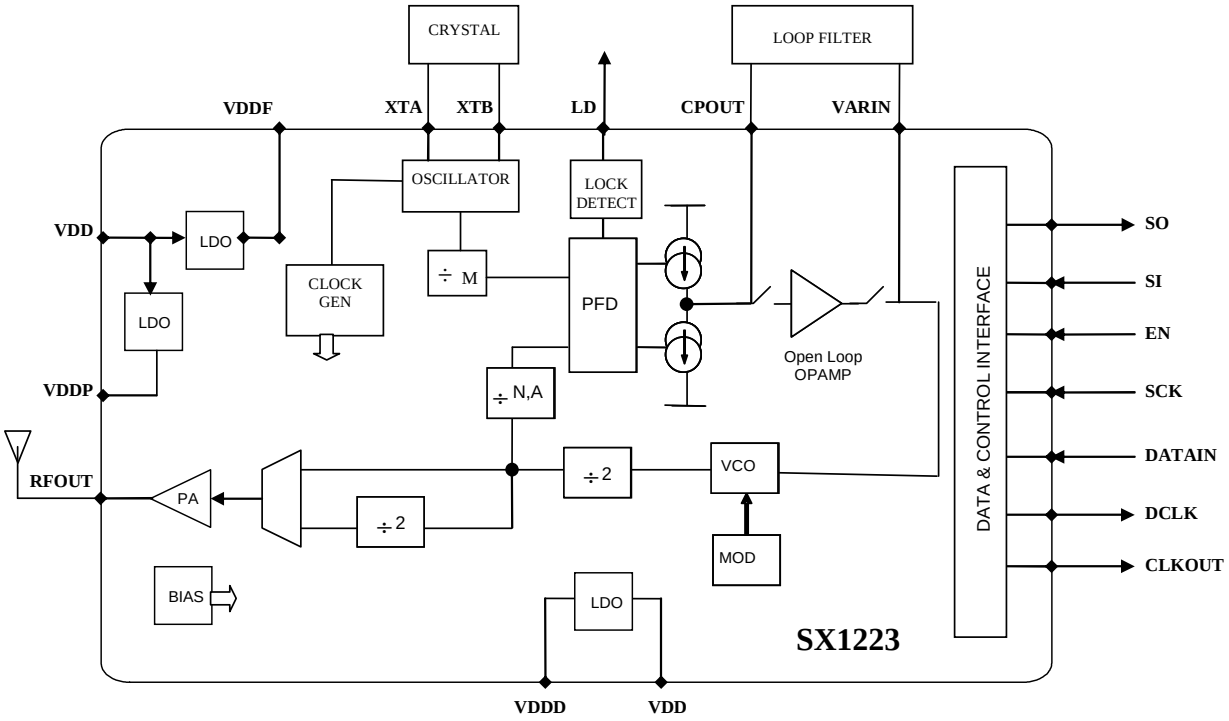
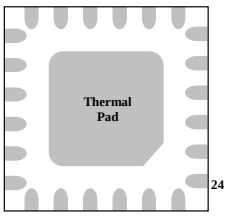


Figure 1: *SX1223 block diagram*

2 PIN DESCRIPTION

Pin	Name	I/O	Function
1	VDD	-	Main analog power supply Max 3.6V in sv1-mode Max 2.5V in sv2-mode
2	VSSP	-	PA ground
3	VDDP	-	In sv1-mode: PA LDO output, capacitor needed In sv2-mode: PA power supply, max 2.5 V
4	RFOUT	OUT	RF output
5	VSSP	-	PA ground
6	PTATBIAS/PAC	IN/OUT	PTAT source bias resistor / PA start-up control capacitor
7	XTB	IN/OUT	Crystal oscillator pin & input for external reference
8	XTA	IN/OUT	Crystal oscillator pin
9	VDDD	-	In sv1-mode: Digital LDO output, capacitor needed In sv2-mode: Digital power supply, max 2.5V
10	VSSD	-	Digital ground
11	VDD	-	Main digital power supply Max 3.6V in sv1-mode Max 2.5V in sv2-mode
12	LD	OUT	Lock detect output
13	CLKOUT	OUT	Output clock (1 MHz)
14	DCLK	OUT	Data clock output
15	DATAIN	IN	Data input
16	SCK	IN	3-wire interface clock input
17	EN	IN	Enable signal for the 3-wire interface
18	SI	IN	3-wire interface data input
19	SO	OUT	3-wire interface data output
20	CPOUT	OUT	PLL charge pump output
21	VARIN	IN	VCO varactor input
22	VSSF	-	Analog ground
23	VDDF	-	In sv1-mode: Analog LDO output, capacitor needed In sv2-mode: Analog power supply max 2.5 V
24	CIBIAS	OUT	CI source bias resistor

Note: Thermal Pad on the bottom of the package must be connected to ground.



bottom view

3 ELECTRICAL CHARACTERISTICS

3.1 ABSOLUTE MAXIMUM OPERATING RANGES

Stresses above the values listed below may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Symbol	Description	Min.	Max.	Unit
VDDmax	Supply voltage	-0.4	3.9	V
Tmax	Storage temperature	-55	125	℃

The device is ESD sensitive and should be handled with precaution.

3.2 SPECIFICATIONS

3.2.1 Operating Range

Symbol	Description	Min.	Max.	Unit
VDD	Supply voltage (*)	2.0	3.6	V
T	Temperature	-40	85	℃
CLop	Load capacitance on digital ports	-	25	pF

(*) Divided in two ranges:
- (sv1) high range, 2.2 V – 3.6 V, using on-chip regulators,
- (sv2) low range, 2.0 V – 2.5 V, without using the regulators.

3.2.2 Electrical Specifications

The table below gives the electrical specifications of the transmitter under the following conditions:
Supply Voltage = 3.3 V, temperature = 25 ℃, 2-level FSK, fc = 915 MHz, Output power = 10 dBm, Bit rate = 38.4 kb/s, Δf = 100 kHz, XTAL = 16 MHz, modulation by pulling the VCO in open loop (mw2), and conditions as defined in section 6, unless otherwise specified.

Symbol	Description	Conditions	Min	Typ	Max	Unit
IDDSL	Supply current in sleep mode		-	0.3	1	µA
IDDST	Supply current in standby mode	Crystal oscillator running, CLKOUT off	-	0.2	0.3	mA
IDDFS	Supply current in FS mode	Frequency synthesizer running	-	5	6	mA
IDDT	Supply current during transmission	10 dBm 0dBm	- -	25.8 14	- -	mA mA
FR	Frequency range		425 850	- -	475 950	MHz MHz
FDA	Frequency deviation	For FR from 850 to 950 MHz	5	-	255	kHz
FDA_L	Frequency deviation	For FR from 425 to 475 MHz	5	-	200	kHz
ΔFDA	Variation of frequency deviation		- 15	-	+ 15	%
BR	Bit rate	Modulation modes mw1 mw2	1.2	-	153.6	kbit/s
BR_3	Bit rate for mw3 mode	Modulation mode mw3	1.2	-	19.2	kbit/s
SPICLK	SPI clock frequency (SCK)	SCK duty cycle 50% +/-10%			1	MHz

Symbol	Description	Conditions	Min	Typ	Max	Unit
HRFOP	Highest RF output power	Highest programmable output power	8	10	-	dBm
SRFOP	RF output power steps	RF output power step size (8 steps available)	-	3	-	dB
XTAL	Crystal oscillator frequency	Recommended value: 16 MHz	-	-	40	MHz
TS_OS	Oscillator wake-up time	From sleep mode	-	0.8	2	ms
TS_OS_QS	Oscillator wake-up time in quick start-up mode	Quick start-up mode IDDST_QS_typ=0.9mA (XCO_quick_start, XCO_high_I = 10)	-	0.15	-	ms
TS_FS	Frequency synthesizer wake-up time	From standby mode (oscillator running) frequency at most 5 kHz away from the target	-	-	2	ms
TS_TR	Transmitter wake-up time	From FS mode (frequency synthesizer running)	-	-	500	µs
TD_TX	Transmission duration in mw2 mode	Duration during which the output signal is a proper FSK signal and the carrier frequency doesn't drift by more than 50 kHz from the time when the transmitter has reached its steady-state (including PA)	30	-	-	ms
TD_TXW	Transmission duration in mw2 mode	Same conditions as TD_TX, but over the whole temperature range	15	-	-	ms
ACP	Power transmitted in the 150 kHz adjacent channel	At 10 dBm output power, modulated signal Measured on a 150 kHz bandwidth centered at 150 kHz from the carrier, Δf = 40 kHz	-	-16		dBm
ACP_mw3	Power transmitted in the 250 kHz adjacent channel in mw3 modulation mode	At 10 dBm output power, modulated signal Measured on a 250 kHz bandwidth centered at 250 kHz from the carrier, Δf = 60 kHz	-	-23	-17	dBm
PHN	Phase noise of the output signal	At 10 dBm output power, unmodulated signal Measured at 50 kHz from the carrier in mw3 mode	-	-83	-80	dBc/Hz
CLKOUT	Output clock	On pin CLKOUT	-	1	-	MHz
VIH	Digital input level high	% VDD	75	-	-	%
VIL	Digital input level low	% VDD	-	-	25	%

4 GENERAL DESCRIPTION

The SX1223 is a 2-level FSK transmitter. The circuit operates in one of two frequency ranges, 425 to 475 MHz, and 850 to 950 MHz, allowing the 3 main ISM frequency bands (434 MHz, 869 MHz and 915 MHz) to be addressed by the circuit. It is capable of operating at data rates between 1.2 and 153.6 kbit/s, making it ideally suited for applications where high data rates are required.

The SX1223 is a highly programmable device – channel, bit rate, frequency deviation and output power – which makes it extremely flexible to meet a large number of end user requirements.

The main functional blocks of the SX1223 are the frequency synthesizer, the modulator, the power amplifier (PA), the voltage regulators and some additional service blocks. The device also includes a set of configuration registers and a digital interface. In a typical application, the SX1223 is programmed by a microcontroller via the 3-wire serial bus SI, SO, SCK to write to and read from the internal registers.

The Frequency Synthesizer generates the carrier (the local oscillator (LO) signal).

The Modulator performs the modulation of the carrier by the input bit stream.

The Power Amplifier amplifies the modulated RF signal to the antenna port.

The Voltage Regulators generate regulated supply voltages for the different parts of the chip, and allow battery voltages up to 3.6 V to be used.

The Service Blocks provide the internal voltage and current sources and provide all the necessary functions for the circuit to work properly.

The Configuration Registers are a set of registers that are used to store various settings to operate the SX1223 transmitter circuit. Please refer to Section 5.2 for the detailed descriptions of these registers. These registers are accessed in write or read mode through the 3-wire serial bus, as described in Section 5.1.

The Digital Interface provides internal control signals for the whole circuit according to the configuration register settings.

4.1 FREQUENCY SYNTHESIZER

4.1.1 General Structure

The frequency synthesizer is an integer-N PLL and consists of a voltage-controlled oscillator (VCO), a crystal oscillator, a prescaler, programmable frequency dividers and a phase-detector. The loop-filter is external for flexibility and can be a simple passive circuit. The lengths of the M and N and A counters are respectively 12, 12 and 6 bits.

To enable the prescaler Prescal_s register (address 16, bit 4) has to be written to 1. The M, N and A values can be calculated from the formula:

$$f_{RF} = \frac{f_{XCO}}{M \cdot (2 - FreqBand)} (16 \cdot N + A)$$

where

f_{XCO}:	Crystal oscillator frequency
f_{RF}:	RF frequency
FreqBand:	0: RF frequency 425-475 MHz
	1: RF frequency 850-950 MHz

M is the divide factor applied to the reference frequency, N and A are the counters of the frequency divider in the feedback loop of the PLL.

There are two sets of each of these divide factors (M0, N0, A0 and M1, N1, A1). In modulation modes mw1 and mw2 (register bit Modulation1=0), only the M0, N0 and A0 are used to fix the carrier frequency. If modulation by using the dividers is selected (mw3, Modulation1=1, Modulation0=0), the two sets are used to program the two RF

frequencies corresponding to the transmission of the two possible values '0' and '1'; these frequencies are then separated by twice the specified single sided frequency deviation Δf.

4.1.2 Crystal Oscillator

The crystal oscillator (XCO) provides the PLL with the reference signal. The schematic of the crystal oscillator's external components for 16 MHz is shown in Figure 2.

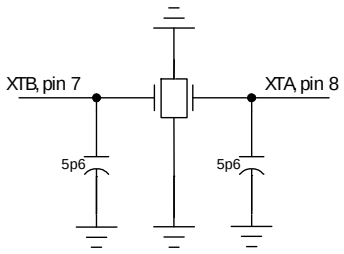


Figure 2: *External crystal oscillator circuit with additional (optional) external capacitances*

The crystal should be connected between pins XTA and XTB (pin 8 and 7). Either internal or external loading capacitors for the crystal can be used. Internal capacitors can be enabled by setting the XCOcap_en bit to 1. Faster start-up time is expected when using external capacitors. The total capacitance when XCOcap_en=1 (and no external capacitors) is 9 pF. Using a crystal with a load capacitance of 9 pF will give the expected oscillation frequency.

If XCOcap_en=0, the loading capacitors can be calculated by the following formula:

$$C_L = \frac{1}{\frac{1}{C_1}+\frac{1}{C_2}} + C_{parasitic}$$

The parasitic capacitance is the pin input capacitance and PCB stray capacitance. For instance, for a 9pF load crystal and a total parasitic capacitance of 6 pF the recommended values of the external load capacitors are 5.6 pF.

If an external reference is going to be used instead of a crystal, the signal shall be applied to pin 7, XTB. Due to internal biasing, AC coupling is recommended for use between the external reference and the XTB pin.

The start-up time of the crystal oscillator can vary from 150us to 800us depending on the settings shown in Table 15. Therefore, to save current consumption, the XCO should be turned on before any other circuit block. During start-up the XCO amplitude will eventually reach a sufficient level to trigger the M-counter. After counting 2 M-counter output pulses the rest of the circuit is enabled.

Two bits are available to speed up the crystal oscillator start-up: XCO_high_I increases the bias current and XCO_quick_start boosts this current but only at the start; the first output pulse from the M-divider turns this boost current off. Typical values for XCO start-up time and current consumption are tablulated below:

XCO_quick_start, XCO_high_I	00	01	10	11
IDDST [uA]	200	250	900	950
TS_OS [us]	800	750	200	150

Table 1: *Oscillator start-up time*

A reference clock can be generated by SX1223 for use by an external microcontroller. The ClkOut_en configuration bit determines the status of the CLKOUT pin. When set high CLKOUT is enabled, otherwise it's disabled. When enabled, the output frequency at CLKOUT is the crystal oscillator frequency divided by 16, and is then 1 MHz for a crystal at 16 MHz. This clock signal is disabled in Sleep Mode. When disabled, the CLKOUT pin is set to ground.

4.1.3 VCO

The VCO is fully integrated and has no external components. It oscillates at 1.8 GHz and is divided by 2 or 4 in the 900 MHz or the 450 MHz band respectively (FreqBand = 1 or 0). Additionally two bits in the configuration registers set the VCO frequency and three bits control the bias current. The two VCO_freq bits have to be programmed by

the user according to the selected frequency band, whereas the three VCO_IB bits can be either forced by the user or set automatically by the circuit which will select the combination having the best phase noise. This automatic setting can be enabled by setting the three VCO_IB bits to '0'.

Table 2 lists the bias setting used for the different VCO_freq settings in automatic mode. When any of the VCO_IB bit is set to 1, it will overrule the automatic setting.

RF frequency	VCO_IB2	VCO_IB1	VCO_IB0	VCO_freq1	VCO_freq0
425/850 MHz	1	1	1	0	0
434/868 MHz	1	0	1	0	1
457/915 MHz	0	1	1	1	0
475/950 MHz	0	0	0	1	1

Table 2: *VCO bit settings.*

The bias bits optimize the phase noise, and the frequency bits control a capacitor bank in the VCO. The tuning range, the RF frequency versus varactor voltage, is dependent on the VCO frequency setting, and is shown in Figure 3. When the tuning voltage is in the range from 1 to 1.6V, the VCO gain is at its maximum, approximately 65-70 MHz/V. It is then recommended that the varactor voltage is kept as much as possible in this range.

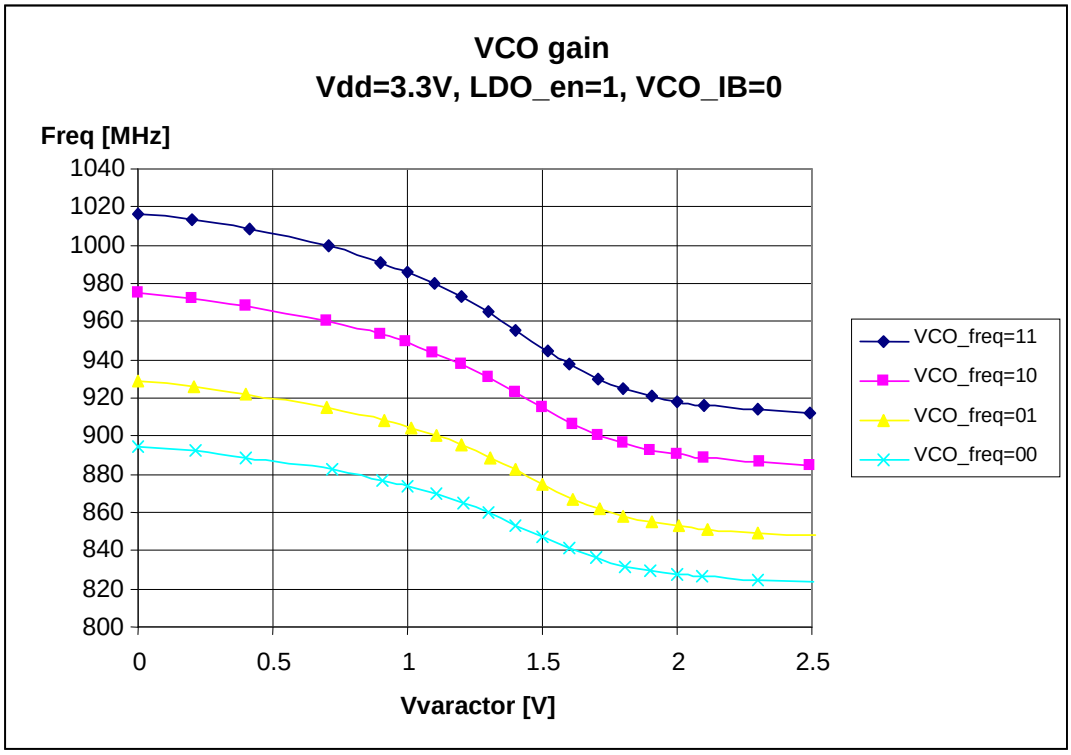


Figure 3: RF frequency vs. varactor voltage and VCO frequency bit

The input capacitance at the varactor pin must be taken into considerations when designing the PLL loop filter. This can be critical when designing a loop filter with high bandwidth, which gives relatively small component values. The input capacitance is approximately 6 pF.

For test purposes, the VCO can be bypassed by applying a differential local oscillator (LO) signal to the device on pin CPOUT and VARIN. A resistor of 18 kΩ to ground and a series capacitor of 47 pF are needed on both pins for proper biasing. The register bit VCO_by must be set to '1'.

4.1.4 Charge Pump

The charge pump current can be set to either 125 or 500 µA by the CP_HI bit. The default value at power-up is 125 µA (CP_HI = '0'). The choice of this current affects the loop filter component values (see section 4.1.5). For most applications the lowest current mode is recommended. For those applications using a high phase detector frequency and a high PLL bandwidth, 500 µA may provide a better solution.

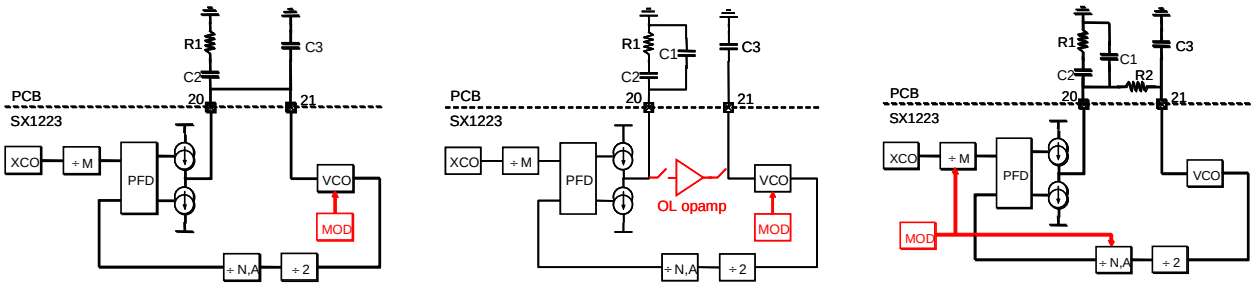
4.1.5 Loop Filter

The design of the PLL filter will strongly affect the performance of the frequency synthesizer. The PLL filter is kept external for flexibility. The parameters to be considered when designing the loop filter for the SX1223 are primarily the modulation mode and bit rate. These will also affect the switching time and phase noise.

The frequency modulation can be done in three different ways with the SX1223, either by closed-, open loop VCO modulation or by modulation with the internal dividers, see Table 3 and modulation selection guide in Table 35.

Modulation1	Modulation0	State	Comments
0	0	Closed loop VCO-modulation (mw1)	VCO is phase-locked
0	1	Open loop VCO-modulation (mw2)	VCO is free-running
1	0	Modulation by A,M and N (mw3)	Modulation inside PLL
1	1	Not used	

Table 3: Modulation modes



Modulation mw1 Modulation mw2 Modulation mw3

Figure 4: Modulation modes

In closed loop VCO modulation (mw1), the PLL bandwidth needs to be sufficiently low (≈ Bit Rate / 20), so as to prevent the VCO tracking the modulation and cancelling the modulation.

Using the dividers in mw3 mode, the PLL needs to lock on a new carrier frequency for every new data bit. Now the PLL bandwidth needs to be sufficiently high (≈ Bit Rate / 2). It may be necessary to implement a third order filter to futher suppress the phase detector frequency spurs,

For the open loop VCO modulation case (mw2), the PLL bandwidth can be large, as the PLL is deactivated during the transmission burst and there is no requirement to supress the phase detector frequency

To increase the transmission time in the open loop case, a capacitor of 47 nF can be connected on pin VARIN to ground (NPO type is advised if the transmission duration is critical). The internal opamp must be enabled to drive this capacitor, by setting the bit OL_opamp_en to 1.

A schematic for a third order loop filter is shown in Figure 5a. For a second order filter, C3 is not connected and R2 is set to 0 Ω. When designing a third order loop filter, the internal capacitance on the VARIN pin of approximately 6 pF must be taken into consideration. Figure 5b shows the loop filter configuration for the open loop VCO modulation case.

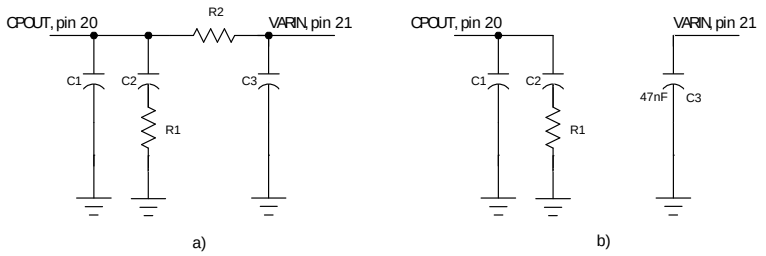


Figure 5: Loop filter for a) closed loop modulation and b) open loop modulation

4.1.6 Lock Detect

A lock detector can be enabled by setting LD_en=1. When enabled pin LD is set high, indicating that the PLL is in lock. The lock detect signal can also be used to control the PA; if LD is low the PA is turned off and vice versa. To enable this function, the PA_LDc_en must be set to '1' (see section 4.3).

Care must be taken when monitoring the LD during data transmission using the closed loop modulation. The LD may show that the PLL is not locked, especially when the loop filter bandwidth is too high relative to the bit rate.

4.2 MODULATOR

4.2.1 Introduction

The modulator has a high degree of flexibility, and there are thus several values that need programming. First, the settings concerning the data bit rate must be determined, then these values will be used in the calculation of the frequency deviation. Finally the user must check that the modulator won't saturate with the values chosen.

4.2.2 Data Interface

The "data interface" can be programmed to synchronous or asynchronous mode (see Table 4).

Sync_en	State	Comments
0	DataClk pin off	Transparent transmission of data
1	DataClk pin on.	Bit-clock is generated by transmitter

Table 4: Synchronizer mode

In asynchronous mode only the DATAIN pin is used for transmitting the data to the SX1223.

In synchronous mode the SX1223 is defined as "Master" and provides a data clock on pin DCLK that allows the user to utilize low cost micro controller reference frequency. The data interface is defined in such a way that all user actions should take place on falling edges of DCLK as illustrated in Figure 6. The data are sampled by the SX1223 on the rising edges of DCLK.

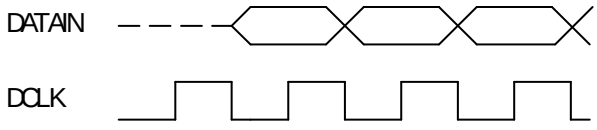


Figure 6: Time diagram of the data interface in synchronous mode

Before entering into transmit mode (mw1 or mw2), it is important to set DATAIN to high impedance. The data is provided directly to the modulation circuit and violation of this may cause abnormal behavior.

4.2.3 Bit Rate Setting for MW1 and MW2

The bit rate is set by first dividing the crystal oscillator frequency by an integer in the range [1..63] in a programmable divider, then this frequency is divided further by powers of two. The equation describing the bit rate as a function of *RefClk_K* and *BRn* is

$$BR = \frac{f_{XTAL}}{\mathrm{Re}\ fClk\_K \cdot 2^{3+BRn}} \quad (4.1)$$

where:

f_{XTAL}: Crystal oscillator frequency.
RefClk_K: Integer in the range [1..63] (6 bit).
BRn: Integer in the range [0..5] (3 bit).

A procedure to determine the settings for the desired bit rate is described below:

1. Set *BRn* to 0.
2. Calculate *RefClk_K* by using this formula: $\mathrm{Re}\ fClk\_K = \frac{f_{XTAL}}{BR \cdot 2^{3+BRn}}$.
3. If *RefClk_K* is too high, increment *n* by one, and repeat step 2, above

In some cases several combinations of *RefClk_K* and *BRn* will provide the required bit rate. In these cases *BRn* should be chosen with the following in mind: A lower *BRn* offers better waveform shaping or spectral efficiency, but may cause modulator saturation at some bit rates.

4.2.4 Deviation Setting for MW1 and MW2

Frequency deviation is controlled by user parameters *RefClk_K*, *MOD_I*, and *MOD_A* together with physical parameters f_{XTAL} and K_{VCO}. All user parameters can be set in software, and f_{XTAL} (crystal oscillator frequency) is set when designing in the radio chip. K_{VCO} (VCO gain) is a parameter of the radio chip, and is not controllable by the user.

The crystal oscillator frequency, f_{XTAL}, is divided by *RefClk_K* to generate the modulator clock. Since this modulator clock is controlling the rise and fall times for the modulator, the frequency deviation is inversely proportional to this clock. The relationship is shown in equation (4.2).

$$f_{DEV} \propto \frac{\mathrm{Re}\ fClk\_K}{f_{XTAL}} \quad (4.2)$$

It is assumed that *K* will be constant for most applications to keep bit-rate and shaping constant, although this is not a requirement.

The control parameters of the frequency deviation are *MOD_I* and *MOD_A*. Of these two, *MOD_I* is the parameter that controls the signal generation, while *MOD_A* controls attenuation of this signal. The reason for using an attenuator is to be able to generate small deviations at high values of *RefClk_K*. The relationship is shown in equation (4.3).

$$f_{DEV} \propto \frac{MOD\_I}{2^{MOD\_A}} \quad (4.3)$$

Finally, the VCO gain is given by equation (4.4).

$$K_{VCO} = \frac{Const_1 + (Const_2 \cdot f_C \cdot (2 - FreqBand))}{2 - FreqBand} \quad (4.4)$$

where:

$Const_1$: -30.6324×10^9
$Const_2$: 54.7
f_C: Carrier frequency.
FreqBand: Frequency band. 0: 400MHz and 1: 900MHz.

From equation (4.4), it can be seen that VCO is proportional to carrier frequency. MOD_I is the best parameter to alter to counteract this effect if necessary.

Combining equations (4.2), (4.3), and (4.4) gives an expression for the frequency deviation:

$$\Delta f = \frac{\text{RefClk\_K}}{f_{XTAL}} \cdot \frac{MOD\_I}{2^{MOD\_A}} \cdot \frac{Const_1 + (Const_2 \cdot f_C \cdot (2 - FreqBand))}{2 - FreqBand} \quad (4.5)$$

4.2.5 Shaping for MW1 and MW2

The modulation waveform will be shaped due to the charging and discharging of a capacitor. The waveform looks like a Gaussian filtered signal with a Bandwidth·Period-product (BT) given by:

$$BT = 2^{BRn} \quad (4.6)$$

It can be seen from this equation that a low *BRn* gives a low shaping factor.

In addition to this, it is possible to smooth the modulator output in a programmable low-pass filter. This filter is controlled by the parameter *MOD_F*. The parameter should be set according to equation (4.7).

$$MOD\_F \le \frac{150 \times 10^3}{BR} \quad (4.7)$$

4.2.6 Modulator Saturation for MW1 and MW2

The modulator output voltage is generated with a capacitor that is being charged. This means that there is a risk of saturating the modulator if the charge received by the capacitor is too large. The maximum value of *MOD_I* can be determined by using equation (4.8).

$$MOD\_I \le \left(\frac{f_{XTAL}}{\text{Re } fClk\_K} \cdot 28 \times 10^{-6} \right) + 1 \quad (4.8)$$

If it turns out that the *MOD_I*-range is too small for the application, the solution can be found by increasing *BRn* and decreasing *RefClk_K* accordingly.

4.2.7 Summary of Modulator Settings for MW1 and MW2

The necessary equations needed for the use of the modulator are (4.1), (4.5), (4.6), (4.7), and (4.8). The table below gives a summary of the meaning of the parameters.

Symbol	**Range (inclusive)**	Explanation
RefClk_K	1..63	The crystal oscillator frequency is divided by this number to produce the modulator clock, and it is divided further down by 8 to produce bit rate clock.
BRn	0..5	Number of extra divide-by-two for the bit rate clock.
MOD_F	0..3	Programmable smoothing filter after attenuator. This can be programmed in four steps, and will produce reasonable results for the highest bit rates.
MOD_I	1..31	Frequency deviation. The deviation is linearly dependent on this variable.
MOD_A	0..4	Frequency deviation attenuator (or range selector). The attenuations are (values 0 through 4, respectively) $1/1$, $1/2$, $1/4$, $1/8$, and $1/16$.

Table 5: Modulator settings

4.2.8 Frequency deviation setting for MW3

In MW3 the modulation is done by switching between two frequency divider ratio sets: M_0, N_0, A_0 and M_1, N_1, A_1. The frequency f_0 will be generated using the first set and frequency f_1 using the second set, corresponding to the transmission of the two possible values '0' and '1'.

The single sided frequency deviation Δf is half of the difference between f_0 and f_1. Bit rates from 1.2 to 19.2 kbit/s are achievable with this method.

4.3 POWER AMPLIFIER

The output power of the PA is programmable in 8 steps, with approximately 3 dB between each step. This is controlled by bits PA2 to PA0 according to Table 6 below. PA2..PA0 = 111 provides the maximum output power of typically 10 dBm.

PA2	PA1	PA0	Output power
0	0	0	21dB attenuation
0	0	1	18dB attenuation
0	1	0	15dB attenuation
0	1	1	12dB attenuation
1	0	0	9dB attenuation
1	0	1	6dB attenuation
1	1	0	3dB attenuation
1	1	1	Maximum power

Table 6: *PA power settings*

The PA is normally controlled by the two Mode bits (off for all cases other than Mode1, Mode0 = '11'). The PA can in addition be controlled by the lock detector, if the bit PALDc_en is set high (and LD_en='1'). In this case, once LD goes high after entering the transmit mode, the PA is turned on and will remain on until a new event changing the working mode occurs (such as a new configuration transmitted through the 3-wire interface).

During open loop VCO modulation, mw2, the PLL is deactivated during the transmission time. After an open loop transmission, the frequency may have drifted off, and it is therefore important that the PA is turned off before the PLL is activated. The PA behaves this way as long as PALDc_en=1. After a transmission burst, DATAIN must be set to high impedance, the PA is turned off and the PLL is reactivated. Once LD goes high again, the PA is turned on and a new burst of data can be transmitted.

To reduce the harmonics for passing the ETSI and FCC regulations a 3rd order LC-filter (T or Π configuration) should be implemented between the output of the PA and the antenna port.

The ramp-up of the PA is achieved using an internal capacitor (approx. 29pF). If this is not sufficient to pass relevant regulations, bit PAC_en can be enabled and an external capacitor connected to pin 6.

Using PA_IB3,2 and PAB_IB3,2 bits the reference current can be selected to bias the PA and the PA buffer as shown in Table 31.

An 82kΩ resistor should be connected between pin 24 and ground for the CI bias. If the option PTAT bias source with external resistor is chosen, an 18kΩ resistor should be connected between pin 6 and ground.

This option can not be used when PAC_en option is selected. In this case the resistor is replaced by a capacitor, and the functionality changes as described above.

4.4 VOLTAGE REGULATORS

The SX1223 has three internal Low Dropout Regulators (LDOs) powering up different parts of the circuit, as can be seen from the block diagram (Figure 1). The LDOs can be turned off (default setting is on) by setting the LDO_en='0'.

When LDO_en='1', the power supply range is 2.2 - 3.6 V (sv1). Power must be applied to pins 1 and 11. A good quality factor capacitor is needed on each of the LDO output for stability (pins 3, 9 and 23). In sleep mode all the LDOs are turned off. The interface and control blocks run on unregulated power, and the register contents will be stored and hence the device can be programmed whilst in this mode.

When LDO_en=0, the power supply range is 2.0 - 2.5 V (sv2). Power must be applied to pin 1, 3, 9, 11 and 23. In this case capacitors are only needed for normal noise decoupling.

5 SERIAL INTERFACE DEFINITION AND PRINCIPLES OF OPERATION

5.1 SERIAL CONTROL INTERFACE

A 3-wire bi-directional bus (SCK, SI, SO) is used to communicate with SX1223 and gives access to the configuration register. SCK and SI are input signals supplied externally, for example by the microcontroller. The SX1223 configures the SO signal as an output pin during read operation, and it is tri-stated in other modes. The falling edge of the SCK signal is used to sample the SI pin to write data into the internal shift register of the SX1223. The rising edge of the SCK signal is used to output data by the SX1223 to the SO pin, so the microcontroller should sample data at the falling edge of SCK. Be aware that reading data on SO output is forbidden whilst in transmit mode.

The signal EN must be low during the whole write and read sequences. In write mode the actual content of the configuration register is updated at the rising edge of the EN signal. Before this, the new data is stored in temporary registers whose content does not affect the transceiver settings.

The timing diagram of a write sequence is given in Figure 7 below. The sequence is initiated when a Start condition is detected, that is when the SI signal is set to “0” during a period of SCK. The next bit is a read/write (R/W) bit which should be “0” to indicate a write operation. The next 5 bits are the address of the control register A[4:0] to be accessed, MSB first. Then, the next 8 bits are the data to be written in the register. The data on SI should change at the rising edges of SCK, and is sampled at the falling edge of SCK. The SI line should be at “1” for at least one clock cycle on SCK before a new write or read sequence can start. In doing this, users can do multiple registers write without a rising EN signal in between. The duty cycle of SCK must be between 40% and 60% and the maximum frequency of this signal is 1 MHz. Over the operating supply and temperature range, set-up and hold time for SI on the falling edge of SCK are 200ns.

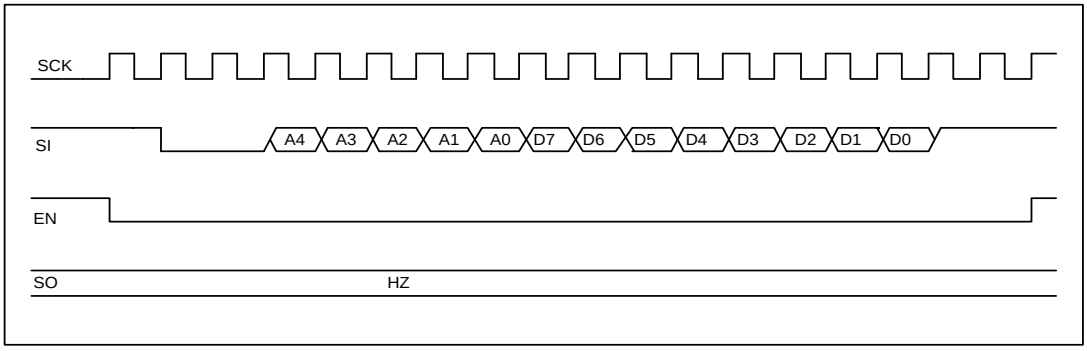


Figure 7: Write sequence into configuration register

The time diagram of a read sequence is given in figure below. The sequence is initiated when a Start condition is detected, that is when the SI signal is set to “0” during a period of SCK. The next bit is a read/write (R/W) bit which should be “1” to indicate a read operation. The next 5 bits are the address of the control register A[4:0] to be accessed, MSB first. Then the data from the register are transmitted on the SO pin. The data become valid at the rising edges of SCK and should be sampled at the falling edge of SCK. After this, the data transfer is terminated. The SI line must stay high for at least one clock cycle on SCK to start a new write or read sequence. The typical current drive on SO is 2mA @ 2.7V, the maximum load is CLop.

When the serial interface is not used for read or write operations, both SCK and SI should be set to “1”. Except in read mode, SO is set to “HZ”.

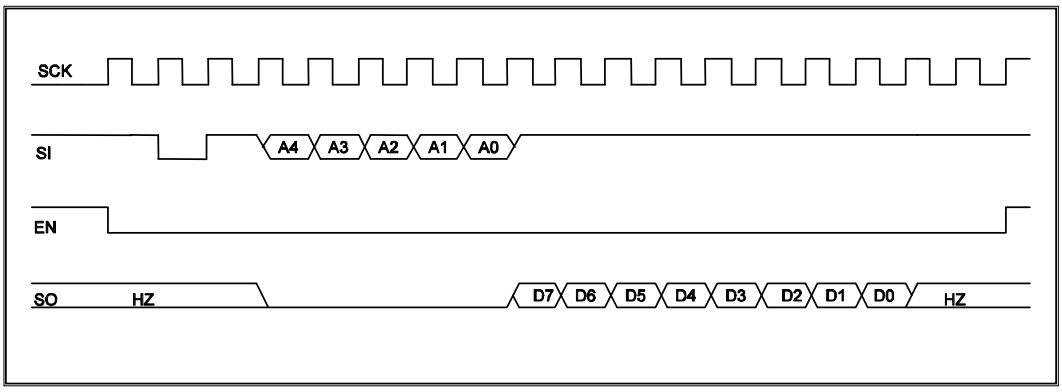


Figure 8: Read sequence of configuration register.

5.2 CONFIGURATION AND STATUS REGISTERS

The SX1223 has several operating modes and configuration parameters which can be programmed by the user. These modes and parameters are stored in a set of internal configuration registers that can be accessed by the microcontroller through the 3-wire serial interface.

The detailed contents of the configuration registers are given in the next table. The value attached to each parameter is the default value at power-up. All the undefined bits in the table below should be kept to 0.

Address	Default Value	Data							
A[6:0]	D[7:0] Hex	D7	D6	D5	D4	D3	D2	D1	D0
0000000	0x3F	-	Mode [1:0]		PA [2:0]			ClkOut_en	Sync_en
0000001	0x7D	Modulation [1:0]		Freq_Band	XCOcap_en	LDO_en	OL_opamp_en	PA_LDc_en	LD_en
0000010	0x02	-	-	PAC_en	XCO_Quick_Start	XCO_High_Current	CP_HI	VCO_freq [1:0]	
0000011	0x4B	Mod_I [4:0]					Mod_A [2:0]		
0000100	0x0C	-	-	BRn [2:0]			Mod_F [2:0]		
0000101	0x1A	-	-	RefClk_K [5:0]					
0000110	0x02	-	-	A0 [5:0]					
0000111	0x00	-	-	-	-	N0 [11.8]			
0001000	0x76	N0 [7:0]							
0001001	0x00	-	-	-	-	M0 [11:8]			
0001010	0x22	M0 [7:0]							
0001011	0x02	-	-	A1 [5:0]					
0001100	0x00	-	-	-	-	N1 [11:8]			
0001101	0x76	N1 [7:0]							
0001110	0x00	-	-	-	-	M1 [11:8]			
0001111	0x22	M1 [7:0]							
0010000	0x20	VCO_IB [2:0]			Prescal_s	VCO_by	-	-	-
0010001	0xDD	PA_IB [3:0]				PAB_IB [3:0]			

Table 7: Contents of the configuration registers and their values at power-on

5.2.1 Operating Modes

The SX1223 can be programmed into four different modes by the Mode1 and Mode0 bits, as illustrated in Table 8.

Add	Bits	Mode1	Mode0	Mode	Description
0	6-5	0	0	Sleep mode	All blocks off, Register configuration kept (default)
		0	1	Standby mode	Crystal oscillator enabled
		1	0	Synthesizer mode	Crystal oscillator, Frequency synthesizer enabled
		1	1	Transmit mode	Crystal oscillator, Frequency synthesizer, PA enabled

Table 8: SX1223 Operating Modes

5.2.2 Other Settings

The tables below give the definition of all the parameters of the configuration registers besides the working modes.

Add	Bits	PA2	PA1	PA0	State
0	4-2	0	0	0	21dB attenuation
		0	0	1	18dB attenuation
		0	1	0	15dB attenuation
		0	1	1	12dB attenuation
		1	0	0	9dB attenuation
		1	0	1	6dB attenuation
		1	1	0	3dB attenuation
		1	1	1	Max output (default)

Table 9: Power amplifier output power

Add	Bit	ClkOut_en	State	Comments
0	1	0	ClkOut off	Output is 0 volt on pin CLKOUT.
		1	ClkOut on	A clock at XCO frequency divided by 16 is available on pin CLKOUT. (default)

Table 10: Output clock

Add	Bit	Sync_en	State	Comments
0	0	0	DCLK pin off	Transparent transmission of data
		1	DCLK pin on	Bit-clock is generated by transceiver (default)

Table 11: Synchronizer mode

Add	Bit	Modulation1	Modulation0	State	Comments
1	7-6	0	0	Closed loop VCO-modulation (mw1)	VCO is phase-locked
		0	1	Open loop VCO-modulation (mw2)	VCO is free-running (default)
		1	0	Modulation by M, N and A (mw3)	Modulation inside PLL
		1	1	Not used	

Table 12: Modulation mode

Add	Bit	FreqBand	Comments
1	5	0	RF frequency 425-475 MHz
		1	RF frequency 850-950 MHz (default)

Table 13: Frequency band

Add	Bit	XCOcap_en	Comments
1	4	0	Internal capacitors for the crystal oscillator turned off
		1	Internal capacitors for the crystal oscillator turned on, external capacitors not needed (default)

Table 14: XCO internal capacitor

Add	Bit	XCO_quick_start	XCO_high_current	Comments
2	4-3	0	0	Normal XCO bias current (default)
		0	1	Higher XCO bias current
		1	0	Quick start of XCO with normal bias current in steady state
		1	1	Quick start of XCO with higher bias current in steady state

Table 15: XCO start-up control

Add	Bit	LDO_en	Comments
1	3	0	LDO turned off, min/max VDD is 2.0/2.5 V
		1	LDO turned on, min/max VDD is 2.2/3.6 V (default)

Table 16: Low DropOut voltage regulator on/off

Add	Bit	OL_opamp_en	State	Comments
1	2	0	Open loop opamp off	When opamp is enabled, a capacitor can be added to the varactor pin that will increase the transmission time in open loop modulation (mw2)
		1	Open loop opamp on (default)	

Table 17: Open loop opamp on/off

Add	Bit	PA_C	Comments
2	5	0	Startup time of PA controlled by internal capacitor; PTAT source using the resistor connected to pin6 can be used (default)
		1	Startup time of PA controlled by external capacitor connected to pin 6; PTAT source using the resistor connected to pin6 is not available

Table 18: PA start-up control

Add	Bit	PALDc_en	Comments
1	1	0	PA is only controlled by Mode1 and Mode0: PA on in transmit mode (Mode1=Mode0=1) (default)
		1	In transmit mode, PA is turned on/off by Lock Detect (i.e. LD=1 -> PA on)

Table 19: Lock Detect controlled PA

Add	Bit	LD_en	State	Comments
1	0	0	LD off	Output is low
		1	LD on	A high indicate a PLL lock (default)

Table 20: Lock Detector

Add	Bit	CP_HI	Comments
2	2	0	PLL charge pump current is 125 µA (default)
		1	PLL charge pump current is 500 µA

Table 21: Charge pump current

Add	Bits	VCO_freq1	VCO_freq0	Comments (*)
2	1-0	0	0	Setting for 850 MHz
		0	1	Setting for 868 MHz
		1	0	Setting for 915 MHz (default)
		1	1	Setting for 950 MHz

(*) Assuming FreqBand=1. When FreqBand=0, the RF frequency is halved.

Table 22: VCO frequency

Add	Bits	MOD_I	Comments
3	7-3	1..31	The deviation frequency is linearly dependent of MOD_I

Table 23: Modulator current setting for frequency deviation

Add	Bits	MOD_A	Comments
3	2-0	0..4	Frequency deviation attenuator (or range selector). The attenuations are (values 0 through 4, respectively) $1/1$, $1/2$, $1/4$, $1/8$, and $1/16$.

Table 24: Modulator attenuator setting for frequency deviation

Add	Bits	BRn	Comments
4	5-3	0..5	The bit rate clock is set by dividing the crystal oscillator frequency by RefClk_K*2^(3+BRn)

Table 25: Bit Rate setting

Add	Bits	MOD_F	Comments
4	2-0	0..3	Programmable smoothing filter after attenuator. This can be programmed in four steps, and will produce reasonable results for the highest bit rates.

Table 26: Modulator filter setting

Add	Bits	RefClk_K	Comments
5	5-0	1..63	The crystal oscillator is divided by this number to produce modulator clock and it is divided further down by 2^(3+BRn) to produce the bit rate clock.

Table 27: Modulator and Bit Rate clock setting

Add	Bit	Prescal_s	State	Comments
16	4	0	(default)	Reserved.
		1	Prescaler enabled	$f_{RF} = \frac{f_{XCO}}{M \cdot (2 - FreqBand)}(16 \cdot N + A)$

Table 28: Prescaler enable bit

"1" should be written in Prescal_s register to operate SX1223 PLL dividers.

5.2.3 Optional and Test Parameters

In most applications, the user has only to be concerned with the parameters given in sections 5.2.1 and 5.2.2. However some options and test modes are available for special purposes. They are described in the tables below.

Add	Bits	VCO_IB2	VCO_IB1	VCO_IB0	**Comments** - default = [0 0 1]
16	7-5	1	1	1	Bias setting for 850 MHz
		1	0	1	Bias setting for 868 MHz
		0	1	1	Bias setting for 915 MHz
		0	0	0	Bias setting for 950 MHz

Table 29: VCO bias

The two VCO_freq bits have to be programmed by the user according to the selected frequency band, whereas the three VCO_IB bits can be either forced by the user or set automatically by the circuit which will select the combination having the best phase noise. This automatic setting can be enabled by setting the three VCO_IB bits to '0'.

Add	Bit	VCO_by	State	Comment
16	3	0	VCO is active (default)	When VCO is bypassed, a differential signal can be applied to the circuit using pin CPOUT and VARIN
		1	VCO is bypassed	

Table 30: VCO bypass bit

Add	Bits	PA_IB3	PA_IB2	State
17	7-6	0	0	PA uses bias current from PTAT bias source, external resistor (Pin 6)
		0	1	PA uses bias current from CI bias source, external resistor (Pin 24)
		1	0	PA uses bias current from internal bias source, PTAT
		1	1	PA uses bias current from internal bias source, PTAT + CI (default)
Add	**Bits**	**PA_IB1**	**PA_IB0**	**State**
17	5-4	0	0	PA bias current setting, lowest bias current
		0	1	PA bias current setting (default)
		1	0	PA bias current setting
		1	1	PA bias current setting, highest bias current
Add	**Bits**	**PAB_IB3**	**PAB_IB2**	**State**
17	3-2	0	0	PAbuffer uses bias current from PTAT bias source, external resistor (Pin 6)
		0	1	PAbuffer uses bias current from CI bias source, external resistor (Pin 24)
		1	0	PAbuffer uses bias current from internal bias source, PTAT
		1	1	PAbuffer uses bias current from internal bias source, PTAT + CI (default)
Add	**Bits**	**PAB_IB1**	**PAB_IB0**	**State**
17	1-0	0	0	PAbuffer bias current setting, lowest bias current
		0	1	PAbuffer bias current setting (default)
		1	0	PAbuffer bias current setting
		1	1	PAbuffer bias current setting, highest bias current

Table 31: PA and PAbuffer bias current setting

6 APPLICATION INFORMATION

This section provides details of the recommended components values for the frequency dependant blocks of the SX1223. Note that these values are dependent upon circuit layout and PCB structure.

6.1 MATCHING NETWORK OF THE TRANSMITTER

The optimum load impedances for 10 dBm output power at the three main frequencies are given in the following table.

	434 MHz	869 MHz	915 MHz
PA optimum load	19.4-j2.6	23.5-j1	23.5+j8

Table 32: Optimum load impedances for 10 dBm output power

The schematic of the recommended matching network at the output of the transmitter is given in Figure 9 on the next page.

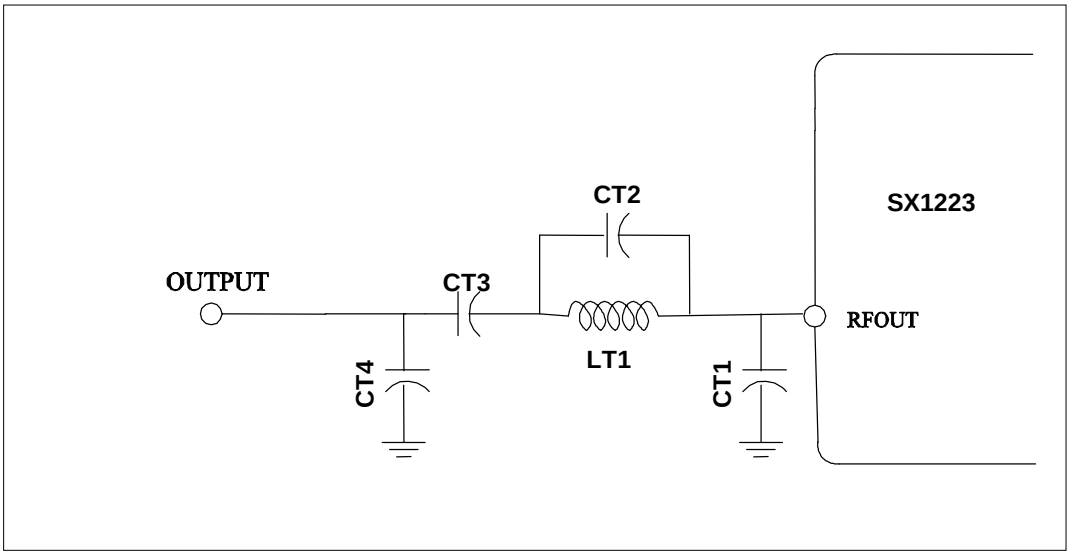


Figure 9: Transmitter output network

The Π-section is used to provide harmonic filtering in order to satisfy FCC and ETSI regulations.
The typical component values of this matching circuit are given below.

Name	Typical Value for 434 MHz	Typical Value for 869 MHz	Typical Value for 915 MHz	Tolerance
CT1	6.8pF	6.8 pF	6.8 pF	± 5%
CT2	1pF	NC	NC	± 5%
CT3	10pF	15 pF	33 pF	± 5%
CT4	10pF	6.8 pF	4.7 pF	± 5%
LT1	22nH	4.7 nH	4.7 nH	± 5%

Table 33: Typical component values for the recommended matching network at the output of the transmitter

6.2 REFERENCE CRYSTAL FOR THE FREQUENCY SYNTHESIZER

The crystal for the reference oscillator of the frequency synthesizer should have the following typical characteristics:

Name	Description	Min. value	Typ. value	Max. value
Fs	Nominal frequency	-	16.0 MHz (fundamental)	-
CL	Load capacitance for fs (on-chip)	-	9 pF	-
Rm	Motional resistance	-	-	40Ω
Cm	Motional capacitance	-	-	30 fF
C0	Shunt capacitance	-	-	7 pF

Table 34: Crystal characteristics

6.3 LOOP FILTER COMPONENTS

The loop filter component values used in MW2 mode for specification validation are presented below; (see fig.5b)

R1	C1	C2	C3
12kΩ	470pF	4.7nF	33nF

6.4 RECOMMENDED MODULATION CONDITIONS

Bit rate [kb/s]	Frequency deviation [kHz]	Modulation type	Max. carrier frequency step	Coding	Allowed transmission mode
1.2	5 to 255	mw3	Up to 300 kHz, not regularly spaced	NRZ	Continuous
2.4	5 to 255				
4.8	5 to 255				
9.6	10 to 255				
19.2	20 to 255				
32.8	40 to 255	mw1	≤ 100 kHz	Manchester	Continuous
	100 to 255	mw2	≤ 100 kHz	NRZ	Burst (1 kbits for $\Delta f \geq 100$ kHz)
38.4	40 to 255	mw1	≤ 100 kHz	Manchester	Continuous
	100 to 255	mw2	≤ 100 kHz	NRZ	Burst (1 kbits for $\Delta f \geq 100$ kHz)
76.8	80 to 255	mw1	≤ 100 kHz	Manchester	Continuous
	100 to 255	mw2	≤ 100 kHz	NRZ	Burst (2 kbits for $\Delta f \geq 100$ kHz)
153.6	200 to 255	mw1	≤ 100 kHz	Manchester	Continuous
	100 to 255	mw2	≤ 100 kHz	NRZ	Burst (4 kbits for $\Delta f \geq 100$ kHz)

Table 35: Modulation Type Selection

6.5 TYPICAL APPLICATION SCHEMATICS

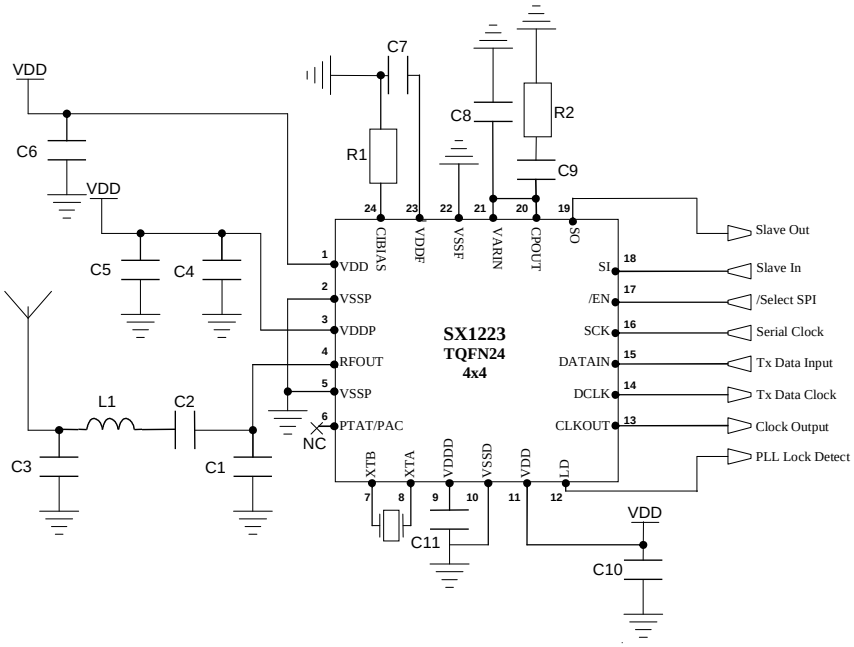


Figure 10: Application Schematics

Note: refer to chapter 4.3 for pin 6.

Please contact Semtech for applications schematics and bills of materials for Reference Designs.

7 PACKAGING INFORMATION

SX1223 comes in a 24-pin RoHS green TQFN 4x4 package as shown in Figure 11 below.

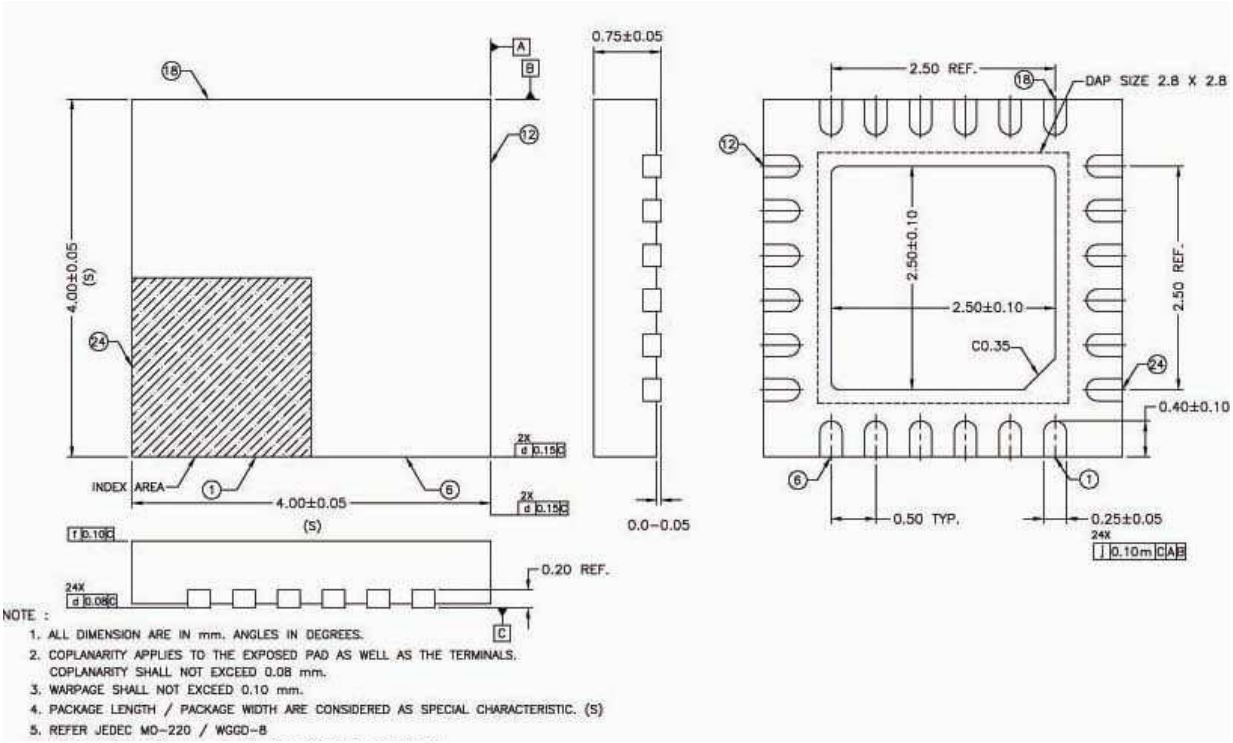


Figure 11: *Package dimensions*

The exposed die pad on the bottom of the chip should be soldered. Please contact Semtech for foot print recommendations and PCB gerber files of Semtech reference designs.

Contact Information

Semtech Corporation
Wireless and Sensing Products Division
200 Flynn Road, Camarillo, CA 93012
Phone (805) 498-2111 Fax : (805) 498-3804

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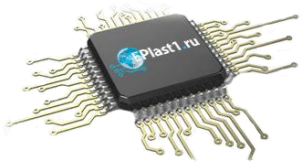
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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